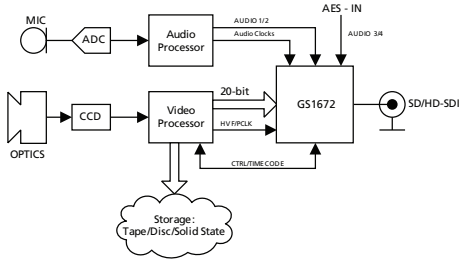
GS1672 HD/SD-SDI Serializer with Complete SMPTE Audio & Video Support

Key Features

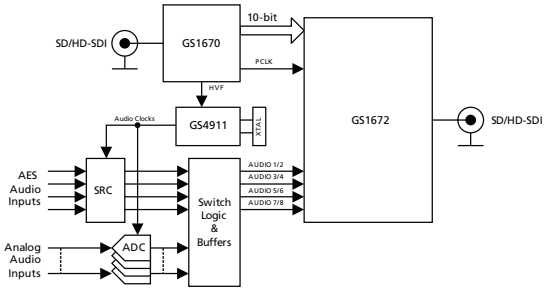
- Operation at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- Supports SMPTE 292, SMPTE 259M-C and DVB-ASI
- Integrated Cable Driver
- Integrated, low-noise VCO
- Integrated Narrow-Bandwidth PLL
- Integrated Audio Embedder for up to 8 channels of 48kHz audio
- Ancillary data insertion
- Parallel data bus selectable as either 20-bit or 10-bit
- SMPTE video processing including TRS calculation and insertion, line number calculation and insertion, line based CRC calculation and insertion, illegal code re-mapping, SMPTE 352M payload identifier generation and insertion
- GSPI host interface
- 1.2V digital core power supply, 1.2V and 3.3V analog power supplies, and selectable 1.8V or 3.3V I/O power supply
- -20°C to +85°C operating temperature range
- Low power operation (typically at 350mW, including Cable Driver)
- Small 11mm x 11mm 100-ball BGA package
- Pb-free and RoHS compliant

Applications

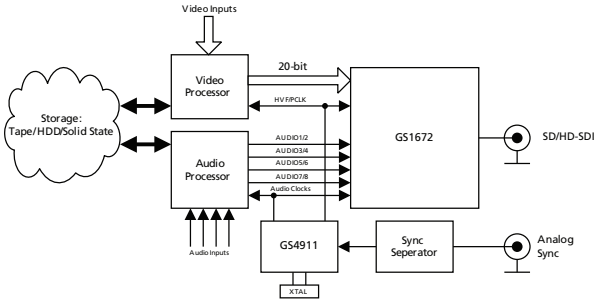
Application: 1080p 30 Camera/Camcorder



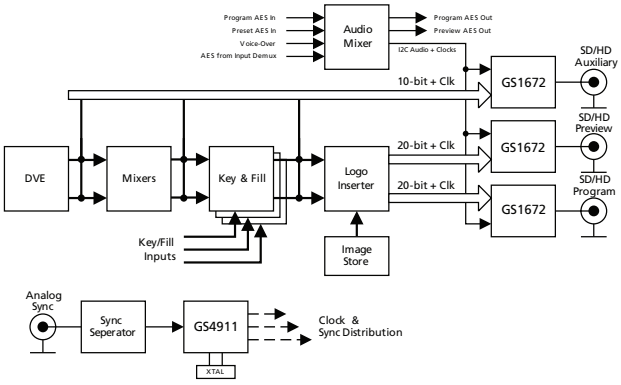
Application: Multi-format Audio Embedded Module



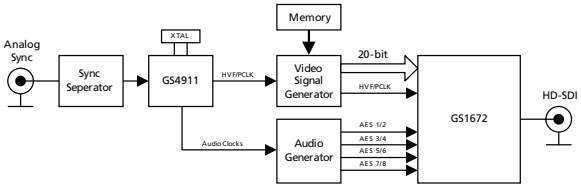
Application: Multi-format Digital VTR/Video Server



Application: Multi-format Presentation Switcher (Output Stage)



Application: HD-SDI Test Signal Generator



Description

The GS1672 is a complete SDI Transmitter, generating a SMPTE 292, SMPTE 259M-C or DVB-ASI compliant serial digital output signal.

The integrated Narrow BW PLL allows the device to accept parallel clocks with high input jitter, and still provide a SMPTE compliant serial digital output.

The device can operate in four basic user selectable modes: SMPTE mode, DVB-ASI mode, Data-Through mode, or Standby mode.

In DVB-ASI mode, the device will perform 8b/10b encoding prior to transmission.

In Data-Through mode, all SMPTE and DVB-ASI processing is disabled. The device can be used as a simple parallel to serial converter.

The device can also operate in a lower power Standby mode. In this mode, no signal is generated at the output.

The GS1672 integrates a fully SMPTE-compliant Cable Driver for SMPTE 259M-C and SMPTE 292 interfaces. It features automatic dual slew-rate selection, depending on HD or SD operational requirements.

In accordance with SMPTE 272M and SMPTE 299M, up to eight channels (two audio groups) of serial digital audio may be embedded into the video data stream.The input audio signal formats supported by the device include AES/EBU, I^2C and serial audio. 16, 20 and 24-bit audio formats are supported at 48kHz synchronous for SD modes and 48kHz synchronous or asynchronous in HD modes.

Functional Block Diagram

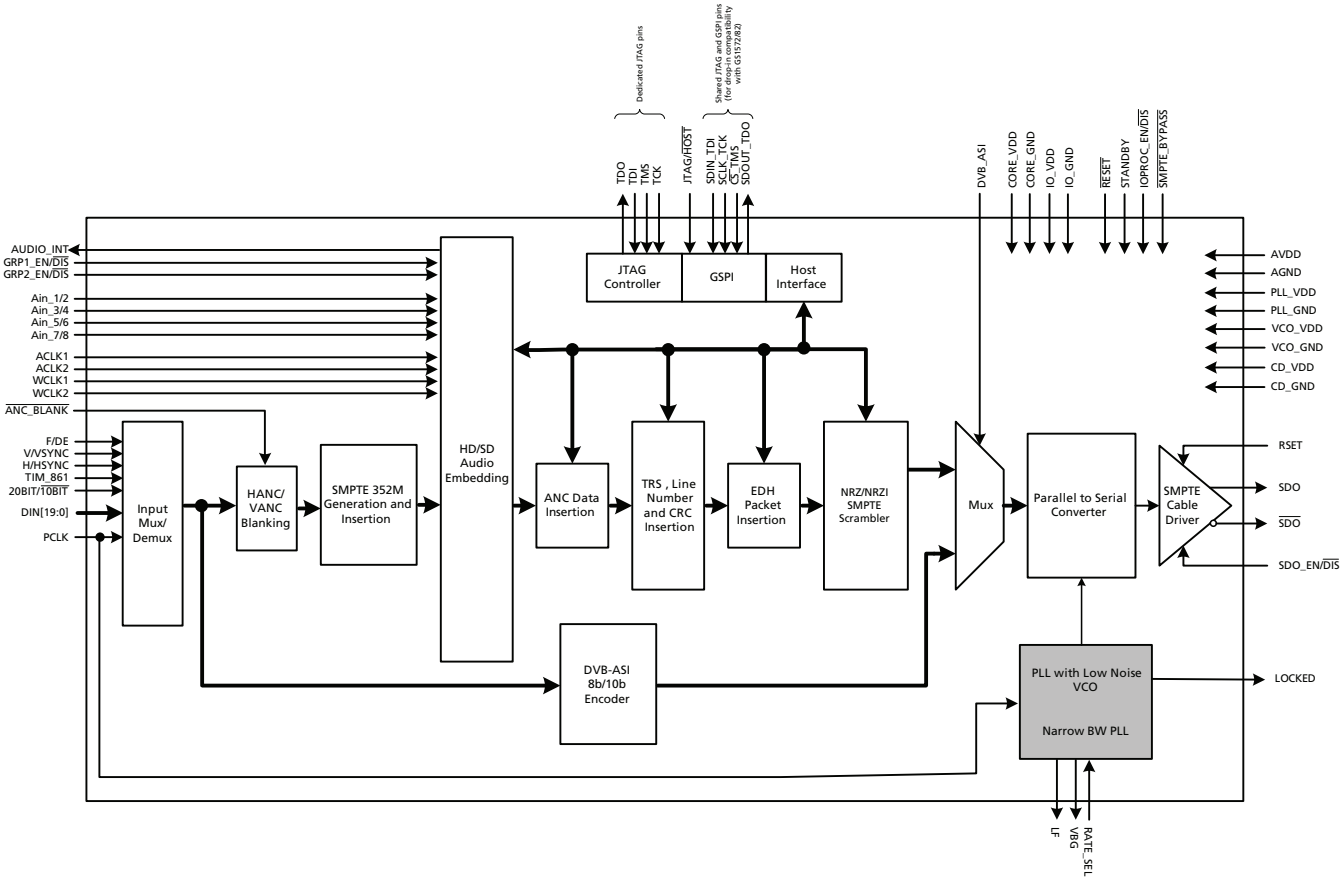


Figure A: GS1672 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
6	156652	–	July 2011	Correction to the Typical Application Circuit.
5	155608	–	January 2011	Clarified the function of the ACS_REGEN bit in Section 4.7.10 Audio Channel Status.
4	155080	56060	October 2010	Revised power rating in standby mode. Documented CSUM behaviour in Section 4.8, Section 4.9.3 and Video Core Configuration and Status Registers.
3	153743	–	March 2010	Correction to ANC Data Insertion addresses 040h - 13Fh in Table 4-34: Video Core Configuration and Status Registers. Changed Reset Pulse width from 10ms to 1ms in Table 2-4: AC Electrical Characteristics and 4.18 Device Reset. Changed Pin E4 to IO_GND.
2	153550	–	January 2010	Removed VCO Supply Voltage from Table 2-2: Recommended Operating Conditions, and revised VCO_VDD Pin Description in Table 1-1: Pin Descriptions.
1	153472	–	January 2010	Converted to Data Sheet.
0	153211	–	November 2009	Converted to Preliminary Data Sheet. Changed pin E4 to RSV in Pin Assignment, Pin Descriptions and Typical Application Circuit.
A	152842	–	October 2009	New Document.

Contents

List of Figures

List of Tables

1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	DIN17	DIN18	F/DE	H/HSYNC	CORE_VDD	PLL_VDD	LF	VBG	RSV	A_VDD
B	DIN15	DIN16	DIN19	PCLK	CORE_GND	PLL_VDD	VCO_VDD	VCO_GND	A_GND	A_GND
C	DIN13	DIN14	DIN12	V/VSYNC	CORE_GND	PLL_GND	PLL_GND	PLL_GND	CD_GND	SDO
D	DIN11	DIN10	STANDBY	SDO_EN/$\overline{DIS}$	RSV	RSV	RSV	RSV	CD_GND	$\overline{SDO}$
E	CORE_VDD	CORE_GND	RATE_SEL	IO_GND	CORE_GND	CORE_GND	TDI	TMS	CD_GND	CD_VDD
F	DIN9	DIN8	DETECT_TRS	RSV	CORE_GND	CORE_GND	RSV	TDO	CD_GND	RSET
G	IO_VDD	IO_GND	TIM_861	20bit/$\overline{10bit}$	DVB_ASI	$\overline{SMPTE\_BYPASS}$	IOPROC_EN/$\overline{DIS}$	$\overline{RESET}$	CORE_GND	CORE_VDD
H	DIN7	DIN6	$\overline{ANC\_BLANK}$	LOCKED	GRP2_EN/$\overline{DIS}$	GRP1_EN/$\overline{DIS}$	AUDIO_INT	JTAG/$\overline{HOST}$	IO_GND	IO_VDD
J	DIN5	DIN4	DIN1	AIN_5/6	WCLK2	AIN_1/2	WCLK1	TCK	SDOUT_TDO	SCLK_TCK
K	DIN3	DIN2	DIN0	AIN_7/8	ACLK2	AIN_3/4	ACLK1	CORE_VDD	$\overline{CS}$_TMS	SDIN_TDI

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description	
A1, A2, B1, B2, B3, C1, C2, C3, D1, D2	DIN[19:10]		Input	PARALLEL DATA BUS Signal levels are LVCMOS / LVTTL compatible.	
				20-bit mode 20BIT/$\overline{10BIT}$ = HIGH	Luma data input in SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH) Data input in data through mode ($\overline{SMPTE\_BYPASS}$ = LOW)
				10-bit mode 20BIT/$\overline{10BIT}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode ($\overline{SMPTE\_BYPASS}$ = HIGH) Data input in data through mode ($\overline{SMPTE\_BYPASS}$ = LOW) DVB-ASI data input in DVB-ASI mode ($\overline{SMPTE\_BYPASS}$ = LOW) (DVB_ASI = HIGH)
A3	F/DE	Synch-ronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. TIM_861 = LOW: Used to indicate the ODD / EVEN field of the video signal when DETECT_TRS is set LOW. The device will set the F bit in all outgoing TRS signals for the entire period that the F input signal is HIGH (IOPROC_EN/$\overline{DIS}$ must also be HIGH). The F signal should be set HIGH for the entire period of field 2 and should be set LOW for all lines in field 1 and for all lines in progressive scan systems. The F signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The DE signal is used to indicate the active video period when DETECT_TRS is LOW. DE is HIGH for active data and LOW for blanking. See Section 4.3 and Section 4.3.2 for timing details. The DE signal is ignored when DETECT_TRS = HIGH.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A4	H/HSYNC	Synch-ronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. TIM_861 is LOW: The H signal is used to indicate the portion of the video line containing active video data, when DETECT_TRS is set LOW. Active Line Blanking The H signal should be LOW for the active portion of the video line. The signal goes LOW at the first active pixel of the line, and then goes HIGH after the last active pixel of the line. The H signal should be set HIGH for the entire horizontal blanking period, including both EAV and SAV TRS words, and LOW otherwise. TRS Based Blanking (H_CONFIG = 1_h) The H signal should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise. TIM_861 = HIGH: The HSYNC signal indicates horizontal timing. See Section 4.3. When DETECT_TRS is HIGH, this pin is ignored at all times. If DETECT_TRS is set HIGH and TIM_861 is set HIGH, the DETECT_TRS feature will take priority.
A5, E1, G10, K8	CORE_VDD		Input Power	Power supply connection for digital core logic. Connect to 1.2V DC digital.
A6, B6	PLL_VDD		Input Power	Power supply pin for PLL. Connect to 1.2V DC analog.
A7	LF		Analog Output	Loop Filter component connection.
A8	VBG		Output	Bandgap voltage filter connection.
A9, D6, D7, D8, F4	RSV		–	These pins are reserved and should be left unconnected.
A10	A_VDD		Input Power	VDD for sensitive analog circuitry. Connect to 3.3VDC analog.
B4	PCLK		Input	PARALLEL DATA BUS CLOCK. Signal levels are LVCMOS / LVTTL compatible. HD 20-bit mode — PCLK @ 74.25MHz HD 10-bit mode — PCLK @ 148.5MHz SD 20-bit mode — PCLK @ 13.5MHz SD 10-bit mode — PCLK @ 27MHz DVB-ASI mode — PCLK @ 27MHz
B5, C5, E2, E5, E6, F5, F6, G9	CORE_GND		Input Power	GND connection for digital logic. Connect to digital GND.
B7	VCO_VDD		Input Power	Power pin for the VCO. Connect to a 1.2V±5% analog supply, followed by a RC filter (see Typical Application Circuit on page 111). A 105Ω 1% resistor must be used in the RC filter circuit. VCO_VDD is nominally 0.7V.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
B8	VCO_GND		Input Power	Ground connection for VCO. Connect to analog GND.
B9, B10	A_GND		Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.
C4	V/VSYNC	Synch-ronous with PCLK	Input	PARALLEL DATA TIMING. Signal levels are LVCMOS / LVTTL compatible. TIM_861 = LOW: The V signal is used to indicate the portion of the video field/frame that is used for vertical blanking, when DETECT_TRS is set LOW. The V signal should be set HIGH for the entire vertical blanking period and should be set LOW for all lines outside of the vertical blanking interval. The V signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The VSYNC signal indicates vertical timing. See Section 4.3 for timing details. The VSYNC signal is ignored when DETECT_TRS = HIGH.
C6, C7, C8	PLL_GND		Input Power	Ground connection for PLL. Connect to analog GND.
C9, D9, E9, F9	CD_GND		Input Power	Ground connection for the serial digital cable driver. Connect to analog GND.
C10, D10	SDO, $\overline{\text{SDO}}$		Output	Serial Data Output Signal. Serial digital output signal operating at 1.485Gb/s, 1.485 /1.001Gb/s or 270Mb/s. The slew rate of the output is automatically controlled to meet SMPTE 292 and 259M specifications according to the setting of the RATE_SEL pin.
D3	STANDBY		Input	Power Down input. HIGH to power down device.
D4	SDO_EN/$\overline{\text{DIS}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to enable or disable the serial digital output stage. When SDO_EN/$\overline{\text{DIS}}$ is LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When SDO_EN/$\overline{\text{DIS}}$ is HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled.
D5, F7	RSV		–	These pins are reserved and should be connected to CORE_GND.
E3	RATE_SEL		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to configure the operating data rate. RATE_SEL: 0 — Data Rate: 1.485 or 1.485/1.001Gb/s RATE_SEL: 1 — Data Rate: 270Mb/s

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
E7	TDI		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Dedicated JTAG pin. Test data in. This pin is used to shift JTAG test data into the device when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
E8	TMS		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Dedicated JTAG pin. Test mode start. This pin is JTAG Test Mode Start, used to control the operation of the JTAG test when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
E10	CD_VDD		Input Power	Power for the serial digital cable driver. Connect to 3.3V DC analog.
F1, F2, H1, H2, J1, J2, J3, K1, K2, K3	DIN[9:0]		Input	PARALLEL DATA BUS. Signal levels are LVCMOS / LVTTL compatible. In 10-bit mode, these pins are not used. 20-bit mode (20BIT/$\overline{\text{10BIT}}$ = HIGH): Chroma data input in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH, DVB_ASI = LOW); Data input in data through mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW, DVB_ASI = LOW); Not Used in DVB-ASI mode ($\overline{\text{SMPTE\_BYPASS}}$ = LOW, DVB_ASI = HIGH) 10-bit mode (20BIT/$\overline{\text{10BIT}}$ = LOW): High impedance.
F3	DETECT_TRS		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to select external HVF timing mode or TRS extraction timing mode. When DETECT_TRS is LOW, the device extracts all internal timing from the supplied H:V:F or CEA-861 timing signals, dependent on the status of the TIM861 pin. When DETECT_TRS is HIGH, the device extracts all internal timing from TRS signals embedded in the supplied video stream.
F8	TDO		Output	COMMUNICATION SIGNAL OUTPUT. Signal levels are LVCMOS/LVTTL compatible. Dedicated JTAG pin. JTAG Test Data Output. This pin is used to shift results from the device when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
F10	RSET		Input	An external 1% resistor connected to this input is used to set the SDO/$\overline{\text{SDO}}$ output signal amplitude.
G1, H10	IO_VDD		Input Power	Power connection for digital I/O. Connect to 3.3V or 1.8V DC digital.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
E4, G2, H9	IO_GND		Input Power	Ground connection for digital I/O. Connect to digital GND.
G3	TIM_861		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to select external CEA-861 timing mode. When DETECT_TRS is LOW and TIM-861 is LOW, the device extracts all internal timing from the supplied H:V:F timing signals. When DETECT_TRS is LOW and TIM-861 is HIGH, the device extracts all internal timing from the supplied HSYNC, VSYNC, DE timing signals. When DETECT_TRS is HIGH, the device extracts all internal timing from TRS signals embedded in the supplied video stream.
G4	20BIT/$\overline{10BIT}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to select the input bus width.
G5	DVB_ASI		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable the DVB-ASI data transmission. When DVB_ASI is set HIGH and $\overline{SMPTE\_BYPASS}$ is set LOW, then the device will carry out DVB-ASI word alignment, I/O processing and transmission. When $\overline{SMPTE\_BYPASS}$ and DVB_ASI are both set LOW, the device operates in data-through mode.
G6	$\overline{SMPTE\_BYPASS}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to enable / disable all forms of encoding / decoding, scrambling and EDH insertion. When set LOW, the device operates in data through mode (DVB_ASI= LOW), or in DVB-ASI mode (DVB_ASI = HIGH). No SMPTE scrambling takes place and none of the I/O processing features of the device are available when $\overline{SMPTE\_BYPASS}$ is set LOW. When set HIGH, the device carries out SMPTE scrambling and I/O processing.
G7	IOPROC_EN/$\overline{DIS}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the I/O processing features. When IOPROC_EN/$\overline{DIS}$ is HIGH, the I/O processing features of the device are enabled. When IOPROC_EN/$\overline{DIS}$ is LOW, the I/O processing features of the device are disabled. Only applicable in SMPTE mode.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G8	$\overline{\text{RESET}}$		Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG sequence. Normal mode (JTAG/$\overline{\text{HOST}}$ = LOW). When LOW, all functional blocks will be set to default conditions and all input and output signals become high-impedance. When HIGH, normal operation of the device resumes. JTAG test mode (JTAG/$\overline{\text{HOST}}$ = HIGH). When LOW, all functional blocks will be set to default and the JTAG test sequence will be reset. When HIGH, normal operation of the JTAG test sequence resumes.
H3	$\overline{\text{ANC\_BLANK}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. When $\overline{\text{ANC\_BLANK}}$ is LOW, the Luma and Chroma input data is set to the appropriate blanking levels during the H and V blanking intervals. When $\overline{\text{ANC\_BLANK}}$ is HIGH, the Luma and Chroma data pass through the device unaltered. Only applicable in SMPTE mode.
H4	LOCKED		Output	STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. PLL lock indication. HIGH indicates PLL is locked. LOW indicates PLL is not locked.
H5	GRP2_EN/$\overline{\text{DIS}}$		Input	Enables Audio Group 2 embedding. Set HIGH to enable.
H6	GRP1_EN/$\overline{\text{DIS}}$		Input	Enables Audio Group 1 embedding. Set HIGH to enable.
H7	AUDIO_INT		Output	STATUS SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. Summary Interrupt from Audio Processing. This signal is set HIGH by the device to indicate a problem with the audio processing which requires the Host processor to interrogate the interrupt status registers. IO_VDD = 3.3V Drive Strength = 8mA IO_VDD = 1.8V Drive Strength = 4mA NOTE: By default, out of reset, the AUDIO_INT pin will output the HD_AUDIO_CLOCK, rather than the audio interrupt signal. In order to output the interrupt flags from the audio core as intended, the user must write 0001h to register 0232h.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
H8	JTAG/$\overline{\text{HOST}}$		Input	CONTROL SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Used to select JTAG test mode or host interface mode. When JTAG/$\overline{\text{HOST}}$ is HIGH, the host interface port is configured for JTAG test. When JTAG/$\overline{\text{HOST}}$ is LOW, normal operation of the host interface port resumes and the separate JTAG pins become the JTAG port.
J4	AIN_5/6		Input	Serial Audio Input; Channels 5 and 6.
J5	WCLK2		Input	48kHz Word Clock associated with AIN_5/6 and AIN_7/8 (channels 5, 6, 7 and 8).
J6	AIN_1/2		Input	Serial Audio Input; Channels 1 and 2.
J7	WCLK1		Input	48kHz Word Clock associated with AIN_1/2 and AIN_3/4 (channels 1, 2, 3 and 4).
J8	TCK		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS/LVTTL compatible. JTAG Serial Data Clock Signal. This pin is the JTAG clock when the JTAG/$\overline{\text{HOST}}$ pin is LOW.
J9	SDOUT_TDO		Output	COMMUNICATION SIGNAL OUTPUT. Signal levels are LVCMOS / LVTTL compatible. Shared JTAG/$\overline{\text{HOST}}$ pin. Provided for compatibility with the GS1582. Serial Data Output/Test Data Output. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) This pin operates as the host interface serial output, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is used to shift test results and operates as the JTAG test data output, TDO (for new designs, use the dedicated JTAG port). NOTE: If the host interface is not being used leave this pin unconnected. IO_VDD = 3.3V Drive Strength = 12mA IO_VDD = 1.8V Drive Strength = 4mA

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
J10	SCLK_TCK		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Shared JTAG/HOST pin. Provided for pin compatibility with GS1582. Serial data clock signal. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SCLK_TCK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is the TEST MODE START pin, used to control the operation of the JTAG test clock, TCK (for new designs, use the dedicated JTAG port). NOTE: If the host interface is not being used, tie this pin HIGH.
K4	AIN_7/8		Input	Serial Audio Input; Channels 7 and 8.
K5	ACLK2		Input	64 x WCLK associated with AIN_5/6 and AIN_7/8 (channels 5, 6, 7 and 8).
K6	AIN_3/4		Input	Serial Audio Input; Channels 3 and 4.
K7	ACLK1		Input	64 x WCLK associated with AIN_1/2 and AIN_3/4 (channels 1, 2, 3and 4).
K9	$\overline{\text{CS}}$_TMS		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Chip select / test mode start. JTAG Test mode (JTAG/$\overline{\text{HOST}}$ = HIGH) $\overline{\text{CS}}$_TMS operates as the JTAG test mode start, TMS, used to control the operation of the JTAG test, and is active HIGH (for new designs, use the dedicated JTAG port). Host mode (JTAG/$\overline{\text{HOST}}$ = LOW), $\overline{\text{CS}}$_TMS operates as the host interface Chip Select, $\overline{\text{CS}}$, and is active LOW.
K10	SDIN_TDI		Input	COMMUNICATION SIGNAL INPUT. Signal levels are LVCMOS / LVTTL compatible. Shared JTAG/HOST pin. Provided for pin compatibility with GS1582. Serial data in/test data in. In JTAG mode, this pin is used to shift test data into the device (for new designs, use the dedicated JTAG port). In host interface mode, this pin is used to write address and configuration data words into the device.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +3.6V
Supply Voltage, Analog 1.2V (PLL_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (CD_VDD, A_VDD)	-0.3V to +3.6V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Operating Temperature Range	-20°C to +85°C
Functional Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

NOTES:

Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Analog	A_VDD	–	3.13	3.3	3.47	V	–
Supply Voltage, CD	CD_VDD	–	3.13	3.3	3.47	V	–

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current		10/20bit HD	–	100	160	mA	–
		10/20bit SD	–	75	120	mA	–
		DVB_ASI	–	75	120	mA	–
+1.8V Supply Current		10/20bit HD	–	15	32	mA	–
		10/20bit SD	–	3	10	mA	–
		DVB_ASI	–	3	10	mA	–
+3.3V Supply Current		10/20bit HD	–	90	110	mA	–
		10/20bit SD	–	70	90	mA	–
		DVB_ASI	–	70	90	mA	–
Total Device Power (IO_VDD = 1.8V)		10/20bit HD	–	350	510	mW	–
		10/20bit SD	–	300	450	mW	–
		DVB_ASI	–	300	450	mW	–
		Reset	–	200	–	mW	–
		Standby	–	110	180	mW	–
Total Device Power (IO_VDD = 3.3V)		10/20bit HD	–	420	550	mW	–
		10/20bit SD	–	320	450	mW	–
		DVB_ASI	–	320	450	mW	–
		Reset	–	230	–	mW	–
		Standby	–	110	180	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_VSS-0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_VDD+0.3	V	–
Output Logic LOW	V_{OL}	IOL=5mA, 1.8V operation	–	–	0.2	V	–
		IOL=8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	IOH=-5mA, 1.8V operation	1.4	–	–	V	–
		IOH=-8mA, 3.3V operation	2.4	–	–	V	–
Serial Output							
Serial Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET = 750Ω SD and HD mode	–	CD_VDD - $V_{SDD/2}$	–	V	–

NOTES:

1. Devices manufactured prior to April 1, 2011 consume 150mW of power in Standby mode.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Device Latency	–	HD bypass (PCLK = 148MHz)	–	54	–	PCLK	–
	–	HD SMPTE without audio (PCLK = 148MHz)	–	95	–	PCLK	–
	–	HD SMPTE with audio (PCLK = 148MHz)	–	1106	–	PCLK	–
	–	SD bypass (PCLK = 27 MHz)	–	54	–	PCLK	–
	–	SD SMPTE without audio	–	112	–	PCLK	–
	–	SD SMPTE with audio	–	638	–	PCLK	–
	–	DVB-ASI	–	52	–	PCLK	–
Reset Pulse Width	t_{reset}	–	1	–	–	ms	–
Parallel Input							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Input Data Setup Time	t_{su}	50% levels; 3.3V or 1.8V operation	1.2	–	–	ns	1
Input Data Hold Time	t_{ih}		0.8	–	–	ns	1
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	–	1.485	–	Gb/s	–
		–	–	1.485/1.001	–	Gb/s	–
		–	–	270	–	Mb/s	–
Serial Output Swing	V_{SDD}	RSET = 750Ω 75Ω load	750	800	850	mVp-p	2
Serial Output Rise/Fall Time 20% ~ 80%	trf_{SDO}	HD mode	–	120	135	ps	–
	trf_{SDO}	SD mode	400	660	800	ps	–
Mismatch in rise/fall time	$\Delta t_r, \Delta t_f$	–	–	–	35	ps	–
Duty Cycle Distortion	–	–	–	–	5	%	2
Overshoot	–	HD mode	–	5	10	%	2
	–	SD mode	–	3	8	%	2
Output Return Loss	ORL	5 MHz - 1.485 GHz	–	-18	–	dB	3

Table 2-4: AC Electrical Characteristics (Continued)

V_{CC} = 3.3V ±5%, T_A = -20°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Output Intrinsic Jitter	t_{OJ}	Pseudorandom and SMPTE Colour Bars HD signal	–	50	95	ps	4, 6
	t_{OJ}	Pseudorandom and SMPTE Colour Bars SD signal	–	200	400	ps	5
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	80	MHz	–
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	–
GSPI Input Data Setup Time	–		1.5	–	–	ns	–
GSPI Input Data Hold Time	–		1.5	–	–	ns	–
GSPI Output Data Hold Time	–	15pF load	1.5	–	–	ns	–
$\overline{CS}$ low before SCLK rising edge	t_0	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	t_4	50% levels 3.3V or 1.8V operation	PCLK (MHz) / ns	–	–	ns	–
			unlocked / 445				
			13.5 / 74.2				
			27.0 / 37.1				
			74.25 / 13.5				
			148.5 / 6.7				
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	t_5	50% levels 3.3V or 1.8V operation	PCLK (MHz) / ns	–	–	ns	–
			unlocked / 1187				
			13.5 / 297				
			27.0 / 148.4				
			74.25 / 53.9				
			148.5 / 27				
$\overline{CS}$ high after SCLK falling edge	t_7	50% levels 3.3V or 1.8V operation	PCLK (MHz) / ns	–	–	ns	–
			unlocked / 445				
			13.5 / 74.2				
			27.0 / 37.1				
			74.25 / 13.5				
			148.5 / 6.7				

NOTES:

1. Input setup and hold time is dependent on the rise and fall time on the parallel input. Parallel clock and data with rise time or fall time greater than 500ps require larger setup and hold times.
2. Single Ended into 75Ω external load.
3. ORL depends on board design.
4. Alignment Jitter = measured from 100kHz to serial data rate/10.
5. Alignment Jitter = measured from 1kHz to 27MHz.
6. This is the maximum jitter for a BER of 10-12. The equivalent jitter value as per RP184 is 40ps max.

3. Input/Output Circuits

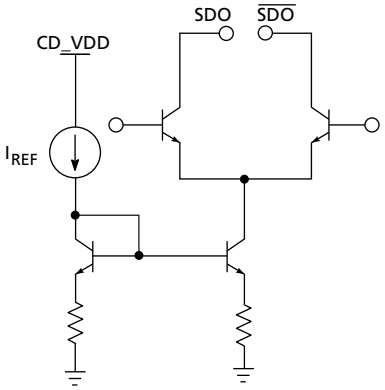


Figure 3-1: Differential Output Stage (SDO/SDO)

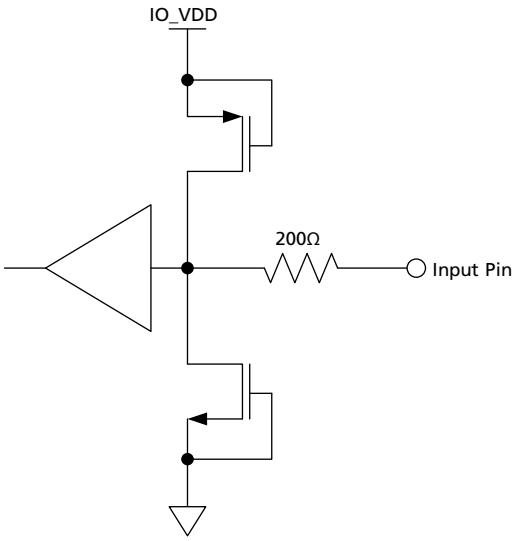


Figure 3-2: Digital Input Pin (20bit/10bit, ANC_BLANK, DETECT_TRS, DVB_ASI, RATE_SEL, SMPTE_BYPASS, TIM_861, F/DE, H/HSYNC, PCLK, V/VSYNC)

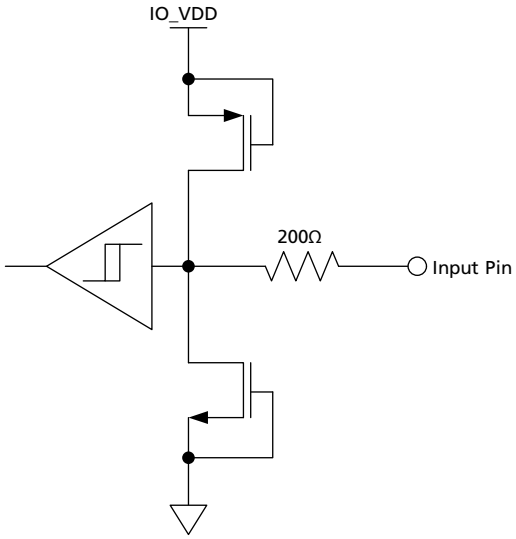


Figure 3-3: Digital Input Pin with Schmitt Trigger ($\overline{\text{RESET}}$)

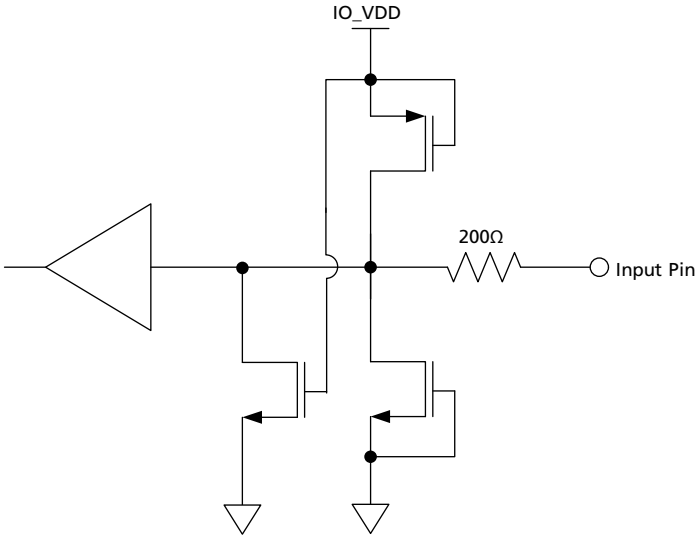


Figure 3-4: Digital Input Pin with weak pull-down - maximum pull-down current <110mA (JTAG/$\overline{\text{HOST}}$, STANDBY, SCLK_TCK, SDIN_TDI, TCK, TDI)

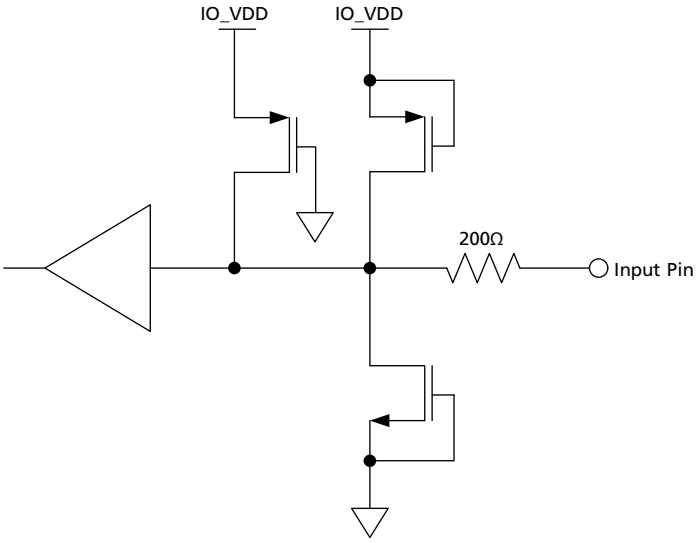


Figure 3-5: Digital Input Pin with weak pull-up - maximum pull-up current <110mA (ACLK1, ACLK2, AIN_7/8, AIN_5/6, AIN_3/4, AIN_1/2, $\overline{CS}$_TMS, GRP1_EN/$\overline{DIS}$, GRP2_EN/$\overline{DIS}$, IOPROC_EN/$\overline{DIS}$, SDO_EN/$\overline{DIS}$, TMS, WCLK1, WCLK2)

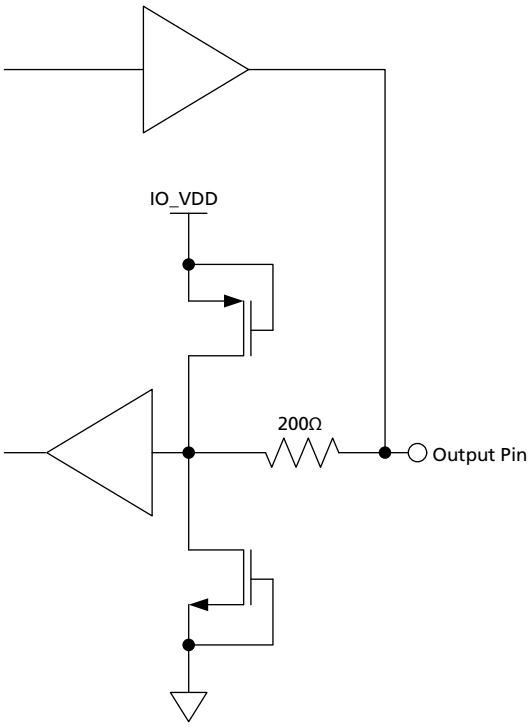


Figure 3-6: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to input at all times except in test mode. (DIN0, DIN2, DIN3, DIN4, DIN5, DIN6, DIN7, DIN8, DIN9, DIN10, DIN11, DIN12, DIN13, DIN14, DIN15, DIN16, DIN17, DIN18, DIN19, DIN1)

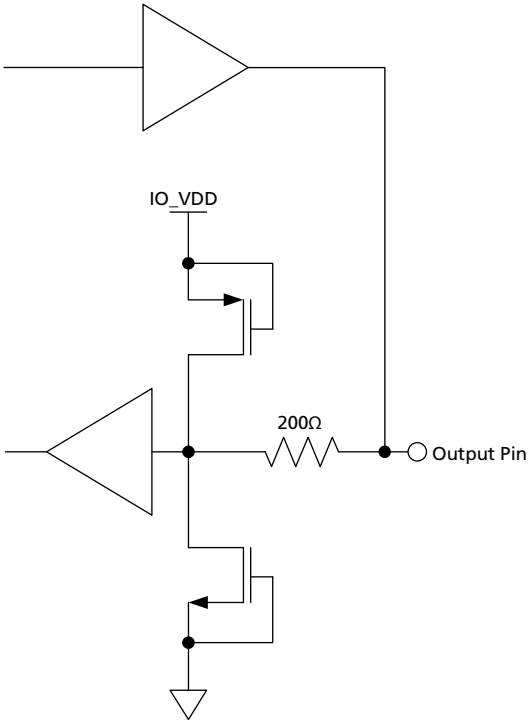


Figure 3-7: Bidirectional Digital Input/Output Pin with programmable drive strength. These pins are configured to output at all times except in reset mode. (LOCKED, AUDIO_INT, SDOUT_TDO, TDO)

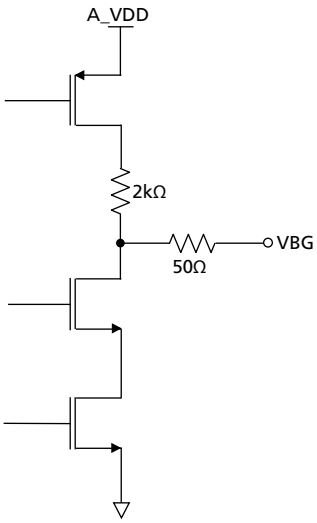


Figure 3-8: VBG

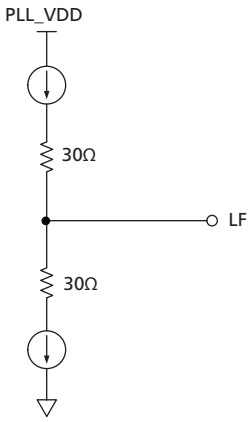


Figure 3-9: Loop Filter

4. Detailed Description

4.1 Functional Overview

The GS1672 is a Multi-Rate Transmitter with integrated SMPTE digital video processing and an integrated Cable Driver and embedded Audio Multiplexer. It provides a complete transmit solution at 1.485Gb/s, 1.485/1.001Gb/s or 270Mb/s.

The device has four basic modes of operation that must be set through external device pins: SMPTE mode, DVB-ASI mode, Data-Through mode and Standby mode.

In SMPTE mode, the device will accept 10-bit multiplexed or 20-bit demultiplexed SMPTE compliant data. By default, the device's additional processing features, including audio embedding, will be enabled in this mode.

In DVB-ASI mode, the GS1672 will accept an 8-bit parallel DVB-ASI compliant transport stream on DIN[17:10]. The serial output data stream will be 8b/10b encoded with stuffing characters added as per the standard.

Data-Through mode allows for the serializing of data not conforming to SMPTE or DVB-ASI streams. No additional processing will be done in this mode.

In addition, the device may be put into Standby, to reduce power consumption.

The serial digital output features a high-impedance mode and adjustable signal swing. The output slew rate is automatically set by the RATE_SEL pin setting.

The GS1672 provides several data processing functions; including generic ANC insertion, SMPTE 352M and EDH data packet generation and insertion, automatic video standards detection, and TRS, CRC, ANC data checksum, and line number calculation and insertion. These features are all enabled/disabled collectively using the external I/O processing pin, but may be individually disabled via internal registers accessible through the GSPI host interface.

Finally, the GS1672 contains a JTAG interface for boundary scan test implementations.

4.2 Parallel Data Inputs

Data signal inputs enter the device on the rising edge of PCLK, as shown in Figure 4-1.

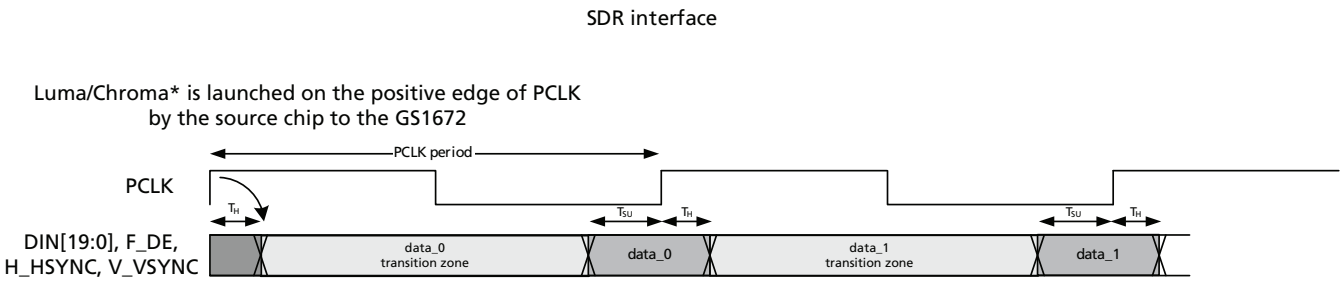


Figure 4-1: GS1672 Video Host Interface Timing Diagrams

Table 4-1: GS1672 Digital Input AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input data set-up time	t_{SU}	50% levels; 1.8V operation	1.2	–	–	ns
Input data hold time	t_{IH}		0.8	–	–	ns
Input data set-up time	t_{SU}	50% levels; 3.3V operation	1.3	–	–	ns
Input data hold time	t_{IH}		0.8	–	–	ns

Table 4-2: GS1672 Input Video Data Format Selections

Input Data Format	Pin/Register Bit Settings				DIN[9:0]	DIN[19:10]
	20BIT /10BIT	RATE _SEL	SMPTE _BYPASS	DVB_ASI		
20-bit demultiplexed HD format	HIGH	LOW	HIGH	LOW	Chroma	Luma
20-bit data Input HD format	HIGH	LOW	LOW	LOW	DATA	DATA
20-bit demultiplexed SD format	HIGH	HIGH	HIGH	LOW	Chroma	Luma
20-bit data input SD format	HIGH	HIGH	LOW	LOW	DATA	DATA
10-bit multiplexed HD format	LOW	LOW	HIGH	LOW	High Impedance	Luma/Chroma
10-bit data input HD format	LOW	LOW	LOW	LOW	High Impedance	DATA

Table 4-2: GS1672 Input Video Data Format Selections (Continued)

Input Data Format	Pin/Register Bit Settings				DIN[9:0]	DIN[19:10]
	20BIT /10BIT	RATE _SEL	SMPTE _BYPASS	DVB_ASI		
10-bit multiplexed SD format	LOW	HIGH	HIGH	LOW	High Impedance	Luma/Chroma
10-bit multiplexed SD format	LOW	HIGH	LOW	LOW	High Impedance	DATA
10-bit ASI input SD format	LOW	HIGH	LOW	HIGH	High Impedance	DVB-ASI data

The GS1672 is a high performance SD/HD-capable transmitter. In order to optimize the output jitter performance across all operating conditions, input levels and overshoot at the parallel video data inputs of the device need to be controlled. In order to do this, source series termination resistors should be used to match the impedance of the PCB data trace line. IBIS models can be used to simulate the board effects and then optimize the output drive strength and the termination resistors to allow for the best transition (one that produces minimal overshoot). If this is not viable, Gennum recommends matching the source series resistance to the trace impedance, and then adjusting the output drive strength to the minimum value that will give zero errors.

The above also applies to the PCLK input line. HVF and the Audio inputs should also be well terminated, however due to the lower data rates and transition density it is not as critical.

4.2.1 Parallel Input in SMPTE Mode

When the device is operating in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH), data must be presented to the input bus in either multiplexed or demultiplexed form, depending on the setting of the 20BIT/$\overline{\text{10BIT}}$ pin.

When operating in 20-bit mode (20BIT/$\overline{\text{10BIT}}$ = HIGH), the input data format must be word aligned, demultiplexed Luma and Chroma data (SD or HD).

When operating in 10-bit mode (20BIT/$\overline{\text{10BIT}}$ = LOW), the input data format must be multiplexed Luma (Y) and Chroma (C) data (SD, HD). C words precede Y words. In this mode, the data must be presented on the DIN[19:10] pins. The DIN[9:0] inputs are ignored.

4.2.1.1 Input Data Format in SDTI Mode

SDTI and HD-SDTI are a sub-set of SDI and HD-SDI formats. They may contain SDTI data on any line in the frame. Those lines which contain SDTI or HD-SDTI data are identified with an SDTI or HD-SDTI header packet in the HANC space.

The GS1672 does not differentiate between a signal carrying video and a signal carrying SDTI or HD-SDTI data in SD or HD formats. The user is responsible for ensuring that the headers and data are not corrupted.

4.2.2 Parallel Input in DVB-ASI Mode

The GS1672 is in DVB-ASI mode when the $\overline{\text{SMPTE\_BYPASS}}$ pin is set LOW, the DVB_ASI pin is set HIGH, and the RATE_SEL0 pin is set HIGH. In this mode, all SMPTE processing features are disabled.

When operating in DVB-ASI mode, the device must be set to 10-bit mode by setting the 20BIT/$\overline{\text{10BIT}}$ pin LOW. The device will accept 8-bit data words on DIN[17:10], where DIN17 = HIN is the most significant bit of the encoded transport stream data and DIN10 = AIN is the least significant bit. In addition, DIN19 and DIN18 will be configured as the DVB-ASI control signals INSSYNCIN and KIN respectively.

DIN19 = INSSYNCIN
DIN18 = KIN
DIN17~10 = HIN ~ AIN where AIN is the least significant bit of the transport stream data.

4.2.3 Parallel Input in Data-Through Mode

Data-Through mode is enabled when the $\overline{\text{SMPTE\_BYPASS}}$ pin and the DVB_ASI pin are LOW.

In this mode, data at the input bus is serialized without any encoding, scrambling or word alignment taking place.

The input data width is controlled by the setting of the 20BIT/$\overline{\text{10BIT}}$ pin as shown in Table 4-2 above.

NOTE: When in HD 10-bit mode, asserting the $\overline{\text{SMPTE\_BYPASS}}$ LOW to put the device in SMPTE-BYPASS mode will create video errors. If the user desires to use the device as a simple serializer in HD 10-bit mode, all video processing features may be disabled by setting the IOPROC_EN/$\overline{\text{DIS}}$ pin LOW.

4.2.4 Parallel Input Clock (PCLK)

The frequency of the PCLK input signal of the GS1672 is determined by the input data format and operating mode selection.

Table 4-3 below lists the input PCLK rates and input signal formats according to the external selection pins for the GS1672.

Table 4-3: GS1672 PCLK Input Rates

Input Data Format	Pin Settings				PCLK Rate
	20BIT/$\overline{10BIT}$	RATE_SEL	$\overline{SMPTE\_BYPASS}$	DVB-ASI	
20-bit demultiplexed HD format	HIGH	LOW	HIGH	X	74.25 or 74.25/1.001MHz
20-bit data input HD format	HIGH	LOW	LOW	LOW	74.25 or 74.25/1.001MHz
20-bit demultiplexed SD format	HIGH	HIGH	HIGH	LOW	13.5MHz
20-bit data input SD format	HIGH	HIGH	LOW	LOW	13.5MHz
10-bit multiplexed HD format	LOW	LOW	HIGH	LOW	148.5 or 148.5/1.001MHz
10-bit data input HD format	LOW	LOW	LOW	LOW	148.5 or 148.5/1.001MHz
10-bit multiplexed SD format	LOW	HIGH	HIGH	X	27MHz
10-bit data input SD format	LOW	HIGH	LOW	LOW	27MHz
10-bit ASI input SD format	LOW	HIGH	LOW	HIGH	27MHz

4.3 SMPTE Mode

The function of this block is to carry out data scrambling according to SMPTE 292M, and to carry out NRZ to NRZI encoding prior to presentation to the parallel to serial converter.

These functions are only enabled when the $\overline{SMPTE\_BYPASS}$ pin is HIGH.

In addition, the GS1672 requires the DVB_ASI pin to be set LOW to enable this feature.

4.3.1 H:V:F Timing

In SMPTE mode, the GS1672 can automatically detect the video standard and generate all internal timing signals. The total line length, active line length, total number of lines per field/frame and total active lines per field/frame are calculated for the received parallel video.

When DETECT_TRS is LOW, the video standard and timing signals are based on the externally supplied H_Blanking, V_Blanking, and F_Digital signals. These signals are supplied by the H/HSYNC, V/VSYNC and F/DE pins respectively. When DETECT_TRS is HIGH, the video standard timing signals will be extracted from the embedded TRS ID words in the parallel input data. Both 8-bit and 10-bit TRS code words will be identified by the device.

NOTE: I/O processing must be enabled for the device to remap 8-bit TRS words to the corresponding 10-bit value for transmission.

The GS1672 determines the video standard by timing the horizontal and vertical reference information supplied at the H/HSYNC, V/VSYNC, and F/DE input pins, or contained in the TRS ID words of the received video data. Therefore, full synchronization to the received video standard requires at least one complete video frame.

Once synchronization has been achieved, the GS1672 will continue to monitor the received TRS timing or the supplied H, V, and F timing information to maintain synchronization. The GS1672 will lose all timing information immediately following loss of H, V and F.

The H signal timing should also be configured via the H_CONFIG bit of the internal IOPROC register as either active line based blanking or TRS based blanking.

Active line based blanking is enabled when the H_CONFIG bit is set LOW. In this mode, the H input should be HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words. This is the default H timing used by the device.

The timing of these signals is shown in Figure 4-2, Figure 4-3, Figure 4-4 and Figure 4-5.

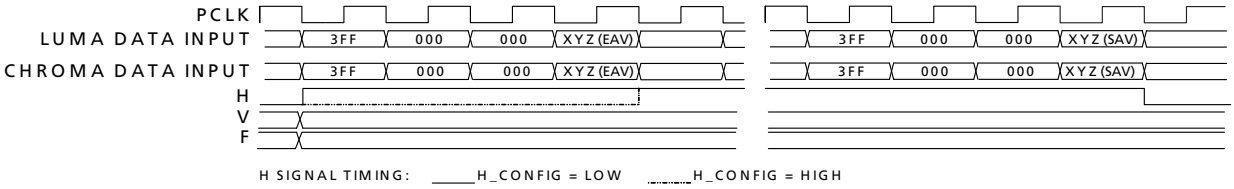


Figure 4-2: H:V:F Input Timing - HD 20-bit Input Mode

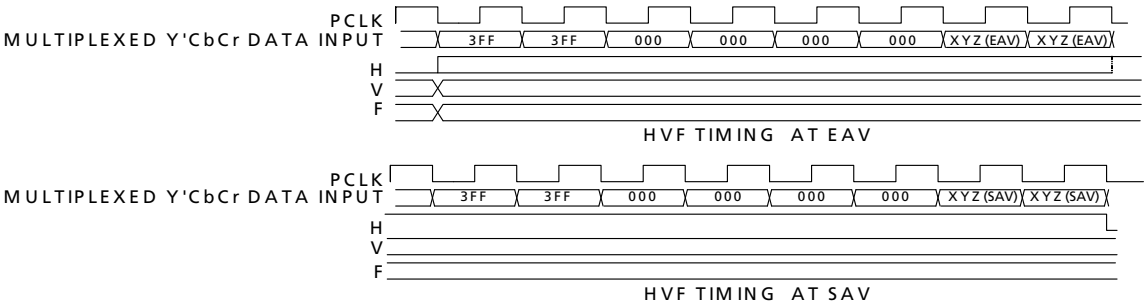


Figure 4-3: H:V:F Input Timing - HD 10-bit Input Mode

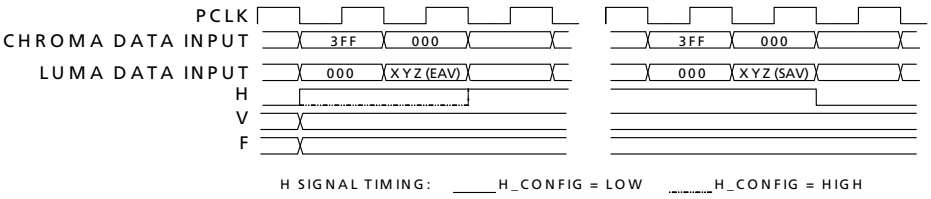


Figure 4-4: H:V:F Input Timing - SD 20-bit Mode

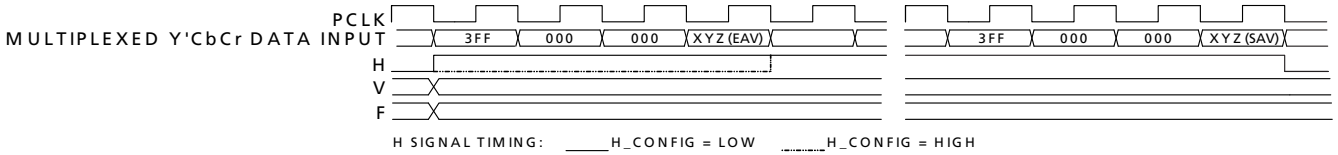


Figure 4-5: H:V:F Input Timing - SD 10-bit Mode

4.3.2 CEA 861 Timing

The GS1672 extracts timing information from externally provided HSYNC, VSYNC, and DE signals when CEA 861 timing mode is selected by setting DETECT_TRS = LOW and TIM_861 = HIGH.

Horizontal sync (H), Vertical sync (V), and Data Enable (DE) timing must be provided via the H/HSYNC, V/VSYNC and F/DE input pins. The host interface register bit H_CONFIG is ignored in CEA 861 input timing mode.

The GS1672 determines the EIA/CEA-861 standard and embeds EAV and SAV TRS words in the output serial video stream.

Video standard detection is not dependent on the HSYNC pulse width or the VSYNC pulse width and therefore the GS1672 tolerates non-standard pulse widths. In addition, the device can compensate for up to ±1 PCLK cycle of jitter on VSYNC with respect to HSYNC and sample VSYNC correctly.

NOTE 1: The period between the leading edge of the HSYNC pulse and the leading edge of Data Enable (DE) must follow the timing requirements described in the EIA/CEA-861 specification. The GS1672 embeds TRS words according to this timing relationship to maintain compatibility with the corresponding SMPTE standard.

NOTE 2: When CEA 861 standards 6 & 7 [720(1440)x480i] are presented to the GS1672, the device embeds TRS words corresponding to the timing defined in SMPTE 125M to maintain SMPTE compatibility.

CEA 861 standards 6 & 7 [720(1440)x480i] define the active area on lines 22 to 261 and 285 to 524 inclusive (240 active lines per field). SMPTE 125M defines the active area on lines 20 to 263 and 283 to 525 inclusive (244 lines on field 1, 243 lines on field 2).

Therefore, in the first field, the GS1672 adds two active lines above and two active lines below the original active image. In the second field, it adds two lines above and one line below the original active image.

The CEA861 Timing Formats are summarized in Table 4-4. and are shown in Figure 4-6 to Figure 4-14.

Table 4-4: CEA861 Timing Formats

Format	Parameters
4	H:V:DE Input Timing 1280 x 720p @ 59.94/60Hz
5	H:V:DE Input Timing 1920 x 1080i @ 59.94/60Hz
6&7	H:V:DE Input Timing 720 (1440) x 480i @ 59.94/60Hz
19	H:V:DE Input Timing 1280 x 720p @ 50Hz
20	H:V:DE Input Timing 1920 x 1080i @ 50Hz
21&22	H:V:DE Input Timing 720 (1440) x 576 @ 50Hz
32	H:V:DE Input Timing 1920 x 1080p @ 23.94/24Hz
33	H:V:DE Input Timing 1920 x 1080p @ 25Hz
34	H:V:DE Input Timing 1920 x 1080p @ 29.97/30Hz

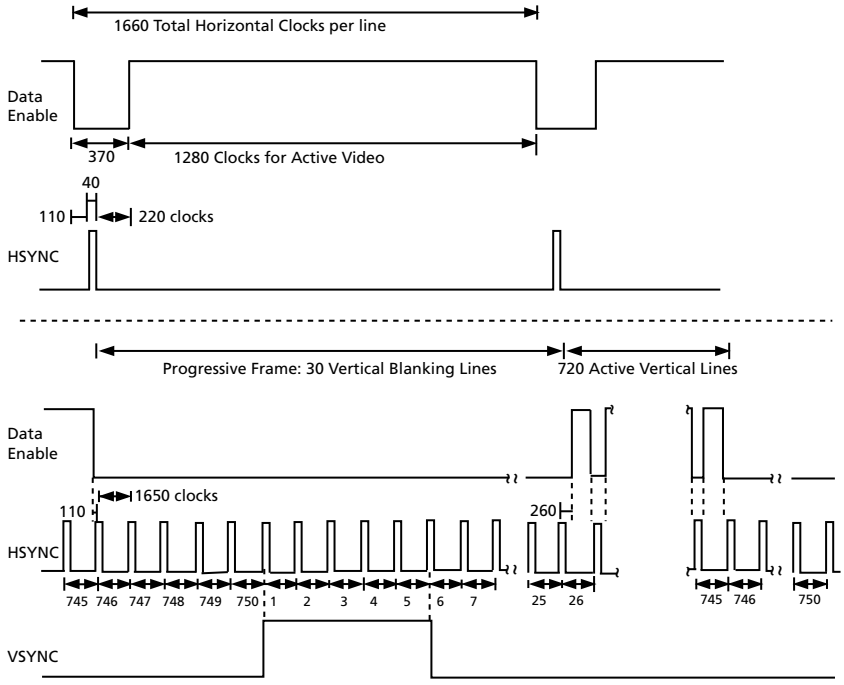


Figure 4-6: H:V:DE Input Timing 1280 x 720p @ 59.94/60 (Format 4)

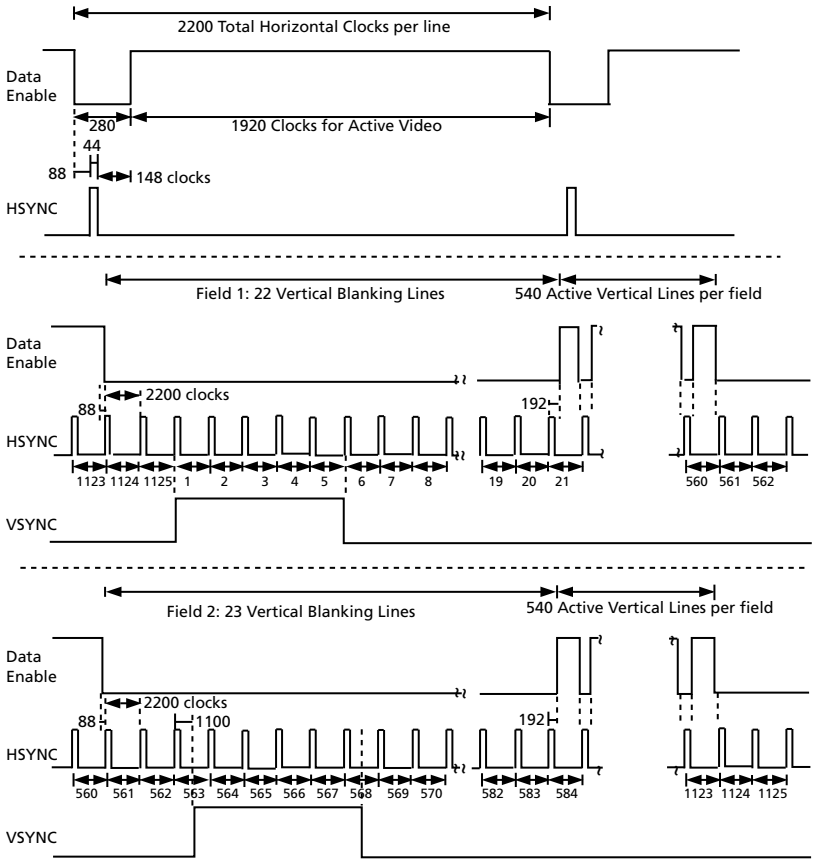


Figure 4-7: H:V:DE Input Timing 1920 x 1080i @ 59.94/60 (Format 5)

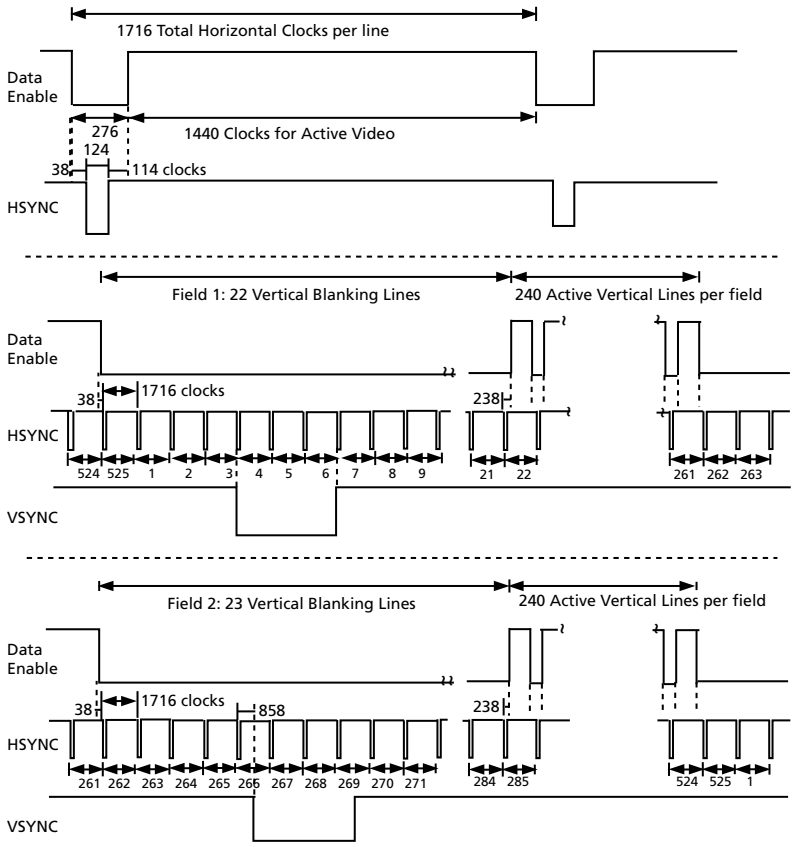


Figure 4-8: H:V:DE Input Timing 720 (1440) x 480i @ 59.94/60 (Format 6&7)

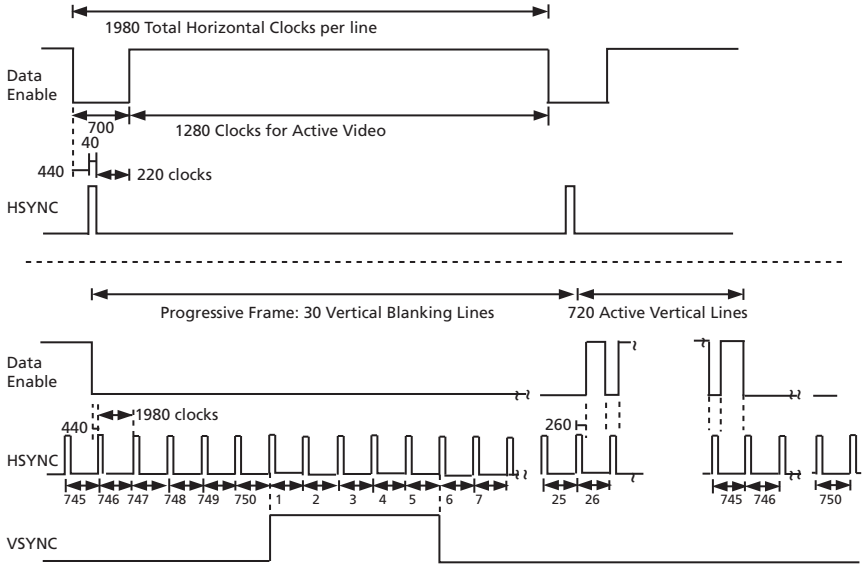


Figure 4-9: H:V:DE Input Timing 1280 x 720p @ 50 (Format 19)

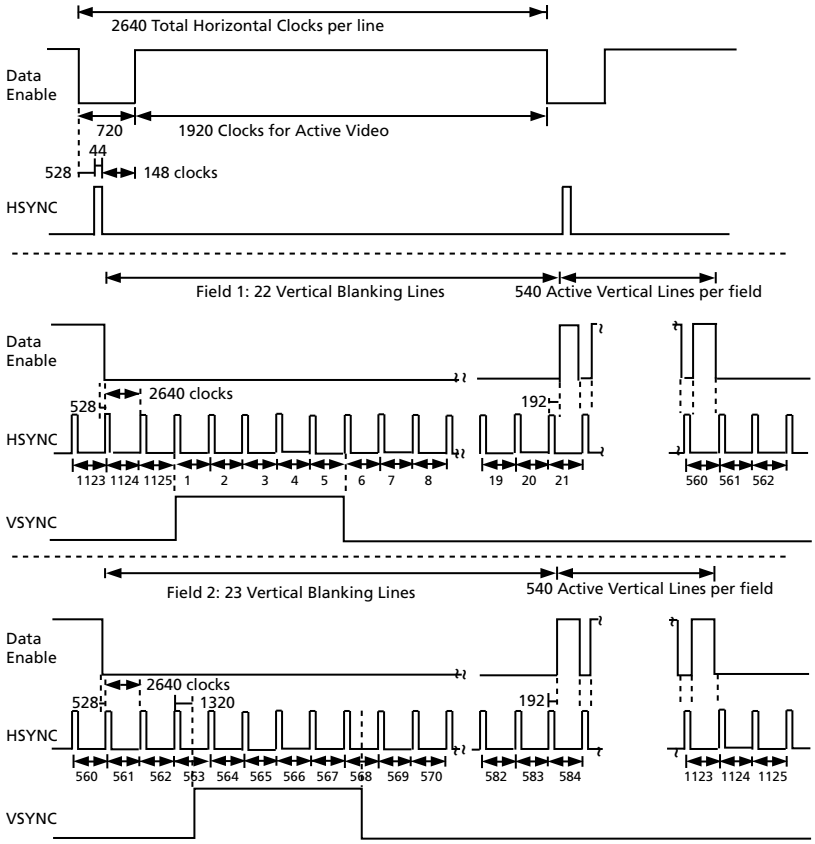


Figure 4-10: H:V:DE Input Timing 1920 x 1080i @ 50 (Format 20)

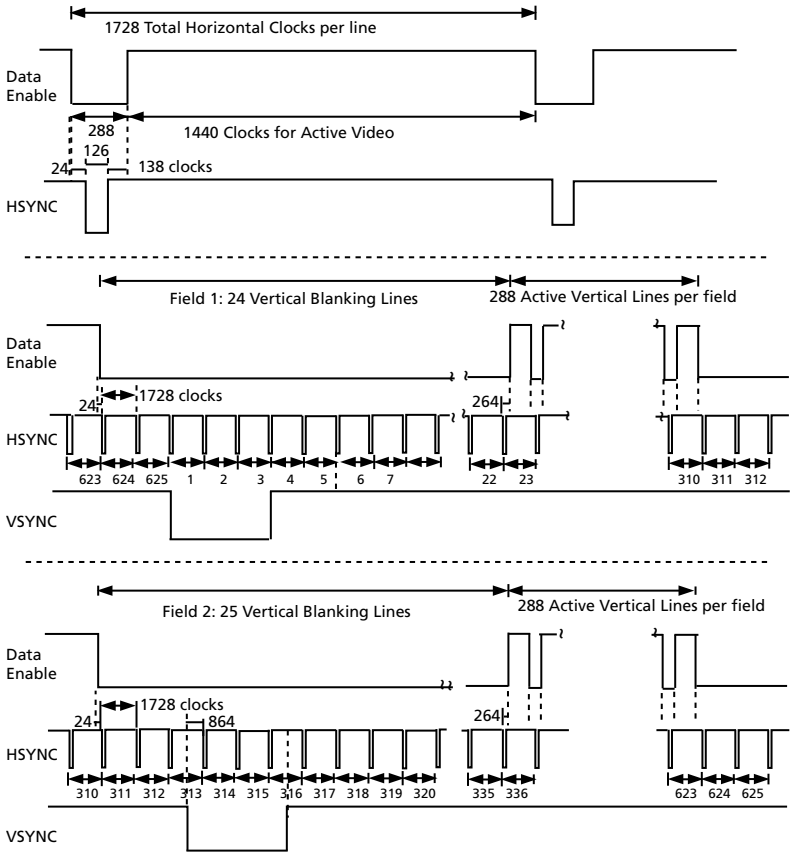


Figure 4-11: H:V:DE Input Timing 720 (1440) x 576 @ 50 (Format 21&22)

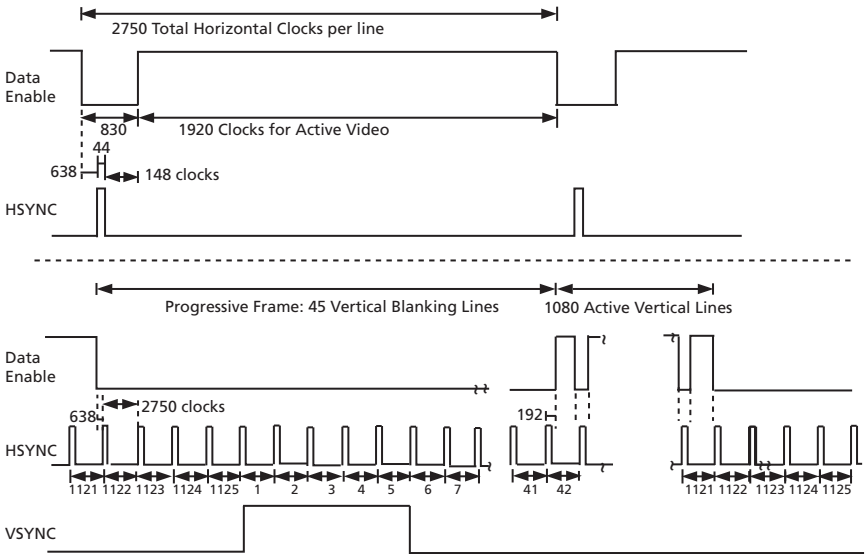


Figure 4-12: H:V:DE Input Timing 1920 x 1080p @ 23.94/24 (Format 32)

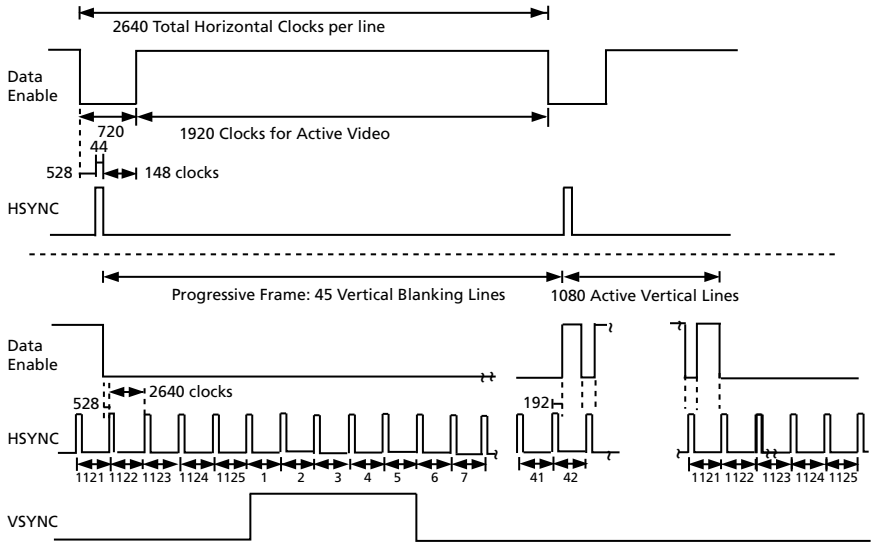


Figure 4-13: H:V:DE Input Timing 1920 x 1080p @ 25 (Format 33)

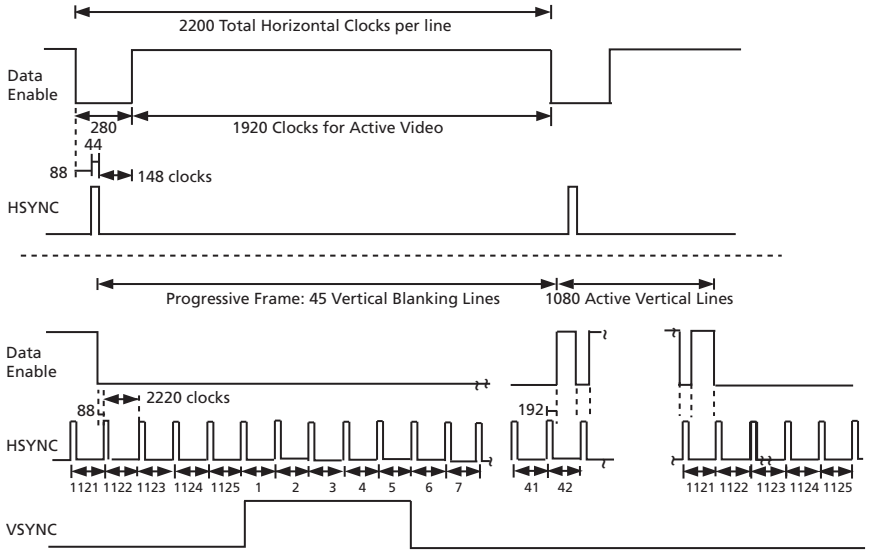


Figure 4-14: H:V:DE Input Timing 1920 x 1080p @ 29.97/30 (Format 34)

4.4 DVB-ASI Mode

When operating in DVB-ASI mode, all SMPTE processing features are disabled, and the device accepts 8-bit transport stream data and control signal inputs on the DIN[19:10] port.

This mode is only enabled when $\overline{\text{SMPTE\_BYPASS}}$ pin is LOW, DVB_ASI pin is HIGH and the RATE_SEL pin is HIGH.

The interface consists of eight data bits and two control signals, INSSYNCIN and KIN.

When INSSYNCIN is set HIGH, the GS1672 inserts K28.5 sync characters into the data stream. This function is used to assist system implementations where the GS1672 may be preceded by a data FIFO.

The FIFO can be fed data at a rate somewhat less than 27MHz. The 'FIFO empty' signal could be used to feed the INSSYNCIN pin, causing the GS1672 to pad the data up to the transmission rate of 27MHz.

When KIN is set HIGH the data input is interpreted as a special character (such as a K28.5 sync character), as defined by the DVB-ASI standard. When KIN is set LOW the input is interpreted as data.

After sync signal insertion, the GS1672 8b/10b encodes the data, generating a 10-bit data stream for the parallel to serial conversion and transmission process.

4.5 Data-Through Mode

The GS1672 may be configured to operate as a simple parallel-to-serial converter. In this mode, the device passes data to the serial output without performing any scrambling or encoding.

Data-through mode is enabled only when both the $\overline{\text{SMPTE\_BYPASS}}$ and DVB_ASI pins are set LOW.

4.6 Standby Mode

The STANDBY pin reduces power to a minimum by disabling all circuits except for the register configuration. Upon removal of the signal to the STANDBY pin, the device returns to its previous operating condition within 1 second, without requiring input from the host interface.

In addition, the serial digital output signals becomes high-impedance when the device is powered-down.

4.7 Audio Embedding

The GS1672 includes an Audio Multiplexer, which by default will be active when the Transmitter is configured for SMPTE mode.

Audio embedding is controlled by:

- GRP1_EN/$\overline{\text{DIS}}$ and GRP2_EN/$\overline{\text{DIS}}$ pins are set HIGH to enable embedding of their respective groups
- The AUDIO_INS bit in the IOPROC register is set LOW to enable audio embedding
- The IOPROC_EN/$\overline{\text{DIS}}$ pin is set HIGH to enable audio embedding

In non-SMPTE modes, the Audio Multiplexer will be powered down to reduce power.

NOTE: When audio is embedded by the GS1672, if either of the GRP1_EN/$\overline{\text{DIS}}$ or GRP2_EN/$\overline{\text{DIS}}$ pins are toggled, the output video stream is lost.

Toggling the audio disable pins on the fly must be avoided. The user has to set the pins before resetting the chip, and not change the setting during normal operation. The audio may be enabled or disabled during the operation of the chip by writing to the Host Interface registers. SD audio group embedding may be enabled, or disabled, by writing to ACT1...ACT8 bits of register 40Fh. HD audio group embedding may be enabled, or disabled, by writing to ACT1...ACT8 bits of register 80Eh.

4.7.1 Serial Audio Data Inputs

The GS1672 supports the insertion of up to 8 channels of embedded audio, in two groups of 4 channels.

Each audio group has a dedicated audio group enable input pin; a Word Clock (WCLK) input pin operating at 48kHz; an Audio Clock input pin (ACLK) operating at 3.072MHz (64 x WCLK); and two serial digital audio input pins (AIN_1/2, etc.), supporting one stereo audio signal pair per pin.

The Serial Audio Data Inputs for each audio group are listed in Table 4-5.

Table 4-5: Serial Audio Input Pin Description

Pin Name	Description
Audio Group 1	
GRP1_EN/$\overline{DIS}$	Enable Input for Audio Group 1
AIN_1/2	Serial Audio Input; Channels 1 and 2
AIN_3/4	Serial Audio Input; Channels 3 and 4
ACLK1	64 x WCLK associated with AIN_1/2 and AIN_3/4 (channels 1, 2, 3and 4)
WCLK1	48kHz Word Clock associated with AIN_1/2 and AIN_3/4 (channels 1, 2, 3 and 4)
Audio Group 2	
GRP2_EN/$\overline{DIS}$	Enable Input for Audio Group 2
AIN_5/6	Serial Audio Input; Channels 5 and 6
AIN_7/8	Serial Audio Input; Channels 7 and 8
ACLK2	64 x WCLK associated with AIN_5/6 and AIN_7/8 (channels 5, 6, 7 and 8)
WCLK2	48kHz Word Clock associated with AIN_5/6 and AIN_7/8 (channels 5, 6, 7 and 8)

The serial audio input signals and WCLK input signals will enter the device on the rising edge of ACLK as shown in Figure 4-15.

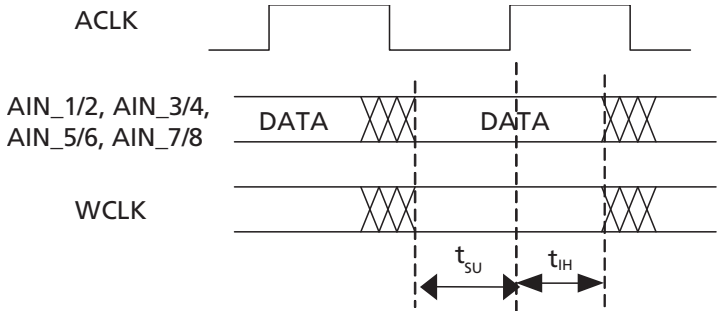


Figure 4-15: ACLK to Data and Control Signal Input Timing

Table 4-6: GS1672 Serial Audio Data Inputs - AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input data set-up time	t_{SU}	50% levels; 3.3v or 1.8v operation	1.3	–	–	ns
Input data hold time	t_{IH}		0.8	–	–	ns

When GRP1_EN/$\overline{DIS}$ and GRP2_EN/$\overline{DIS}$ are set HIGH, the respective audio group is enabled, and the audio input signals associated with that group are processed and embedded into the video data stream.

When GRP1_EN/$\overline{DIS}$ and GRP2_EN/$\overline{DIS}$ are set LOW, the respective audio group is disabled and the audio input signals associated with that group are ignored. In addition, all functional logic associated with audio insertion for the disabled audio group is placed in a static operating mode, such that system power is reduced while the device configuration is retained.

4.7.2 Serial Audio Data Format Support

The GS1672 supports the following serial audio data formats:

- I^2S Audio (default)
- AES/EBU
- Serial Audio, Left Justified, MSB First
- Serial Audio, Left Justified, LSB First
- Serial Audio, Right Justified, MSB First
- Serial Audio, Right Justified, LSB First

By default (at power up or after system reset), the I^2S data format is enabled.

The audio format can be different for both audio groups. Normally, AIN_1/2 and AIN_3/4 are embedded in Audio Group A, and AIN_5/6 and AIN_7/8 are embedded in Audio Group B. As well, the audio formats can be different within the same group.

Under normal conditions:

AMA sets the audio format for AIN_1/2
AMB sets the audio format for AIN_3/4
AMC sets the audio format for AIN_5/6
AMD sets the audio format for AIN_7/8

NOTE: These four formats can all be set to different modes if desired.

Table 4-7 shows the audio input formats for the GS1672. Note that the same values apply for AMB + LSB_FIRSTB, AMC + LSB_FIRSTC and AMD + LSB_FIRSTD.

Table 4-7: Audio Input Formats

AMA[1:0] (Address 40Bh for SD, Address 80Ah for HD)	LSB_FIRSTA (Address 40Fh for SD, Address 80Eh for HD)	Audio Input Formats
00	X	AES/EBU audio input
01	0	Serial audio input: Left Justified; MSB first
01	1	Serial audio input: Left Justified; LSB first
10	0	Serial audio input: Right Justified; MSB first

Table 4-7: Audio Input Formats (Continued)

AMA[1:0] (Address 40Bh for SD, Address 80Ah for HD)	LSB_FIRSTA (Address 40Fh for SD, Address 80Eh for HD)	Audio Input Formats
10	1	Serial audio input: Right Justified; LSB first
11	X	1^2S (default)

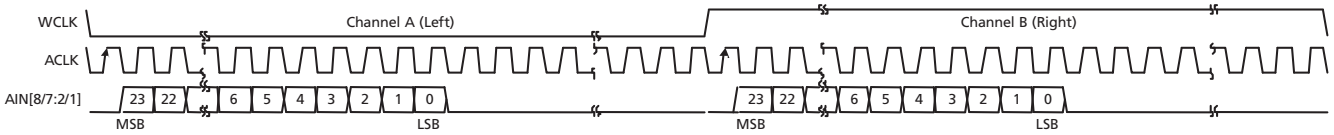


Figure 4-16: I^2S Audio Input Format

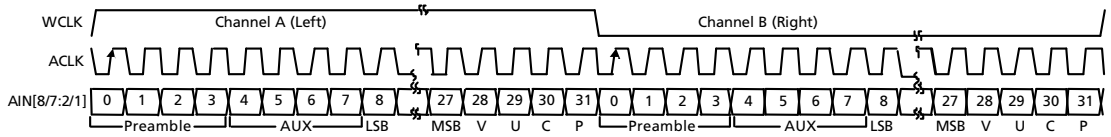


Figure 4-17: AES/EBU Audio Input Format

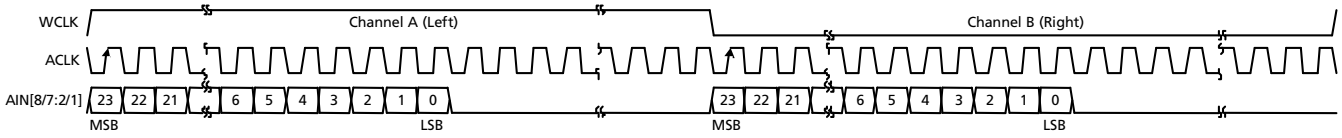


Figure 4-18: Serial Audio, Left Justified, MSB First

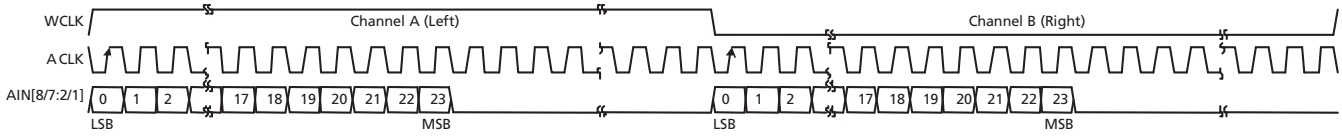


Figure 4-19: Serial Audio, Left Justified, LSB First

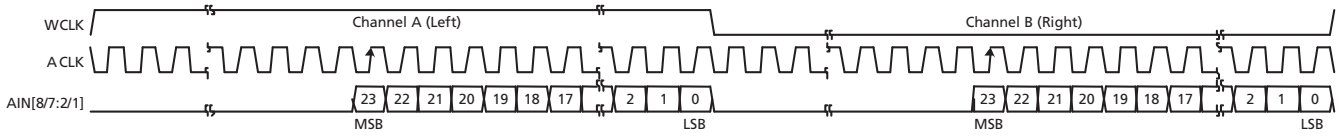


Figure 4-20: Serial Audio, Right Justified, MSB First

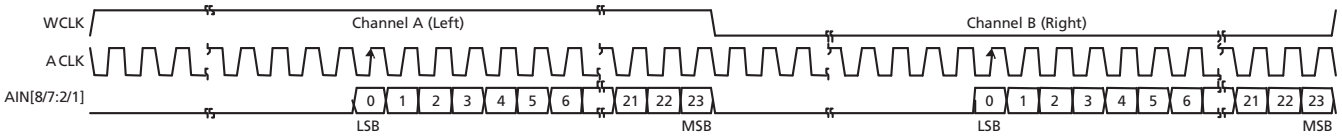


Figure 4-21: Serial Audio, Right Justified, LSB First

4.7.3 HD Mode

When the GS1672 is operating in HD mode, 8 channels of audio in 4 pairs are embedded in the serial output signal, according to SMPTE 299M-2004.

The 8 channels will be in 2 groups, which are selectable via the host interface from the 4 groups allowed by SMPTE 299M-2004. The default group is Group One and Group Two.

4.7.4 SD Mode

When the GS1672 is operating in SD mode, eight channels of audio in four pairs are embedded in the serial output signal, according to SMPTE 272M. The eight channels will be in two groups, which are selectable via the host interface from the four groups allowed by SMPTE 272M. The default group is Group One and Group Two.

4.7.5 Audio Embedding Operating Modes

Audio Embedding operates in one of three distinct modes:

1. Normal Mode (Default)

All previously embedded audio packets are deleted from the video stream.
Arbitrary packets, SDTI packets and SMPTE 352M packets are not deleted.
Up to two audio groups can be added to the video output.
SDTI packets and SMPTE 352M packets are placed before the audio packets.
Arbitrary packets are placed after the audio packets.

2. Cascade Mode

No previously embedded packets are deleted from the video stream.
Up to two audio groups can be added to the video output.
The added audio groups will not replace existing embedded audio groups.
The added audio packets are appended to the last packet in the video input.

3. Group Replacement Mode

No previously embedded packets are deleted from the video stream.
Up to two audio groups can be added to the video output.
The added audio groups replace any embedded audio groups with the same group number.
The embedded audio groups are sorted in ascending order by audio group number.
SDTI packets and SMPTE 352M packets are placed before the audio packets.
Arbitrary packets are placed after the audio packets.
The operating mode is selected using a combination of the EN_CASCADE and the AGR bits in the host interface, as stated in Table 4-8 below.

Table 4-8: GS1672 Audio Operating Mode Selection

Control Signals	Operating Mode
EN_CASCADE=0, AGR=0	Normal Mode
EN_CASCADE=1, AGR=0	Cascade Mode
EN_CASCADE=0, AGR=1	Group Replacement Mode
EN_CASCADE=1, AGR=1	Group Replacement Mode

4.7.6 Audio Packet Detection

The input video stream to the GS1672 may already contain embedded audio packets.

The GS1672 detects these embedded packets, and signals their presence to the host interface. Register 404h is used for SD, register 803h is used for HD.

4.7.7 Audio Packet Deletion

In **Normal Mode** (default), the GS1672 deletes all audio packets from the input video data stream.

In **Cascade Mode**, the GS1672 does not delete any audio packets from the input video data stream.

In **Group Replacement Mode**, the GS1672 does not delete any audio packets from the input video data stream.

In all operating modes, the GS1672 deletes all audio packets from the input video stream if any embedded audio packets do not fully comply with the SMPTE 291M-1998 standard.

4.7.8 Audio Packet Detection and Deletion

In SD modes, the first Ancillary Data Flag (ADF) must always be contiguous after the EAV words. For HD mode, the first ADF must always be contiguous after the two line CRC words.

Ancillary data packets with non-audio data ID words, such as arbitrary, EDH (SD only), SDTI header and SMPTE 352M, are not deleted from the data stream. On lines where SMPTE 352M or SDTI header packets exist, the audio data packets must be contiguous from the 352M and SDTI packets. If this is not the case, all existing audio data and control packets will be deleted.

When CASCADE is set HIGH, all pre-existing audio data and control packets remain in the video stream.

When the AGR bit in the host interface is set HIGH, Audio Group Replacement mode is selected. In this mode, existing audio data and control packets are not deleted from the data stream.

In cases where the ADF is not placed immediately after the CRC or EAV words, or there are gaps between the packets, the audio core deletes all existing audio data and control packets, regardless of the CASCADE or AGR setting. Figure 4-22 shows an example of correct and incorrect placement of ancillary data packets for SD Mode.

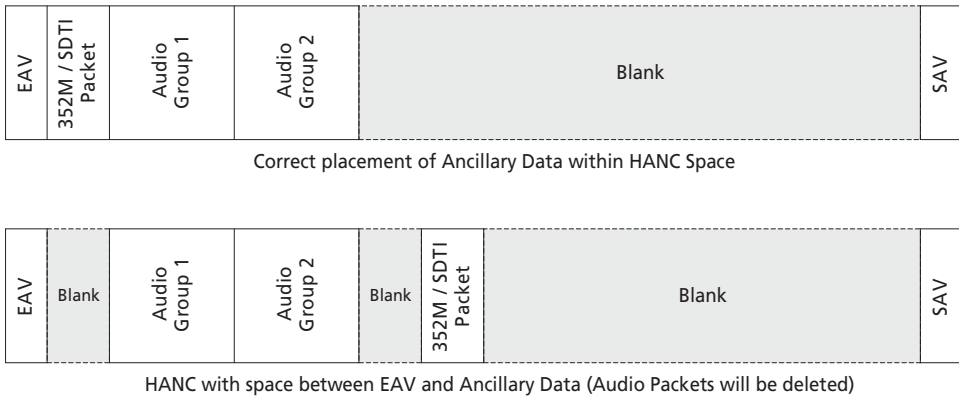


Figure 4-22: Ancillary Data Packet Placement Example for SD Mode

4.7.9 Audio Mute (Default Off)

The GS1672 mutes all of the input channels when the MUTE_ALL host interface bit is set HIGH.

The GS1672 mutes any individual audio inputs as commanded by the following host interface fields:

MUTE1 - Mute input channel 1

MUTE2 - Mute input channel 2

MUTE3 - Mute input channel 3

MUTE4 - Mute input channel 4

MUTE5 - Mute input channel 5

MUTE6 - Mute input channel 6

MUTE7 - Mute input channel 7

MUTE8 - Mute input channel 8

4.7.10 Audio Channel Status

The GS1672 adds audio channel status to those audio input channels that do not use the AES/EBU format.

The Audio Channel Status block complies with the AES3-1992 (ANSI S4.40-1992) standard.

The GS1672 uses the ACSR[183:0] host interface field as the source of audio channel status for those input channels that do not use the AES/EBU format.

The GS1672 replaces the Audio Channel Status block in all eight channels as commanded by the ACS_REGEN host interface bit. The status block information is supplied by the ACSR[183:0] host interface field.

The ACS_REGEN bit (SD core register 403h, HD/3G core register 802h) is set in two states:

ACS_REGEN = 0 -> Incoming Audio Channel Status is passed through the device to the output. For I^2S audio formats, the transmitter will embed default audio channel status to the output stream.

ACS_REGEN = 1 -> Channel Status is based on user-defined data stored in the ACSR. With ACS_REGEN = 1, the GS1672 will serialize user-defined information to the output data. The user-defined data is applied to the output when the following steps are followed, and the time that the new status boundary occurs for the audio channel.

Audio channel status replacement follows the same procedure when replacing audio channel status for either AES or I^2S audio formats.

To replace audio channel status, the following procedure should be used:

1. Write the desired ACS data to the ACSR [183:0] (SD Core registers 420h-42Ch, HD/3G Core registers 820h-82Ch).
2. Set ACS_REGEN bit = 1.
3. The Audio Channel Status on the serialized output will now contain the user defined ACS data.

To replace audio channel status on the fly, the following procedure should be used:

1. Write the desired ACS data to the ACSR [183:0] (SD Core registers 420h-42Ch, HD/3G Core registers 820h-82Ch)
2. Set ACS_REGEN bit = 1, if ACS_REGEN is already set, re-write ACS_REGEN = 1 again.
3. The Audio Channel Status on the serialized output will now contain the user-defined ACS data.

The GS1672 automatically calculates the CRC required for the Audio Channel Status block.

4.7.11 Audio Crosspoint

The GS1672 is capable of mapping any input channel to any Primary or Secondary group channel.

Each group channel specifies the audio source using a 3-bit selector defined below in Table 4-9:

Table 4-9: GS1672 SD Audio Crosspoint Channel Selection

Audio Source	SD Selector	HD Selector
Input channel 1	000	000
Input channel 2	001	001
Input channel 3	010	010
Input channel 4	011	011
Input channel 5	100	100
Input channel 6	101	101
Input channel 7	110	110
Input channel 8	111	111

Each Primary and Secondary group channel specifies the audio source using the following host interface fields:

Table 4-10: Audio Source Host Interface Fields

Host Interface Field	Description	Default
GPA_CH1_SRC[2:0]	Primary Group Channel 1 Source Selector	000
GPA_CH2_SRC[2:0]	Primary Group Channel 2 Source Selector	001
GPA_CH3_SRC[2:0]	Primary Group Channel 3 Source Selector	010
GPA_CH4_SRC[2:0]	Primary Group Channel 4 Source Selector	011
GPB_CH1_SRC[2:0]	Secondary Group Channel 1 Source Selector	100
GPB_CH2_SRC[2:0]	Secondary Group Channel 2 Source Selector	101
GPB_CH3_SRC[2:0]	Secondary Group Channel 3 Source Selector	110
GPB_CH4_SRC[2:0]	Secondary Group Channel 4 Source Selector	111

Audio channels can be paired only when both channels are derived from the same Word Clock and are synchronous.

The same audio channel cannot be used in both Primary and Secondary groups at the same time.

The GS1672 asserts the XPOINT_ERROR host interface bit if any audio channel is programmed to be included in both the Primary and Secondary groups.

4.7.12 Audio Word Clock

When the GS1672 combines two stereo pair inputs into one audio group, the format allows for only one Word Clock, or sampling clock.

For the Primary group, the GS1672 uses the Word Clock associated with the source selected by the GPA_WCLK_SRC[2:0] host interface field. If in SD mode, address 40Ch. If in HD mode, address 80Bh.

For the Secondary group, the GS1672 uses the Word Clock associated with the source selected by the GPB_WCLK_SRC[2:0] host interface field. If in SD mode, address 40Dh. If in HD mode, address 80Ch.

For proper operation, the combined Stereo Pair inputs must have identical Word Clocks. WCLK is not required for AES/EBU audio.

4.7.13 Channel & Group Activation

The GS1672 embeds Primary group packets when any of the following host interface bits are set and the associated audio group enable pin is HIGH:

ACT1 Embed Primary group audio channel 1
ACT2 Embed Primary group audio channel 2
ACT3 Embed Primary group audio channel 3
ACT4 Embed Primary group audio channel 4

If none of the bits are set, then no audio will be embedded.

The GS1672 will embed Secondary group packets when any of the following host interface bits are set and the associated audio group enable pin is HIGH:

ACT5 Embed Secondary group audio channel 1
ACT6 Embed Secondary group audio channel 2
ACT7 Embed Secondary group audio channel 3
ACT8 Embed Secondary group audio channel 4

When an embedded packet contains one or more channels with the ACTx bit set to zero, the GS1672 replaces the data for those channels with null samples (all bits set to zero).

In the default state, the GS1672 embeds all audio channels in accordance with the setting of the respective audio group enable pins of the device.

4.7.14 Audio FIFO - SD

Each input channel has a First In First Out (FIFO) buffer that can hold up to 52 samples.

Samples are added (written) to the FIFO as they are received from the audio inputs.

Samples are removed (read) from the FIFO as they are embedded in audio data packets and audio extended packets.

After power up, reset or clear, the FIFO is in the start-up state where it will output zeroes until it has accumulated the start-up count of 26 samples.

When the start-up state ends, the buffer operates as a normal FIFO, and expects to receive an equal number of read and write operations over the period of five frames. At the end of five frames, the FIFO still has 26 samples in the buffer.

When the FIFO does not receive an equal number of read and write operations, the FIFO checks for the overflow and underflow conditions.

When a sample is required for embedding into a packet and the FIFO is holding less than 6 samples, the GS1672 prevents the underflow condition by repeating the last sample without removing a sample from the FIFO. Therefore, a sample will be duplicated.

When an input sample is received and the FIFO has room for less than six more samples, the GS1672 prevents the overflow condition by discarding the sample. Therefore, a sample will be dropped.

If 28 consecutive samples are duplicated or dropped, the audio FIFO is cleared and placed into the start-up state.

If the CLEAR_AUDIO host interface bit is set, the audio FIFO is cleared and put into the start-up state.

When the detected video standard changes, the audio FIFO is cleared and put into the start-up state.

The buffer size and start-up count can be reduced using the OS_SEL host interface field, as seen in Table 4-11 below:

Table 4-11: GS1672 SD Audio Buffer Size Selection

Address OS_SEL[1:0]	Buffer Size	Start-Up Count
00	52 samples (default)	26 samples
01	24 samples	12 samples
10	12 samples	6 samples
11	Reserved	Reserved

4.7.15 Audio FIFO - HD

For HD formats, the audio FIFO block is a maximum of seven samples deep. According to SMPTE 299M, audio samples are multiplexed immediately in the next HANC region after the audio sample occurs. A buffer size of seven samples takes into account that there are no samples after the switching line (for one line) and the worst-case video standard of 720p/24, plus a one-sample safety margin.

Due to the sample distribution used in HD video standards and the size of the buffer in HD mode, no checking is made for buffer underflow/overflow conditions. The pointers should maintain a variable offset between 0 and 6.

4.7.16 Five-frame Sequence Detection - SD

The GS1672 detects the frame sequence that describes the sample distribution for synchronous audio.

The frame sequence is used in the generation of audio control packets; where the Audio Frame Number (AFN) field describes the position of the current frame within the frame sequence.

The frame sequence is also used in the generation of Audio Sample Distribution for formats with 525 lines. Each frame has 1602 samples or 1601 samples, depending upon the frame sequence.

The GS1672 sets the AFN of the Primary group control packets to zero, unless the AFNA_AUTO host interface bit (400h bit 7) is set to produce automatic AFN generation.

The Multiplexer sets the AFN of the Secondary group control packets to zero unless the AFNB_AUTO host interface bit (800h bit 10) is set to produce automatic AFN generation.

When the frame rate is 25Hz, every frame has 1920 samples and the AFN is always set to one.

When the frame rate is 29.97Hz, an even number of samples (8008) are distributed over five frames in the following sequence:

1602 1601 1602 1601 1602

The GS1672 sets the AFN field to a number between one and five, depending on where the current frame lies within the sequence.

The GS1672 adds the offset specified in the AFN_OFS host interface field (400h bits 6-4) to the generated AFN. The result of the addition wraps around such that the AFN will always be in the range of one to five.

4.7.16.1 525-Line Audio Sample Distribution

As per the SMPTE 272M standard, the following sample distribution allows the embedding of 16 channels (4 audio groups) of 24-bit sampled audio into the HANC of 525-line based video formats.

The sample distribution is established for Group One and then offset by one line for each subsequent group. The sample distribution is as follows (start line is 12):

$\{[3]^{(10+G)},([4],[3]^{15})^{15},[4],[3]^{(11-G)},[0],[3]^{(3+G)},([4],[3]^{15})^{15},[4/3],[3]^{12},[4],[3]^{(4-G)},[0]\}^{5}$

[#] = Number of samples / line
[4/3] = One line with either 3 or 4 samples depending on five-frame sequence
$^{(\#)}$ = Number of times to repeat the sequence. When this # is 0, no samples are inserted
G = Audio group number from 1 to 4
$\{\ldots\}^{5}$ = 5-frame sequence as shown in Table 4-12:

Table 4-12: GS1672 SD Audio Five Frame Sequence Sample Count

Frame	Number of Samples
1	1602
2	1601
3	1602
4	1601
5	1602

The following tables show the audio sample distribution for each of the four audio groups.

Each distribution has 525 lines.

Each distribution has 1602 samples or 1601 samples, based on the frame number in the five-frame sequence.

When 1602 samples are required in a frame, the [4/3] term represents a line with four samples.

When 1601 samples are required in a frame, the [4/3] term represents a line with three samples.

Table 4-13: GS1672 SD Audio Group 1 Audio Sample Distribution - 525 line

	$[3]^{(6)},[4],[3]^{(3)}$	$[0],[3]^{(11)}$	$([4],[3]^{15})^{15}$	$[4],[3]^{(10)}$	$[0],[3]^{(4)}$	$([4],[3]^{15})^{15}$	$[4/3],[3]^{(6)}$
Samples	31	33	735	34	12	735	22/21
Lines	10	12	240	11	5	240	7

Table 4-14: GS1672 SD Audio Group 2 Audio Sample Distribution - 525 line

	$[3]^{(7)},[4],[3]^{(2)}$	$[0],[3]^{(12)}$	$([4],[3]^{15})^{15}$	$[4],[3]^{(9)}$	$[0],[3]^{(5)}$	$([4],[3]^{15})^{15}$	$[4/3],[3]^{(5)}$
Samples	31	36	735	31	15	735	19/18
Lines	10	13	240	10	6	240	6

Table 4-15: GS1672 SD Audio Group 3 Audio Sample Distribution - 525 line

	$[3]^{(8)},[4],[3]^{(1)}$	$[0],[3]^{(13)}$	$([4],[3]^{15})^{15}$	$[4],[3]^{(8)}$	$[0],[3]^{(6)}$	$([4],[3]^{15})^{15}$	$[4/3],[3]^{(4)}$
Samples	31	39	735	28	21	735	16/15
Lines	10	14	240	9	7	240	5

Table 4-16: GS1672 SD Audio Group 4 Audio Sample Distribution - 525 line

	$[3]^{(9)},[4],[3]^{(0)}$	$[0],[3]^{(14)}$	$([4],[3]^{15})^{15}$	$[4],[3]^{(7)}$	$[0],[3]^{(7)}$	$([4],[3]^{15})^{15}$	$[4/3],[3]^{(3)}$
Samples	31	42	735	25	21	735	13/12
Lines	10	15	240	8	8	240	4

4.7.16.2 625-Line Audio Sample Distribution

The GS1672 uses the following sample distribution to maximize the available space in the Ancillary Data region.

NOTE: the following formula starts from line 1:

$[3]^{6}$,[0],[3](G-1),([4],[3]11)25,[4],[3](12-G),[0],[3](G-1),([4],[3]11)24,[4],[3](17-G)

- [#] represents one line with # samples
- (#) represents the number of times to repeat the line sequence
- [3](0) represents no lines and no samples
- G is the audio group number from one to four

The following tables show the audio sample distribution for each of the four audio groups:

Each distribution has 625 lines.

Each distribution has 1920 samples.

Table 4-17: GS1672 SD Audio Group 1 Audio Sample Distribution - 625 line

	$[3]^{6}$	$[0],[3]^{(0)}$	$([4],[3]^{11})^{25}$	$[4],[3]^{(11)}$	$[0],[3]^{(0)}$	$([4],[3]^{11})^{24}$	$[4],[3]^{(16)}$
Samples	18	0	925	37	0	888	52
Lines	6	1	300	12	1	288	17

Table 4-18: GS1672 SD Audio Group 2 Audio Sample Distribution - 625 line

	$[3]^{6}$	$[0],[3]^{(1)}$	$([4],[3]^{11})^{25}$	$[4],[3]^{(10)}$	$[0],[3]^{(1)}$	$([4],[3]^{11})^{24}$	$[4],[3]^{(15)}$
Samples	18	3	925	34	3	888	49
Lines	6	2	300	11	2	288	16

Table 4-19: GS1672 SD Audio Group 3 Audio Sample Distribution - 625 line

	$[3]^{6}$	$[0],[3]^{(2)}$	$([4],[3]^{11})^{25}$	$[4],[3]^{(9)}$	$[0],[3]^{(2)}$	$([4],[3]^{11})^{24}$	$[4],[3]^{(14)}$
Samples	18	6	925	31	6	888	46
Lines	6	3	300	10	3	288	15

Table 4-20: GS1672 SD Audio Group 4 Audio Sample Distribution - 625 line

	$[3]^{6}$	$[0],[3]^{(3)}$	$([4],[3]^{11})^{25}$	$[4],[3]^{(8)}$	$[0],[3]^{(3)}$	$([4],[3]^{11})^{24}$	$[4],[3]^{(13)}$
Samples	18	9	925	28	9	888	43
Lines	6	4	300	9	4	288	14

4.7.17 Frame Sequence Detection - HD

The GS1672 detects the frame sequence that describes the sample distribution for synchronous audio.

The frame sequence is only used in the generation of audio control packets; where the Audio Frame Number (AFN) field describes the position of the current frame within the frame sequence.

The GS1672 sets the AFN of the Primary group control packets to zero when the ASXA host interface bit is set for asynchronous audio. The GS1672 sets the AFN of the Primary group control packets to zero, unless the AFNA_AUTO host interface bit is set to produce automatic AFN generation.

The GS1672 sets the AFN of the Secondary group control packets to zero, when the ASXB host interface bit is set for asynchronous audio. The GS1672 sets the AFN of the Secondary group control packets to zero, unless the AFNB_AUTO host interface bit is set to produce automatic AFN generation.

The GS1672 sets the AFN to one when every frame has the same number of samples:

Frame Rate 23.976Hz - Each frame has exactly 2002 samples

Frame Rate 24.000Hz - Each frame has exactly 2000 samples

Frame Rate 25.000Hz - Each frame has exactly 1920 samples

Frame Rate 30.000Hz - Each frame has exactly 1600 samples

Frame Rate 50.000Hz - Each frame has exactly 960 samples

Frame Rate 60.000Hz - Each frame has exactly 800 samples

When the frame rate is 29.97Hz, an even number of samples (8008) are distributed over five frames in the following sequence:

1602 1601 1602 1601 1602

When the frame rate is 59.94Hz, an even number of samples (4004) are distributed over five frames in the following sequence:

801 800 801 801 801

The GS1672 sets the AFN field to a number between one and five, depending on where the current frame lies within the sequence.

The GS1672 adds the offset specified in the AFN_OFS host interface field to the generated AFN. The result of the addition wraps around such that the AFN will always be in the range of one to five.

4.7.18 ECC Error Detection and Correction

The GS1672 generates the error detection and correction fields in the audio data packets.

The error detection and correction complies with SMPTE 299M-2004.

4.7.19 Audio Control Packet Insertion - SD

The GS1672 embeds audio control packets associated with the Primary Group audio and the Secondary Group audio.

The Primary Group audio to be embedded is specified using the IDA[1:0] host interface field (Address 400h).

The Secondary Group audio to be embedded is specified using the IDB[1:0] host interface field.

The Primary Group audio control packets is embedded as commanded by the CTRA_ON host interface bit. (Default is ON)

The Secondary Group audio control packets is embedded as commanded by the CTRB_ON host interface bit. (Default is ON)

The Primary Group audio control packets is replaced as commanded by the CTR_AGR host interface bit. (Default is OFF)

The Secondary Group audio control packets is replaced as commanded by the CTR_AGR and ONE_AGR host interface bits. (Default is OFF)

The contents of the Primary Group audio control packet is specified using the following host interface fields:

AFNA_AUTO Primary Group audio frame number generation.
EBIT1A Primary Group delay valid flag for channel 1.
DEL1A[25:0] Primary Group delay for channel 1.
EBIT2A Primary Group delay valid flag for channel 2.
DEL2A[25:0] Primary Group delay for channel 2.
EBIT3A Primary Group delay valid flag for channel 3.
DEL3A[25:0] Primary Group delay for channel 3.
EBIT4A Primary Group delay valid flag for channel 4.
DEL4A[25:0] Primary Group delay for channel 4.

The contents of the Secondary Group audio control packet is specified using the following host interface fields:

AFNB_AUTO Secondary Group audio frame number generation.
EBIT1B Secondary Group delay valid flag for channel 1.
DEL1B[25:0] Secondary Group delay for channel 1.
EBIT2B Secondary Group delay valid flag for channel 2.
DEL2B[25:0] Secondary Group delay for channel 2.
EBIT3B Secondary Group delay valid flag for channel 3.
DEL3B[25:0] Secondary Group delay for channel 3.
EBIT4B Secondary Group delay valid flag for channel 4.
DEL4B[25:0] Secondary Group delay for channel 4.

4.7.20 Audio Control Packet Insertion - HD

The GS1672 embeds audio control packets associated with the Primary Group audio and the Secondary Group audio.

The Primary Group audio to be embedded is specified using the IDA[1:0] host interface field. (Default is 00 in NORMAL mode).

The Secondary Group audio to be embedded is specified using the IDB[1:0] host interface field. (Default is 01 in NORMAL mode).

The Primary Group audio control packets are embedded as commanded by the CTRA_ON host interface bit. (Default is 1).

The Secondary Group audio control packets are embedded as commanded by the CTRB_ON host interface bit. (Default is 1).

The Primary Group audio control packets are replaced as commanded by the CTR_AGR host interface bit. (Default is 0).

The Secondary Group audio control packets are replaced as commanded by the CTR_AGR and ONE_AGR host interface bits. (Default is 0).

The Primary Group audio control packets are not embedded or replaced unless one or more of the ACT1, ACT2, ACT3 or ACT4 host interface bits are set.

The Secondary Group audio control packets are not embedded or replaced unless one or more of the ACT5, ACT6, ACT7 or ACT8 host interface bits are set.

The contents of the Primary Group audio control packet is specified using the following host interface fields:

AFNA_AUTO - Primary Group audio frame number auto-generation.
ASXA - Primary Group asynchronous mode.
DEL1_2A[25:0] - Primary Group audio delay for channels 1 and 2.
DEL3_4A[25:0] - Primary Group audio delay for channels 3 and 4.

The contents of the Secondary Group audio control packet is specified using the following host interface fields:

AFNB_AUTO - Secondary Group audio frame number auto-generation.
ASXB - Secondary Group asynchronous mode.

DEL1_2B[25:0] - Secondary Group audio delay for channels 1 and 2.
DEL3_4B[25:0] - Secondary Group audio delay for channels 3 and 4.

4.7.21 Audio Data Packet Insertion

In Normal Mode, the GS1672 embeds audio data packets into a space where all pre-existing embedded audio data packets have been removed.

In Cascade Mode, the GS1672 embeds audio data packets contiguously after all of the pre-existing audio data packets. The GS1672 does not replace any pre-existing audio data packets with new audio packets, even if the new audio packets have the same group number. In this situation, the new audio data packets are appended to the last packet, and there is an illegal mix of different groups using the same group number. This condition will be indicated by the following host interface bits:

- MUX_ERRA: Set in Cascade Mode when Primary Group audio data packets are added to video that already contains audio data packets with the same group number
- MUX_ERRB: Set in Cascade Mode when Secondary Group audio data packets are added to video that already contains audio data packets with the same group number

In Group Replacement Mode the GS1672 embeds audio data packets and sorts all of the embedded audio data packets in order of group number. If there are any pre-existing audio data packets with the same group number as the new audio packets, then the pre-existing packets will be replaced.

In Group Replacement Mode the GS1672 replaces only the Primary Group audio if the ONE_AGR host interface bit is set.

The GS1672 deletes arbitrary data packets if there is not enough room in the horizontal ancillary data space to embed the selected audio data packets.

The GS1672 does not embed audio data packets when there is insufficient room in the horizontal ancillary data space after deleting arbitrary data packets.

4.7.21.1 Audio Data Packet Insertion - SD only

The GS1672 embeds the audio channels specified by the ACT[8:1] host interface fields.

The GS1672 detects and preserves embedded EDH packets.

The GS1672 generates extended packets for 24-bit audio when the AUDIO_24BIT host interface bit is set.

4.7.22 Audio Interrupt Control

The GS1672 will assert the interrupt signal when an internal interrupt condition becomes true and the type of interrupt is enabled.

The following host interface bits enable the various interrupt sources:

Table 4-21: Audio Interrupt Control – Host Interface Bit Description

Bit Name	Description	Bit Address (SD)	Bit Address (HD)
EN_NO_VIDEO	Asserts interrupt when video format is unknown	40Eh-14	80Dh-14
EN_ACPG1_DET	Asserts interrupt when ACPG1_DET flag is set	40Eh-4	80Dh-4
EN_ACPG2_DET	Asserts interrupt when ACPG2_DET flag is set	40Eh-5	80Dh-5
EN_ACPG3_DET	Asserts interrupt when ACPG3_DET flag is set	40Eh-6	80Dh-6
EN_ACPG4_DET	Asserts interrupt when ACPG4_DET flag is set	40Eh-7	80Dh-7
EN_ADPG1_DET	Asserts interrupt when ADPG1_DET flag is set	40Eh-0	80Dh-0
EN_ADPG2_DET	Asserts interrupt when ADPG2_DET flag is set	40Eh-1	80Dh-1
EN_ADPG3_DET	Asserts interrupt when ADPG3_DET flag is set	40Eh-2	80Dh-2
EN_ADPG4_DET	Asserts interrupt when ADPG4_DET flag is set	40Eh-3	80Dh-3
EN_AES_ERRA	Asserts interrupt when AES_ERRA flag is set	40Eh-8	80Dh-8
EN_AES_ERRB	Asserts interrupt when AES_ERRB flag is set	40Eh-9	80Dh-9
EN_AES_ERRC	Asserts interrupt when AES_ERRC flag is set	40Eh-10	80Dh-10
EN_AES_ERRD	Asserts interrupt when AES_ERRD flag is set	40Eh-11	80Dh-11
EN_MUX_ERRA	Asserts interrupt when MUX_ERRA flag is set	40Eh-12	80Dh-12
EN_MUX_ERRB	Asserts interrupt when MUX_ERRB flag is set	40Eh-13	80Dh-13

By default, the interrupts are all disabled.

4.8 ANC Data Insertion

Horizontal or vertical ancillary data words may be inserted on up to four different lines per video frame.

Up to 512 data words may be inserted per frame with all Data Words - including the ANC packet ADF, DBN, DCNT, DID, SDID and CSUM words - being provided by the user via host interface configuration.

The CSUM word is re-calculated and inserted by the ANC Data Checksum Calculation and Insertion function.

Note that any value may be used for the CSUM word, provided that it is outside the protected ranges from 000h to 003h and from 3FCh to 3FFh. If a CSUM value in either of these ranges is used, it will not be corrected by the device.

The GS1672 does not provide error checking or correction to the ANC data provided by user via the host interface. It is the responsibility of the user to ensure that all data provided for insertion is fully standard compliant.

In HD mode, ANC data packets are inserted into the Y or C video stream, as selected via the host interface. The default insertion will be in the Y stream. For Y or C, see Registers 026h, 028h, 02Ah and 02Ch.

In SD mode, the ANC data packets are inserted into the multiplexed CbYCr data stream.

ANC data insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and $\overline{\text{SMPTE\_BYPASS}}$ is HIGH.

In addition to this, the GS1672 requires the ANC_INS bit to be set LOW in the IOPROC register.

The ANC_PACKET_BANK register (040h - 13Fh) is used to program the ANC data words for ANC data insertion.

4.8.1 ANC Insertion Operating Modes

User selection of one of the two operating modes is provided through host interface configuration, using the ANC_INS_MODE register bit (see Table 4-34: Video Core Configuration and Status Registers).

The supported operating modes are Concatenated mode and Separate Line operating mode.

By default (at power up or after system reset), the Separate Line operating mode is enabled.

Ancillary data packets are programmed into the ANC_PACKET_BANK host register at addresses 040h to BFFh.

4.8.1.1 Separate Line Operating Mode

In Separate Line mode, it is possible to insert horizontal or vertical ancillary data on up to four lines per video frame. HANC or VANC can be specified, independently of each other, on a per-line basis. 025h FIRST_LINE_NUMBER, 027h SECOND_LINE_NUMBER, 029h THIRD_LINE_NUMBER and 02Bh FOURTH_LINE_NUMBER. For each of the four video lines, up to 128 8-bit HANC or VANC data words can be inserted. Separate Line mode is selected by setting the ANC_INS_MODE bit in the host interface LOW. By default, at power up, Separate Line mode is selected.

The lines on which ancillary data is to be inserted is programmed in the host register addresses 025h to 02Ch.

For HD formats, the stream into which the ancillary data is to be inserted (Luma or Chroma) is also programmed in these register addresses.

The non-zero video line numbers on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert per line must be provided via the host interface (see Section 4.14). At power up, or after system reset, all ancillary data insertion line numbers and total number of words default to zero.

If the total number of Data Words specified per line exceeds 128 only the first 128 Data Words will be inserted, the rest will be ignored.

The data words are programmed as two 8-bit values per address, starting at host interface address 040h in the ANC_PACKET_BANK register (see Table 4-34).

The device automatically converts the provided 8-bit Data Words into the 10-bit data, formatted according to SMPTE 291M prior to insertion.

4.8.1.2 Concatenated Operating Mode

In Concatenated mode, it is possible to insert up to 512 8-bit horizontal or vertical ancillary Data Words on one line per video frame. Concatenated Line mode can be selected by setting the ANC_INS_MODE bit in the host interface HIGH. By default, at power up, Separate Line mode is selected.

In Concatenated mode, only the FIRST_LINE registers of the host interface need to be programmed (addresses 025h and 026h). See Table 4-34.

The non-zero video line number on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert must be provided via the host interface. At power up, or after system reset, the ancillary data insertion line number and total number of words default to zero.

If the total number of data words specified exceeds 512 only the first 512 Data Words will be inserted, the rest will be ignored.

The data words are programmed as two 8-bit values per address, starting at host interface address 040h in the ANC_PACKET_BANK register. See Table 4-34.

The device automatically converts the provided 8-bit data words into the 10-bit data formatted according to SMPTE 291M prior to insertion.

4.8.2 HD ANC Insertion

When operating in HD mode (RATE_SEL = LOW), the GS1672 inserts VANC or HANC data packets into either the Y data stream or C data stream.

By default (at power up or after system reset), all ANC data insertion takes place in the Y data stream.

The user can select between Y or C data stream for insertion on a per line basis in Separate Line mode. The Y data stream is selected when the STREAM_TYPE_0 bit is LOW (default). The C data stream is selected when the STREAM_TYPE_0 bit is HIGH.

The user can select between Y or C data stream for insertion on a single line basis in Concatenated mode. The Y data stream is selected when the STREAM_TYPE_0 bit is LOW (default). The C data stream is selected when the STREAM_TYPE_0 bit is HIGH.

Horizontal Ancillary data (HANC), is inserted into the Y or C data stream on the video line(s) defined by the user.

Data insertion starts at the first available location in the HANC space, following any audio and pre-existing arbitrary data packets. All Data Words identified by the user are inserted in a contiguous fashion starting at the first available data space.

HANC data insertion terminates when all Data Words identified by the user have been inserted; or by the start of the four word TRS SAV code, regardless of the number of Data Words actually inserted.

Vertical Ancillary data (VANC), is inserted into the Y or C data stream on the video line(s) defined by the user.

Data insertion starts at the first active pixel immediately following the last word of the TRS SAV code. All Data Words identified by the user are inserted in a contiguous fashion, starting at the first active pixel.

VANC data insertion terminates when all Data Words identified by the user have been inserted; or by the start of the four word TRS EAV code, regardless of the number of Data Words actually inserted.

The total number of Data Words to be inserted and the line number on which ANC data insertion takes place is provided by the user via the host interface as part of the configuration of the ANC data insertion function.

The user data for insertion is provided via host interface configuration. STREAM_TYPE_1 = address 02Dh, STREAM_TYPE_0 for the four lines of insertion is at addresses 026h (bit 14), 028h (bit 14), 02Ah (bit 14) and 02Ch (bit 14).

4.8.3 SD ANC Insertion

When operating in SD mode (RATE_SEL = HIGH), the GS1672 inserts VANC or HANC data packets into the multiplexed CbYCr data stream.

Horizontal Ancillary data (HANC), is inserted on the video line(s) defined by the user.

Data insertion starts at the first available location in the HANC space following any audio and pre-existing arbitrary data packets. All Data Words identified by the user are inserted in a contiguous fashion, starting at the first available data space.

HANC data insertion terminates when all Data Words identified by the user have been inserted; or by the start of the four word TRS SAV code, regardless of the number of Data Words actually inserted.

For the case where HANC data insertion is required on the same line as the EDH packet, data insertion is terminated by the start of the EDH packet, regardless of the number of Data Words actually inserted.

Vertical Ancillary data (VANC), is inserted into the data stream on the video line(s) defined by the user.

Data insertion starts at the first active Cb pixel immediately following the last word of the TRS SAV code. All data words identified by the user are inserted in a contiguous fashion, starting at the first active pixel.

VANC data insertion terminates when all Data Words identified by the user have been inserted; or by the start of the four word TRS EAV code, regardless of the number of Data Words actually inserted.

The total number of data words to be inserted and the line number on which ANC data insertion takes place is provided by the user via the host interface as part of the configuration of the ANC data insertion function.

The user data for insertion is provided via host interface configuration. STREAM_TYPE_1 = address 02Dh, STREAM_TYPE_0 for the four lines of insertion is at addresses 026h (bit 14), 028h (bit 14), 02Ah (bit 14) and 02Ch (bit 14).

4.9 Additional Processing Functions

The GS1672 contains a number of signal processing features. These features are only enabled in SMPTE mode of operation ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH), and when I/O processing is enabled (IOPROC_EN/$\overline{\text{DIS}}$ = HIGH).

Signal processing features include:

- TRS generation and insertion
- Line number calculation and insertion
- Line based CRC calculation and insertion
- Illegal code re-mapping
- SMPTE 352M payload identifier packet insertion
- ANC checksum calculation and correction
- EDH generation and insertion
- Audio Embedding

To enable these features in the GS1672, the $\overline{\text{SMPTE\_BYPASS}}$ pin must be HIGH, the IOPROC_EN/$\overline{\text{DIS}}$ pin must be HIGH and the individual feature must be enabled via bits set in the IOPROC register of the host interface. By default, all of the processing features are enabled.

4.9.1 Video Format Detection

By using the timing parameters extracted from the received TRS signals, or the supplied external timing signals, the GS1672 calculates the video format.

The total samples per line, active samples per line, total lines per field/frame, and active lines per field/frame are measured and reported to the user via the four RASTER_STRUC_X registers in the host interface.

These line and sample count registers are updated once per frame at the end of line 12.

The RASTER_STRUC_X registers also contain two status bits: STD_LOCK and INT/$\overline{\text{PROG}}$.

The STD_LOCK bit is set HIGH whenever the automatic video format detection circuit has achieved full synchronization.

The INT/$\overline{\text{PROG}}$ bit is set LOW if the detected video standard is Progressive, and is set HIGH if the detected video standard is Interlaced.

The Gennum video standard code (VD_STD), as used in the GS1672, GS1582 and GS1572, is included in Table 4-22 for reference purposes.

Table 4-22: Supported Video Standards

SMPTE STANDARD	ACTIVE VIDEO AREA	LENGTH OF HANC	LENGTH OF ACTIVE VIDEO	TOTAL SAMPLES	SMPTE 352M LINES	Gennum VD_STD [4:0]	RATE_ SEL1
428.1M	2048x1080/24 (1:1)	690	2048	2750	10	1Ch	1
428.1M	2048x1080/25 (1:1)	580	2048	2640	10	1Ch	1

Table 4-22: Supported Video Standards (Continued)

SMPTE STANDARD	ACTIVE VIDEO AREA	LENGTH OF HANC	LENGTH OF ACTIVE VIDEO	TOTAL SAMPLES	SMPTE 352M LINES	Gennum VD_STD [4:0]	RATE_ SEL1
260M (HD)	1920x1035/60 (2:1)	268	1920	2200	10, 572	15h	0
295M (HD)	1920x1080/50 (2:1)	444	1920	2376	10, 572	14h	0
274M (HD)	1920x1080/60 (2:1) or 1920x1080/30 (PsF)	268	1920	2200	10, 572	0Ah	0
	1920x1080/50 (2:1) or 1920x1080/25 (PsF)	708	1920	2640	10, 572	0Ch	0
	1920x1080/30 (1:1)	268	1920	2200	10 (18)[1]	0Bh	0
	1920x1080/25 (1:1)	708	1920	2640	10 (18)[1]	0Dh	0
	1920x1080/24 (1:1)	818	1920	2750	10 (18)[1]	10h	0
	1920x1080/24 (PsF)	818	1920	2750	10, 572	11h	0
	1920x1080/25 (1:1) – EM	324	2304	2640	10 (18)[1]	0Eh	0
	1920x1080/25 (PsF) – EM	324	2304	2640	10, 572	0Fh	0
	1920x1080/24 (1:1) – EM	338	2400	2750	10 (18)[1]	12h	0
	1920x1080/24 (PsF) – EM	338	2400	2750	10, 572	13h	0
296M (HD)	1280x720/30 (1:1)	2008	1280	3300	10 (13)[1]	02h	0
	1280x720/30 (1:1) – EM	408	2880	3300	10 (13)[1]	03h	0
	1280x720/50 (1:1)	688	1280	1980	10 (13)[1]	04h	0
	1280x720/50 (1:1) – EM	240	1728	1980	10 (13)[1]	05h	0
	1280x720/25 (1:1)	2668	1280	3960	10 (13)[1]	06h	0
	1280x720/25 (1:1) – EM	492	3456	3960	10 (13)[1]	07h	0
	1280x720/24 (1:1)	2833	1280	4125	10 (13)[1]	08h	0
	1280x720/24 (1:1) – EM	513	3600	4125	10 (13)[1]	09h	0
	1280x720/60 (1:1)	358	1280	1650	10 (13)[1]	00h	0
	1280x720/60 (1:1) – EM	198	1440	1650	10 (13)[1]	01h	0
125M (SD)	1440x487/60 (2:1) (Or dual link progressive)	280	1440	1716	13, 276	16h	X
	1440x507/60 (2:1)	280	1440	1716	13, 276	17h	X
	525-line 487 generic	–	–	1716	13, 276	19h	X
	525-line 507 generic	–	–	1716	13, 276	1Bh	X

Table 4-22: Supported Video Standards (Continued)

SMPTE STANDARD	ACTIVE VIDEO AREA	LENGTH OF HANC	LENGTH OF ACTIVE VIDEO	TOTAL SAMPLES	SMPTE 352M LINES	Gennum VD_STD [4:0]	RATE_ SEL1
ITU-R BT.656 (SD)	1440x576/50 (2:1) (Or dual link progressive)	280	1440	1728	9, 322	18h	X
	625-line generic (EM)	–	–	1728	9, 322	1Ah	X
Unknown HD	RATE_SEL = 0	–	–	–	–	1Dh	
Unknown SD	RATE_SEL = 1	–	–	–	–	1Eh	X

NOTE 1: The part may provide full or limited functionality with standards that are not included in this table. Please consult a Gennum technical representative.

By default (at power up or after system reset), the four RASTER_STRUC_X, STD_LOCK and INT/$\overline{\text{PROG}}$ registers are set to zero. These registers are also cleared when the $\overline{\text{SMPTE\_BYPASS}}$ pin is LOW, or the LOCKED pin is LOW.

NOTE 2: The Line Numbers in brackets refer to Version zero SMPTE 352M packet locations, if they are different from the Version one locations.

4.9.2 ANC Data Blanking

The GS1672 can blank the video input data during the H and V blanking periods. This function will be enabled by setting the $\overline{\text{ANC\_BLANK}}$ pin LOW.

This function is only available when the device is operating in SMPTE mode ($\overline{\text{SMPTE\_BYPASS}}$ = HIGH).

In this mode, input video data in the horizontal and vertical blanking periods will be replaced by SMPTE compliant blanking values.

The blanking function will operate only on the video input signal and will remove all ancillary data already embedded in the input video stream.

In SD mode, SAV and EAV code words already embedded in the input video stream will be protected and will not be blanked.

In HD mode, SAV and EAV code words, line numbers and line based CRC's already embedded in the input video stream will be protected and will not be blanked.

The above two statements are really implementation specific, and are provided only to ensure that the “Detect TRS” function for timing generation is supported by the device, even when the blanking function is enabled.

From a system perspective, use of the input blanking function is not recommended unless TRS, line number and CRC generation and insertion functions are enabled.

The active image area will not be blanked.

The input blanking function will not blank any of the ancillary data, TRS words, line numbers, CRC's, EDH, SMPTE 352M payload identifiers or audio control and data packets inserted by the device itself.

4.9.3 ANC Data Checksum Calculation and Insertion

The GS1672 calculates checksums for all detected ancillary data packets and audio data presented to the device.

ANC data checksum insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH, the $\overline{\text{SMPTE\_BYPASS}}$ is HIGH and the ANC_CSUM_INS bit is set LOW in the IOPROC register.

NOTE: The device will correct any CSUM value outside the protected ranges from 000h to 003h and from 3FCh to 3FFh. If a CSUM value in either of these ranges is presented to the device, it will not be corrected.

4.9.4 TRS Generation and Insertion

The GS1672 is capable of generating and inserting TRS codes.

TRS word generation and insertion are performed in accordance with the timing parameters generated by the timing circuits, which is locked to the externally provided H:V:F or CEA-861 signals, or the TRS signals embedded in the input data stream. The GS1672 will overwrite the TRS signals if they're already embedded.

10-bit TRS code words are inserted at all times.

The insertion of TRS ID words only take place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and the $\overline{\text{SMPTE\_BYPASS}}$ pin is HIGH.

In addition to this, the GS1672 requires the TRS_INS bit to be set LOW in the IOPROC register.

If the TIM_861 pin is HIGH, then the timing circuits are locked to CEA-861 timing.

4.9.5 HD Line Number Calculation and Insertion

The GS1672 is capable of line number generation and insertion, in accordance with the relevant HD video standard, as determined by the automatic video standard detector. Line numbers are inserted into both the Y and C channels.

NOTE: Line number generation and insertion only occurs in HD mode (RATE_SEL = LOW).

The insertion of line numbers only take place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and $\overline{\text{SMPTE\_BYPASS}}$ pin is HIGH.

In addition to this, the GS1672 requires the LNUM_INS bit to be set LOW in the IOPROC register.

4.9.6 Illegal Code Re-Mapping

The GS1672 detects and corrects illegal code words within the active picture area.

All codes within the active picture (outside the horizontal and vertical blanking periods), between the values of 3FCh and 3FFh are re-mapped to 3FBh. All codes within the active picture area between the values of 000h and 003h are remapped to 004h.

8-bit TRS code words and ancillary data preambles are also re-mapped to 10-bit values.

The illegal code re-mapping will only take place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and $\overline{\text{SMPTE\_BYPASS}}$ is HIGH.

In addition to this, the GS1672 requires the ILLEGAL_WORD_REMAP bit to be set LOW in the IOPROC register.

4.9.7 SMPTE 352M Payload Identifier Packet Insertion

When enabled by the SMPTE_352M_INS bit in the IOPROC register, new SMPTE 352M payload identifier packets are inserted into the data stream. These packets are supplied by the user via the host interface. Setting the SMPTE_352M_INS bit LOW enables this insertion.

The device will automatically calculate the checksum and generate Version One compliant 352M ancillary data preambles: DID, SDID, DBN, DC.

The SMPTE 352M packet is inserted into the data stream according to the line number and sample position rules defined in the 2002 standard.

For HDTV video systems the SMPTE 352M packet is placed in the Y channel only.

By default (at power up or after system reset), the four VIDEO_FORMAT_IN_DS1 registers and the four VIDEO_FORMAT_OUT_DS1 registers are set to zero.

4.9.8 Line Based CRC Generation and Insertion (HD)

When operating in HD mode (RATE_SEL pin = LOW), the GS1672 generates and inserts line based CRC words into both the Y and C channels of the data stream.

The line based CRC insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH and $\overline{\text{SMPTE\_BYPASS}}$ is HIGH.

In addition to this, the GS1672 requires the EDH_CRC_INS bit to be set LOW in the IOPROC register.

4.9.9 EDH Generation and Insertion

When operating in SD mode, the GS1672 generates and inserts EDH packets into the data stream.

The EDH packet generation and insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is HIGH, $\overline{\text{SMPTE\_BYPASS}}$ pin is HIGH, the RATE_SEL pin is HIGH and the EDH_CRC_INS bit is set LOW in the IOPROC register.

Calculation of both Full Field (FF) and Active Picture (AP) CRCs is carried out by the device.

EDH error flags EDH, EDA, IDH, IDA and UES for ancillary data, full field and active picture are also inserted.

- When the EDH_CRC_UPDATE bit of the host interface is set LOW, these flags are sourced from the ANC_EDH_FLAG, FF_EDH_FLAG and AP_EDH_FLAG registers of the device, where they are programmed by the application layer
- When the EDH_CRC_UPDATE bit of the host interface is set HIGH, incoming EDH flags are preserved and inserted in the outgoing EDH packets. In this mode the ANC_EDH_FLAG, FF_EDH_FLAG and AP_EDH_FLAG registers contain the incoming EDH flags, and will be read only

The GS1672 generates all of the required EDH packet data including all ancillary data preambles: DID, DBN, DC, reserved code words and checksum.

The prepared EDH packet is inserted at the appropriate line of the video stream (in accordance with RP165). The start pixel position of the inserted packet is based on the SAV position of that line, such that the last byte of the EDH packet (the checksum) is placed in the sample immediately preceding the start of the SAV TRS word.

NOTE 1: When the EDH_CRC_UPDATE bit of the host interface is set LOW, it is the responsibility of the application interface to ensure that the EDH flag registers are updated regularly (once per field).

NOTE 2: It is also the responsibility of the application interface to ensure that there is sufficient space in the horizontal blanking interval for the EDH packet to be inserted.

4.9.10 HD HANC Space Considerations when Embedding Audio

Standards having more than 1024 HANC words in the blanking can potentially re-transmit pre-embedded packets twice in CASCADE or AGR modes.

Here is the list of standards at risk:

(1920x1080/24/1:1, 444) = 1648 words in HANC (2048x1080/25/1:1, 444) = 1172 words in HANC

(2048x1080/24/1:1, 444) = 1392 words in HANC

(1280x720/24/1:1, 444) = 5678 words in HANC

(1280x720/23.98/1:1, 444) = 5678 words in HANC

(1280x720/25/1:1, 444) = 5348 words in HANC

(1280x720/50/1:1, 444) = 1388 words in HANC

(1920x1080/23.98/1:1, 444) = 1648 words in HANC

(1920x1080/50/2:1, 444) = 1428 words in HANC

(1920x1080/25/1:1, 444) = 1428 words in HANC

(1920x1080/25/PsF, 444) = 1428 words in HANC

(1280x720/30/1:1, 422) = 2008 words in HANC

(1280x720/29.97/1:1, 422) = 2008 words in HANC

(1280x720/25/1:1, 422) = 2668 words in HANC

(1280x720/24/1:1, 422) = 2833 words in HANC

(1280x720/23.98/1:1, 422) = 2833 words in HANC

NOTE: For all of the standards listed above, Gennum recommends using the GS1672 as the source of any ancillary data packets. If packets already exist in the video coming in to the GS1672, Gennum recommends deleting all ANC packets if this problem is to be avoided.

4.9.11 Processing Feature Disable

The GS1672 contains an IOPROC register. This register contains one bit for each processing feature, allowing the user to enable/disable each process individually.

By default (at power up or after system reset), all of the IOPROC register bits are LOW.

To disable an individual processing feature, the application interface must set the corresponding bit HIGH in the IOPROC register. To enable these features, the IOPROC_EN/$\overline{\text{DIS}}$ pin must be HIGH, and the individual feature must be enabled by setting bits LOW in the IOPROC register of the host interface.

The I/O processing functions supported by the GS1672 are shown in Table 4-25 below.

Table 4-23: IOPROC Register Bits

I/O Processing Feature	IOPROC Register Bit
TRS insertion	TRS_INS (000h Bit 0)
Y and C line number insertion	LNUM_INS (000h Bit 1)
Y and C line based CRC insertion	CRC_INS (000h Bit 2)
Ancillary data checksum correction	ANC_CSUM_INS (000h Bit 3)
EDH CRC error calculation and insertion	EDH_ CRC_INS (000h Bit 4)
Illegal word re-mapping	ILLEGAL_WORD_REMAP (000h Bit 5)
SMPTE 352M packet insertion	SMPTE_352M_INS (000h Bit 6)
Audio embedding	AUDIO_EMBED (000h Bit 10)

4.10 352M Data Extraction

If there are no SMPTE 352M packets embedded in the input signal, the GS1672 will raise an error flag in the “NO_352_ERR” bit.

If there are 352M packets present in the stream, the GS1672 reports the extracted SMPTE 352M packets in the VIDEO_FORMAT_352_IN registers in the host interface. The user can use this information, along with the RASTER_STRUC_X registers, to determine the video format.

If there is a conflict between the numbers in the RASTER_STRUC_X registers and the format defined in the SMPTE 352M packets, the GS1672 will raise a TIMING_ERR flag via the host interface.

NOTE: SMPTE 352M packets will not be present in an HD-SDTI input stream, and will not be embedded in an output HD-SDTI serial stream. This is controlled by the user.

By default (at power up or after system reset), the VIDEO_FORMAT_352_IN registers are set to zero (undefined video format). These registers are also cleared when the $\overline{\text{SMPTE\_BYPASS}}$ pin is set LOW, or the LOCKED pin is LOW. The SMPTE 352M packet should be received once per field for interlaced systems and once per frame for progressive video systems. If the packet is not received for two complete video frames, the VIDEO_FORMAT_352_IN registers are cleared to zero.

Table 4-24: SMPTE 352M Packet Data

Register Name	Bit	Bit Name	Description	R/W	Default
VIDEO_FORMAT_352_IN_WORD_2	15-8	VIDEO_FORMAT_IN_DS1_4 (Byte 4)	Data will be available in this register when Video Payload Identification Packets are detected in the data stream (luma).	R	0
	7-0	VIDEO_FORMAT_IN_DS1_3 (Byte 3)	Data will be available in this register when Video Payload Identification Packets are detected in the data stream (luma).	R	0
VIDEO_FORMAT_352_IN_WORD_1	15-8	VIDEO_FORMAT_IN_DS1_2 (Byte 2)	Data will be available in this register when Video Payload Identification Packets are detected in the data stream (luma).	R	0
	7-0	VIDEO_FORMAT_IN_DS1_1 (Byte 1)	Data will be available in this register when Video Payload Identification Packets are detected in the data stream (luma).	R	0
VIDEO_FORMAT_352_IN_WORD_4	15-8	VIDEO_FORMAT_IN_DS2_4 (Byte 4)	Data will be available in this register when Video Payload Identification Packets are detected in the data stream (chroma).	R	0
	7-0	VIDEO_FORMAT_IN_DS2_3 (Byte 3)	Data will be available in this register when Video Payload Identification Packets are detected in the data stream (chroma).	R	0
VIDEO_FORMAT_352_IN_WORD_3	15-8	VIDEO_FORMAT_IN_DS2_2 (Byte 2)	Data will be available in this register when Video Payload Identification Packets are detected in the data stream (chroma).	R	0
	7-0	VIDEO_FORMAT_IN_DS2_1 (Byte 1)	Data will be available in this register when Video Payload Identification Packets are detected in the data stream (chroma).	R	0

4.11 Serial Clock PLL

An internal VCO provides the transmission clock rates for the GS1672.

The power supply to the VCO is provided to the VCO_VDD/VCO_GND pins of the device.

This VCO is locked to the input PCLK via an on-chip PLL and Charge Pump.

Internal division ratios for the PCLK are determined by the setting of the RATE_SEL pin and the 20BIT/$\overline{10BIT}$ pin as shown in Table 4-25:

Table 4-25: PCLK and Serial Digital Clock Rates

External Pin Setting		Supplied PCLK Rate	Serial Digital Output Rate
RATE_SEL	20BIT/$\overline{10BIT}$		
LOW	HIGH	74.25 or 74.25/1.001MHz	1.485 or 1.485/1.001Gb/s
LOW	LOW	148.5 or 148.5/1.001MHz	1.485 or 1.485/1.001Gb/s
HIGH	HIGH	13.5MHz	270Mb/s
HIGH	LOW	27MHz	270Mb/s

As well as generating the serial digital output clock signals, the PLL is also responsible for generating all internal clock signals required by the device.

4.11.1 PLL Bandwidth

Table 4-26 shows the GS1672 PLL loop bandwidth variations. PLL bandwidth is a function of the external loop filter resistor and the charge pump current. We recommend using a 200Ω loop filter resistor, however, this value can be varied from 100Ω to 380Ω, depending on application. Values other than 200Ω are not guaranteed. As the resistor is changed, the bandwidth will scale proportionately (for example, a change from a 200Ω to 300Ω resistor will cause a 50% increase in bandwidth). The charge pump current is preset to 100µA and should not be changed. The external loop filter capacitor does not affect the PLL loop bandwidth. The external loop filter capacitor affects PLL loop settling time, phase margin and noise. It is selectable from 1µF to 33µF. However, it should be kept at 10µF for optimal performance. A smaller capacitor results in shorter lock time but less stability. A larger capacitor results in longer lock time but more stability. Narrower loop bandwidths require a larger capacitor to be stable. In other words, a small loop filter resistor requires a larger loop capacitor.

Table 4-26: GS1672 PLL Bandwidth

Mode	PCLK Frequency (MHz)	Filter Resistor (Ω)	Charge Pump Current (µA)	Bandwidth (MHz)
SD	13.50	200	100	4.78
SD	27.00	200	100	9.57
HD	74.25	200	100	26.32
HD	148.50	200	100	52.63

4.11.2 Lock Detect

The Lock Detect block controls the serial digital output signal and indicates to the application layer the lock status of the device.

The LOCKED output pin is provided to indicate the device operating status.

The LOCKED output signal is set HIGH by the lock detect block under the following conditions (see Table 4-27):

Table 4-27: GS1672 Lock Detect Indication

$\overline{\text{RESET}}$	PLL Lock	$\overline{\text{SMPTE\_BYPASS}}$	DVB_ASI	RATE_SEL
HIGH	HIGH	HIGH	LOW	X
HIGH	HIGH	LOW	HIGH	HIGH
HIGH	HIGH	LOW	LOW	X

Any other combination of signal states not included in the above table results in the LOCKED pin being LOW.

NOTE: When the LOCKED pin is LOW, the serial digital output is in the muted state.

4.12 Serial Digital Output

The GS1672 has a single, low-impedance current mode differential output driver, capable of driving at least 800mV into a 75Ω single-ended load.

The output signal amplitude, or swing, will be user-configurable using an external resistor on the RSET pin.

The serial digital output data rate supports SMPTE 292, SMPTE 259M-C and DVB-ASI operation. This is summarized in Table 4-28:

Table 4-28: Serial Digital Output - Serial Output Data Rate

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial Output Data Rate	BRSDO	SMPTE 292 signal	–	1.485, 1.485/1.001	–	Gb/s
		SMPTE 259M-C signal	–	270	–	Mb/s
		DVB-ASI signal	–	270	–	Mb/s

The SDO and $\overline{\text{SDO}}$ pins of the device provide the serial digital output.

Compliance with all requirements defined in Section 4.12.1 through Section 4.12.4 is guaranteed when measured across a 75Ω terminated load at the output of 1m of Belden 1694A cable, including the effects of the Gennum recommended ORL matching network, BNC and coaxial cable connection, except where otherwise stated.

Figure 4-23 illustrates this requirement, which is in accordance with the measurement methodology defined in SMPTE 292 and SMPTE 259M.

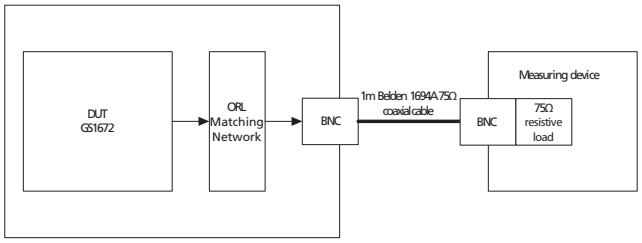


Figure 4-23: ORL Matching Network, BNC and Coaxial Cable Connection

4.12.1 Output Signal Interface Levels

The Serial Digital Output signals (SDO and $\overline{\text{SDO}}$ pins), of the device meet the amplitude requirements as defined in SMPTE 424M for an unbalanced generator (single-ended).

The signal amplitude is controlled to better than +/-7% of the nominal level defined in SMPTE 424M, when an external 750Ω 1% resistor is connected between the RSET pin of the device and VCC.

The output signal amplitude can be reduced to less than 1/10th of the nominal amplitude, defined above, by increasing the value of the resistor connected between the RSET pin of the device and VCC.

These requirements are met across all ambient temperature and power supply operating conditions described in the Electrical Characteristics on page 18.

The output amplitude of the GS1672 can be adjusted by changing the value of the RSET resistor as shown in Table 4-29. For a 800mVp-p output a value of 750Ω is required. A ±1% SMT resistor should be used.

The RSET resistor is part of the high speed output circuit of the GS1672. The resistor should be placed as close as possible to the RSET pin. In addition, an anti-pad should be used underneath the resistor.

Table 4-29: R_{SET} Resistor Value vs. Output Swing

R_{SET} Resistor Values (Ω)	Output Swing (mV_{p-p})
995	608
824	734
750	800
680	884

4.12.2 Overshoot/Undershoot

The serial digital output signal overshoot and undershoot is controlled to be less that 7% of the output signal amplitude, when operating as an unbalanced generator (single-ended).

This requirement is met for nominal signal amplitudes as defined by SMPTE 292.

This requirement is met regardless of the output slew rate setting of the device.

This requirement is met across all ambient temperature and power supply operating conditions described in the Electrical Characteristics on page 18.

This requirement is summarized in Table 4-30:

Table 4-30: Serial Digital Output - Overshoot/Undershoot

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial output overshoot /undershoot	–	–	–	0	7	%

4.12.3 Slew Rate Selection

The GS1672 supports two user-selectable output slew rates.

Control of the slew rate is determined by the setting of the RATE_SEL input pin.

When this pin is set HIGH, the output slew rate matches the requirements as defined by the SMPTE 259M-C standard.

When this pin is set LOW, the output slew rate is better than the requirements as defined by the SMPTE 424M standard.

These requirements is met across all ambient temperature and power supply operating conditions described in the Electrical Characteristics on page 18.

This requirement is summarized in Table 4-31:

Table 4-31: Serial Digital Output - Rise/Fall Time

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Serial Output Rise/Fall Time 20% ~ 80%	SDO_{TR}	SMPTE 292 signal	–	–	135	ps
		SMPTE 259M-C signal	400	–	800	ps

4.12.4 Serial Digital Output Mute

When the SDO_EN/$\overline{DIS}$ pin is LOW, the serial digital output signals of the device become high-impedance, reducing system power.

The serial digital output is also placed in the high-impedance state when the LOCKED pin is LOW, or when the STANDBY pin is HIGH.

4.13 GSPI Host Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the application layer to access additional status information through configuration registers in the GS1672.

The GSPI comprises a Serial Data Input signal (SDIN), Serial Data Output signal (SDOUT), an active low Chip Select ($\overline{CS}$) and a Burst Clock (SCLK).

Because these pins can be shared with the JTAG interface port for compatibility with the GS1582, an additional control signal pin JTAG/$\overline{HOST}$ is provided.

When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled. When JTAG/$\overline{HOST}$ is HIGH, the JTAG interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the application interface. The SDOUT pin is a non-clocked loop-through of SDIN, and may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain. The interface is illustrated in Figure 4-24 below.

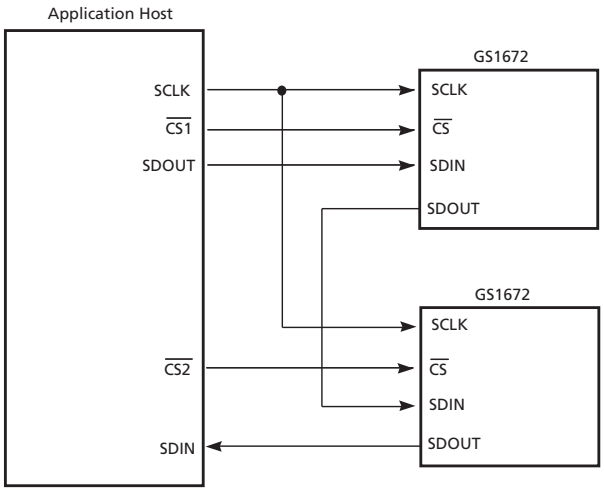


Figure 4-24: GSPI Application Interface Connection

All read or write access to the GS1672 is initiated and terminated by the application host processor. Each access always begins with a Command/Address Word followed by a data read to or written from the GS1672.

4.13.1 Command Word Description

The Command Word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Increment bit and a 12-bit address. Figure 4-25 shows the command word format and bit configurations.

Command Words are clocked into the GS1672 on the rising edge of the Serial Clock SCLK, which operates in a burst fashion.

When the Auto-Increment bit is set LOW, each Command Word must be followed by only one Data Word to ensure proper operation. If the Auto-Increment bit is set HIGH, the following Data Word will be written into the address specified in the Command Word, and subsequent data words will be written into incremental addresses from the previous Data Word. This facilitates multiple address writes without sending a Command Word for each Data Word.

NOTE: All registers can be written to through single address access or through the Auto-increment feature. However, the LSB of the video registers cannot be read through single address read-back. Single address read-back will return a zero value for the LSB. If auto-increment is used to read back the values from at least two registers, the LSB value read will always be correct. Therefore, for register read-back, it is recommended that auto-increment be used and that at least two registers be read back at a time.

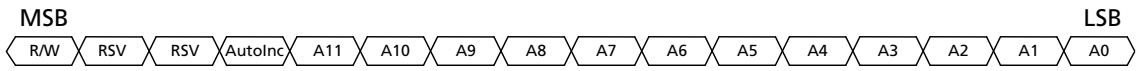


Figure 4-25: Command Word Format

4.13.2 Data Read or Write Access

Serial data is transmitted or received MSB first synchronous with the rising edge of the Serial Clock, SCLK. The Chip Select ($\overline{CS}$) signal must be active LOW a minimum of 1.5ns (t0 in Figure 4-27) before the first clock edge to ensure proper operation.

During a Read sequence (Command Word R/W bit set HIGH), a wait state of 148ns (4 x 1/fPCLK, t5 in Figure 4-27) is required between writing the Command Word and reading the following Data Word. The read bits are clocked out on the negative edges of SCLK.

NOTE 1: Where several devices are connected to the GSPI chain, only one $\overline{CS}$_TMS may be asserted during a read sequence.

During a Write sequence (Command Word R/W bit set LOW), a wait state of 37ns (1 x 1/fPCLK, t4 in Figure 4-27) is required between the Command Word and the following Data Word. This wait state must also be maintained between successive Command Word/Data Word write sequences. When Auto-increment mode is selected (AutoInc = 1), the wait state must be maintained between successive Data Words after the initial Command Word/Data Word sequence.

During the write sequence, all command and following Data Words input at the SDIN pin are output at the SDOUT pin as is.

When several devices are connected to the GSPI chain, data can be written simultaneously to all the devices which have $\overline{CS}$ set LOW.

NOTE 2: If the application interface performs a Read or Write access after power-up, prior to the application of a valid serial video input signal, the SCLK frequency must not exceed 10MHz.

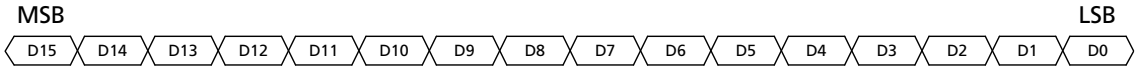


Figure 4-26: Data Word Format

4.13.3 GSPI Timing

Write and Read Mode timing for the GSPI interface is as shown in the following diagrams:

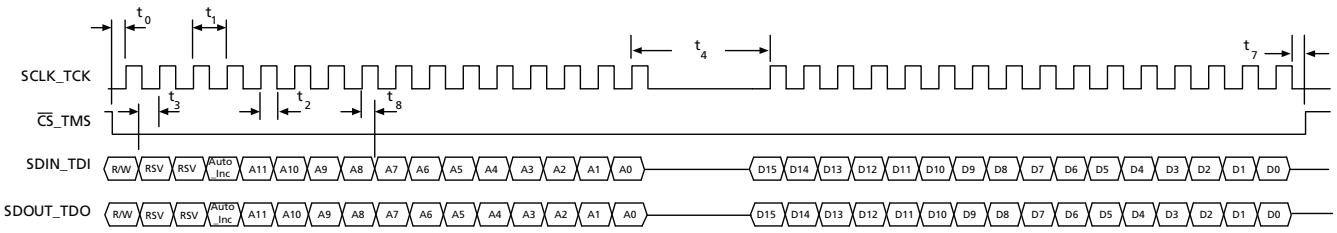


Figure 4-27: Write Mode

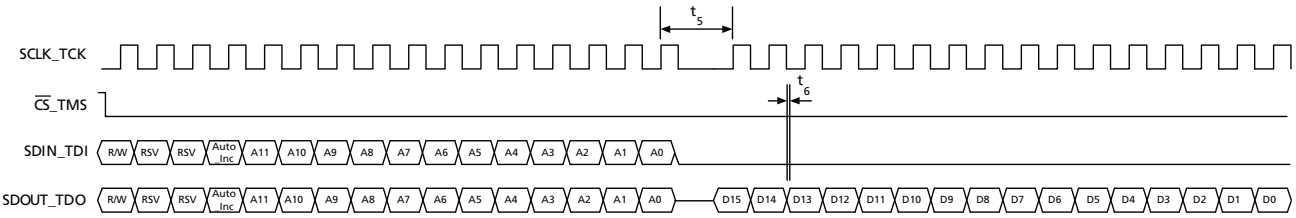


Figure 4-28: Read Mode

SDIN_TDI to SDOUT_TDO combinational path for daisy chain connection of multiple GS1672 devices.

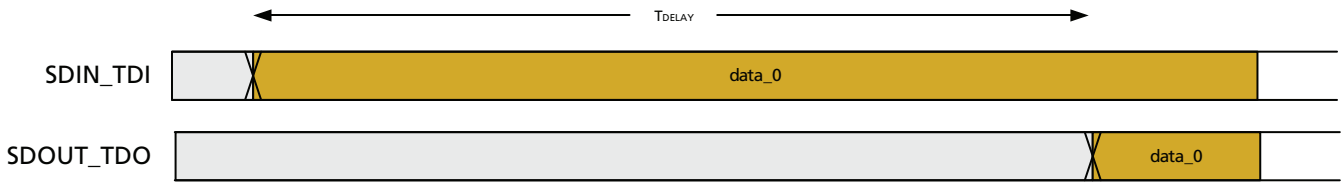


Figure 4-29: GSPI Time Delay

Table 4-32: GSPI Time Delay

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Delay time	t_{DELAY}	50% levels; 1.8V operation	–	–	10.5	ns
Delay time	t_{DELAY}	50% levels; 3.3V operation	–	–	8.7	ns

Table 4-33: GSPI AC Characteristics

Parameter	Symbol	Conditions	Min		Typ	Max	Units
$\overline{CS}$ low before SCLK rising edge	t_0	50% levels; 3.3V or 1.8V operation	1.5		–	–	ns
SCLK period	t_1		12.5		–	–	ns
SCLK duty cycle	t_2		40		50	60	%
Input data setup time	t_3		1.5		–	–	ns
Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – write cycle.	t_4		PCLK (MHz)	ns	–	–	ns
			unlocked	445			
			13.5	74.2			
			27.0	37.1			
			74.25	13.5			
			148.5	6.7			
Time between end of Command Word (or data in Auto-Increment mode) and the first SCLK of the following Data Word – read cycle.	t_5		PCLK (MHz)	ns	–	–	ns
			unlocked	1187			
			13.5	297			
			27.0	148.5			
			74.25	53.9			
			148.5	27			
Output hold time (15pF load)	t_6		1.5		–	–	ns
$\overline{CS}$ HIGH after last SCLK rising edge	t_7		PCLK (MHz)	ns	–	–	ns
			unlocked	445			
			74.2	74.2			
			37.10	37.1			
			74.25	13.5			
			148.5	6.7			
Input data hold time	t_8		1.5		–	–	ns

NOTE: If the application interface performs a Read or Write access after power-up, prior to the application of a valid serial video input signal, the SCLK frequency must not exceed 10MHz.

4.14 Host Interface Register Maps

4.14.1 Video Core Registers

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
000h	IOPROC	RSVD	15	Reserved.	R	0
		DELAY_LINE_ENABLE	14	HIGH - enables the delay line. LOW - disables the delay line.	R/W	0
		RSVD	13	Reserved.	R/W	0
		EDH_CRC_UPDATE	12	HIGH - preserve incoming EDH flags and insert into outgoing EDH packets. LOW - embed flags from 003 in EDH packet.	R/W	0
		ANC_INS	11	HIGH - disable ancillary data insertion. LOW - embeds ANC packet stored at 040h - 13Fh according to parameters at 005h -02Dh.	R/W	0
		AUDIO_EMBED	10	HIGH - disable audio embedding. LOW - enables audio embedding.	R/W	0
		RSVD	9	Reserved.	R/W	1
		H_CONFIG	8	Chooses H configuration; LOW - Active-line based blanking is enabled. HIGH - SMPTE H timing.	R/W	0
		RSVD	7	Reserved.	R/W	0
		SMPTE_352M_INS	6	HIGH - disables insertion of SMPTE 352M packets. LOW - enables insertion of SMPTE 352M packets	R/W	0
		ILLEGAL_WORD_REMAP	5	HIGH - disables illegal word remapping.	R/W	0
		EDH_CRC_INS	4	HIGH - disables EDH CRC error correction and insertion.	R/W	0
		ANC_CSUM_INS	3	HIGH - disables insertion of ancillary data checksums.	R/W	0
		CRC_INS	2	HIGH - disables insertion of HD CRC words.	R/W	0
		LNUM_INS	1	HIGH = disables insertion of HD line numbers.	R/W	0
		TRS_INS	0	HIGH = disables insertion of TRS words.	R/W	0

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
001h	ERROR_STAT	RSVD	15-7	Reserved.	R	0
		TRS_PERR	6	TRS protection error. LOW - No errors in TRS. HIGH - Errors in TRS.	R	0
		Y1_EDH_CS_ERR	5	Same as CS_ERR but only updates its state when packet being inspected is an EDH packet.	R	0
		Y1_CS_ERR	4	HIGH indicates that a checksum error is detected. It is updated every time a $\overline{CS}$ word is present on the output. **NOTE:** This bit will not be set for CSUM values in the protected ranges (from 000h to 003h and from 3FCh to 3FFh).	R	0
		FORMAT_ERR	3	HIGH indicates standard is not recognized for 861D conversion.	R	0
		TIMING_ERR	2	HIGH indicates that the RASTER measurements do not line up with the extracted 352M packet information.	R	0
		NO_352M_ERR	1	HIGH indicates no 352M packet embedded in incoming video.	R	0
		LOCK_ERR	0	HIGH indicates PLL lock error indication.	R	0

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
002h	EDH_FLAG_EXT	RSVD	15	Reserved.	R	0
		ANC_UES_EXT	14	Ancillary data - unknown error status flag.	R	0
		ANC_IDA_EXT	13	Ancillary data - internal error detected already flag.	R	0
		ANC_IDH_EXT	12	Ancillary data - internal error detected here flag.	R	0
		ANC_EDA_EXT	11	Ancillary data - error detected already flag.	R	0
		ANC_EDH_EXT	10	Ancillary data - error detected here flag.	R	0
		FF_UES_EXT	9	EDH Full Field - unknown error status flag.	R	0
		FF_IDA_EXT	8	EDH Full Field - internal error detected already flag.	R	0
		FF_IDH_EXT	7	EDH Full Field - internal error detected here flag.	R	0
		FF_EDA_EXT	6	EDH Full Field - error detected already flag.	R	0
		FF_EDH_EXT	5	EDH Full Field - error detected here flag.	R	0
		AP_UES_EXT	4	EDH Active Picture - unknown error status flag.	R	0
		AP_IDA_EXT	3	EDH Active Picture - internal error detected already flag.	R	0
		AP_IDH_EXT	2	EDH Active Picture - internal error detected here flag.	R	0
		AP_EDA_EXT	1	EDH Active Picture - error detected already flag.	R	0
		AP_EDH_EXT	0	EDH Active Picture - error detected here flag.	R	0

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
003h	EDH_FLAG_PGM	RSVD	15	Reserved.	R	0
		ANC_UES_PGM	14	Ancillary data - unknown error status flag.	R	0
		ANC_IDA_PGM	13	Ancillary data - internal error detected already flag.	R/W	0
		ANC_IDH_PGM	12	Ancillary data - internal error detected here flag.	R/W	0
		ANC_EDA_PGM	11	Ancillary data - error detected already flag.	R/W	0
		ANC_EDH_PGM	10	Ancillary data - error detected here flag.	R/W	0
		FF_UES_PGM	9	EDH Full Field - unknown error status flag.	R/W	0
		FF_IDA_PGM	8	EDH Full Field - internal error detected already flag.	R/W	0
		FF_IDH_PGM	7	EDH Full Field - internal error detected here flag.	R/W	0
		FF_EDA_PGM	6	EDH Full Field - error detected already flag.	R/W	0
		FF_EDH_PGM	5	EDH Full Field - error detected here flag.	R/W	0
		AP_UES_PGM	4	EDH Active Picture - unknown error status flag.	R/W	0
		AP_IDA_PGM	3	EDH Active Picture - internal error detected already flag.	R/W	0
		AP_IDH_PGM	2	EDH Active Picture - internal error detected here flag.	R/W	0
		AP_EDA_PGM	1	EDH Active Picture - error detected already flag.	R/W	0
		AP_EDH_PGM	0	EDH Active Picture - error detected here flag.	R/W	0

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
004h	DATA_FORMAT	RSVD	15-10	Reserved.	R	0
		VD_STD	9-5	Detected video standard.	R	0
		INT/$\overline{\text{PROGB}}$	4	HIGH = interlaced signal LOW = progressive signal	R	0
		RSVD	3	Reserved.	R	0
		STD_LOCK	2	Standard lock indication. Active HIGH.	R	0
		V_LOCK	1	Vertical lock indication. Active HIGH.	R	0
		H_LOCK	0	Horizontal lock indication. Active HIGH.	R	0
005h	RSVD	RSVD	15-0	Reserved.	R	0
006h	VSD_FORCE	RSVD	15-6	Reserved.	R	0
		VSD_FORCE	5	Use the CSR register STD value rather than the flywheels STD value. Active HIGH.	R/W	0
		VID_STD_FORCE	4-0	Force VID STD CSR.	R/W	0
007h	EDH_STATUS	RSVD	15-2	Reserved.	R	0
		FF_CRC_V	1	Full Field extracted V bit.	R	0
		AP_CRC_V	0	Active Picture extracted V bit.	R	0
008h	FIRST_AVAIL_POSITION	RSVD	15-1	Reserved.	R	0
		FIRST_AVAIL_POSITION	0	HIGH - 352M insertion occurs on first available ANC space. LOW - insert 352M packets right after EAV/CRC1.	R/W	1
009h	RESERVED	RESERVED_7	15-0	Reserved.	R	0
00Ah	VIDEO_FORMAT_352_OUT_WORD_1	VIDEO_FORMAT_OUT_DS1_2	15-8	SMPTE 352M luma embedded packet - byte 2.	R/W	0
		VIDEO_FORMAT_OUT_DS1_1	7-0	SMPTE 352M luma embedded packet - byte 1.	R/W	0
00Bh	VIDEO_FORMAT_352_OUT_WORD_2	VIDEO_FORMAT_OUT_DS1_4	15-8	SMPTE 352M luma embedded packet - byte 4.	R/W	0
		VIDEO_FORMAT_OUT_DS1_3	7-0	SMPTE 352M luma embedded packet - byte 3.	R/W	0
00Ch	VIDEO_FORMAT_352_OUT_WORD_3	VIDEO_FORMAT_OUT_DS2_2	15-8	SMPTE 352M chroma embedded packet - byte 2.	R/W	0
		VIDEO_FORMAT_OUT_DS2_1	7-0	SMPTE 352M chroma embedded packet - byte 1.	R/W	0

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
00Dh	VIDEO_FORMAT_352_OUT_WORD_4	VIDEO_FORMAT_OUT_DS2_4	15-8	SMPTE 352M chroma embedded packet - byte 4.	R/W	0
		VIDEO_FORMAT_OUT_DS2_3	7-0	SMPTE 352M chroma embedded packet - byte 3.	R/W	0
00Eh	VIDEO_FORMAT_352_IN_WORD_1	VIDEO_FORMAT_IN_DS1_2	15-8	SMPTE 352M luma extracted packet - byte 2.	R	0
		VIDEO_FORMAT_IN_DS1_1	7-0	SMPTE 352M luma extracted packet - byte 1.	R	0
00Fh	VIDEO_FORMAT_352_IN_WORD_2	VIDEO_FORMAT_IN_DS1_4	15-8	SMPTE 352M luma extracted packet - byte 4.	R	0
		VIDEO_FORMAT_IN_DS1_3	7-0	SMPTE 352M luma extracted packet - byte 3.	R	0
010h	VIDEO_FORMAT_352_IN_WORD_3	VIDEO_FORMAT_IN_DS2_2	15-8	SMPTE 352M chroma extracted packet - byte 2.	R	0
		VIDEO_FORMAT_IN_DS2_1	7-0	SMPTE 352M chroma extracted packet - byte 1.	R	0
011h	VIDEO_FORMAT_352_IN_WORD_4	VIDEO_FORMAT_IN_DS2_4	15-8	SMPTE 352M chroma extracted packet - byte 4.	R	0
		VIDEO_FORMAT_IN_DS2_3	7-0	SMPTE 352M chroma extracted packet - byte 3.	R	0
012h	RASTER_STRUC_1	RSVD	15-11	Reserved.	R	0
		LINES_PER_FRAME	10-0	Total lines per frame.	R	0
013h	RASTER_STRUC_2	RSVD	15-14	Reserved.	R	0
		WORDS_PER_LINE	13-0	Total words per line.	R	0
014h	RASTER_STRUC_3	RSVD	15-13	Reserved.	R	0
		ACTIVE_WORDS_PER_LINE	12-0	Words per active line.	R	0
015h	RASTER_STRUC_4	RSVD	15-11	Reserved.	R	0
		ACTIVE_LINES_PER_FIELD	10-0	Active lines per frame.	R	0
016h - 023h	RSVD	RSVD	15-0	Reserved.	R	0
024h	FIRST_LINE_NUMBER_STATUS	RSVD	15-2	Reserved.	R	0
		PACKET_MISSED	1	ANC data packet could not be inserted in its entirety. HIGH - ANC packet cannot be inserted in it's entirety.	R	0
		RW_CONFLICT	0	Same RAM address was read and written to at the same time. HIGH - one of the addresses from 040h to 13Fh was read and written to at the same time.	R	0

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
025h	FIRST_LINE_ NUMBER	RSVD	15-12	Reserved.	R	0
		ANC_INS_MODE	11	ANC data insertion mode. HIGH - Concatenate LOW - Separate	R/W	0
		FIRST_LINE_NUMBER	10-0	First line number to insert ANC packet on.	R/W	0
026h	FIRST_LINE_ NUMBER_OF_ WORDS	FIRST_LINE_NUMBER_ANC_T YPE	15	ANC region to insert packet in HIGH - VANC, LOW - HANC.	R/W	0
		FIRST_LINE_NUMBER _STREAM_TYPE	14	Stream to insert packet in HIGH - C stream, LOW - Y stream.	R/W	0
		RSVD	13-10	Reserved.	R	0
		FIRST_LINE_NUMBER _OF_WORDS	9-0	Total number of words in ANC packet to be inserted in first line.	R/W	0
027h	SECOND_LINE_ NUMBER	RSVD	15-11	Reserved.	R	0
		SECOND_LINE_NUMBER	10-0	Second line number to insert ANC packet on in Separate Line mode.	R/W	0
028h	SECOND_LINE_ NUMBER_OF_ WORDS	SECOND_LINE_NUMBER _ANC_TYPE	15	ANC region to insert packet in. HIGH - VANC, LOW - HANC.	R/W	0
		SECOND_LINE_NUMBER _STREAM_TYPE	14	Stream to insert packet in. HIGH - C stream, LOW - Y stream.	R/W	0
		RSVD	13-10	Reserved.	R	0
		SECOND_LINE_NUMBER _OF_WORDS	9-0	Total number of words in ANC packet to be inserted in second line.	R/W	0
029h	THIRD_LINE_ NUMBER	RSVD	15-11	Reserved.	R	0
		THIRD_LINE_NUMBER	10-0	Third line number to insert ANC packet on in Separate Line mode.	R/W	0
02Ah	THIRD_LINE_ NUMBER_OF_ WORDS	THIRD_LINE_NUMBER _ANC_TYPE	15	ANC region to insert packet in. HIGH - VANC, LOW - HANC.	R/W	0
		THIRD_LINE_NUMBER _STREAM_TYPE	14	Stream to insert packet in. HIGH - C stream, LOW - Y stream.	R/W	0
		RSVD	13-10	Reserved.	R	0
		THIRD_LINE_NUMBER _OF_WORDS	9-0	Total number of words in ANC packet to be inserted in third line.	R/W	0

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
02Bh	FOURTH_LINE_NUMBER	RSVD	15-11	Reserved.	R	0
		FOURTH_LINE_NUMBER	10-0	Fourth line number to insert ANC packet on in Seperate Line mode.	R/W	0
02Ch	FOURTH_LINE_NUMBER_OF_WORDS	FOURTH_LINE_NUMBER_ANC_TYPE	15	ANC region to insert packet in HIGH - VANC, LOW - HANC.	R/W	0
		FOURTH_LINE_NUMBER_STREAM_TYPE	14	Stream to insert packet in. HIGH - C stream, LOW - Y stream.	R/W	0
		RSVD	13-10	Reserved.	R	0
		FOURTH_LINE_NUMBER_OF_WORDS	9-0	Total number of words in ANC packet to be inserted in fourth line.	R/W	0
02Dh	STREAM_TYPE_1	RSVD	15-5	Reserved.	R	0
		EDH_LINE_CHECK_EN	4	HIGH=ANC block will not insert data into the EDH region of the HANC space. LOW=ANC block will insert data into the EDH region.	R/W	1
		STREAM_TYPE1_LINE_4	3	HIGH=data for the fourth line in separate mode is inserted into the Chroma Stream. LOW - Luma Stream.	R/W	0
		STREAM_TYPE1_LINE_3	2	HIGH - data for the third line in separate mode is inserted into the Chroma Stream. LOW - Luma Stream.	R/W	0
		STREAM_TYPE1_LINE_2	1	HIGH - data for the second line in separate mode is inserted into the Chroma Stream. LOW - Luma Stream.	R/W	0
		STREAM_TYPE1_LINE_1	0	HIGH - data for the first line in separate mode is inserted into the Chroma Stream. LOW - Luma Stream.	R/W	0
02Eh - 03Fh	RSVD	RSVD	15-0	Reserved.	R	0
040h - 07Fh	ANC_PACKET_BANK_1	ANC_PACKET_BANK	15-0	First bank of user-defined 8-bit ancillary data. Bit 15 - 8: 2nd byte (MSB to LSB) Bit 7 - 0: 1st byte (MSB to LSB) See 4.8 ANC Data Insertion.	R/W	–

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
080h - 0BFh	ANC_PACKET _BANK_2	ANC_PACKET_BANK	15-0	First bank of user-defined 8-bit ancillary data. Bit 15 - 8: 2nd byte (MSB to LSB) Bit 7 - 0: 1st byte (MSB to LSB) See 4.8 ANC Data Insertion.	R/W	–
0C0h - 0FFh	ANC_PACKET _BANK_3	ANC_PACKET_BANK	15-0	First bank of user-defined 8-bit ancillary data. Bit 15 - 8: 2nd byte (MSB to LSB) Bit 7 - 0: 1st byte (MSB to LSB) See 4.8 ANC Data Insertion.	R/W	–
100h - 13Fh	ANC_PACKET _BANK_4	ANC_PACKET_BANK	15-0	First bank of user-defined 8-bit ancillary data. Bit 15 - 8: 2nd byte (MSB to LSB) Bit 7 - 0: 1st byte (MSB to LSB) See 4.8 ANC Data Insertion.	R/W	–
140h - 209h	RSVD	RSVD	–	Reserved.	R	0
20Ah	SDTI_TDM	RSVD	15-8	Reserved.	R	0
		SDTI_TDM_DS2	7	HIGH indicates an SDTI type signal on input for Chroma Stream.	R/W	0
		SDTI_TDM_DS1	6	HIGH indicates an SDTI type signal on input for Luma Stream.	R/W	0
		RSVD	5-0	Reserved.	R	0
20Bh - 20Ch	RSVD	RSVD	–	Reserved.	R	0
20Dh	LEVELB_ INDICATION	RSVD	15-0	Reserved.	R	0

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
20Eh	DRIVE_ STRENGTH	RSVD	15-6	Reserved.	R/W	0
		AUDIO_INT_DS	5-4	Drive strength value for AUDIO_INT pin. 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V)	R/W	0
		LOCKED_DS	3-2	Drive strength value for LOCKED pin. 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V)	R/W	0
		SDOUT_TDO_DS	1-0	Drive strength value for SDOUT_TDO pin. 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V)	R/W	2
20Fh	RSVD	RSVD	15-0	Reserved.	R/W	0
210h	DRIVE_ STRENGTH2	TDO_DS	15-14	Drive strength value for TDO pin. 00: 4mA; 01: 6mA; 10: 8mA(1.8V), 10mA(3.3V); 11: 10mA(1.8V), 12mA(3.3V)	R/W	0
		RSVD	13-0	Reserved.	R/W	0
211h - 232h	RSVD	RSVD	15-0	Reserved.	R	0

4.14.2 SD Audio Core

Table 4-35: SD Audio Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
400h	CFG_AUD	CTR_AGR	15	Selects replacement of audio control packets. LOW - Do not replace audio control packets HIGH - Replace all audio control packets	R/W	0
		AGR	14	Selects Audio Group Replacement operating mode. Active HIGH.	R/W	0
		ONE_AGR	13	Specifies the replacement of just the primary group. LOW - Replace both the primary and secondary groups HIGH - Replace only the primary group	R/W	0
		CTRB_ON	12	Specifies the embedding of the secondary group audio control packets. Active HIGH.	R/W	1
		CLEAR_AUDIO	11	Clears all audio FIFO buffers and puts them in the start-up state. Active HIGH.	R/W	0
		AFNB_AUTO	10	Enables Secondary group audio frame number generation. Active HIGH.	R/W	1
		CTRA_ON	9	Specifies the embedding of primary group audio control packets. Active HIGH.	R/W	1
		AUDIO_24BIT	8	Specifies the sample size for embedded audio. HIGH - 24-bit LOW - 20-bit/16-bit	R/W	0
		AFNA_AUTO	7	Enables Primary group audio frame number generation. Active HIGH.	R/W	1
		AFN_OFS	6-4	Offset to add to generated Audio Frame Number. Must be in the range of 0 to 4.	R/W	0
		IDB	3-2	Specifies the secondary audio group to embed. NOTE: Should IDA and IDB be set to the same value, they automatically revert to their default values.	R/W	1
		IDA	1-0	Specifies the primary audio group to embed. NOTE: Should IDA and IDB be set to the same value, they automatically revert to their default values.	R/W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
401h	FIFO_BUF_SIDE	RSVD	15-3	Reserved.	R	0
		OFFSET_DISABLE	2	Set to disable staggering of secondary group audio sample distribution by one line. Active HIGH.	R/W	0
		OS_SEL	1-0	Specifies the audio FIFO buffer size. 00-52 samples deep, 26 sample start-up count 01-24 samples deep, 12 sample start-up count 10-12 samples deep, 6 sample start-up count 11-Reserved	R/W	0
402h	AES_EBU_ERR_STATUS	RSVD	15-4	Reserved.	R	0
		AES_ERRD	3	Stereo Pair D (7&8) audio input parity error when using AES format. Automatically cleared when read.	R	0
		AES_ERRC	2	Stereo Pair C (5&6) audio input parity error when using AES format. Automatically cleared when read.	R	0
		AES_ERRB	1	Stereo Pair B (3&4) audio input parity error when using AES format. Automatically cleared when read.	R	0
		AES_ERRA	0	Stereo Pair A (1&2) audio input parity error when using AES format. Automatically cleared when read.	R	0
403h	CHANNEL_STAT_REGEN	RSVD	15-1	Reserved.	R	0
		ACS_REGEN	0	Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. LOW: Do not replace Channel Status HIGH: Replace Channel Status of all channels	R/W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
404h	PACKET_DET_ STATUS	RSVD	15-14	Reserved.	R	0
		AXPG4_DET	13	Set while Group 4 audio extended packets are detected.	R	0
		AXPG3_DET	12	Set while Group 3 audio extended packets are detected.	R	0
		AXPG2_DET	11	Set while Group 2 audio extended packets are detected.	R	0
		AXPG1_DET	10	Set while Group 1 audio extended packets are detected.	R	0
		ACPG4_DET	9	Set while Group 4 audio control packets are detected.	R	0
		ACPG3_DET	8	Set while Group 3 audio control packets are detected.	R	0
		ACPG2_DET	7	Set while Group 2 audio control packets are detected.	R	0
		ACPG1_DET	6	Set while Group 1 audio control packets are detected.	R	0
		ADPG4_DET	5	Set while Group 4 audio data packets are detected.	R	0
		ADPG3_DET	4	Set while Group 3 audio data packets are detected.	R	0
		ADPG2_DET	3	Set while Group 2 audio data packets are detected.	R	0
		ADPG1_DET	2	Set while Group 1 audio data packets are detected.	R	0
		ACS_APPLY_WAITB	1	Set while the GS1672 is waiting for a status boundary in the Secondary group before applying the ACSR[183:0] data to that group.	R	0
		ACS_APPLY_WAITA	0	ACS_APPLY_WAITA: Set while the GS1672 is waiting for a status boundary in Primary group before applying the ACSR[183:0] data.	R	0
405h	AES_EBU_ERR_ STATUS1	RSVD	15-6	Reserved.	R	0
		FINAL_HELD_ASD_ERR	5	Final audio sample distribution error.	R	0
		HELD_ASD_ERR	4	Audio sample distribution error.	R	0
		HELD_AES_ERR	3-0	AES received errors for the 4 audio lines.	R	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
406h	CASCADE	RSVD	15-1	Reserved.	R	0
		EN_CASCADE	0	If HIGH, puts the GS1672 into cascade mode. This bit is only effective if the AGR bit = LOW.	R/W	0
407h - 40Ah	RSVD	RSVD	15-0	Reserved.	R	0
40Bh	SERIAL_AUDIO_ FORMAT	AMD	15-14	Audio input format selector for Stereo Pair D input channels 7 and 8. 00: AES/EBU 01: Serial Left Justified 10: Serial Right Justified 11: I^2S	R/W	3
		AMC	13-12	Audio input format selector for Stereo Pair C input channels 5 and 6. (See above for decoding).	R/W	3
		AMB	11-10	Audio input format selector for Stereo Pair B input channels 3 and 4. (See above for decoding).	R/W	3
		AMA	9-8	Audio input format selector for Stereo Pair A input channels 1 and 2. (See above for decoding).	R/W	3
		MUTE8	7	Audio input channel 8 mute enable. Active HIGH.	R/W	0
		MUTE7	6	Audio input channel 7 mute enable. Active HIGH.	R/W	0
		MUTE6	5	Audio input channel 6 mute enable. Active HIGH.	R/W	0
		MUTE5	4	Audio input channel 5 mute enable. Active HIGH.	R/W	0
		MUTE4	3	Audio input channel 4 mute enable. Active HIGH.	R/W	0
		MUTE3	2	Audio input channel 3 mute enable. Active HIGH.	R/W	0
		MUTE2	1	Audio input channel 2 mute enable. Active HIGH.	R/W	0
		MUTE1	0	Audio input channel 1 mute enable. Active HIGH.	R/W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
40Ch	CHANNEL_XP_GRPA	RSVD	15	Reserved.	R	0
		GPA_WCLK_SRC	14-12	Primary Audio group word clock source selector. Input channel 1 000 Input channel 2 001 Input channel 3 010 Input channel 4 011 Input channel 5 100 Input channel 6 101 Input channel 7 110 Input channel 8 111	R/W	0
		GPA_CH4_SRC	11-9	Primary Audio group channel 4 source selector. 011.	R/W	3
		GPA_CH3_SRC	8-6	Primary Audio group channel 3 source selector. 010.	R/W	2
		GPA_CH2_SRC	5-3	Primary Audio group channel 2 source selector. 001.	R/W	1
		GPA_CH1_SRC	2-0	Primary Audio group channel 1 source selector. 000 - Input channel	R/W	0
40Dh	CHANNEL_XP_GRPB	RSVD	15	Reserved.	R	0
		GPB_WCLK_SRC	14-12	Secondary Audio group word clock source selector.	R/W	4
		GPB_CH4_SRC	11-9	Secondary Audio group channel 4 source selector.	R/W	7
		GPB_CH3_SRC	8-6	Secondary Audio group channel 3 source selector.	R/W	6
		GPB_CH2_SRC	5-3	Secondary Audio group channel 2 source selector.	R/W	5
		GPB_CH1_SRC	2-0	Secondary Audio group channel 1 source selector.	R/W	4

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
40Eh	INTERRUPT_ MASK	EN_ASD_ERR	15	Asserts ASD error flag.	R/W	0
		EN_NO_VIDEO	14	Mask bit when the video format is unknown.	R/W	0
		EN_MUX_ERRB	13	Asserts AUDIO_INT when the MUX_ERRB flag is set.	R/W	0
		EN_MUX_ERRA	12	Asserts AUDIO_INT when the MUX_ERRA flag is set.	R/W	0
		EN_AES_ERRD	11	Asserts AUDIO_INT when the AES_ERRD flag is set.	R/W	0
		EN_AES_ERRC	10	Asserts AUDIO_INT when the AES_ERRC flag is set.	R/W	0
		EN_AES_ERRB	9	Asserts AUDIO_INT when the AES_ERRB flag is set.	R/W	0
		EN_AES_ERRA	8	Asserts AUDIO_INT when the AES_ERRA flag is set.	R/W	0
		EN_ACPG4_DET	7	Asserts AUDIO_INT when the ACPG4_DET flag is set.	R/W	0
		EN_ACPG3_DET	6	Asserts AUDIO_INT when the ACPG3_DET flag is set.	R/W	0
		EN_ACPG2_DET	5	Asserts AUDIO_INT when the ACPG2_DET flag is set.	R/W	0
		EN_ACPG1_DET	4	Asserts AUDIO_INT when the ACPG1_DET flag is set.	R/W	0
		EN_ADPG4_DET	3	Asserts AUDIO_INT when the ADPG4_DET flag is set.	R/W	0
		EN_ADPG3_DET	2	Asserts AUDIO_INT when the ADPG3_DET flag is set.	R/W	0
		EN_ADPG2_DET	1	Asserts AUDIO_INT when the ADPG2_DET flag is set.	R/W	0
		EN_ADPG1_DET	0	Asserts AUDIO_INT when the ADPG1_DET flag is set.	R/W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
40Fh	ACTIVE_ CHANNEL	RSVD	15-13	Reserved.	R	0
		MUTE_ALL	12	Mutes all input audio channels.	R/W	0
		LSB_FIRSTD	11	Causes the fourth stereo pair serial input formats to use LSB first. Used in conjunction with AMD, and only relevant when AMD is 01 or 10 Figure 4-16 to 4-19.	R/W	0
		LSB_FIRSTC	10	Causes the third stereo pair serial input formats to use LSB first. Used in conjunction with AMC and only relevant when AMC is 01 or 10 Figure 4-16 to 4-19.	R/W	0
		LSB_FIRSTB	9	Causes the second stereo pair serial input formats to use LSB first. Used in conjunction with AMB and only relevant when AMD is 01 or 10 Figure 4-16 to 4-19.	R/W	0
		LSB_FIRSTA	8	Causes the first stereo pair serial input formats to use LSB first. Used in conjunction with AMA and only relevant when AMA is 01 or 10 Figure 4-16 to 4-19.	R/W	0
		ACT8	7	Specifies embedding of secondary audio group channel 8. Active HIGH.	R/W	1
		ACT7	6	Specifies embedding of secondary audio group channel 7. Active HIGH.	R/W	1
		ACT6	5	Specifies embedding of secondary audio group channel 6. Active HIGH.	R/W	1
		ACT5	4	Specifies embedding of secondary audio group channel 5. Active HIGH.	R/W	1
		ACT4	3	Specifies embedding of primary audio group channel 4. Active HIGH.	R/W	1
		ACT3	2	Specifies embedding of primary audio group channel 3. Active HIGH.	R/W	1
		ACT2	1	Specifies embedding of primary audio group channel 2. Active HIGH.	R/W	1
		ACT1	0	Specifies embedding of primary audio group channel 1. Active HIGH.	R/W	1

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
410h	XPOINT_ERROR	RSVD	15-3	Reserved.	R	0
		MUX_ERRB	2	Set in Cascade mode when the incoming video contains packets with the same group number as the Secondary Group.	R	0
		MUX_ERRA	1	Set in Cascade mode when the incoming video contains packets with the same group number as the Primary Group.	R	0
		XPOINT_ERROR	0	Set when the crosspoint switch is configured to put the same audio channel in both Primary and Secondary Groups.	R	0
411h-41Fh	RSVD	RSVD	–	Reserved.	R	0
420h	CHANNEL_STATUS_REG_1	RSVD	15-8	Reserved.	R	0
		ACSR_BYTE_1	7-0	Audio channel status block byte 1.	R/W	133
421h	CHANNEL_STATUS_REG_2	RSVD	15-8	Reserved.	R	0
		ACSR_BYTE_2	7-0	Audio channel status block byte 2.	R/W	8
422h	CHANNEL_STATUS_REG_3	ACSR_BYTE_4	15-8	Audio channel status block byte 4.	R/W	0
		ACSR_BYTE_3	7-0	Audio channel status block byte 3.	R/W	44
423h	CHANNEL_STATUS_REG_4	ACSR_BYTE_6	15-8	Audio channel status block byte 6.	R/W	0
		ACSR_BYTE_5	7-0	Audio channel status block byte 5.	R/W	0
424h	CHANNEL_STATUS_REG_5	ACSR_BYTE_8	15-8	Audio channel status block byte 8.	R/W	0
		ACSR_BYTE_7	7-0	Audio channel status block byte 7.	R/W	0
425h	CHANNEL_STATUS_REG_6	ACSR_BYTE_10	15-8	Audio channel status block byte 10.	R/W	0
		ACSR_BYTE_9	7-0	Audio channel status block byte 9.	R/W	0
426h	CHANNEL_STATUS_REG_7	ACSR_BYTE_12	15-8	Audio channel status block byte 12.	R/W	0
		ACSR_BYTE_11	7-0	Audio channel status block byte 11.	R/W	0
427h	CHANNEL_STATUS_REG_8	ACSR_BYTE_14	15-8	Audio channel status block byte 14.	R/W	0
		ACSR_BYTE_13	7-0	Audio channel status block byte 13.	R/W	0
428h	CHANNEL_STATUS_REG_9	ACSR_BYTE_16	15-8	Audio channel status block byte 16.	R/W	0
		ACSR_BYTE_15	7-0	Audio channel status block byte 15.	R/W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
429h	CHANNEL_ STATUS_REG_10	ACSR_BYTE_18	15-8	Audio channel status block byte 18.	R/W	0
		ACSR_BYTE_17	7-0	Audio channel status block byte 17.	R/W	0
42Ah	CHANNEL_ STATUS_REG_11	ACSR_BYTE_20	15-8	Audio channel status block byte 20.	R/W	0
		ACSR_BYTE_19	7-0	Audio channel status block byte 19.	R/W	0
42Bh	CHANNEL_ STATUS_REG_12	ACSR_BYTE_22	15-8	Audio channel status block byte 22.	R/W	0
		ACSR_BYTE_21	7-0	Audio channel status block byte 21.	R/W	0
42Ch	CHANNEL_ STATUS_REG_13	RSVD	15-8	Reserved.	R/W	0
		ACSR_BYTE_23	7-0	Audio channel status block byte 23.	R/W	0
42Dh - 43Fh	RSVD	RSVD	–	Reserved.	R	0
440h	AUDIO_CTRL_ GRPA_REG_1	RSVD	15-9	Reserved.	R	0
		DEL1A_BYTE_1	8-1	Primary Audio group delay data for channel 1 byte 1.	R/W	0
		EBIT1A	0	Primary Audio group delay data for channel 1. HIGH - indicates delay specified at DEL1A_BYTE_1 is valid. See SMPTE Standard 272M for additional information.	R/W	0
441h	AUDIO_CTRL_ GRPA_REG_2	RSVD	15-9	Reserved.	R	0
		DEL1A_BYTE_2	8-0	Primary Audio group delay data for channel 1 byte 2.	R/W	0
442h	AUDIO_CTRL_ GRPA_REG_3	RSVD	15-9	Reserved.	R	0
		DEL1A_BYTE_3	8-0	Primary Audio group delay data for channel 1 byte 3.	R/W	0
443h	AUDIO_CTRL_ GRPA_REG_4	RSVD	15-9	Reserved.	R	0
		DEL2A_BYTE_1	8-1	Primary Audio group delay data for channel 2 byte 1.	R/W	0
		EBIT2A	0	Primary Audio group delay data valid flag for channel 2.	R/W	0
444h	AUDIO_CTRL_ GRPA_REG_5	RSVD	15-9	Reserved.	R	0
		DEL2A_BYTE_2	8-0	Primary Audio group delay data for channel 2 byte 2.	R/W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
445h	AUDIO_CTRL_GRPA_REG_6	RSVD	15-9	Reserved.	R	0
		DEL2A_BYTE_3	8-0	Primary Audio group delay data for channel 2 byte 3.	R/W	0
446h	AUDIO_CTRL_GRPA_REG_7	RSVD	15-9	Reserved.	R	0
		DEL3A_BYTE_1	8-1	Primary Audio group delay data for channel 3 byte 1.	R/W	0
		EBIT3A	0	Primary Audio group delay data valid flag for channel 3.	R/W	0
447h	AUDIO_CTRL_GRPA_REG_8	RSVD	15-9	Reserved.	R	0
		DEL3A_BYTE_2	8-0	Primary Audio group delay data for channel 3 byte 2.	R/W	0
448h	AUDIO_CTRL_GRPA_REG_9	RSVD	15-9	Reserved.	R	0
		DEL3A_BYTE_3	8-0	Primary Audio group delay data for channel 3 byte 3.	R/W	0
449h	AUDIO_CTRL_GRPA_REG_10	RSVD	15-9	Reserved.	R	0
		DEL4A_BYTE_1	8-1	Primary Audio group delay data for channel 4 byte 1.	R/W	0
		EBIT4A	0	Primary Audio group delay data valid flag for channel 4.	R/W	0
44Ah	AUDIO_CTRL_GRPA_REG_11	RSVD	15-9	Reserved.	R	0
		DEL4A_BYTE_2	8-0	Primary Audio group delay data for channel 4 byte 2.	R/W	0
44Bh	AUDIO_CTRL_GRPA_REG_12	RSVD	15-9	Reserved.	R	0
		DEL4A_BYTE_3	8-0	Primary Audio group delay data for channel 4 byte 3.	R/W	0
44Ch	AUDIO_CTRL_GRPB_REG_1	RSVD	15-9	Reserved.	R	0
		DEL1B_BYTE_1	8-1	Secondary Audio group delay data for channel 1 byte 1.	R/W	0
		EBIT1B	0	Secondary Audio group delay data valid flag for channel 1.	R/W	0
44Dh	AUDIO_CTRL_GRPB_REG_2	RSVD	15-9	Reserved.	R	0
		DEL1B_BYTE_2	8-0	Secondary Audio group delay data for channel 1 byte 2.	R/W	0
44Eh	AUDIO_CTRL_GRPB_REG_3	RSVD	15-9	Reserved.	R	0
		DEL1B_BYTE_3	8-0	Secondary Audio group delay data for channel 1 byte 3.	R/W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit Name	Bit	Description	R/W	Default
44Fh	AUDIO_CTRL_GRPB_REG_4	RSVD	15-9	Reserved.	R	0
		DEL2B_BYTE_1	8-1	Secondary Audio group delay data for channel 2 byte 1.	R/W	0
		EBIT2B	0	Secondary Audio group delay data valid flag for channel 2.	R/W	0
450h	AUDIO_CTRL_GRPB_REG_5	RSVD	15-9	Reserved.	R	0
		DEL2B_BYTE_2	8-0	Secondary Audio group delay data for channel 2 byte 2.	R/W	0
451h	AUDIO_CTRL_GRPB_REG_6	RSVD	15-9	Reserved.	R	0
		DEL2B_BYTE_3	8-0	Secondary Audio group delay data for channel 2 byte 3.	R/W	0
452h	AUDIO_CTRL_GRPB_REG_7	RSVD	15-9	Reserved.	R	0
		DEL3B_BYTE_1	8-1	Secondary Audio group delay data for channel 3 byte 1.	R/W	0
		EBIT3B	0	Secondary Audio group delay data valid flag for channel 3.	R/W	0
453h	AUDIO_CTRL_GRPB_REG_8	RSVD	15-9	Reserved.	R	0
		DEL3B_BYTE_2	8-0	Secondary Audio group delay data for channel 3 byte 2.	R/W	0
454h	AUDIO_CTRL_GRPB_REG_9	RSVD	15-9	Reserved.	R	0
		DEL3B_BYTE_3	8-0	Secondary Audio group delay data for channel 3 byte 3.	R/W	0
455h	AUDIO_CTRL_GRPB_REG_10	RSVD	15-9	Reserved.	R	0
		DEL4B_BYTE_1	8-1	Secondary Audio group delay data for channel 4 byte 1.	R/W	0
		EBIT4B	0	Secondary Audio group delay data valid flag for channel 4.	R/W	0
456h	AUDIO_CTRL_GRPB_REG_11	RSVD	15-9	Reserved.	R	0
		DEL4B_BYTE_2	8-0	Secondary Audio group delay data for channel 4 byte 2.	R/W	0
457h	AUDIO_CTRL_GRPB_REG_12	RSVD	15-9	Reserved.	R	0
		DEL4B_BYTE_3	8-0	Secondary Audio group delay data for channel 4 byte 3.	R/W	0

4.14.3 HD Audio Core Registers

Table 4-36: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
800h	CFG_AUD	CTR_AGR	15	Selects replacement of audio control packets. LOW-Do not replace audio control packets HIGH-Replace all audio control packets	R/W	0
		AGR	14	Selects Audio Group Replacement operating mode. Active HIGH.	R/W	0
		ONE_AGR	13	Specifies the replacement of just the primary group. LOW - Replace both the primary and secondary groups. HIGH - Replace only the primary group.	R/W	0
		CTRB_ON	12	Specifies the embedding of the secondary group audio control packets. Active HIGH.	R/W	1
		ASXB	11	Secondary Group asynchronous mode. Active HIGH.	R/W	0
		AFNB_AUTO	10	Enables Secondary group audio frame number generation. Active HIGH.	R/W	1
		CTRA_ON	9	Specifies the embedding of primary group audio control packets. Active HIGH.	R/W	1
		ASXA	8	Primary Group asynchronous mode.	R/W	0
		AFNA_AUTO	7	Enables Primary group audio frame number generation.	R/W	1
		ANF_OFS	6-4	Offset to add to generated Audio Frame Number. Must be in the range of 0 to 4.	R/W	0
		IDB	3-2	Specifies the Secondary audio group to extract. 00: Audio group #1 01: Audio group #2 10: Audio group #3 11: Audio group #4	R/W	1
		IDA	1-0	Specifies the Primary audio group to extract. 00: Audio group #1 01: Audio group #2 10: Audio group #3 11: Audio group #4	R/W	0
801h	RSVD	RSVD	15-0	Reserved.	R	0

Table 4-36: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
802h	CHANNEL_STAT_REGREN	RSVD	15-1	Reserved.	R	0
		ACS_REGEN	0	Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. LOW: Do not replace Channel Status HIGH: Replace Channel Status of all channels	R/W	0
803h 803h	PACKET_DET_STATUS	RSVD	15-14	Reserved.	R	0
		AES_ERRD	13	Stereo Pair D audio input parity error when using AES format. Automatically cleared when read.	R	0
		AES_ERRC	12	Stereo Pair C audio input parity error when using AES format. Automatically cleared when read.	R	0
		AES_ERRB	11	Stereo Pair B audio input parity error when using AES format. Automatically cleared when read.	R	0
		AES_ERRA	10	Stereo Pair A audio input parity error when using AES format. Automatically cleared when read.	R	0
		ACPG4_DET	9	Set while Group 4 audio control packets are detected.	R	0
		ACPG3_DET	8	Set while Group 3 audio control packets are detected.	R	0
		ACPG2_DET	7	Set while Group 2 audio control packets are detected.	R	0
		ACPG1_DET	6	Set while Group 1 audio control packets are detected.	R	0
		ADPG4_DET	5	Set while Group 4 audio data packets are detected.	R	0
		ADPG3_DET	4	Set while Group 3 audio data packets are detected.	R	0
		ADPG2_DET	3	Set while Group 2 audio data packets are detected.	R	0
		ADPG1_DET	2	Set while Group 1 audio data packets are detected.	R	0
		ACS_APPLY_WAITB	1	Set while the GS1672 is waiting for a status boundary in the Secondary group before applying the ACSR[183:0] data to that group.	R	0
		ACS_APPLY_WAITA	0	ACS_APPLY_WAITA: Set while the multiplexer is waiting for a status boundary in Primary group before applying the ACSR[183:0] data.	R	0

Table 4-36: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
804h	AES_EBU_ERR_STATUS	RSVD	15-4	Reserved.	R	0
		HELD_AES_ERR	3-0	AES received errors for the 4 audio lines.	R	0
805h	CASCADE	RSVD	15-1	Reserved.	R	0
		EN_CASCADE	0	If HIGH, puts the GS1672 into cascade mode. This bit is only effective if the AGR bit = LOW.	R/W	0
806h - 809h	RSVD	RSVD	15-0	Reserved.	R	0
80Ah	SERIAL_AUDIO_FORMAT	AMD	15-14	Audio input format selector for Stereo Pair D input channels 7 and 8. 00: AES/EBU 01: Serial Left Justified 10: Serial Right Justified 11: I^2S	R/W	3
		AMC	13-12	Audio input format selector for Stereo Pair C input channels 5 and 6. (See above for decoding).	R/W	3
		AMB	11-10	Audio input format selector for Stereo Pair B input channels 3 and 4. (See above for decoding).	R/W	3
		AMA	9-8	Audio input format selector for Stereo Pair A input channels 1 and 2. (See above for decoding).	R/W	3
		MUTE8	7	Audio input channel 8 mute enable.	R/W	0
		MUTE7	6	Audio input channel 7 mute enable.	R/W	0
		MUTE6	5	Audio input channel 6 mute enable.	R/W	0
		MUTE5	4	Audio input channel 5 mute enable.	R/W	0
		MUTE4	3	Audio input channel 4 mute enable.	R/W	0
		MUTE3	2	Audio input channel 3 mute enable.	R/W	0
		MUTE2	1	Audio input channel 2 mute enable.	R/W	0
		MUTE1	0	Audio input channel 1 mute enable.	R/W	0

Table 4-36: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
80Bh	CHANNEL_XP_GRPA	RSVD	15	Reserved.	R	0
		GPA_WCLK_SRC	14-12	Primary Audio group word clock source selector.	R/W	0
		GPA_CH4_SRC	11-9	Primary Audio group channel 4 source selector.	R/W	3
		GPA_CH3_SRC	8-6	Primary Audio group channel 3 source selector.	R/W	2
		GPA_CH2_SRC	5-3	Primary Audio group channel 2 source selector.	R/W	1
		GPA_CH1_SRC	2-0	Primary Audio group channel 1 source selector.	R/W	0
80Ch	CHANNEL_XP_GRPB	RSVD	15	Reserved.	R	0
		GPB_WCLK_SRC	14-12	Secondary Audio group word clock source selector.	R/W	4
		GPB_CH4_SRC	11-9	Secondary Audio group channel 4 source selector.	R/W	7
		GPB_CH3_SRC	8-6	Secondary Audio group channel 3 source selector.	R/W	6
		GPB_CH2_SRC	5-3	Secondary Audio group channel 2 source selector.	R/W	5
		GPB_CH1_SRC	2-0	Secondary Audio group channel 1 source selector.	R/W	4

Table 4-36: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
80Dh	INTERRUPT_ MASK	RSVD	15	Reserved.	R	0
		EN_NO_VIDEO	14	Asserts AUDIO_INT mask bit when the video format is unknown i.e. when NO_VIDEO register bit is set.	R/W	0
		EN_MUX_ERRB	13	Asserts AUDIO_INT when the MUX_ERRB flag is set.	R/W	0
		EN_MUX_ERRA	12	Asserts AUDIO_INT when the MUX_ERRA flag is set.	R/W	0
		EN_AES_ERRD	11	Asserts AUDIO_INT when the AES_ERRD flag is set.	R/W	0
		EN_AES_ERRC	10	Asserts AUDIO_INT when the AES_ERRC flag is set.	R/W	0
		EN_AES_ERRB	9	Asserts AUDIO_INT when the AES_ERRB flag is set.	R/W	0
		EN_AES_ERRA	8	Asserts AUDIO_INT when the AES_ERRA flag is set.	R/W	0
		EN_ACPG4_DET	7	Asserts AUDIO_INT when the ACPG4_DET flag is set.	R/W	0
		EN_ACPG3_DET	6	Asserts AUDIO_INT when the ACPG3_DET flag is set.	R/W	0
		EN_ACPG2_DET	5	Asserts AUDIO_INT when the ACPG2_DET flag is set.	R/W	0
		EN_ACPG2_DET	5	Asserts AUDIO_INT when the ACPG2_DET flag is set.	R/W	0
		EN_ACPG1_DET	4	Asserts AUDIO_INT when the ACPG1_DET flag is set.	R/W	0
		EN_ADPG4_DET	3	Asserts AUDIO_INT when the ADPG4_DET flag is set.	R/W	0
		EN_ADPG3_DET	2	Asserts AUDIO_INT when the ADPG3_DET flag is set.	R/W	0
		EN_ADPG2_DET	1	Asserts AUDIO_INT when the ADPG2_DET flag is set.	R/W	0
		EN_ADPG1_DET	0	Asserts AUDIO_INT when the ADPG1_DET flag is set.	R/W	0

Table 4-36: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
80Eh	ACTIVE_ CHANNEL	RSVD	15-13	Reserved.	R	0
		MUTE_ALL	12	Mutes all input audio channels.	R/W	0
		LSB_FIRSTD	11	Causes the fourth stereo pair serial input formats to use LSB first.	R/W	0
		LSB_FIRSTC	10	Causes the third stereo pair serial input formats to use LSB first.	R/W	0
		LSB_FIRSTB	9	Causes the second stereo pair serial input formats to use LSB first.	R/W	0
		LSB_FIRSTA	8	Causes the first stereo pair serial input formats to use LSB first.	R/W	0
		ACT8	7	Specifies embedding of secondary audio group channel 8. Active HIGH.	R/W	1
		ACT7	6	Specifies embedding of secondary audio group channel 7. Active HIGH.	R/W	1
		ACT6	5	Specifies embedding of secondary audio group channel 6. Active HIGH.	R/W	1
		ACT5	4	Specifies embedding of secondary audio group channel 5. Active HIGH.	R/W	1
		ACT4	3	Specifies embedding of secondary audio group channel 4. Active HIGH.	R/W	1
		ACT3	2	Specifies embedding of secondary audio group channel 3. Active HIGH.	R/W	1
		ACT2	1	Specifies embedding of secondary audio group channel 2. Active HIGH.	R/W	1
		ACT1	0	Specifies embedding of secondary audio group channel 1. Active HIGH.	R/W	1

Table 4-36: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
80Fh	XPOINT_ERROR	RSVD	15-3	Reserved.	R	0
		MUX_ERRB	2	Set in Cascade mode when the incoming video contains packets with the same group number as the Secondary Group.	R	0
		MUX_ERRA	1	Set in Cascade mode when the incoming video contains packets with the same group number as the Primary Group.	R	0
		XPOINT_ERROR	0	Set when the crosspoint switch is configured to put the same audio channel in both Primary and Secondary Groups.	R	0
810h -81Fh	RSVD	RSVD	–	Reserved.	R	0
820h	CHANNEL_ STATUS_REG_1	RSVD	15-8	Reserved.	R	0
		ACSR_BYTE_1	7-0	Audio channel status block byte 1.	R/W	133
821h	CHANNEL_ STATUS_REG_2	RSVD	15-8	Reserved.	R	0
		ACSR_BYTE_2	7-0	Audio channel status block byte 2.	R/W	8
822h	CHANNEL_ STATUS_REG_3	ACSR_BYTE_4	15-8	Audio channel status block byte 4.	R/W	0
		ACSR_BYTE_3	7-0	Audio channel status block byte 3.	R/W	44
823h	CHANNEL_ STATUS_REG_4	ACSR_BYTE_6	15-8	Audio channel status block byte 6.	R/W	0
		ACSR_BYTE_5	7-0	Audio channel status block byte 5.	R/W	0
824h	CHANNEL_ STATUS_REG_5	ACSR_BYTE_8	15-8	Audio channel status block byte 8.	R/W	0
		ACSR_BYTE_7	7-0	Audio channel status block byte 7.	R/W	0
825h	CHANNEL_ STATUS_REG_6	ACSR_BYTE_10	15-8	Audio channel status block byte 10.	R/W	0
		ACSR_BYTE_9	7-0	Audio channel status block byte 9.	R/W	0
826h	CHANNEL_ STATUS_REG_7	ACSR_BYTE_12	15-8	Audio channel status block byte 12.	R/W	0
		ACSR_BYTE_11	7-0	Audio channel status block byte 11.	R/W	0
827h	CHANNEL_ STATUS_REG_8	ACSR_BYTE_14	15-8	Audio channel status block byte 14.	R/W	0
		ACSR_BYTE_13	7-0	Audio channel status block byte 13.	R/W	0
828h	CHANNEL_ STATUS_REG_9	ACSR_BYTE_16	15-8	Audio channel status block byte 16.	R/W	0
		ACSR_BYTE_15	7-0	Audio channel status block byte 15.	R/W	0
829h	CHANNEL_ STATUS_REG_10	ACSR_BYTE_18	15-8	Audio channel status block byte 18.	R/W	0
		ACSR_BYTE_17	7-0	Audio channel status block byte 17.	R/W	0
82Ah	CHANNEL_ STATUS_REG_11	ACSR_BYTE_20	15-8	Audio channel status block byte 20.	R/W	0
		ACSR_BYTE_19	7-0	Audio channel status block byte 19.	R/W	0

Table 4-36: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
82Bh	CHANNEL_ STATUS_REG_12	ACSR_BYTE_22	15-8	Audio channel status block byte 22.	R/W	0
		ACSR_BYTE_21	7-0	Audio channel status block byte 21.	R/W	0
82Ch	CHANNEL_ STATUS_REG_13	RSVD	15-8	Reserved.	R	0
		ACSR_BYTE_23	7-0	Audio channel status block byte 23.	R/W	0
82Dh-83Fh	RSVD	RSVD	–	Reserved.	R	0
840h	AUDIO_CTRL_ GRPA_REG_1	RSVD	15-9	Reserved.	R	0
		DEL1_2A_BYTE_1	8-1	Primary Audio group delay data for channel 1 & 2.	R/W	0
		EBIT1_2A	0	Primary Audio group delay data valid flag for channel 1 & 2.	R/W	0
841h	AUDIO_CTRL_ GRPA_REG_2	RSVD	15-9	Reserved.	R	0
		DEL1_2A_BYTE_2	8-0	Primary Audio group delay data for channel 1 & 2.	R/W	0
842h	AUDIO_CTRL_ GRPA_REG_3	RSVD	15-9	Reserved.	R	0
		DEL1_2A_BYTE_3	8-0	Primary Audio group delay data for channel 1 & 2.	R/W	0
843h	AUDIO_CTRL_ GRPA_REG_4	RSVD	15-9	Reserved.	R	0
		DEL3_4A_BYTE_1	8-1	Primary Audio group delay data for channel 3 & 4.	R/W	0
		EBIT3_4A	0	Primary Audio group delay data valid flag for channel 3 & 4.	R/W	0
844h	AUDIO_CTRL_ GRPA_REG_5	RSVD	15-9	Reserved.	R	0
		DEL3_4A_BYTE_2	8-0	Primary Audio group delay data for channel 3 & 4.	R/W	0
845h	AUDIO_CTRL_ GRPA_REG_6	RSVD	15-9	Reserved.	R	0
		DEL3_4A_BYTE_3	8-0	Primary Audio group delay data for channel 3 & 4.	R/W	0
846h	AUDIO_CTRL_ GRPB_REG_1	RSVD	15-9	Reserved.	R	0
		DEL1_2B_BYTE_1	8-1	Secondary Audio group delay data for channel 1 & 2.	R/W	0
		EBIT1_2B	0	Secondary Audio group delay data valid flag for channel 1 & 2.	R/W	0
847h	AUDIO_CTRL_ GRPB_REG_2	RSVD	15-9	Reserved.	R	0
		DEL1_2B_BYTE_2	8-0	Secondary Audio group delay data for channel 1 & 2.	R/W	0

Table 4-36: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit Name	Bit	Description	R/W	Default
848h	AUDIO_CTRL_GRPB_REG_3	RSVD	15-9	Reserved.	R	0
		DEL1_2B_BYTE_3	8-0	Secondary Audio group delay data for channel 1 & 2.	R/W	0
849h	AUDIO_CTRL_GRPB_REG_4	RSVD	15-9	Reserved.	R	0
		DEL3_4B_BYTE_1	8-1	Secondary Audio group delay data for channel 3 & 4.	R/W	0
		EBIT3_4B	0	Secondary Audio group delay data for channel 3 & 4.	R/W	0
84Ah	AUDIO_CTRL_GRPB_REG_5	RSVD	15-9	Reserved.	R	0
		DEL3_4B_BYTE_2	8-0	Secondary Audio group delay data for channel 3 & 4.	R/W	0
84Bh	AUDIO_CTRL_GRPB_REG_6	RSVD	15-9	Reserved.	R	0
		DEL3_4B_BYTE_3	8-0	Secondary Audio group delay data for channel 3 & 4.	R/W	0

4.15 JTAG ID Codeword

The Platform ID for the GS16x2 family is 0Fh.

The part number field of the JTAG ID codeword for the GS1672 is set to 0F01h.

4.16 JTAG Test Operation

When the JTAG/$\overline{\text{HOST}}$ pin is HIGH, the GSPI host interface port is configured for JTAG test operation.

In this mode the SCLK, SDIN, SDOUT and $\overline{\text{CS}}$ become TCK, TDI, TDO and TMS. In addition, the TRST pin becomes active.

Boundary scan testing using the JTAG interface is enabled in this mode. When the JTAG/$\overline{\text{HOST}}$ pin is LOW, the dedicated JTAG interface is used. In this mode the TCK, TDI, TDO and TMS pins are active. This is the recommended mode for new designs.

4.17 Device Power-Up

Because the GS1672 is designed to operate in a multi-voltage environment, any power-up sequence is allowed. The Charge Pump, Phase Detector, Core Logic, Serial Digital Output and I/O Buffers can all be powered up in any order.

4.18 Device Reset

NOTE: At power-up, the device must be reset to operate correctly.

In order to initialize all internal operating conditions to their default states, hold the $\overline{\text{RESET}}$ signal LOW for a minimum of t_{reset} = 1ms after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs will be driven to a high-impedance state.

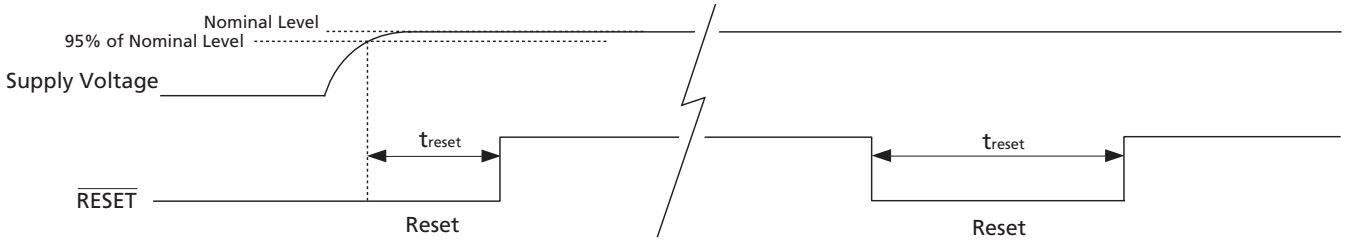
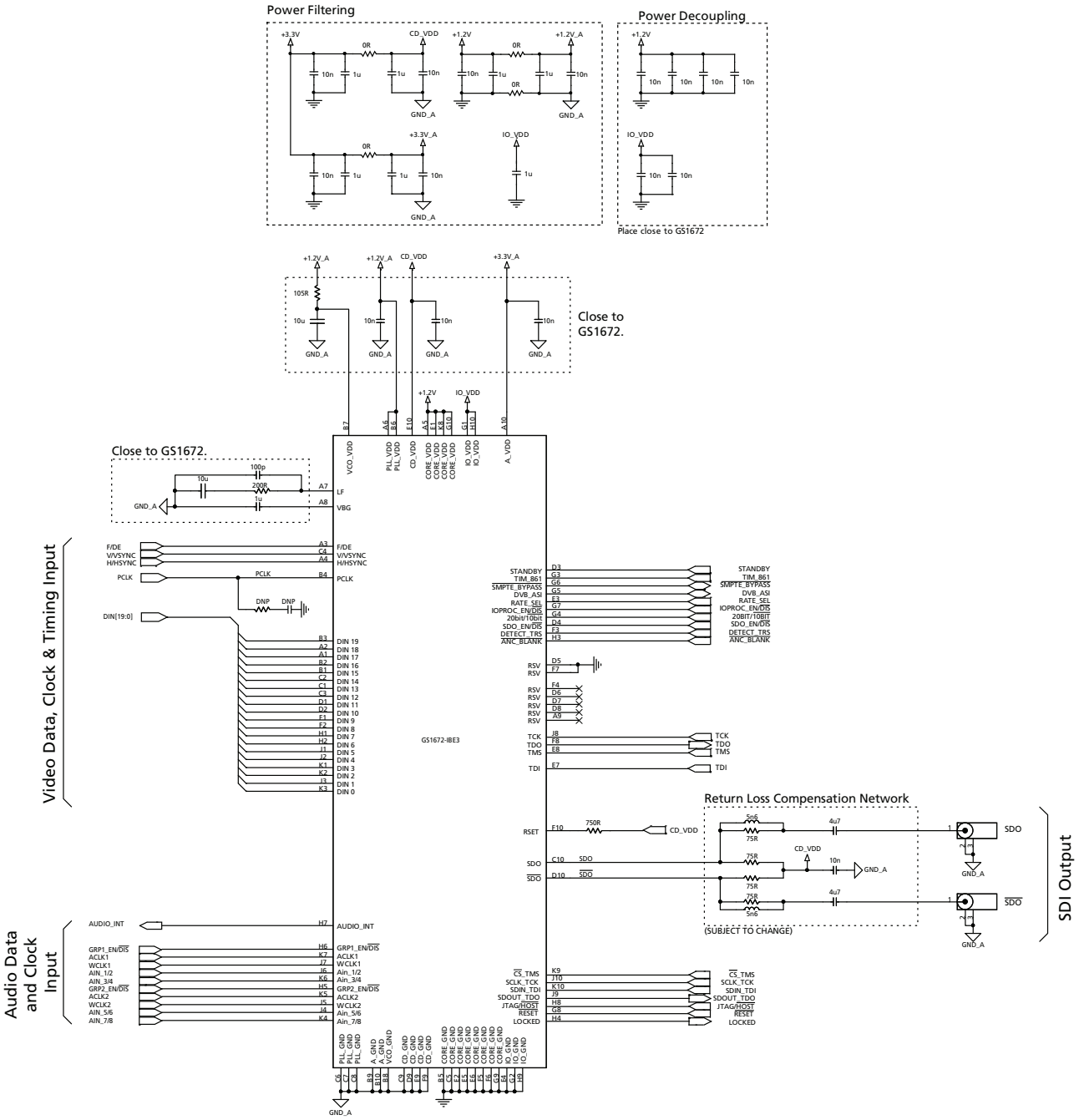


Figure 4-30: Reset Pulse

5. Application Reference Design

5.1 Typical Application Circuit



Notes:

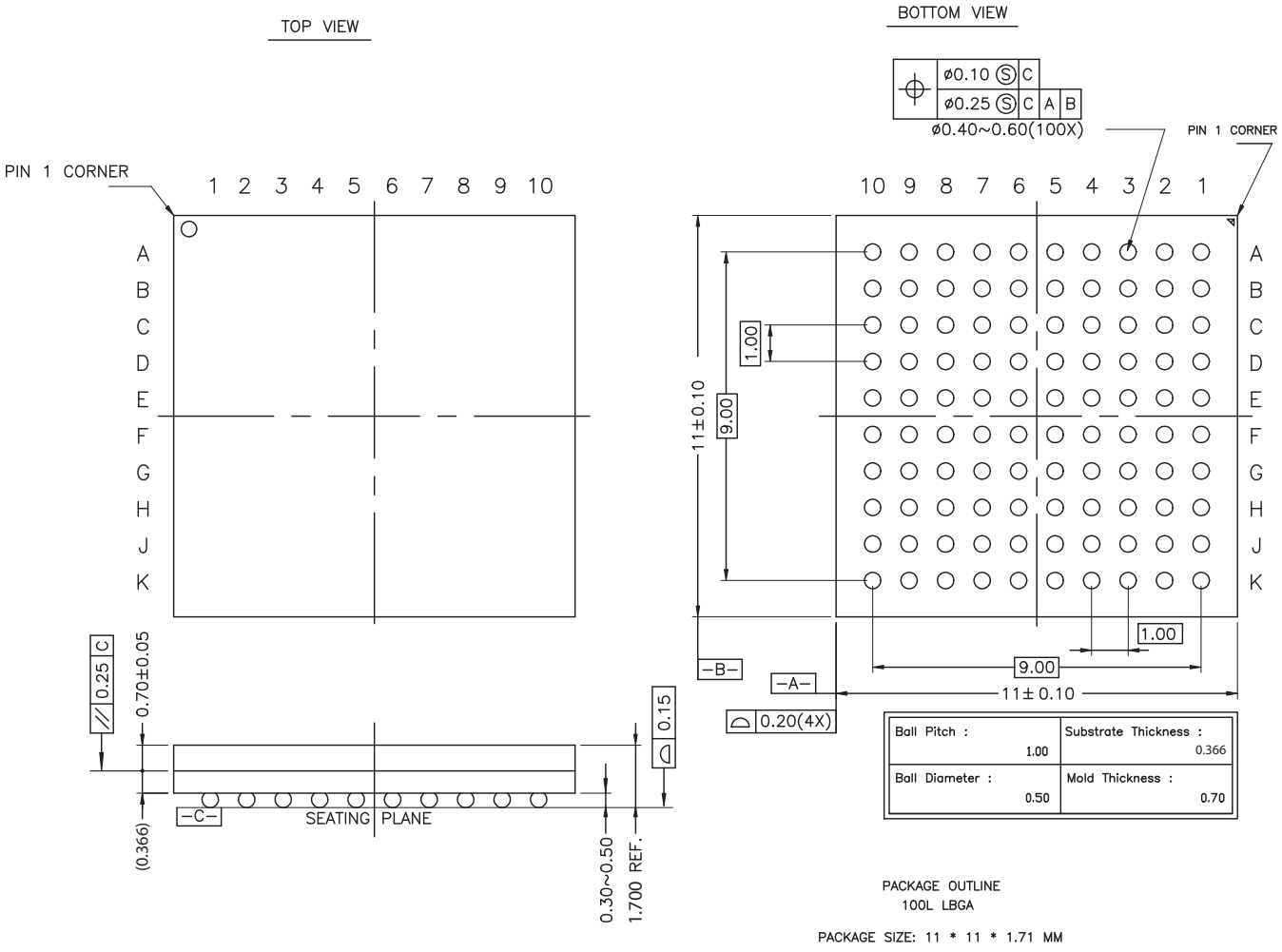
1. DNP (Do Not Populate).
2. The value of the series resistors on video data, clock, and timing connections should be determined by board signal integrity test (See Section 4.1.1).
3. For analog power and ground isolation refer to PCB layout guide.
4. For impedance controlled signals refer to PCB layout guide.

6. References & Relevant Standards

SMPTE 125M	Component video signal 4:2:2 – bit parallel interface
SMPTE 259M	10-bit 4:2:2 Component and 4fsc Composite Digital Signals - Serial Digital Interface
SMPTE 260M	1125 / 60 high definition production system – digital representation and bit parallel interface
SMPTE 267M	Bit parallel digital interface – component video signal 4:2:2 16 x 9 aspect ratio
SMPTE 272M	Formatting AES/EBU Audio and Auxiliary Data into Digital Video Ancillary Data Space
SMPTE 274M	1920 x 1080 scanning analog and parallel digital interfaces for multiple picture rates
SMPTE 291M	Ancillary Data Packet and Space Formatting
SMPTE 292	Bit-Serial Digital Interface for High-Definition Television Systems
SMPTE 293M	720 x 483 active line at 59.94Hz progressive scan production – digital representation
SMPTE 296M	1280 x 720 scanning, analog and digital representation and analog interface
SMPTE 299M	24-Bit Digital Audio Format for HDTV Bit-Serial Interface
SMPTE 305M	Serial Data Transport Interface
SMPTE 348M	High Data-Rate Serial Data Transport Interface (HD-SDTI)
SMPTE 352M	Video Payload Identification for Digital Television Interfaces
SMPTE 372	Dual Link 292M Interface for 1920 x 1080 Picture Raster
SMPTE RP165	Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television
SMPTE RP168	Definition of Vertical Interval Switching Point for Synchronous Video Switching
CEA 861	Video Timing Requirements

7. Package & Ordering Information

7.1 Package Dimensions



PACKAGE OUTLINE
100L LBGA

PACKAGE SIZE: 11 * 11 * 1.71 MM

* THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC M0192 (LOW PROFILE BGA FAMILY)

7.2 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	11mm x 11mm 100-ball LBGA
Package Drawing Reference	JEDEC M0192 (with exceptions noted in Package Dimensions on page 113).
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	10.4°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	37.1°C/W
Junction to Board Thermal Resistance, θ_{j-b}	26.4°C/W
Psi, ψ	0.4°C/W
Pb-free and RoHS Compliant	Yes

7.3 Marking Diagram

7.4 Solder Reflow Profiles

The GS1672 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 7-1.

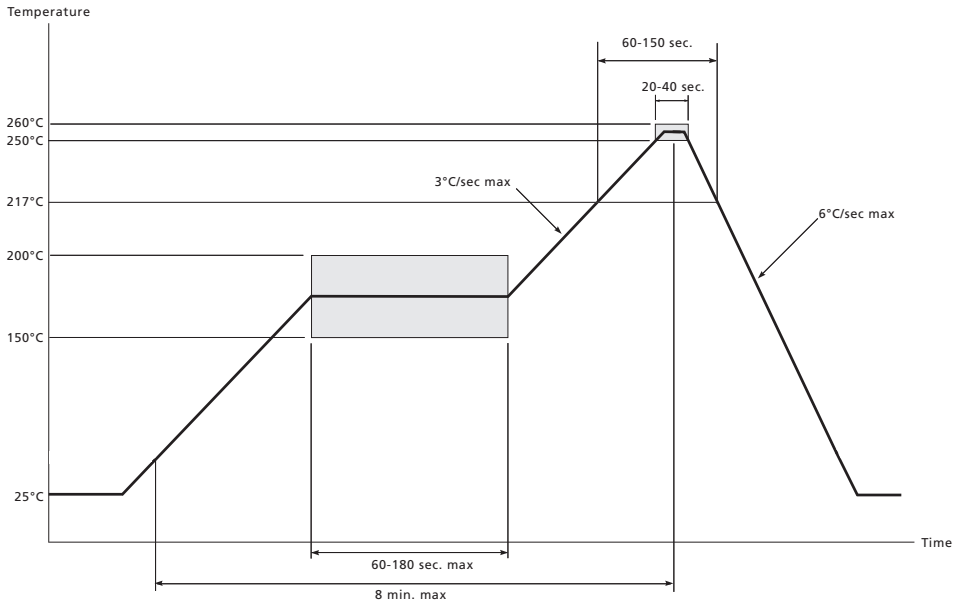


Figure 7-1: Pb-free Solder Reflow Profile

7.5 Ordering Information

Part Number	Package	Pb-free	Temperature Range
GS1672-IBE3	100-ball BGA	Yes	-20°C to 85°C

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

GENNUM CORPORATE HEADQUARTERS
4281 Harvester Road, Burlington, Ontario L7L 5M4 Canada
Phone: +1 (905) 632-2996
E-mail: corporate@gennum.com
Fax: +1 (905) 632-2055
www.gennum.com

OTTAWA
232 Herzberg Road, Suite 101
Kanata, Ontario K2K 2A1
Canada
Phone: +1 (613) 270-0458
Fax: +1 (613) 270-0429

CALGARY
3553 - 31st St. N.W., Suite 210
Calgary, Alberta T2L 2K7
Canada
Phone: +1 (403) 284-2672

UNITED KINGDOM
North Building, Walden Court
Parsonage Lane,
Bishop's Stortford Hertfordshire, CM23 5DB
United Kingdom
Phone: +44 1279 714170
Fax: +44 1279 714171

INDIA
#208(A), Nirmala Plaza,
Airport Road, Forest Park Square
Bhubaneswar 751009
India
Phone: +91 (674) 653-4815
Fax: +91 (674) 259-5733

SNOWBUSH IP - A DIVISION OF GENNUM
439 University Ave. Suite 1700
Toronto, Ontario M5G 1Y8
Canada
Phone: +1 (416) 925-5643
Fax: +1 (416) 925-0581
E-mail: sales@snowbush.com
Web Site: http://www.snowbush.com

MEXICO
288-A Paseo de Maravillas
Jesus Ma., Aguascalientes
Mexico 20900
Phone: +1 (416) 848-0328

JAPAN KK
Shinjuku Green Tower Building 27F
6-14-1, Nishi Shinjuku
Shinjuku-ku, Tokyo, 160-0023
Japan
Phone: +81 (03) 3349-5501
Fax: +81 (03) 3349-5505
E-mail: gennum-japan@gennum.com
Web Site: http://www.gennum.co.jp

TAIWAN
6F-4, No.51, Sec.2, Keelung Rd.
Sinyi District, Taipei City 11502
Taiwan R.O.C.
Phone: (886) 2-8732-8879
Fax: (886) 2-8732-8870
E-mail: gennum-taiwan@gennum.com

GERMANY
Hainbuchenstraße 2
80935 Muenchen (Munich), Germany
Phone: +49-89-35831696
Fax: +49-89-35804653
E-mail: gennum-germany@gennum.com

NORTH AMERICA WESTERN REGION
691 South Milpitas Blvd., Suite #200
Milpitas, CA 95035
United States
Phone: +1 (408) 934-1301
Fax: +1 (408) 934-1029
E-mail: naw_sales@gennum.com

NORTH AMERICA EASTERN REGION
4281 Harvester Road
Burlington, Ontario L7L 5M4
Canada
Phone: +1 (905) 632-2996
Fax: +1 (905) 632-2055
E-mail: nae_sales@gennum.com