GS3140

Multi-Rate Adaptive 3G SDI Equalizer

Key Features

- Multi-standard operation at rates between 1Mb/s and 2.97Gb/s
- SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259 compliant
- AES10 (MADI) compatible
- Industry leading cable reach, with automatic cable equalization for different lengths of cable
- Performance optimized for 125Mb/s, 270Mb/s, 1.485Gb/s, and 2.97Gb/s. Typical equalized length of Belden 1694A cable up to:
  - 200m at 2.97Gb/s
  - 280m at 1.485Gb/s
  - 500m at 270Mb/s
- 1.8V core power supply
- Typical power consumption of 84mW when DC-coupled at 1.2V with OUTPUT_SWING = 0011_b (see Table 4-2)
- Ultra-low power mode for shorter cable reach applications
- Upstream launch swing compensation from $250mV_{ppd}$ to $1V_{ppd}$ in approximately $50mV_{ppd}$ steps (Default $750mV_{ppd}$)
- Auto/Manual bypass (useful for low data rates with slow rise/fall times)
- Robust, noise-immune signal detection with squelch threshold adjustment
- Auto/Manual control of SLEEP/MUTE/DISABLE OUTPUT modes
- Data Rate detection and indication
  - <MADI, MADI, SD, HD, 3G differentiation
- Digital cable length indication (CLI)
- Differential output supports DC-coupling from 1.2V to 2.5V CML logic and AC-coupling for other logic families
- Programmable/Rate-dependent output de-emphasis level and delay
- Host interface for status and control
- 3kV HBM ESD protection on all pins
- Wide operating temperature range of -40°C to +85°C
- Small footprint QFN–COL package (16-pin, 4mm x 4mm)
- Pb-free and RoHS compliant
- Pin-compatible with the GS6140

Applications

- SMPTE ST 424, SMPTE ST 292, SMPTE ST 259 and AES10 coaxial cable serial digital interfaces

Description

The GS3140 is a high-speed BiCMOS device designed to equalize and restore signals received over cable.

The device is designed to support SMPTE ST 424, SMPTE ST 292, SMPTE ST 259 and AES10 (MADI), and it is optimized for performance at 125Mb/s, 270Mb/s, 1.485Gb/s, and 2.97Gb/s.

The device supports MADI serial signals at 125Mb/s with peak-to-peak launch amplitude between $300mV_{ppd}$ and $600mV_{ppd}$ (with AES10 spec rise and fall times) and $800mV_{ppd}$±10% (with SD-SDI rise and fall times).

The GS3140 features DC restoration to compensate for the DC content of SMPTE pathological signals.

Loss of Signal (LOS) is detected when the input carrier is lost or signal amplitude falls below a programmable threshold. This is further processed by a filter programmable up to 1.6s before LOS status is asserted. The device can be programmed to automatically sleep/mute/disable the output on loss of signal.

An interrupt pin (INT) indicates LOS by default, and can be programmed to signal various other statuses.

When the BYPASS control bit is set, the equalizing and DC restore stages are disengaged. This is useful for signals launched at the source with low data rates and/or slow rise and fall times.

The differential output can be DC-coupled to Semtech's reclockers and cable drivers, as well as industry-standard +1.2V, +1.8V and +2.5V CML logic by changing the voltage applied to the VCC_O pin.

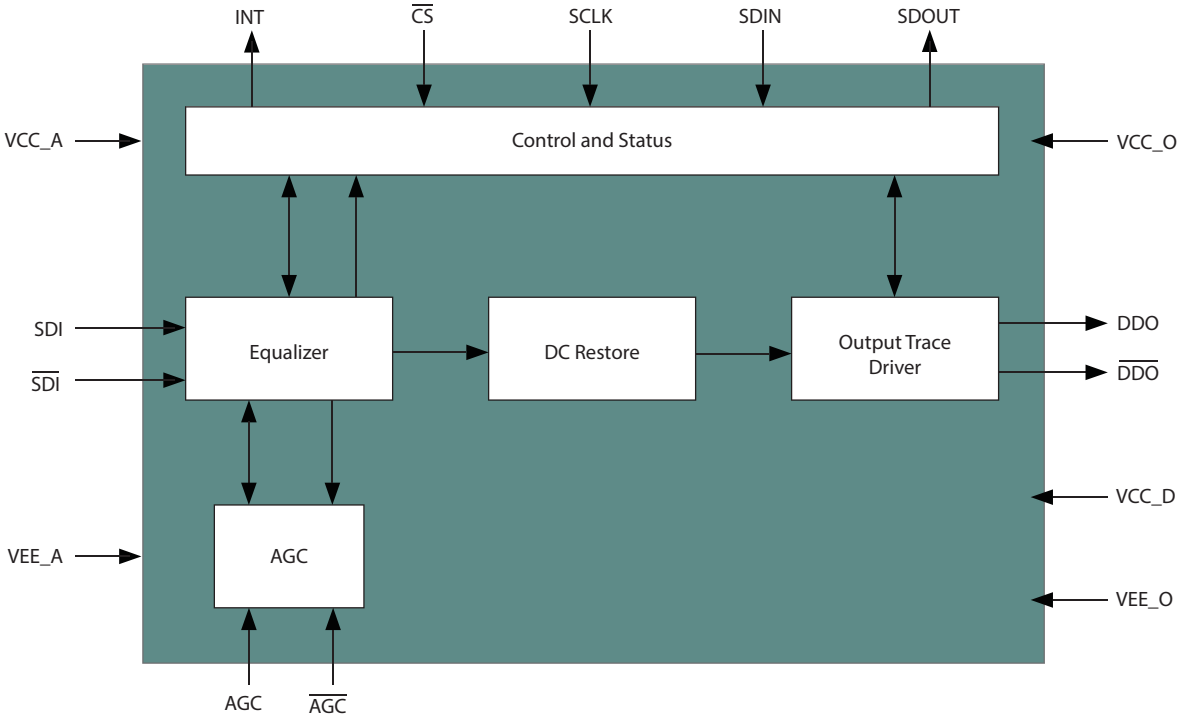
The GS3140 also features programmable output de-emphasis with eight user-selectable operating levels to support long PCB traces at the output of the device. The output swing can be programmed, via the user interface, from approximately 250mV$_{ppd}$ to 1V$_{ppd}$ in 50mV$_{ppd}$ steps.

The device comes in a 16-pin, 4mm x 4mm QFN–COL package.

Power consumption of the GS3140 is typically 84mW when DC-coupled to a +1.2V termination voltage with OUTPUT_SWING = 0011$_b$ (see Table 4-2).

The GS3140 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



GS3140 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
1	025657	—	May 2015	Converted document from Draft Data Sheet to Final Data Sheet.
0	024058	—	January 2015	New Document.

Contents

1. Pin Out

1.1 GS3140 Pin Assignment

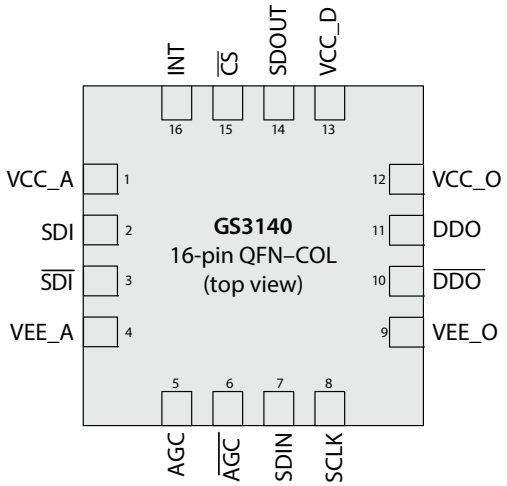


Figure 1-1: GS3140 Pin Out

1.2 GS3140 Pin Descriptions

Table 1-1: GS3140 Pin Descriptions

Pin Number	Name	Type	Description
1	VCC_A	Power	Most positive power supply connection for the input buffer and core. Connect to 1.8V.
2, 3	SDI, $\overline{\text{SDI}}$	Input	Serial digital differential input.
4	VEE_A	Power	Most negative power supply connection for the input buffer and core. Connect to GND.
5, 6	AGC, $\overline{\text{AGC}}$	Analog I/O	External Automatic Gain Control capacitor.
7	SDIN	Digital Input	Host Interface Serial Data Input.
8	SCLK	Digital Input	Host Interface Serial Clock Input.
9	VEE_O	Power	Most negative power supply connection for the output buffers, digital IO and digital circuits. Connect to GND.
10, 11	DDO, $\overline{\text{DDO}}$	Output	Serial digital differential output.
12	VCC_O	Power	Most positive power supply connection for the output buffer. Connect to 1.2V - 2.5V.

Table 1-1: GS3140 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
13	VCC_D	Power	Most positive power supply connection for the digital IO and the digital circuits. Connect to 1.8V.
14	SDOUT	Digital Output	Host Interface Serial Data Output
15	$\overline{CS}$	Digital Input	Host Interface Chip Select (active LOW)
16	INT	Digital Output	Interrupt, programmable status pin. Default is Loss of Signal (LOS)

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage - Core (VCC_A and VCC_D)	-0.5V to +2.1V
Supply Voltage - Output Driver (VCC_O)	-0.5V to +2.8V
Input ESD Voltage	3kV HBM
Storage Temperature Range (T_S)	-50°C to 125°C
Input Voltage Range (any input)	-0.3 to (VCC_A +0.3)V
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

V_{CC_A},V_{CC_D}, V_{CC_O} = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage - Core	V_{CC_A},V_{CC_D}	—	1.710	1.8	1.890	V	—
Supply Voltage - Output Driver	V_{CC_O}	—	1.140	—	2.625	V	—
Power	P_D	V_{CC_O} = 1.2V OUTPUT_SWING = 0011_b	—	85	135	mW	1, 2
		V_{CC_O} = 1.2V OUTPUT_SWING = 1011_b	—	95	148	mW	1, 2
		V_{CC_O} = 1.8V OUTPUT_SWING = 0011_b	—	90	143	mW	1, 2
		V_{CC_O} = 1.8V OUTPUT_SWING = 1011_b	—	104	162	mW	1, 2
		V_{CC_O} = 2.5V OUTPUT_SWING = 0011_b	—	96	152	mW	1, 2
		V_{CC_O} = 2.5V OUTPUT_SWING = 1011_b	—	116	178	mW	1, 2

Table 2-2: DC Electrical Characteristics (Continued)

V_{CC_A},V_{CC_D}, V_{CC_O} = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Power Consumption – Bypass Mode	P_{D_BYPASS}	—	—	58	88	mW	—
Power Consumption – Output Mute	P_{D_MUTE}	—	—	83	127	mW	—
Power Consumption – Output Disable	$P_{D\_DISABLE}$	—	—	70	114	mW	—
Power Consumption – Sleep-Mute	$P_{D\_SLEEP\_MUTE}$	—	—	49	—	mW	—
Power Consumption – Sleep	P_{D_SLEEP}	—	—	11	27	mW	—
Supply Current – Core	I_{DD_A}	V_{CC_A} = 1.8V	—	37	56	mA	1, 3
Supply Current - Digital	I_{DD_D}	V_{CC_D} = 1.8V	—	5	7.5	mA	—
Supply Current - Output Driver	I_{DD_O}	V_{DD_O} = +1.2V to +2.5V OUTPUT_SWING = 0011_b	—	8	12	mA	1, 2
		V_{DD_O} = +1.2V to +2.5V OUTPUT_SWING = 1011_b	—	16	22	mA	1, 2
Serial Input Common Mode Voltage	V_{CMIN}	—	1.4	—	1.6	V	—
Serial Output Common Mode Voltage	V_{CMOUT}	See Section 4.9.2					
Input Voltage - Digital Pins ($\overline{CS}$, SDIN, SCLK)	V_{IH}	—	0.65* VDD_DIG	—	VDD_DIG	V	—
	V_{IL}	—	0	—	0.35* VDD_DIG	V	—
Output Voltage - Digital Pins (INT, SDOUT)	V_{OH}	I_{OH} = -2mA	VDD_DIG – 0.45	—	—	V	—
	V_{OL}	I_{OH} = 2mA	—	—	0.45	V	—

Notes:

1. De-emphasis off.
2. See Table 4-2 for all the output swing settings.
3. With de-emphasis enabled, add a typical 4mA.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

V_{CC_A},V_{CC_D}, V_{CC_O} = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR_{DDO}	—	1	—	2970	Mb/s	—
Input Voltage Swing	ΔV_{SDI}	Differential, 1.485Gb/s	720	800	960	mV_{ppd}	—
		Differential, 125Mb/s, 270Mb/s, and 2.97Gb/s	720	800	880	mV_{ppd}	—
Input Sensitivity	—	16 increments of approximately 50mV_{ppd}	250	—	1000	mV_{ppd}	1
Output Voltage Swing	ΔV_{DDO}	OUTPUT_SWING = 0100_b	345	410	475	mV_{ppd}	2
		OUTPUT_SWING = 1100_b	665	800	935	mV_{ppd}	2
Output Jitter at Various Cable Lengths and Data Rates	J_{pp}	2.97Gb/s Belden 1694A: 0-120m, -20°C to +70°C	—	0.2	0.25	UI	3, 4, 5
		2.97Gb/s Belden 1694A: 120-180m, -20°C to +70°C	—	0.4	0.5	UI	3, 4, 5
		2.97Gb/s Belden 1694A: 180-200m, -20°C to +70°C	—	0.4	—	UI	3, 4, 5
		1.485Gb/s Belden 1694A: 0-180m	—	0.15	0.25	UI	—
		1.485Gb/s Belden 1694A: 180-240m	—	0.3	0.4	UI	—
		1.485Gb/s Belden 1694A: 240-280m	—	0.35	0.45	UI	—
		270Mb/s Belden 1694A: 0-300m	—	0.1	0.2	UI	—
		270Mb/s Belden 1694A: 300-350m		0.2	0.3		—
		270Mb/s Belden 1694A: 350-450m	—	0.3	0.4	UI	—
		270Mb/s Belden 1694A: 450-500m	—	0.3	—	UI	—
		125Mb/s Belden 1694A: 0-200m	—	—	0.1	UI	—
Output Rise/Fall time		2.97Gb/s and 1.485Gb/s 20% - 80%	—	45	90	ps	—
		270Mb/s 20% - 80%	—	50	200	ps	—
Mismatch in rise/fall time		2.97Gb/s and 1.485Gb/s	—	—	30	ps	—
		270Mb/s	—	—	50	ps	—

Table 2-3: AC Electrical Characteristics (Continued)

V_{CC_A},V_{CC_D}, V_{CC_O} = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Duty Cycle Distortion		2.97Gb/s and 1.485Gb/s	—	—	65	ps	—
		270Mb/s	—	—	65	ps	—
Input Resistance		Single ended	—	3.1	—	kΩ	—
Input Capacitance		Single ended	—	1.1	—	pF	—
Output Resistance		Single ended	—	50	—	Ω	—
Input Capacitance - Digital Pins ($\overline{CS}$, SDIN, SCLK)		—	—	0.8	—	pF	—
Output Capacitance - Digital Pins (INT, SDOUT)		—	—	1.0	—	pF	—
Input Return Loss		1.485GHz to 2.97GHz	10	—	—	dB	6
		5MHz to 1.485GHz	15	—	—	dB	6

Note:

1. For input swing < 720mV_{ppd}, the overall cable reach may be reduced.
2. See Table 4-2 for all the output swing settings.
3. For -40°C to -20°C operation at less than 40m of Belden 1694A cable, add 0.1UI to jitter specification.
4. For -40°C to -20°C operation at greater than 40m of Belden 1694A cable, jitter specification does not change.
5. Operation from +70°C to +85°C is not supported.
6. Using Semtech's recommended application circuit and design guides.

3. Input/Output Circuits

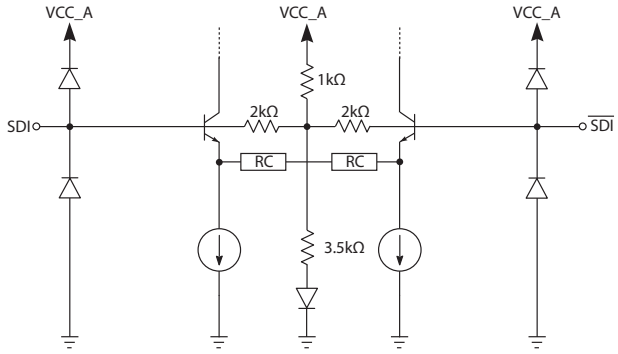


Figure 3-1: Serial Data Input

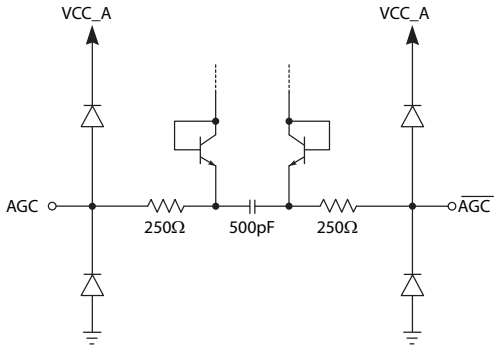


Figure 3-2: AGC, $\overline{\text{AGC}}$

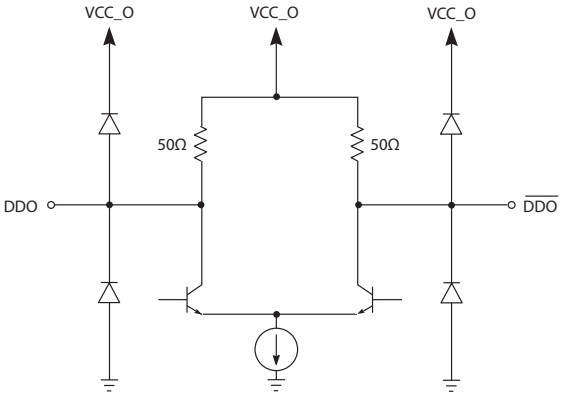


Figure 3-3: Serial Data Output

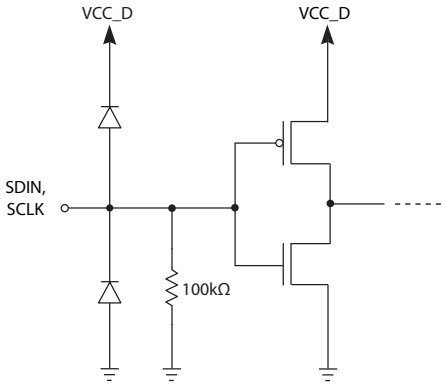


Figure 3-4: SDIN and SCLK

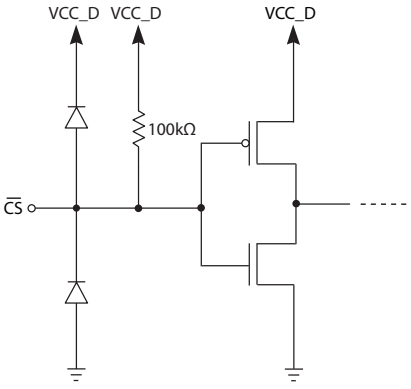


Figure 3-5: $\overline{\text{CS}}$

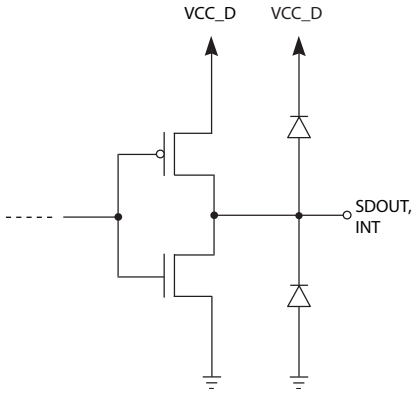


Figure 3-6: SDOUT and INT

4. Detailed Description

The GS3140 is a high-speed BiCMOS IC designed to equalize serial digital signals.

The GS3140 can equalize 3G SDI, HD-SDI, SD-SDI and AES10 serial digital signals, and will typically equalize up to 200m at 2.97Gb/s, 280m at 1.485Gb/s, 500m at 270Mb/s and 200m at 125Mb/s. When DC coupling the output of a device to a 1.2V CML load, the GS3140 typically consumes 84mW of power with a 400mV$_{ppd}$ output swing.

4.1 Serial Digital Inputs (SDI/$\overline{SDI}$)

The GS3140 has a high-impedance input buffer.

The received serial data signal can be connected to the input pins (SDI/$\overline{SDI}$) in either a differential or single-ended configuration.

The input circuit is self-biasing to allow for simple AC-coupling of input signals to the device.

4.1.1 Upstream Launch Swing Compensation

The GS3140 has automatic gain control that is based on the assumption that the cable driver in the upstream device is SMPTE compliant and has a launch swing of 800mV$_{ppd}$ ± 10%.

When the source amplitude is known to be non-SMPTE compliant, a compensation adjustment can be made. The GS3140 can adjust for nominal launch swings between 250mV$_{ppd}$ to 1000mV$_{ppd}$, in approximately 50mV$_{ppd}$ increments. Upstream launch swing compensation can be adjusted using the LAUNCH_SWING_COMPENSATION bits in EQ_CONF_REG_2 register. The default value is 800mV$_{ppd}$ (1011_b).

4.2 Automatic (Adaptive) Cable Equalization

The GS3140 automatically adjusts its gain to equalize and restore signals received over different lengths of coaxial cable having loss characteristics similar to Belden 8281 or 1694A. The device is designed to automatically equalize SMPTE SDI signal rates up to 2.97Gb/s, DVB-ASI signals at 270Mb/s, and MADI signals at 125Mb/s.

The GS3140 has the ability to limit the reach of the device to one of four values through its host interface. The default value is the maximum range. The maximum range of the device is also a function of the detected data rate, so the maximum cable will not exceed the supported reach for that rate.

4.3 Cable Length Indication

The GS3140 reports the input signal strength through the CABLE_LENGTH_INDICATOR bits in the STATUS_REG_0 register, accessible through the device's host interface. The Cable Length Indication (CLI) is a simple, numeric value in the range from 0_h to EF_h. This number can be approximated as a cable length in meters by applying one of the cable scaling factors shown in Table 4-1 below for some commonly used coaxial cables.

Table 4-1: Cable Length Scaling Factors

Cable Type	CLI Scaling Factor
Belden 1694A	2.5
Belden 8281	1.77

The CLI readout value has a multiplication resolution of 1 between 0_h and $7F_h$. In the range from 80_h to EF_h the measurement resolution of CLI is reduced, and CLI value increments by a multiple of 3.

Note: Any additional loss due to other transmission line elements (such as patch panels, barrels, extra connectors, etc.), also translates to an equivalent cable length based on the cable scaling factor.

4.4 Programmable Squelch Threshold

The GS3140 features a programmable squelch threshold, set through the device's host interface. It impacts Loss of Signal (LOS) status. As shown in Figure 4-1, squelch only affects the LOS status when bits AUTO_BYPASS, BYPASS, and SLEEP[1:0] in EQ_CONF_REG_0 are all 0.

The device continually compares the strength of the input signal as set in the CABLE_LENGTH_INDICATOR bits in the STATUS_REG_0 register to the squelch threshold set by the SQUELCH_THRESHOLD bits in the EQ_CONF_REG_1 register.

When the value reported by the CABLE_LENGTH_INDICATOR bits exceeds the value programmed by the SQUELCH_THRESHOLD bits by 3 or more, the Loss of Signal (LOS) status bit in the STATUS_REG_0 register is set to 1.

When the value reported by the CABLE_LENGTH_INDICATOR bits falls below the value programmed by the SQUELCH_THRESHOLD bits by 3 or more, the Loss of Signal (LOS) status bit in the STATUS_REG_0 register is set to 0.

This ±2 hysteresis around the SQUELCH_THRESHOLD setting avoids chattering of the LOS bit status for input signal strengths right around the threshold setting.

By default, the squelch threshold is set to the maximum possible level, and therefore squelch is disabled.

4.5 Loss of Signal (LOS)

The Loss of Signal (LOS) status indicates whether or not a signal that meets the device's programmed thresholds is present at its input. When LOS is de-asserted (set to 0), a supported input signal has been detected. Figure 4-1 shows how LOS is derived.

The LOS function continuously monitors conditions of the input signal. In Sleep, Auto-Sleep, Bypass or Auto-Bypass modes, this is limited to carrier detection.

When LOS Filter is disabled, LOS will be asserted (set to 1) no less than 10µs and no longer than 40µs after the loss of a valid input signal, and will be de-asserted (set to 0) no more than 5µs after the connection of a valid input signal.

LOS is available via a status bit in STATUS_REG_0, and it is also available on the interrupt (INT) status pin, as selected using the INT_SOURCE_SELECT bits in INT_OUT_CONF_REG_0 register accessible through the device's host interface. LOS is the default output from the INT pin.

4.5.1 Programmable LOS Filter

The LOS Filter delays notification of the change in raw LOS until the new state persists contiguously for the programmed length of time. This increases stability of LOS signalling.

The LOS Filter assertion and de-assertion delays can be programmed through the GS3140 host interface. By default, the LOS Filter is set to 51.8µs assertion delay and 6.6ms de-assertion delay.

The LOS assertion delay can be set in the range from 0ms to 6.6ms in increments of 25.9µs. The LOS de-assertion delay can be set in the range of 0s to 1.7s in increments of 6.6ms. These parameters are accessible using the LOS_FILTER_SET_DELAY and LOS_FILTER_CLEAR_DELAY bits in LOS_FILTER_CONF_REG_0

The use of these parameters can be disabled using the LOS_FILTER_DISABLE bit in LOS_FILTER_CONF_REG_1. Figure 4-1 below shows the derivation of the LOS status indication, and how the LOS filter affects the output.

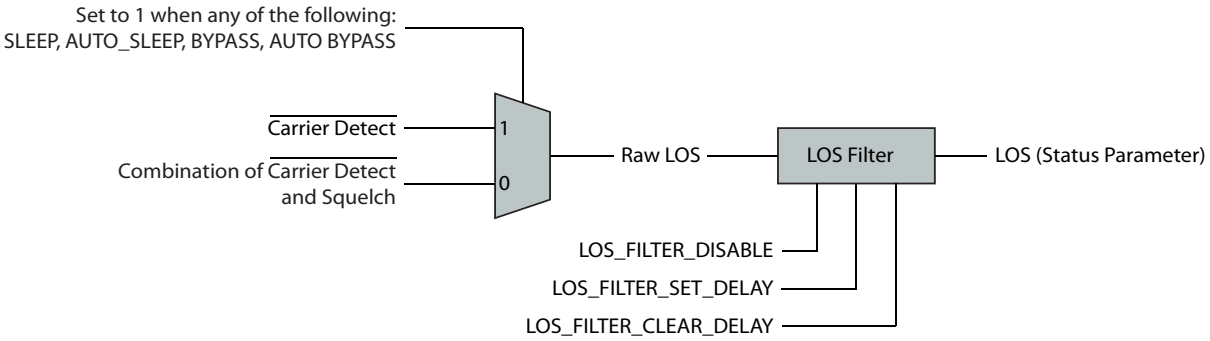


Figure 4-1: Factors Affecting the Assertion of the LOS Status Parameter

4.6 Rate Detection

The GS3140 will differentiate between 2.97Gb/s, 1.485Gb/s, 270Mb/s, 125Mb/s, and <125Mb/s. The detected data rate is reported using the DETECTED_INPUT_RATE bits in STATUS_REG_0 accessible through the device's host interface.

Indication of the detected rate is also available on the interrupt (INT) status pin, as selected using the INT_SOURCE_SELECT and INT_CD_MODE_SELECT bits in INT_OUT_CONF_REG_0 accessible through the device's host interface.

4.7 Interrupt (INT)/ Status Output

The GS3140's programmable interrupt (INT) pin flags internal states, or changes of state to the host system. The default function of this pin is Loss of Signal (LOS). Other functions are programmed via the device's host interface. The additional functions include:

- Rate change detection
- Detection of a specific data rate or set of rates

These functions are chosen using bits INT_SOURCE_SELECT, INT_CD_MODE_SELECT, and DATA_RATE_DETECTION in the INT_OUT_CONF_REG_0 register.

4.8 Power Modes

4.8.1 Bypass

The GS3140 supports a mode of operation where the equalizer core and DC restoration stages are bypassed. This mode is controlled by the settings of the BYPASS and AUTO_BYPASS bits in EQ_CONF_REG_0 of the host interface.

No equalization or DC restoration occurs in BYPASS mode. These functions are disabled in order to reduce power consumption of the device for signals that do not require equalization and DC restoration. When the device is in BYPASS, the LOS continues to function based on carrier detect.

In addition to Manual-BYPASS, Auto-BYPASS is also available. When the AUTO_BYPASS bit in EQ_CONF_REG_0 is set to 1, BYPASS is initiated by detection of an input signal with a data rate below MADI.

4.8.2 Sleep

The GS3140 features a SLEEP function that is controlled through the host interface.

When the part is in SLEEP mode, only carrier based Loss of Signal (LOS) detection remains active. All other sections of the part are powered down.

When in SLEEP mode, the part consumes 13mW of total power.

When Auto-SLEEP is selected, it is initiated by the assertion of LOS. Normal operation, Manual-SLEEP, and Auto-SLEEP are controlled using the SLEEP bits in EQ_CONF_REG_0 accessed through the device's host interface.

4.8.3 Mute

The GS3140 features a MUTE function, in which the two halves of the output buffer are driven statically to opposing levels. One will be set to the level of V_{CC_O} and the other will be set to V_{CC_O} – swing amplitude (swing level set in the OUTPUT_SWING bits of OUT_CONF_REG_0).

When Auto-MUTE is selected, it is initiated by the assertion of LOS. Manual-MUTE and Auto-MUTE are controlled using the MUTE and AUTO_OUTPUT_MUTE bits in OUT_CONF_REG_1 accessed through the device's host interface.

4.8.4 Sleep-Mute

By default, output drivers are powered down when the device is in SLEEP mode. However, the GS3140 also features another power saving sleep mode in which the output driver is muted (as described in Section 4.8.3) instead. All the other blocks are configured similar to the description in Section 4.8.2. The purpose of this mode is to output a noise-immune static signal while the chip is sleeping. Similar to SLEEP mode, both manual and automatic features are available.

When MUTE_OUTPUT_IN_SLEEP bit in EQ_CONF_REG_2 is set to 1, the output drivers will remain powered and enter MUTE whenever the device is in SLEEP.

4.8.5 Output Disable

The GS3140 features a mode of operation in which the output buffer is disabled to save power, but all other parts of the chip remain active.

This mode of operation consumes more power than SLEEP mode, but less power than normal operation. It facilitates faster return to normal operation than SLEEP mode when required, because all internal stages of the EQ core are already active in this mode.

By default, if the device is not set to any other automatic power mode (Auto-SLEEP, Auto-MUTE, Auto-SLEEP-MUTE), then the assertion of LOS will initiate OUTPUT DISABLE mode. The output buffer will remain disabled until a signal is present.

If there is a signal present, the outputs may still be manually disabled by setting the MANUAL_OUTPUT_DISABLE bit in OUT_CONF_REG_1 to 1, accessed through the device's host interface.

4.9 Serial Digital Output (DDO/$\overline{\text{DDO}}$)

The output driver has a separate voltage supply (V_{CC_O}) which operates between 1.2V - 2.5V. The output buffer includes two on-chip 50Ω termination resistors.

The output is compatible with industry standard PECL, LVPECL, LVDS, and CML differential receivers when AC coupled using Semtech's recommended application circuit.

4.9.1 Adjustable Output Swing and De-Emphasis

The serial digital output swing is user-selectable from approximately 250mV$_{ppd}$ to 1V$_{ppd}$ in increments of 50mV$_{ppd}$. For exact values see Table 4-2.

Table 4-2: Serial Digital Output Swing

OUTPUT_SWING	Min	Typ	Max	Units
0000_b	190	230	270	mV
0001_b	230	275	320	mV
0010_b	275	325	375	mV
0011_b	310	370	430	mV
0100_b	345	410	475	mV
0101_b	390	460	530	mV
0110_b	435	510	585	mV
0111_b	480	560	640	mV
1000_b	515	605	695	mV
1001_b	555	655	755	mV
1010_b	590	705	820	mV
1011_b	630	755	880	mV
1100_b	665	800	935	mV
1101_b	695	840	985	mV
1110_b	745	890	1035	mV
1111_b	800	930	1060	mV

To support driving long PCB traces, the GS3140 differential output buffer includes programmable de-emphasis with 8 operating levels between 0dB - 18.1dB. The de-emphasis delay can also be programmed to either 100ps or 200ps.

A second set of de-emphasis level and delay values, specifically targeted for 2.97Gb/s signals, can be selected either manually using the MANUAL_DEEMPHASIS_SELECT bit or automatically using the AUTO_DEEMPHASIS_ENABLE bit in OUT_CONF_REG_0 accessible through the device's host interface.

Table 4-3: De-emphasis Levels

De-emphasis Level	Operating Level	Units
000_b	0	dB
001_b	1.2	dB
010_b	2.5	dB
011_b	4.1	dB
100_b	6.0	dB
101_b	8.5	dB
110_b	12.0	dB
111_b	18.1	dB

4.9.2 Output Common Mode Voltage

The output common mode voltage level (V_{CMOUT}) is a function of the output voltage swing, the output driver supply voltage (V_{CC_O}) and how the transmission line is terminated. If the outputs are terminated through 50Ω resistors to a voltage V_{TERM} equal to V_{CC_O}, as shown in Figure 4-2 below, the output common mode voltage is given by the following expression:

$$V_{CMOUT} = V_{CC\_O} - \frac{\Delta V_{DDO}}{4} \qquad \text{Equation 4-1}$$

If the differential outputs are terminated across a 100Ω resistor, as shown in Figure 4-3 below, the output common mode voltage is given by the following expression:

$$V_{CMOUT} = V_{CC\_O} - \frac{\Delta V_{DDO}}{2} \qquad \text{Equation 4-2}$$

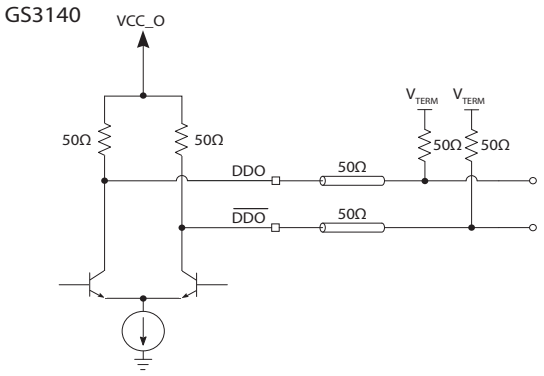


Figure 4-2: 50Ω Termination to V_{TERM}

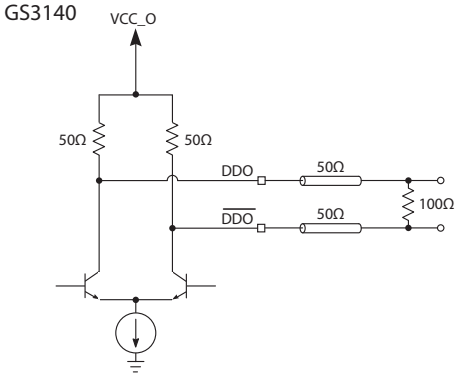


Figure 4-3: 100Ω Parallel Output Termination

4.10 Device Reset

The GS3140 includes a reset function accessible via the device's host interface, which reverts all internal logic and register values to default.

The device can be reset with a single write of AD_h to the RESET_CONTROL bits of RESET_REG_0 register, which will assert and de-assert the device reset within the duration of the GSPI write access Data Word.

The device can be placed and held in reset by writing AA_h to the RESET_CONTROL bits of RESET_REG_0 register. Subsequent writes of DD_h to the RESET_CONTROL bits will de-assert device reset.

The current state of user-initiated device reset can be read from the RESET_CONTROL bits of RESET_REG_0 register.

While in reset, host interface accesses to any other register will not be functional and all logic and configuration registers will be in reset state. While in reset serial digital differential output behaviour is undefined.

The digital logic and registers within the device will exit the reset state 40µs after device reset is de-asserted.

Note: RESET_REG_0 register writes do not support Auto-Increment mode.

4.11 Gennum Serial Peripheral Interface (GSPI)

The Gennum Serial Peripheral Interface (GSPI) is comprised of a serial data input signal (SDIN pin), serial data output signal (SDOUT pin), an active-low chip select ($\overline{CS}$ pin) and a burst clock (SCLK pin).

The GS3140 is a slave device, so the SCLK, SDIN and $\overline{CS}$ signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

4.11.1 $\overline{CS}$ Pin

The Chip Select pin ($\overline{CS}$) is an active-low signal provided by the host processor to the GS3140.

The high-to-low transition of this pin marks the start of serial communication to the GS3140.

The low-to-high transition of this pin marks the end of serial communication to the GS3140.

There is an option for each device to use a separate unique chip select signal from the host processor or for up to 32 devices to be connected to a single chip select when making use of the Unit Address feature.

Only those devices whose Unit Address matches the UNIT ADDRESS in the GSPI Command Word will respond to communication from the host processor (unless the B'CAST ALL bit in the GSPI Command Word is set to 1).

4.11.2 SDIN Pin

The SDIN pin is the GSPI serial data input pin of the GS3140.

16-bit Command and Data Words from the host processor or from the SDOUT pin of other devices are shifted into the device on the rising edge of SCLK when the $\overline{CS}$ pin is low.

4.11.3 SDOUT Pin

The SDOUT pin is the GSPI serial data output of the GS3140.

All data transfers out of the GS3140 to the host processor or to the SDIN pin of other connected devices occur from this pin.

By default at power up or after system reset, the SDOUT pin provides a non-clocked path directly from the SDIN pin, regardless of the $\overline{CS}$ pin state, except during the GSPI Data Word portion for read operations to the device. This allows multiple devices to be connected in Loop-Through configuration.

For read operations, the SDOUT pin is used to output data read from an internal Configuration and Status Register (CSR) when $\overline{CS}$ is LOW. Data is shifted out of the device on the falling edge of SCLK, so that it can be read by the host processor or other downstream connected device on the subsequent SCLK rising edge.

4.11.3.1 GSPI Link Disable Operation

It is possible to disable the direct SDIN to SDOUT (Loop-Through) connection by writing a value of 1 to the GSPI_LINK_DISABLE bit in HOST_CONF_REG_0. When disabled, any data appearing at the SDIN pin will not appear at the SDOUT pin and the SDOUT pin is HIGH.

Note: Disabling the Loop-Through operation is temporarily required when initializing the Unit Address for up to 32 connected devices.

The time required to enable/disable the Loop-Through operation from assertion of the register bit is less than the GSPI configuration command delay as defined by the parameter $t_{cmd\_GSPI\_config}$ (4 SCLK cycles).

Table 4-4: GSPI_LINK_DISABLE Bit Operation

Bit State	Description
0	SDIN pin is looped through to the SDOUT pin
1	Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH.

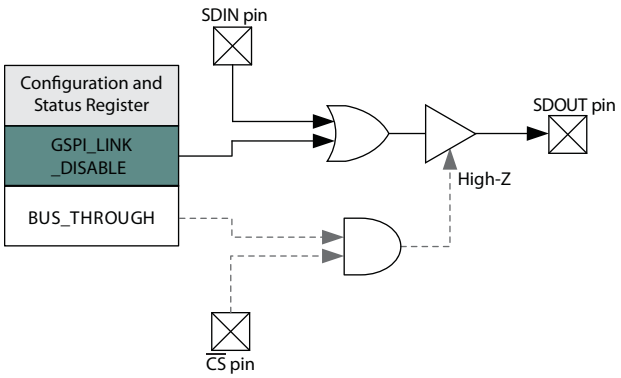


Figure 4-4: GSPI_LINK_DISABLE Operation

4.11.3.2 GSPI Bus-Through Operation

Using GSPI Bus-Through operation, the GS3140 can share a common PCB trace with other GSPI devices for SDOUT output.

When configured for Bus-Through operation, by setting the GSPI_BUS_THROUGH_ENABLE bit to 1, the SDOUT pin will be high-impedance when the $\overline{CS}$ pin is HIGH.

When the $\overline{CS}$ pin is LOW, the SDOUT pin will be driven and will follow regular read and write operation as described in Section 4.11.3.

Multiple chains of GS3140 devices can share a single SDOUT bus connection to host by configuring the devices for Bus-Through operation. In such configuration, each chain requires a separate Chip Select ($\overline{CS}$).

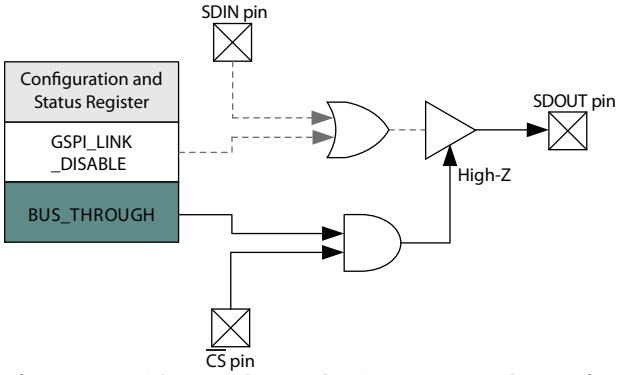


Figure 4-5: GSPI_BUS_THROUGH_ENABLE Operation

Table 4-5: GSPI_BUS_THROUGH_ENABLE Bit Operation

Bit State	Description
0	Disables Bus-Through operation
1	Enables Bus-Through operation When $\overline{CS}$ is HIGH, the SDOUT pin will be high impedance. When $\overline{CS}$ is LOW, the SDOUT pin is driven.

4.11.4 SCLK Pin

The SCLK pin is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GS3140 SDIN pin on the rising edge of SCLK. Serial data is clocked out of the device from the SDOUT pin on the falling edge of SCLK (read operation). SCLK is ignored when $\overline{CS}$ is HIGH.

The maximum interface clock rate is 32MHz.

4.11.5 Command Word Description

All GSPI accesses are a minimum of 32 bits in length (a 16-bit Command Word followed by a 16-bit Data Word) and the start of each access is indicated by the high-to-low transition of the chip select ($\overline{CS}$) pin of the GS3140.

The format of the Command Word and Data Words are shown in Figure 4-6.

Data received immediately following this high-to-low transition will be interpreted as a new Command Word.

4.11.5.1 R/$\overline{W}$ bit - B15 Command Word

This bit indicates a read or write operation.

When R/$\overline{W}$ is set to 1, a read operation is indicated, and data is read from the register specified by the ADDRESS field of the Command Word.

When R/$\overline{W}$ is set to 0, a write operation is indicated, and data specified in the Data Word is written to the register specified by the ADDRESS field of the Command Word.

4.11.5.2 B'CAST ALL - B14 Command Word

This bit is used in write operations to configure all devices connected in Loop-Through and Bus-Through configuration with a single command.

When B'CAST ALL is set to 1, the following Data Word (AUTOINC = 0) or Data Words (AUTOINC = 1) are written to the register specified by the ADDRESS field of the Command Word (and subsequent addresses when AUTOINC = 1), regardless of the setting of the UNIT ADDRESS(es).

When B'CAST ALL is set to 0, a normal write operation is indicated. Only those devices that have a Unit Address matching the UNIT ADDRESS field of the Command Word write the Data Word to the register specified by the ADDRESS field of the Command Word. B'CAST ALL must be set to 0 for read operations.

4.11.5.3 EMEM - B13 Command Word

The EMEM bit should be set to 0 when accessing GS3140. Accesses to other devices (Unit Address field in the Command Word does not match the DEVICE_UNIT_ADDRESS in HOST_CONF_REG_0) with EMEM bit set to 1 are allowed.

4.11.5.4 AUTOINC - B12 Command Word

When AUTOINC is set to 1, Auto-Increment read or write access is enabled.

In Auto Increment Mode, the device automatically increments the register address for each contiguous read or write access, starting from the address defined in the ADDRESS field of the Command Word.

The internal address is incremented for each 16-bit read or write access until a low-to-high transition on the $\overline{CS}$ pin is detected.

When AUTOINC is set to 0, single read or write access is required.

Auto-Increment write must not be used to update values in HOST_CONF_REG_0.

4.11.5.5 UNIT ADDRESS - B11:B7 Command Word

The 5 bits of the UNIT ADDRESS field of the Command Word are used to select one of 32 devices connected on a single chip select in Loop-Through or Bus-Through configurations.

Read and write accesses are only accepted if the UNIT ADDRESS field matches the programmed DEVICE_UNIT_ADDRESS in HOST_CONF_REG_0

By default at power-up or after a device reset, the DEVICE_UNIT_ADDRESS is set to 00_h

4.11.5.6 ADDRESS - B6:B0 Command Word

The 7 bits of the ADDRESS field are used to select one of the register addresses in the device in single read or write access mode, or to set the starting address for read or write accesses in Auto-Increment Mode.

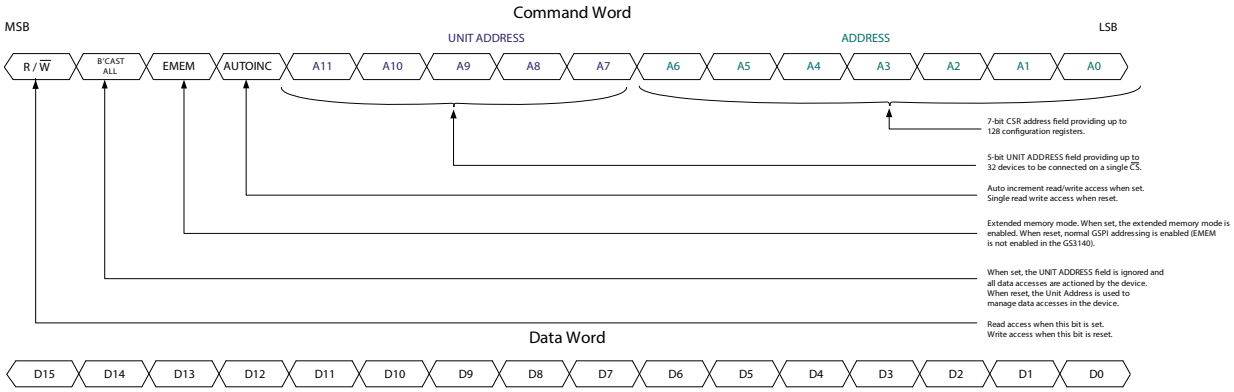


Figure 4-6: Command and Data Word Format

4.11.6 GSPI Transaction Timing

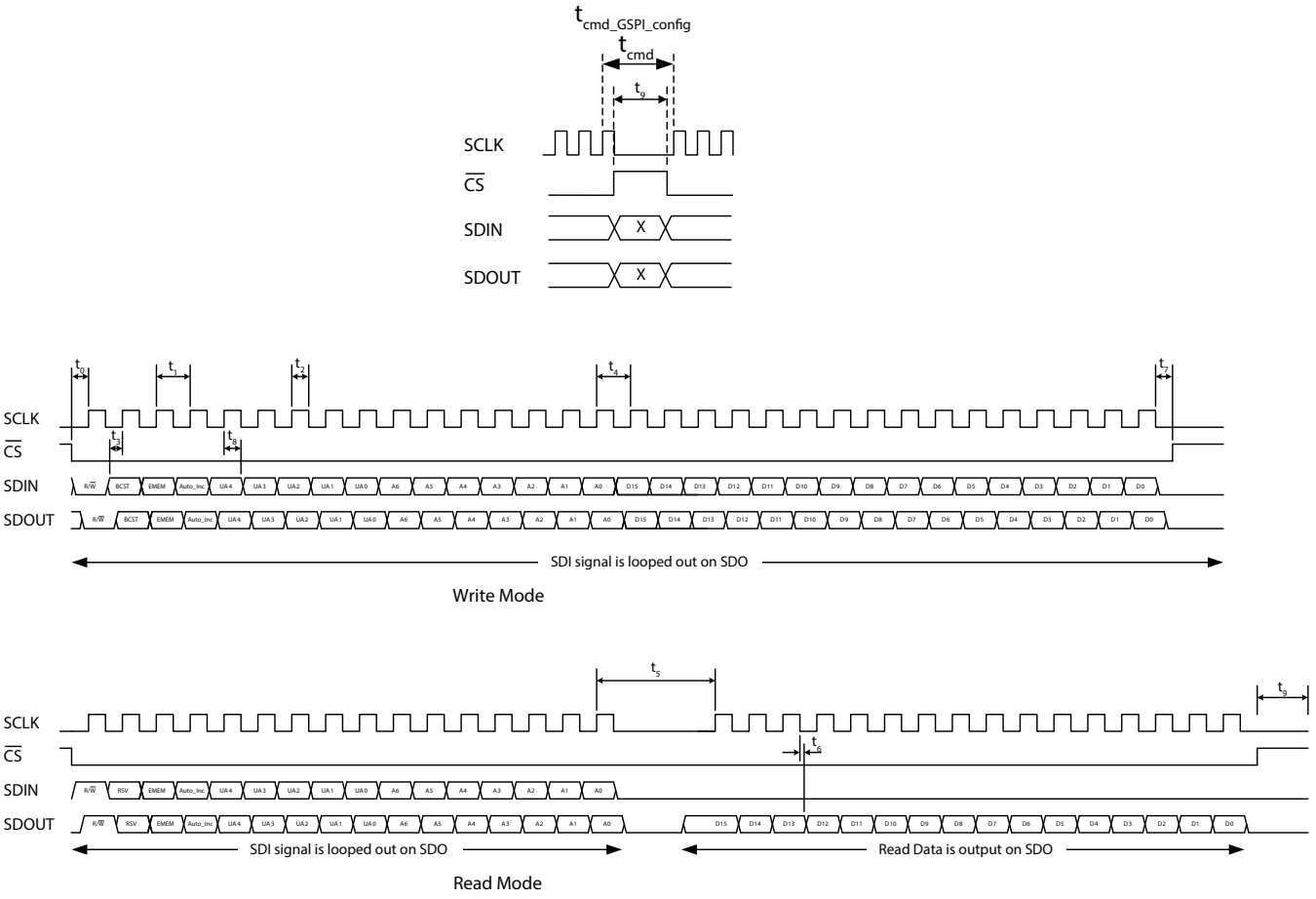


Figure 4-7: GSPI External Interface Timing

Table 4-6: GSPI Timing Parameters

Parameter	Symbol	Equivalent SCLK Cycles	Min	Typ	Max	Units
SCLK frequency			—	—	32	MHz
CS low before SCLK rising edge	t_0		1.3	—	—	ns
SCLK period	t_1		31.25	—	—	ns
SCLK duty cycle	t_2		40	50	60	%
Input data setup time	t_3		1.1	—	—	ns
SCLK idle time -write	t_4	1	31.25[1]	—	—	ns
SCLK idle time - read	t_5	4	114	—	—	ns
Inter-command delay time	t_{cmd}	3	85			
Inter-command delay time (after GSPI configuration write)	$t_{cmd\_GSPI\_conf}$[2]	4	114	—	—	ns

Table 4-6: GSPI Timing Parameters (Continued)

Parameter	Symbol	Equivalent SCLK Cycles	Min	Typ	Max	Units
SDO after SCLK falling edge	t_6		1.9	—	7.5	ns
$\overline{CS}$ high after final SCLK falling edge	t_7		0	—	—	ns
Input data hold time	t_8		1	—	—	ns
$\overline{CS}$ high time	t_9		46.9	—	—	ns
SDIN to SDOUT combinatorial delay			—	—	5	ns
Max. chips daisy chained at max SCLK frequency (32 MHz)	When host clocks in SDOUT data on rising edge of SCLK		—	—	1	GS3140 chips
Max. frequency for 32 daisy-chained devices			—	—	2.1	MHz
Max. chips daisy-chained at max. SCLK frequency (32 Mhz)	When host clocks in SDOUT data on falling edge of SCLK		—	—	3	GS3140 chips
Max. frequency for 32 daisy-chained devices			—	—	2.2	MHz

Notes:

1. Parameter is an exact multiple of SCLK periods and scales proportionally
2. $t_{cmd\_GSPI\_conf}$ inter-command delay must be used whenever modifying HOST_CONF_REG_0 register at address 0x00

4.11.7 Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-8 to Figure 4-12.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 32-bits long, consisting of a Command Word and a single Data Word. The read or write cycle begins with a high-to-low transition of the $\overline{CS}$ pin. The read or write access is terminated by a low-to-high transition of the $\overline{CS}$ pin.

The maximum interface clock rate is 32MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of 3 SCLK clock cycles. After modifying values in HOST_CONF_REG_0, the inter-command delay time, $t_{cmd\_GSPI\_config}$, is a minimum of 4 SCLK clock cycles.

For read access, the time from the last bit of the Command Word to the start of the data output, as defined by t_5, corresponds to no less than 4 SCLK clock cycles at 32MHz.

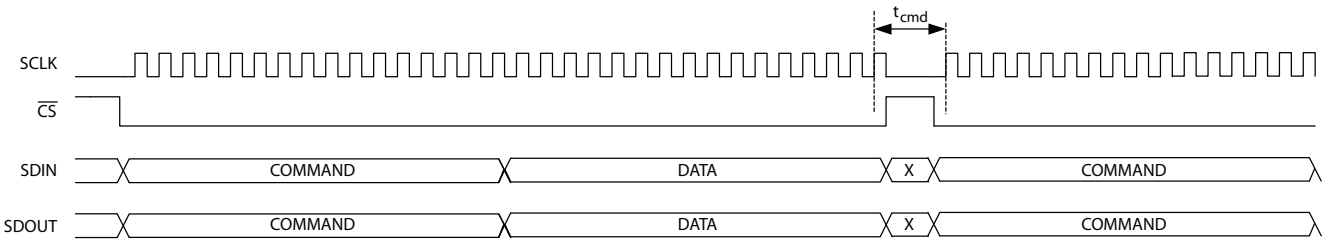


Figure 4-8: GSPI Write Timing – Single Write Access with Loop-Through Operation (default)

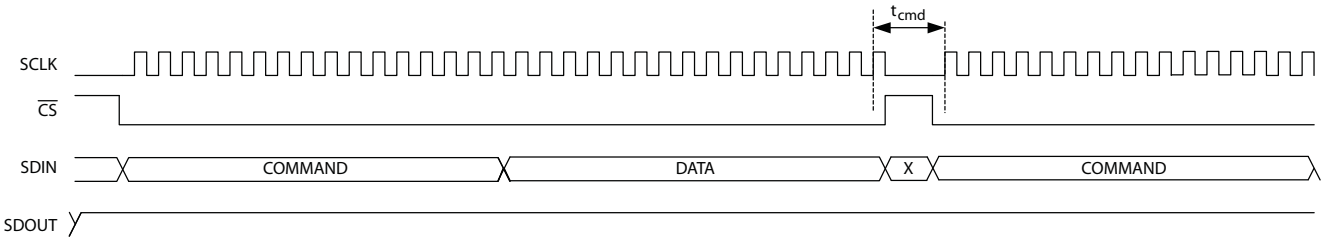


Figure 4-9: GSPI Write Timing – Single Write Access with GSPI Link-Disable Operation

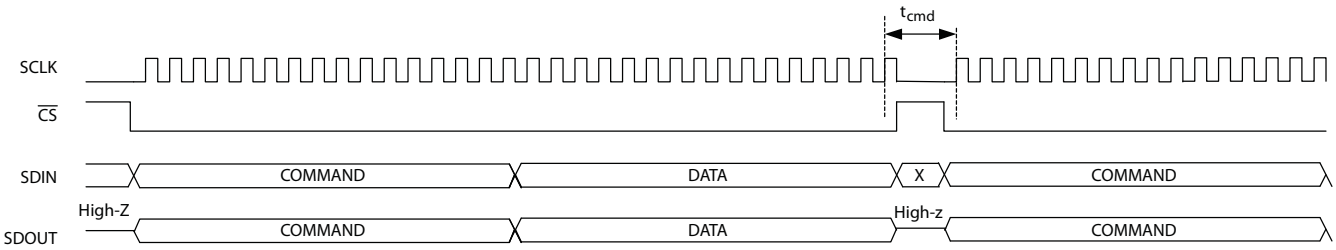


Figure 4-10: GSPI Write Timing – Single Write Access with Bus-Through Operation

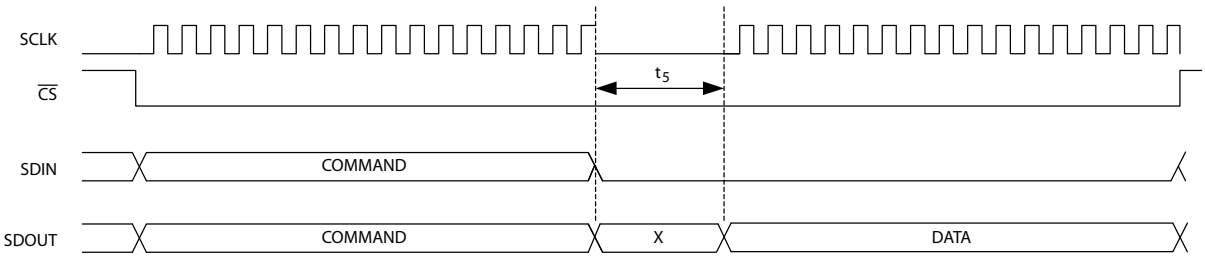


Figure 4-11: GSPI Read Timing – Single Read Access with Loop-Through Operation (default)

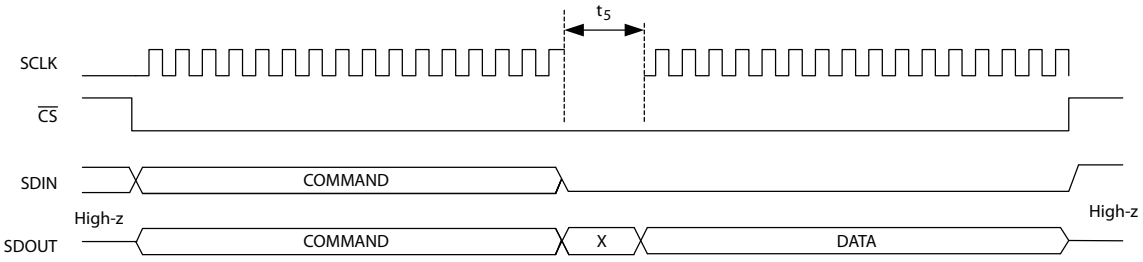


Figure 4-12: GSPI Read Timing – Single Read Access with Bus-Through Operation

4.11.8 Auto-increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in Figure 4-13 to Figure 4-17.

Auto-increment mode is enabled by the setting of the AUTOINC bit of the Command Word.

In this mode, multiple Data Words can be read from/written to the device using only one starting address. Each access is initiated by a high-to-low transition of the $\overline{CS}$ pin, and consists of a Command Word and one or more Data Words. The internal address is automatically incremented after the first read or write Data Word, and continues to increment until the read or write access is terminated by a low-to-high transition of the $\overline{CS}$ pin.

Note: Writing to HOST_CONF_REG_0 using Auto-increment access is not allowed.

The maximum interface clock rate is 32MHz and the inter-command delay time indicated in the diagram as t_{cmd}, is a minimum of 3 SCLK clock cycles.

For read access, the time from the last bit of the first Command Word to the start of the data output of the first Data Word as defined by t_5, will be no less than 4 SCLK cycles at 32MHz. All subsequent read data accesses will not be subject to this delay during an Auto-Increment read.

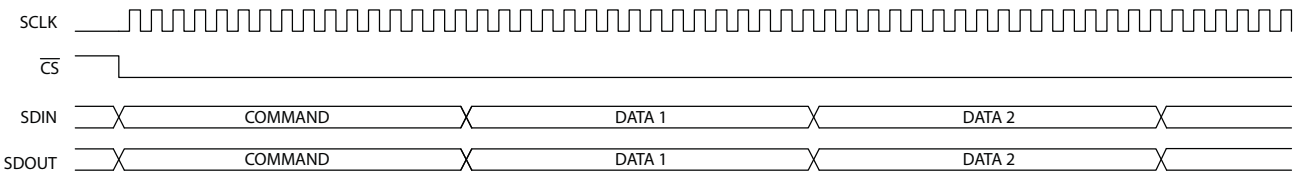


Figure 4-13: GSPI Write Timing – Auto-Increment with Loop-Through Operation (default)

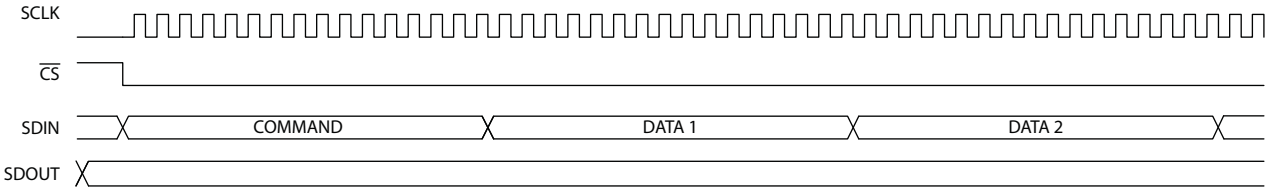


Figure 4-14: GSPI Write Timing – Auto-Increment with GSPI Link Disable Operation

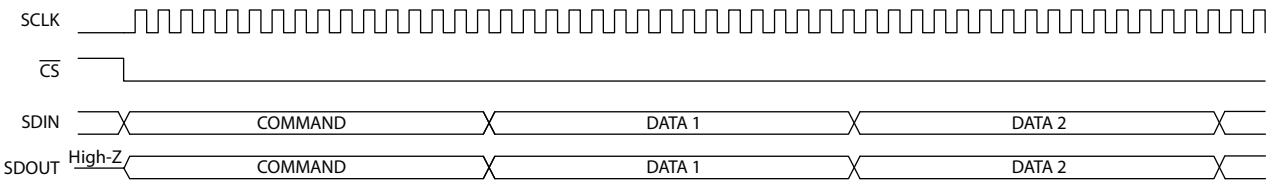


Figure 4-15: GSPI Write Timing – Auto-Increment with Bus-Through Operation

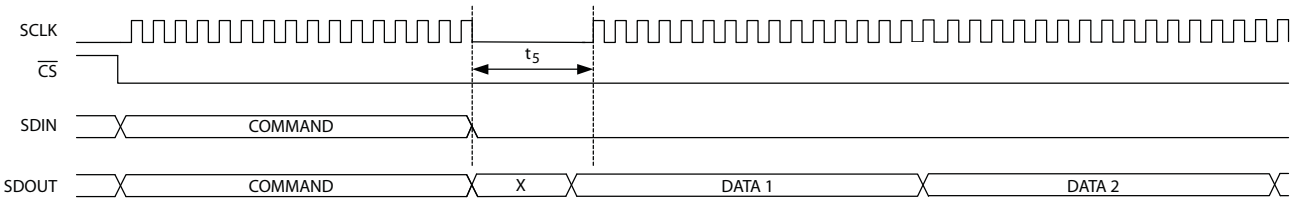


Figure 4-16: GSPI Read Timing – Auto-Increment Read with Loop-Through Operation (default)

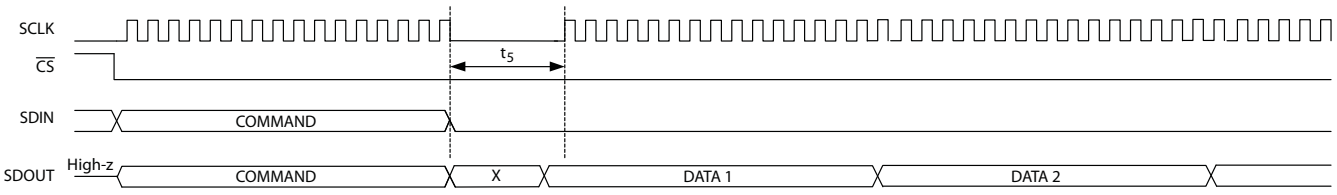


Figure 4-17: GSPI Read Timing – Auto-Increment Read with Bus-through Operation

4.11.9 Default GSPI Operation

By default at power up or after a device reset, the GS3140 is set for Loop-Through Operation and the internal DEVICE_UNIT_ADDRESS field of the device is set to 0.

Figure 4-18 shows a functional block diagram of the Configuration and Status Register (CSR) map in the GS3140.

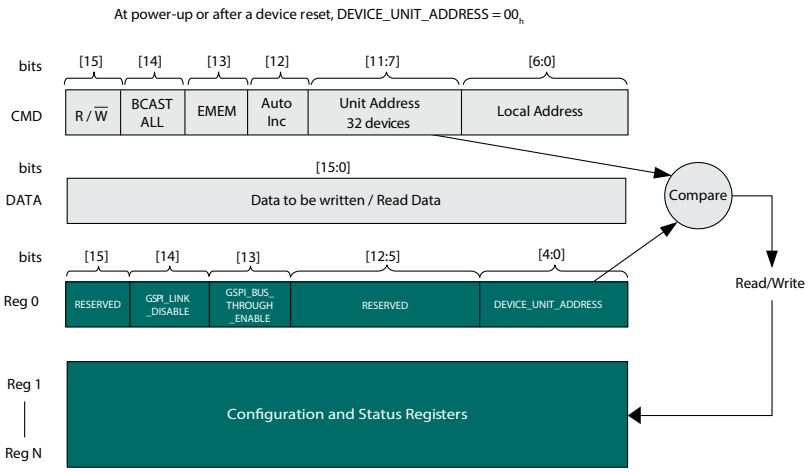


Figure 4-18: Internal Register Map Functional Block Diagram

The steps required for the application host processor to write to the Configuration and Status Registers via the GSPI, are as follows:

1. Set Command Word for write access (R/$\overline{W}$ = 0) and desired Local Address (register address); set Auto Increment; set the Unit Address field in the Command Word to match the configured DEVICE_UNIT_ADDRESS which will be zero. Write the Command Word.
2. Write the Data Word to be written to the first addressed register.
3. Write the Data Word to be written to the next register in Auto Increment mode, etc.

Read access is the same as the above except in step 1 the Command Word is set for read access (R/$\overline{W}$ = 1).

Note: The UNIT ADDRESS field of the Command Word must always match DEVICE_UNIT_ADDRESS for an access to be accepted by the device. Changing DEVICE_UNIT_ADDRESS to a value other than 0 is only required if multiple devices are connected to a single chip select (in Loop-Through or Bus-Through configuration).

4.11.10 Setting a Device Unit Address

Multiple (up to 32) GS3140 devices can be connected to a common Chip Select ($\overline{CS}$) in Loop-Through or Bus-Through operation.

To ensure that each device selected by a common $\overline{CS}$ can be separately addressed, a unique Unit Address must be programmed by the host processor at start-up as part of system initialization or following a device reset.

Note: By default at power up or after a device reset, the DEVICE_UNIT_ADDRESS of each device is set to 0h and the SDIN → SDOUT non-clocked loop-through for each device is enabled.

These are the steps required to set the DEVICE_UNIT_ADDRESS of devices in a chain to values other than 0:

1. Write to Unit Address 0 selecting HOST_CONF_REG_0 (ADDRESS = 0), with the GSPI_LINK_DISABLE bit set to 1 and the DEVICE_UNIT_ADDRESS field set to 0. This disables the direct SDIN → SDOUT non-clocked path for all devices on chip select.
2. Write to Unit Address 0 selecting HOST_CONF_REG_0 (ADDRESS = 0), with the GSPI_LINK_DISABLE bit set to 0 and the DEVICE_UNIT_ADDRESS field set to a unique Unit Address. This configures DEVICE_UNIT_ADDRESS for the first device in the chain. Each subsequent such write to Unit Address 0 will configure the next device in the chain. If there are 32 devices in a chain, the last (32nd) device in the chain must use DEVICE_UNIT_ADDRESS value 0.
3. Repeat step 2 using new, unique values for the DEVICE_UNIT_ADDRESS field in HOST_CONF_REG_0 until all devices in the chain have been configured with their own unique Unit Address value.

Note: $t_{cmd\_GSPI\_conf}$ delay must be observed after every write that modifies HOST_CONFIG_REG_0.

All connected devices receive this command (by default the Unit Address of all devices is 0), and the Loop-Through operation will be re-established for all connected devices.

Once configured, each device will only respond to Command Words with a UNIT ADDRESS field matching the DEVICE_UNIT_ADDRESS in HOST_CONF_REG_0

Note: Although the Loop-Through and Bus-Through configurations are compatible with previous generation GSPI enabled devices (backward compatibility), only devices supporting Unit Addressing can share a chip select. All devices on any single chip select must be connected in a contiguous chain with only the last device's SDOUT connected to the application host processor. Multiple chains configured in Bus-Through mode can have their final SDOUT outputs connected to a single application host processor input.

5. Host Interface Register Map

Table 5-1: Register Descriptions

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset	Description
0_h	HOST_CONF_REG_0	RSVD	15:15	RW	0_h	Reserved. Do not change.
		GSPI_LINK_DISABLE	14:14	RW	0_h	GSPI loop-through disable.
		GSPI_BUS_THROUGH_ENABLE	13:13	RW	0_h	GSPI bus-through enable.
		RSVD	12:5	RW	0_h	Reserved. Do not change.
		DEVICE_UNIT_ADDRESS	4:0	RW	0_h	Device address programmed by application.
1_h	EQ_CONF_REG_0	RSVD	15:9	RW	0_h	Reserved. Do not change.
		MAX_CABLE_LENGTH_CONFIG	8:7	RW	3_h	Manually specify maximum cable length: 00_b = 100m 01_b = 200m 10_b = 300m 11_b = 600m
		AUTO_BYPASS	6:6	RW	0_h	Enable automatic assertion of bypass (equivalent to BYPASS=1) when an input signal is detected with a rate below MADI.
		BYPASS	5:5	RW	0_h	Forces the equalizer core and DC-restore into Bypass mode when set to 1. No equalization occurs in this mode.
		RSVD	4:4	RW	0_h	Reserved. Do not change.
		CUSTOM_DYN_PWR_MODE	3:3	RW	0_h	Enable Dynamic Power Mode. Control bit overrides default when CUSTOM_DYN_PWR_MODE_ ENABLE is set to 1.
		CUSTOM_DYN_PWR_MODE_ ENABLE	2:2	RW	0_h	When set to 1, overrides the Dynamic Power Mode with value specified by parameter CUSTOM_DYN_PWR_MODE. When set to 0 Dynamic Power Mode will default to disabled.
		SLEEP	1:0	RW	0_h	00_b = Normal 01_b = Auto-Sleep 10_b, 11_b = Forced-Sleep

Table 5-1: Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset	Description
2_h	EQ_CONF_REG_1	RSVD	15:12	RW	0_h	Reserved. Do not change.
		SDI_DATA_RATE_VALUE	11:9	RW	0_h	When enabled by FORCE_SDI_DATA_RATE_VALUE. 000_b = Force <MADI rates operation 001_b = Force MADI rates operation 010_b = Force SD rates operation 011_b = Force HD rates operation 100_b = Force 3G rates operation
		FORCE_SDI_DATA_RATE_VALUE	8:8	RW	0_h	Forces the device to operate assuming incoming signal is at rate specified by SDI_DATA_RATE_VALUE.
		SQUELCH_THRESHOLD	7:0	RW	FF_h	Squelch Threshold ED_h - FF_h = No Squelch 0_h - EC_h = See 4.4 Programmable Squelch Threshold
3_h	EQ_CONF_REG_2	RSVD	15:8	RW	0_h	Reserved. Do not change.
		LAUNCH_SWING_ COMPENSATION	7:4	RW	B_h	Selects the upstream launch swing compensation as described in Section 4.1.1. Refer to Table 4-2 for output swing values.
		MUTE_OUTPUT_IN_SLEEP	3:3	RW	0_h	Enables driving outputs in MUTE mode when core is in SLEEP, as explained in Section 4.8.4.
		MADI_AUTO_SWING_DISABLE	2:2	RW	0_h	Disables MADI automatic swing support. if the MADI signal swing is more tightly known, the equalizer jitter and reach performance can be significantly improved by disabling this mode and using the LAUNCH_SWING_COMPENSATION register bits to specify the swing.
		RSVD	1:0	RW	0_h	Reserved. Do not change.

Table 5-1: Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset	Description
4_h	OUT_CONF_REG_0	RSVD	15:15	RW	0_h	Reserved. Do not change.
		OUTPUT_SWING	14:11	RW	B_h	Sets the output swing level (amplitude) when the feature is enabled. See Section 4.9.1.
		OUTPUT_SWING_ENABLE	10:10	RW	0_h	When set to 1, enables overriding of the default output swing with the value written in the OUTPUT_SWING bits. When set to 0, the output swing will default to a setting of OUTPUT_SWING = B_h.
		DEEMPHASIS_DELAY	9:9	RW	0_h	Set the de-emphasis delay when DEEMPHASIS_ENABLE is set to 1. 0_b = 100ps 1_b = 200ps
4_h	OUT_CONF_REG_0	DEEMPHASIS_LEVEL	8:6	RW	0_h	Set the de-emphasis level when DEEMPHASIS_ENABLE is set to 1. See Table 4-3.
		RSVD	5:2	RW	0_h	Reserved. Do not change.
4_h	OUT_CONF_REG_0	DEEMPHASIS_ENABLE	1:1	RW	0_h	Enable or disable the de-emphasis delay and level set using the DEEMPHASIS_DELAY and DEEMPHASIS_LEVEL bits. 0_b = De-emphasis disabled 1_b = De-emphasis enabled
		RSVD	0:0	RW	0_h	Reserved. Do not change.
5_h	OUT_CONF_REG_1	RSVD	15:3	RW	0_h	Reserved. Do not change.
		MANUAL_OUTPUT_DISABLE	2:2	RW	0_h	When set to 1, powers down the output buffer.
		AUTO_OUTPUT_MUTE	1:1	RW	0_h	Enable automatic muting of the output buffer (equivalent to setting MUTE = 1) when LOS is asserted (set to 1).
		MUTE	0:0	RW	0_h	When set to 1, latches the two halves of the output buffer at opposing levels. One will be set to the level of VCC_O and the other will be set to VCC_O – swing amplitude (swing level set in the OUTPUT_SWING bits of OUT_CONF_REG_0).

Table 5-1: Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset	Description
6_h	STATUS_REG_0	CABLE_LENGTH_INDICATOR	15:8	RO	0_h	An 8 bit number representing cable length in increments of 2.5m 00_h = 0m (minimum value) EF_h = ~600m (maximum value) in accordance with Table 4-1.
		RSVD	7:4	RO	—	Reserved.
		DETECTED_INPUT_RATE	3:1	RO	1_h	Detected input data rate. 000_b = <125mB/s 001_b = 125mB/s 010_b = 270Mb/s 011_b = 1.485Gb/s 100_b = 2.97Gb/s **Note:** All other states are invalid.
		LOS	0:0	RO	0_h	Loss of Signal (LOS) Indication. Set to 1 when a qualified signal is present at the input to the device, as detailed in Section 4.5. Set to 0 when such signal is not detected.
7_h	LOS_FILTER_CONF_REG_0	LOS_FILTER_SET_DELAY	15:8	RW	2_h	Loss of Signal (LOS) assertion delay, in increments of approximately 25.9µs to a maximum of approximately 6.6ms. 00_h = 0ms FF_h = 6.6ms
		LOS_FILTER_CLEAR_DELAY	7:0	RW	1_h	Loss of Signal de-assertion delay, in increments of approximately 6.6ms to a maximum of approximately 1.7s. 00_h = 0s FF_h = 1.7s
8_h	LOS_FILTER_CONF_REG_1	RSVD	15:1	RW	0_h	Reserved. Do not change.
		LOS_FILTER_DISABLE	0:0	RW	0_h	Disables Loss of Signal (LOS) Filter as shown in Figure 4-1.

Table 5-1: Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset	Description
		RSVD	15:11	RW	0_h	Reserved. Do not change.
9_h	INT_OUT_CONF_REG_0	DATA_RATE_DETECTION	10:6	RW	0_h	Data Rate Detection Enable. Selects which data rates will be reported on the INT pin when INT_SOURCE_SELECT is set to 100_b or 101_b. Set the corresponding bit to 1 to enable detection reporting for each rate. Bit 0 = < MADI Bit 1 = MADI Bit 2 = SD Bit 3 = HD Bit 4 = 3G
		INT_SOURCE_SELECT	5:3	RW	0_h	Selects the internal signal source for the INT pin. 000_b = Loss of Signal (LOS), filtered per registers LOS_FILTER_CONF_REG_0 and LOS_FILTER_CONF_REG_1 001_b = Specific signal presence status as selected by INT_CD_MODE_SELECT 010_b = Reserved 011_b = An active-high minimum 200ns pulse generated upon each detected change in the rate. 100_b = CD qualified with rate(s) selected by DATA_RATE_DETECTION bits 101 = Same as settings above, with a minimum 200ns low pulse when a rate change is detected 110_b/111_b = Reserved
		INT_CD_MODE_SELECT	2:0	RW	0_h	Carrier Detect Mode, allows INT to assert only for selected rate. 000_b = General Carrier Detect (CD) (any rate) 001_b = CD for below-MADI rates 010_b = CD for MADI rates 011_b = CD for SD 100_b = CD for HD 101_b = CD for 3G 110_b, 111_b = Reserved
A_h	VERSION_ID_REG	VERSION_ID	15:0	RO	0_h	Readout of chip “version_id”.

Table 5-1: Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset	Description
B_h	MISC_CONF_REG_0	HIGH_DRIVE	15:15	RW	0_h	Drive Strength control for digital output pins. 0_b = Low Drive 1_b = High Drive
		RSVD	14:0	RW	0_h	Reserved. Do not change.
C_h – $7E_h$	RESERVED	RSVD	15:0	RO	—	Reserved.
$7F_h$	RESET_REG_0	RESET_CONTROL	15:8	RW	DD_h	Device Reset, Reverts all internal logic and register values to defaults. Write Values: AA_h: asserts device reset DD_h: de-assert device reset AD_h: assert/de-assert device reset in a single write Read Values: AA_h: user-initiated reset is asserted DD_h: user-initiated reset is de-asserted
		RSVD	7:0	RW	0_h	Reserved. Do not change.

6. Application Information

6.1 Typical Application Circuit

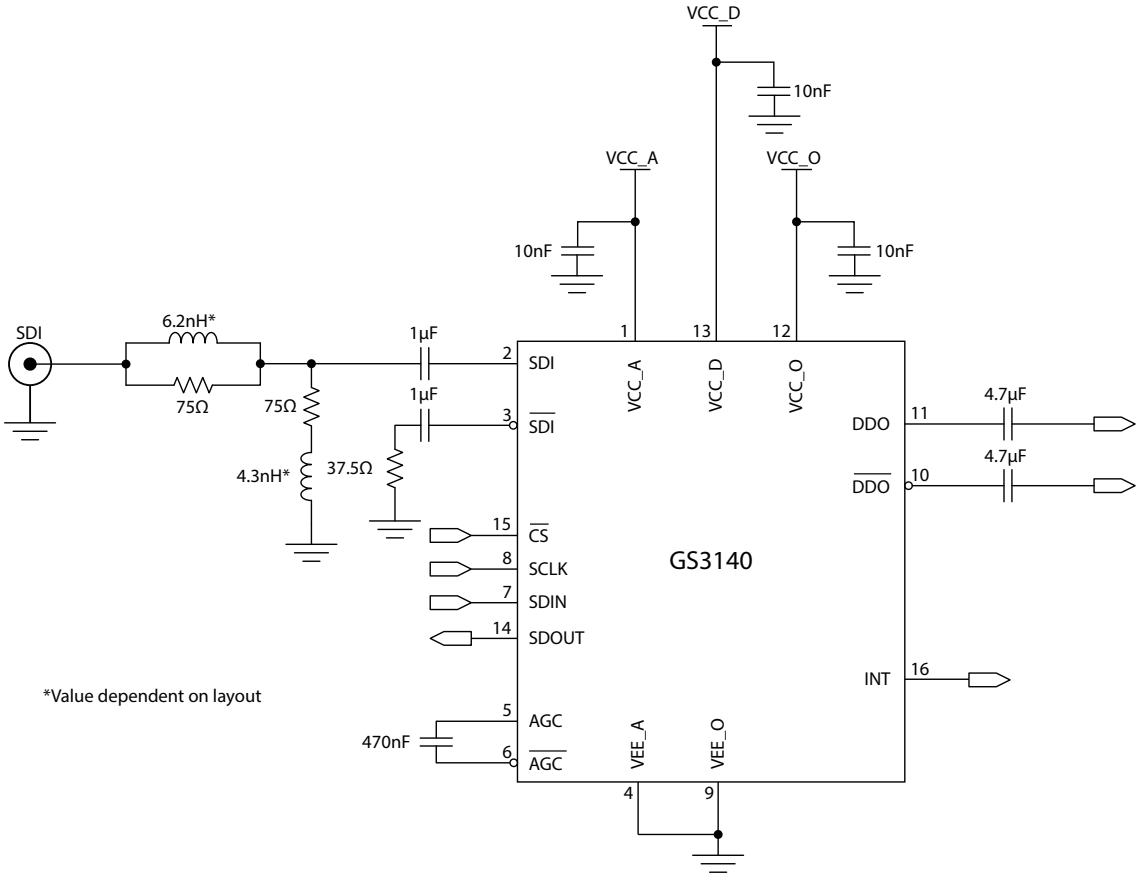
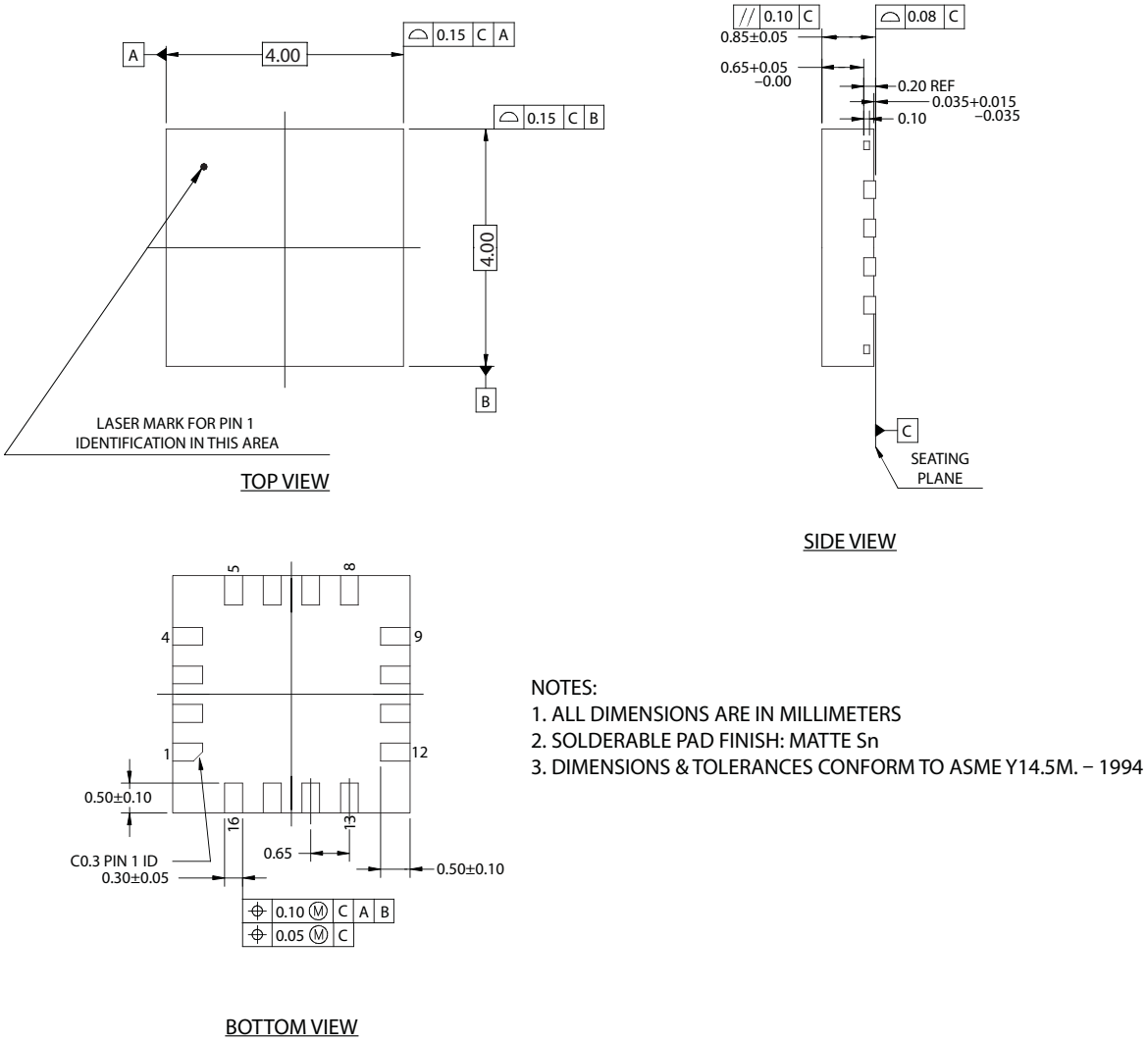


Figure 6-1: Typical Application Circuit

7. Package & Ordering Information

7.1 Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. SOLDERABLE PAD FINISH: MATTE Sn
3. DIMENSIONS & TOLERANCES CONFORM TO ASME Y14.5M. – 1994

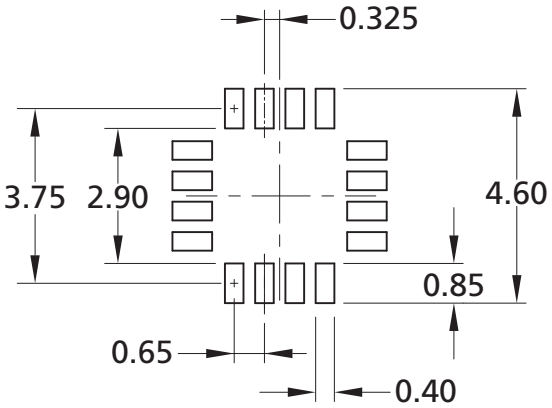
Figure 7-1: Package Dimensions

7.2 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN–COL
Package Drawing Reference	JEDEC MO-220
Moisture Sensitivity Level	3
Junction to Air Thermal Resistance, $\theta_{j\text{-}a}$ (at zero airflow)	63.0°C/W
Junction to Board Thermal Resistance, $\theta_{j\text{-}b}$	37.0°C/W
Junction to Case Thermal Resistance, $\theta_{j\text{-}c}$	44.5°C/W
Psi, Ψ – Junction-to-Top Characterization Parameter	2.5°C/W
Pb-free and RoHS compliant	Yes

7.3 Recommended PCB Footprint



NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS
2. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH "X" AND "Y" DIRECTIONS

Figure 7-2: Recommended PCB Footprint

7.4 Marking Diagram

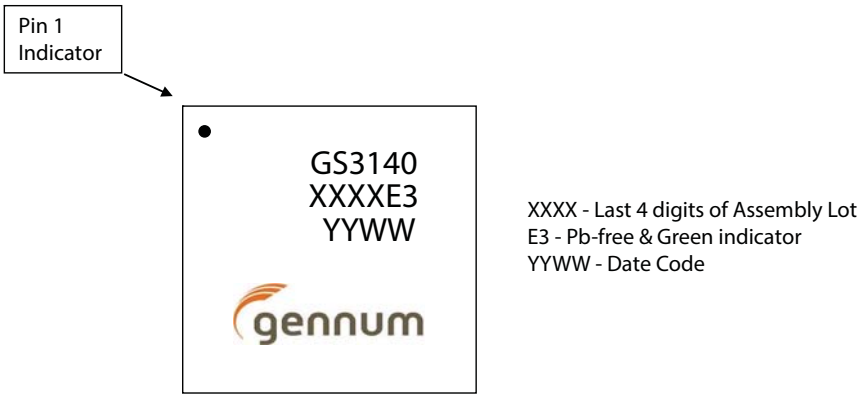


Figure 7-3: Marking Diagram

7.5 Solder Reflow Profiles

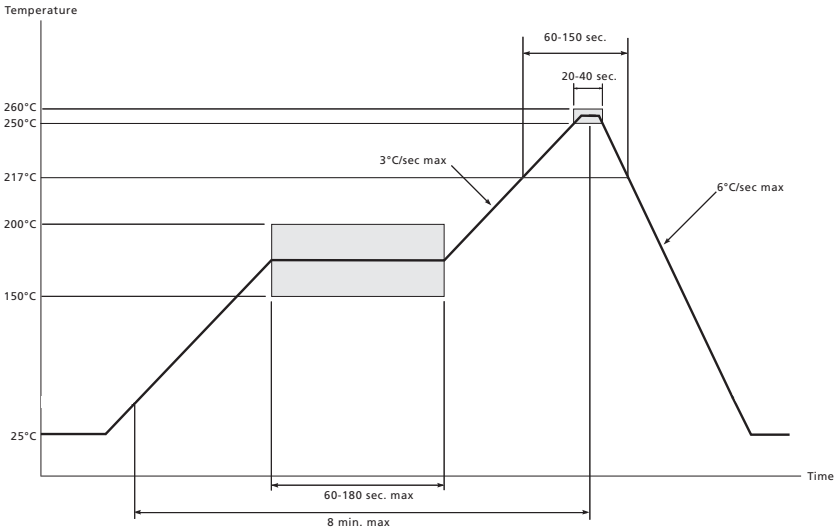


Figure 7-4: Maximum Pb-free Solder Reflow Profile

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Package	Temperature Range
GS3140-INE3	16-pin QFN–COL	-40°C to +85°C

Contact Information

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