GS3490

Configurable Adaptive Cable Equalizer/Cable Driver

Gennum Products

Key Features

- Connection to a single BNC connector as an adaptive cable equalizer or cable driver
- Performance and cable reach optimized for SMPTE ST 424, SMPTE ST 292, and SMPTE ST 259 data rates
- Multi-rate operation from 125Mb/s to 2.97Gb/s in Equalizer Mode and 270Mb/s to 2.97Gb/s in Cable Driver Mode
- Supports DVB-ASI at 270Mb/s
- Integrated 100Ω, differential digital data input/output termination
- Low power operation from a single 3.3V supply:
  - 206mW typical power consumption in EQ mode
  - 190mW typical power consumption in CD mode
- Temperature range: -40°C to +85°C
- 32-pin 5mm x 5mm QFN package

Cable Equalizer Features

- Integrated cable equalizer:
  - 140m - 3G
  - 260m - HD
  - 500m - SD
- Carrier detect with adjustable squelch threshold
- Optional automatic power-down on loss of input signal

Cable Driver Features

- Selectable output slew rate cable driver for compliance with SMPTE ST 424, SMPTE ST 292, and SMPTE ST 259 standards

Applications

- SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259 interfaces requiring switching between cable equalizing or cable driving functionality

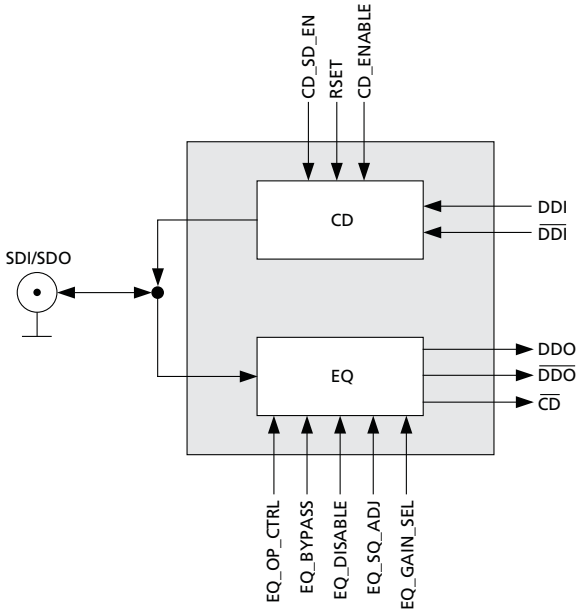
Description

The GS3490 features integrated adaptive cable equalizer and cable driver functionality. The GS3490 can be field-configured as a SMPTE compliant cable equalizer or a SMPTE compliant cable driver.

The GS3490 is optimized for applications with limited I/O space. With its configurable EQ and cable driver functionality, the GS3490 can be utilized as a single-device solution in applications where the interface connector can be configured as either an input or output.

The GS3490's cable equalizer is optimized for operation at 2.97Gb/s, 1.485Gb/s and 270Mb/s while providing typical cable reach of 140m at 2.97Gb/s, 260m at 1.485Gb/s and 500m at 270Mb/s.

In cable driver mode, the dual slew rate capability provides compatibility to SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259 interfaces.



GS3490 Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
1	019093	—	April 2014	Converted to Final Data Sheet. Updated Common Mode Voltage specifications.
0	015642	—	September 2013	Updated to Preliminary Data Sheet. Default state of CD_ENABLE corrected.
B	011682	—	March 2013	Updates throughout the document.
A	158716	—	October 2012	New Document.

Contents

1. Pin Out

1.1 Pin Assignment

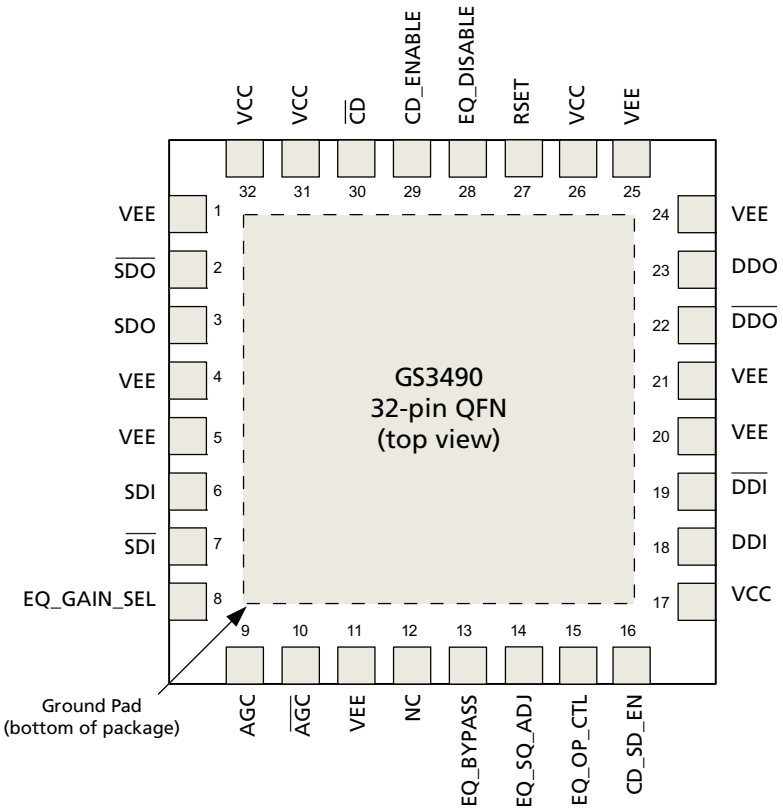


Figure 1-1: Pin Out

1.2 Pin Descriptions

Table 1-1: GS3490 Pin Descriptions

Pin Number	Name	Type	Description
1, 4, 5, 11, 20, 21, 24, 25	VEE	Power	Most negative power supply connection. Connect to GND.
2, 3	$\overline{SDO}$/SDO	Output	Serial data output.
6, 7	SDI/$\overline{SDI}$	Input	Serial data input.

Table 1-1: GS3490 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
8	EQ_GAIN_SEL	Input	Input Sensitivity Control. Please refer to the input logic parameter in Table 2-2: DC Electrical Characteristics for logic level threshold and compatibility. This pin is a 3.3V input. When HIGH, the device compensates for an additional 6dB of loss across the entire operating band. This pin has an internal 100kΩ pull-down resistor.
9, 10	AGC/$\overline{\text{AGC}}$	—	External AGC capacitor connection.
12	NC	—	No Connect. Not bonded internally.
13	EQ_BYPASS	Input	Equalizer Bypass Control. Please refer to the input logic parameter in Table 2-2 for Logic Level threshold and compatibility. For details on operation, refer to Section 4.1.3. This pin has an internal 100kΩ pull-down resistor.
14	EQ_SQ_ADJ	Input	Squelch Threshold Adjust. For details on operation, refer to Section 4.1.5. This pin has an internal 82.4kΩ pull-down resistor.
15	EQ_OP_CTL	Input	Controls the Output Swing, De-emphasis and Mute features of the DDO/$\overline{\text{DDO}}$ outputs. For details on operation, refer to Section 4.1.7. This pin has an internal 1MΩ pull-down resistor.
16	CD_SD_EN	Input	Cable Driver Slew Rate Control. For details on operation, refer to Section 4.2.4. When left unconnected, the default state of this pin is logic HIGH
17, 26, 31, 32	VCC	Power	Most positive power supply connection. Connect to 3.3V DC.
18, 19	DDI/$\overline{\text{DDI}}$	Input	Differential digital data input to cable driver core.
22, 23	$\overline{\text{DDO}}$/DDO	Output	Differential digital data output from cable equalizer core.
27	RSET	—	External cable driver output amplitude control resistor connection.
28	EQ_DISABLE	Input	Equalizer Mode Disable Control. Please refer to the input logic parameter in Table 2-2 for logic level threshold and compatibility. For details on operation, refer to Section 4.1.1. This pin has an internal 100kΩ pull-down resistor.

Table 1-1: GS3490 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
29	CD_ENABLE	Input	Cable Driver Mode Enable Control. Please refer to the input logic parameter in Table 2-2 for logic level threshold and compatibility. For details on operation, refer to Section 4.2.1. When left unconnected, the default state of this pin is logic LOW.
30	$\overline{CD}$	Output	Equalizer Carrier Detect Status Output. Please refer to the output logic parameter in Table 2-2 for logic level threshold and compatibility. For details on operation, refer to Section 4.1.4.
—	Center Pad	Power	Internally bonded to VEE. For more details, refer to Section 6.3.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to 3.6V_{DC}
Input ESD Voltage (HBM)	3kV
Storage Temperature Range	-50°C to 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} + 0.3)V_{DC}
Operating Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

V_{CC} = +3.3V ± 5%, T_A = -20°C to +85°C (unless otherwise shown), Functional Temperature Range: -40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V	–
Power Consumption	P_D	Equalizer Mode DDO Output Swing = 425mV_{ppd}	–	206	248	mW	4
		Equalizer Mode DDO Output Swing = 850mV_{ppd}	–	244	289	mW	4
		Cable Driver Mode	–	190	235	mW	1
		Power-Down Mode EQ_DISABLE = 1, CD_ENABLE = 0	–	39	56	mW	–
Supply Current	I_S	Equalizer Mode DDO Output Swing = 425mV_{ppd}	–	65	77	mA	3
		Equalizer Mode DDO Output Swing = 850mV_{ppd}	–	74	87	mA	3
		Cable Driver Mode	–	58	68	mA	1
		Power-Down Mode EQ_DISABLE = 1, CD_ENABLE = 0	–	12	17	mA	–

Table 2-2: DC Electrical Characteristics (Continued)

V_{CC} = +3.3V ± 5%, T_A = -20°C to +85°C (unless otherwise shown), Functional Temperature Range: -40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
$\overline{CD}$ Output Voltage	$V_{\overline{CD}(OH)}$	Carrier not present	2.0	–	–	V	–
	$V_{\overline{CD}(OL)}$	Carrier present	–	–	0.4	V	–
Input Voltage - Digital Pins	V_{EQ_BYPASS}, $V_{EQ\_DISABLE}$, $V_{EQ\_GAIN\_SEL}$, $V_{CD\_SD\_EN}$, V_{CD_ENABLE}	Minimum to assert and maximum to de-assert	1.7	–	0.4	V	–
SDI/$\overline{SDI}$ Common Mode Voltage	V_{CMIN}	Common Mode	1.62	1.71	1.80	V	–
DDO/$\overline{DDO}$ Common Mode Voltage	V_{CMDDO}	Common Mode	See Section 4.1.6			V	–
DDI/$\overline{DDI}$ Common Mode Voltage	V_{CMDDI}	Common Mode AC-coupled	$1.4 + \Delta V_{DDI} / 4$	–	$V_{CC} - \Delta V_{DDI} / 4$	V	–
SDO/$\overline{SDO}$ Common Mode Voltage	V_{CMOUT}	Common Mode AC-coupled	–	$V_{TERM} - \Delta V_{SDO}$	–	V	2

Notes:

1. Power consumed by GS3490 only. Termination resistors draw extra current.
2. Refer to 4.2.3 Serial Data Outputs (SDO/SDO).
3. De-emphasis off. With De-emphasis enabled, add 3mA at typical conditions.
4. De-emphasis off. With De-emphasis enabled, add 10mW at typical conditions.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics - Equalizer Mode

V_{CC} = +3.3V ± 5%, T_A = -20°C to +85°C (unless otherwise shown), Functional Temperature Range: -40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Data Rate	DR_{SDI}	–	125	–	2970	Mb/s	1
SDI/$\overline{SDI}$ Input Voltage Swing	ΔV_{SDI}	270Mb/s and 1.485Gb/s	720	800	950	mV_{ppd}	2
		2.97Gb/s	720	800	880	mV_{ppd}	2
DDO/$\overline{DDO}$ Output Voltage Swing	ΔV_{DDO}	100Ω load, EQ_OP_CTL set for high swing	700	850	1000	mV_{ppd}	–
		100Ω load, EQ_OP_CTL set for low swing	350	425	500	mV_{ppd}	–
DDO/$\overline{DDO}$ Output Jitter	–	2.97Gb/s Belden 1694A: 0-140m	–	0.2	0.45	UI	3, 4
		1.485Gb/s Belden 1694A: 0-200m	–	–	0.2	UI	3, 4
		1.485Gb/s Belden 1694A: 200-260m	–	0.3	0.4	UI	3, 4
		270Mb/s Belden 1694A: 0-300m	–	0.1	0.2	UI	3, 4
		270Mb/s Belden 1694A: 300-500m	–	0.2	0.3	UI	3, 4
DDO/$\overline{DDO}$ Rise/Fall Time	t_r, t_f	1.485Gb/s and 2.97Gb/s, 20% - 80%	–	75	–	ps	–
		270Mb/s, 20% - 80%	–	150	–	ps	–
Mismatch in Rise/Fall Time	Δt_r, Δt_f	–	–	–	30	ps	–
Duty cycle distortion	–	SD/HD/3G	–	–	30	ps	–
Overshoot	–	–	–	–	10	%	–
Input Return Loss	–	5MHz - 1.485GHz	15	–	–	dB	5
		1.485GHz - 2.97GHz	10	–	–	dB	5
SDI/$\overline{SDI}$ Input Resistance	–	Single-ended	–	1.9	–	kΩ	–
SDI/$\overline{SDI}$ Input Capacitance	–	Single-ended	–	1.3	–	pF	–
DDO/$\overline{DDO}$ Output Resistance	–	Single-ended	–	50	–	W	–
Equalizer Mode Enable Delay	–	–	–	1	–	µs	–

Notes:

1. Device performance is optimized for standard data rates (SD = 270Mb/s, HD = 1.485Gb/s, 3G = 2.970Gb/s).
2. 0m cable length.
3. All parts are production tested. In order to guarantee jitter over the full range of specification (V_{CC} = 3.3V ±5%, T_A = -40°C to +85°C, and 720-880mV launch swing from a SMPTE compliant cable driver) the recommended applications circuit must be used.
4. Based on validation data using the recommended circuit, at V_{CC} = 3.3V, T_A = 25°C and 800mV launch swing from a SMPTE compliant cable driver.
5. IRL depends on board design. The GS3490 achieves this specification on Semtech's evaluation boards.

Table 2-4: AC Electrical Characteristics - Cable Driver Mode

V_{CC} = +3.3V ± 5%, T_A= -20°C to +85°C (unless otherwise shown), Functional Temperature Range: -40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Data Rate	DR_{DDI}	–	270	–	2970	Mb/s	–
Additive Jitter	–	2.97Gb/s	–	15	25	ps_{pp}	–
		1.485Gb/s	–	15	25	ps_{pp}	–
		270Mb/s	–	55	85	ps_{pp}	–
SDO Rise/Fall Time	t_r, t_f	CD_SD_EN = 0, 20% - 80%	–	–	135	ps	–
	t_r, t_f	CD_SD_EN = 1, 20% - 80%	400	–	950	ps	–
Mismatch in Rise/Fall Time	Δt_r, Δt_f	CD_SD_EN = 0 only	–	–	35	ps	–
Duty Cycle Distortion	–	CD_SD_EN = 0, 2.97Gb/s	–	–	14	ps	1, 2
		CD_SD_EN= 0, 1.485Gb/s	–	–	20	ps	1, 2
		CD_SD_EN = 1	–	–	50	ps	1, 2
Overshoot	–	CD_SD_EN = 0	–	–	10	%	1
Output Return Loss	ORL	5MHz - 1.485GHz	15	–	–	dB	3
		1.485GHz - 2.97GHz	10	–	–	dB	3
SDO Output Voltage Swing	ΔV_{SDO}	R_{SET} = 750Ω	750	800	880	mV_{pp}	1
DDI/$\overline{DDI}$ Input Voltage Swing	ΔV_{DDI}	Guaranteed functional	100	–	250	mV_{ppd}	–
		Guaranteed to meet all published specifications	250	–	2200	mV_{ppd}	–
Cable Driver Mode Enable Delay	–	–	–	0.25	–	µs	–

Notes:

1. Single-ended into 75Ω external load.
2. Calculated as the actual positive bit-width compared to the expected positive bit-width using a 1010 pattern.
3. ORL depends on board design. The GS3490 achieves this specification on Semtech's evaluation boards.

3. Input/Output Circuits

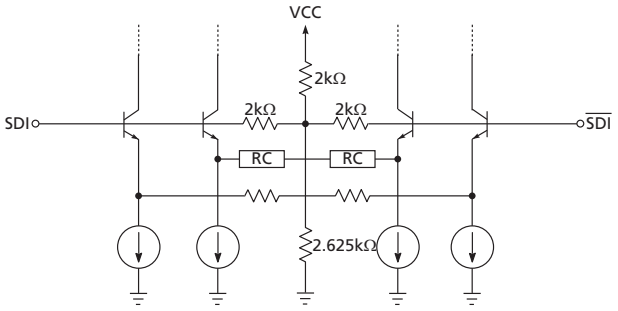


Figure 3-1: Equalizer Serial Digital Input Circuit

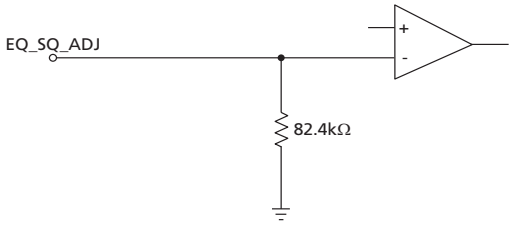


Figure 3-2: EQ_SQ_ADJ Circuit

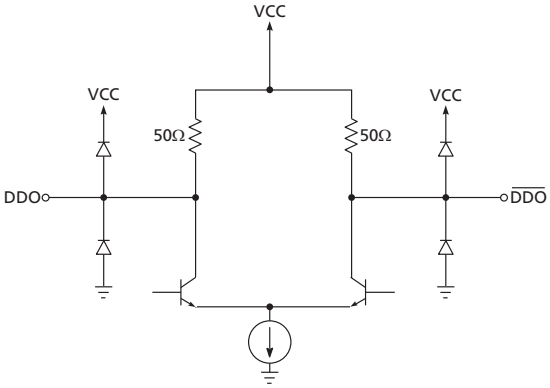


Figure 3-3: Equalizer Differential Digital Data Output Circuit

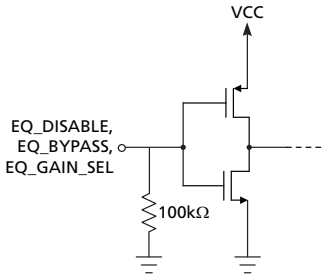


Figure 3-4: EQ_DISABLE, EQ_BYPASS, EQ_GAIN_SEL Circuits

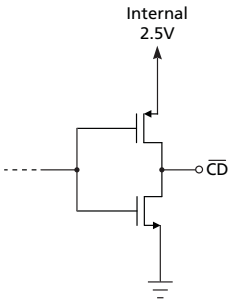


Figure 3-5: $\overline{CD}$ Circuit

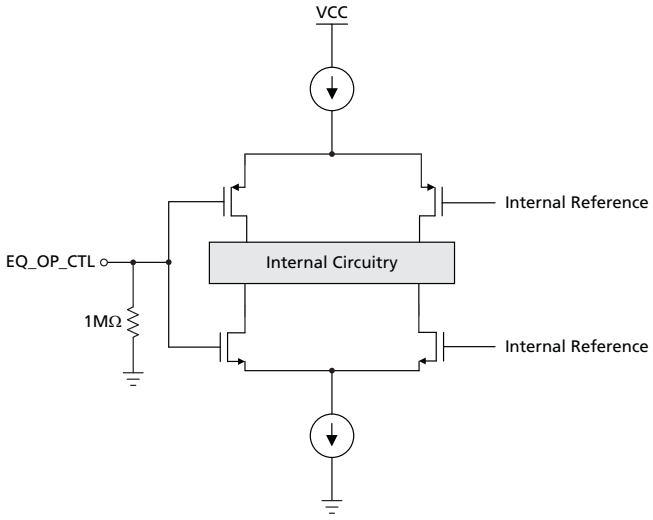


Figure 3-6: EQ_OP_CTL Circuit

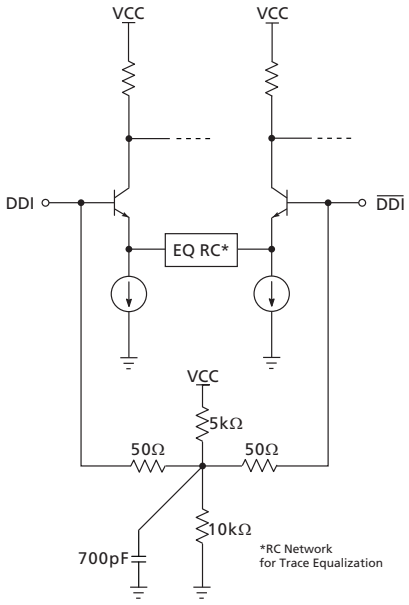


Figure 3-7: Cable Driver Differential Digital Data Input Circuit

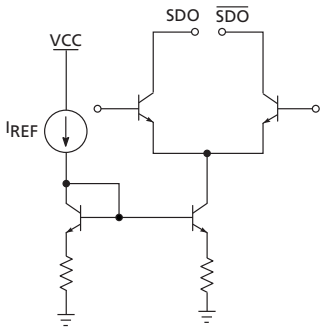


Figure 3-8: Cable Driver Serial Digital Output Circuit

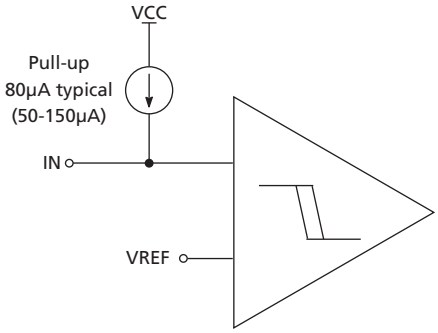


Figure 3-9: CD_SD_EN Circuit

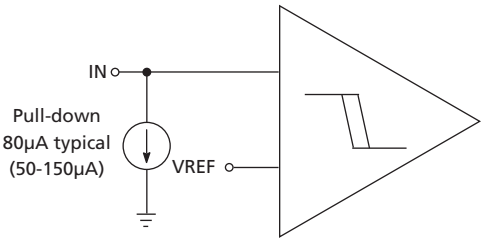


Figure 3-10: CD_ENABLE Circuit

4. Detailed Description

The GS3490 is a half-duplex, bi-directional device that integrates the functions of both a cable equalizer and a cable driver in one package, allowing for a single application circuit to perform both functions through a single BNC connector. The GS3490 pin out enables switching from one mode to another using a single logic control signal.

Table 4-1: GS3490 Operating Modes

EQ_DISABLE	CD_ENABLE	Description
0	0	Equalizer Mode
0	1	Debug Mode*
1	0	Power-Down Mode
1	1	Cable Driver Mode

***Note:** Data represented at the Cable Driver's digital data input is passed through the device, looped back through the Equalizer and appears on the Equalizer's digital data output. The data is looped through the device, provided the SDI/O BNC is terminated with a 75Ω load that is not driving a signal.

4.1 Equalizer Mode

4.1.1 Equalizer Mode Enable

To enable Equalizer Mode, both the EQ_DISABLE and CD_ENABLE pins must be set to logic LOW. These two pins may be tied together and controlled from a single logic signal.

4.1.2 Serial Digital Inputs (SDI/$\overline{\text{SDI}}$)

Please refer to Section 5.1 for the correct way to implement the bi-directional serial input/output. Other application circuits are not supported.

4.1.3 Automatic (Adaptive) Cable Equalization

The GS3490 automatically adjusts its gain to equalize and restore signals received over different lengths of coaxial cable having loss characteristics similar to Belden 8281 or 1694A. The device is designed to automatically equalize SMPTE SDI signal rates from 125Mb/s up to 2.97Gb/s and DVB-ASI signals at 270Mb/s.

The equalized signal is DC-restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC-coupling.

Adaptive Cable Equalization and DC Restoration can be disabled by pulling the EQ_BYPASS pin HIGH.

4.1.4 Carrier Detect ($\overline{CD}$)

The Carrier Detect output pin ($\overline{CD}$) indicates the presence of a signal at the input of the GS3490. When $\overline{CD}$ is LOW, the device has detected an input on its SDI/$\overline{SDI}$ pins. When $\overline{CD}$ is HIGH, the device has not detected an input signal.

When EQ_DISABLE is HIGH, the $\overline{CD}$ output will still function to facilitate the detection of a serial input data signal. As a result, when in Equalizer Mode, auto power-down can be implemented by directly tying $\overline{CD}$ to EQ_DISABLE. When connected, the GS3490 will automatically go into lower power mode when there is a loss of Serial Digital Input signal.

Note 1: $\overline{CD}$ will only operate correctly for data rates greater than 19Mb/s.

Note 2: If EQ_SQ_ADJ is being used to limit the maximum gain of the device, and the maximum cable length is exceeded when EQ_BYPASS pin is set LOW, the $\overline{CD}$ pin will be set HIGH even if a carrier is present.

Note 3: If the $\overline{CD}$ pin is connected to the EQ_DISABLE pin, EQ_SQ_ADJ must be either left open, or connected to ground.

4.1.5 Squelch Adjust (EQ_SQ_ADJ)

The GS3490 features a Squelch Adjust (EQ_SQ_ADJ) threshold.

This feature can be useful in applications where there are multiple input channels using the GS3490, since the maximum gain can be limited to avoid crosstalk.

The EQ_SQ_ADJ pin acts to change the threshold of the Carrier Detect ($\overline{CD}$) pin, through voltage level variances. When the input signal drops below a certain threshold, the $\overline{CD}$ pin will be driven HIGH, indicating that there is not a valid input signal. In applications where squelch adjust is not required, the EQ_SQ_ADJ pin can be left unconnected.

This feature has been designed for use in applications, where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem, since the signal-to-noise ratio on the circuit board could be significantly less than the default signal detection level set by the on-chip reference.

Note: When using EQ_SQ_ADJ to limit the maximum gain of the GS3490, auto power-down is not supported and so $\overline{CD}$ should not be connected to EQ_DISABLE.

4.1.6 Differential Digital Data Outputs (DDO/$\overline{DDO}$)

The digital data output signals have a nominal output voltage swing of either 850mV$_{ppd}$ or 425mV$_{ppd}$, as set by the EQ_OP_CTL pin.

When EQ_DISABLE is HIGH, the differential digital outputs are high impedance and will be pulled HIGH by the on-chip termination.

Table 4-2 shows the typical output common mode voltage levels (V_{CMDDO}) related to the two output swing options and the type of output transmission termination as shown in Figure 4-1 and Figure 4-2.

Table 4-2: Typical Common Mode Output Voltage Levels (V_{CMDDO}) - VCC = 3.3V

Output Voltage Swing (ΔV_{DDO})	Termination Type 1 (See Figure 4-1)	Termination Type 2 (See Figure 4-2)
$425mV_{ppd}$	3.09V	3.19V
$850mV_{ppd}$	2.88V	3.09V

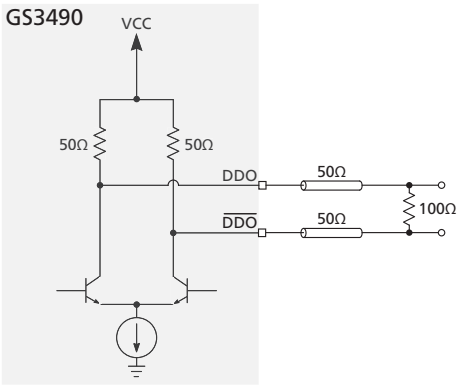


Figure 4-1: 100Ω Parallel Output Termination

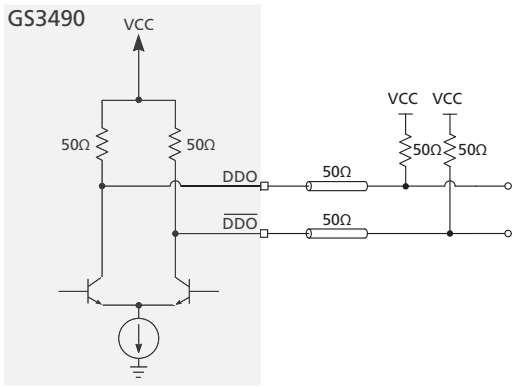


Figure 4-2: 50Ω Termination to VCC

4.1.7 Adjustable Output Swing, De-Emphasis and Mute (EQ_OP_CTL)

The EQ_OP_CTL input pin determines the output swing and De-emphasis settings for DDO/$\overline{DDO}$.

The EQ_OP_CTL pin is an analog input allowing different combinations of output swing, De-emphasis and mute. The possible values are listed in Table 4-3 below:

Table 4-3: EQ_OP_CTL Functions and Levels

Level	Swing (mV_{ppd})	De-emphasis	Mute	Voltage (V)
0	850	Off	N	0.000 - 0.083
1	850	2dB	N	0.234 - 0.394
2	850	4dB	N	0.545 - 0.704
3	850	6dB	N	0.856 - 1.015
4	425	Off	N	1.166 - 1.333
5	425	2dB	N	1.484 - 1.644
6	425	4dB	N	1.795 - 1.954
7	425	6dB	N	2.106 - 2.265
8	425	N/A	Y	2.416 - 2.500

When muted, the output swing is set to 425mV$_{ppd}$ and the DDO/$\overline{DDO}$ outputs are latched.

Automatic muting of the output can be enabled by connecting the $\overline{CD}$ pin to the EQ_OP_CTL pin.

If the connection is made directly, as shown in Figure 4-3, the output would be in its default mode (850mV$_{ppd}$ swing with no De-emphasis) when there is a signal present.

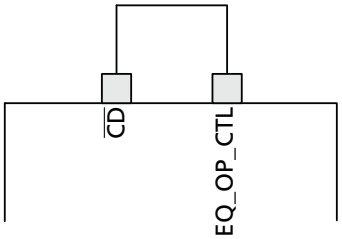


Figure 4-3: Direct Loopback

4.2 Cable Driver Mode

4.2.1 Cable Driver Mode Enable

To enable Cable Driver Mode, EQ_DISABLE and CD_ENABLE must be set to logic HIGH. These two pins may be tied together and controlled from a single logic signal.

4.2.2 Differential Digital Data Inputs (DDI/$\overline{DDI}$)

The GS3490 features a differential input buffer (DDI/$\overline{DDI}$) with on-chip 100Ω differential termination.

The differential data input signal is connected to the DDI and $\overline{DDI}$ input pins of the device.

The serial data input buffer is capable of operation with any binary coded signal that meets the input signal level requirements, in the range of 270Mb/s to 2.97Gb/s in Cable Driver Mode. The input circuit is self-biasing to allow for simple AC or DC-coupling of input signals to the device.

4.2.3 Serial Data Outputs (SDO/$\overline{SDO}$)

The GS3490 features a current-mode differential output driver capable of achieving output swings up to 1040mV$_{pp}$ using a 3.3V termination supply (V_{TERM}).

The output signal amplitude or swing is set using an external R_{SET} resistor. For the most commonly used output swing configurations, please refer to Section 4.2.5.

The SDO/$\overline{SDO}$ pins of the device provide the serial data outputs.

Please refer to Section 5.1 for the correct way to implement the bi-directional serial input/output. Other application circuits are not supported.

4.2.4 Slew Rate Selection (CD_SD_EN)

The GS3490 supports two output slew rates on SDO/$\overline{\text{SDO}}$.

Control of the slew rate is determined by the setting of the CD_SD_EN input pin.

Table 4-4: Slew Rate Selection

CD_SD_EN	Rise/Fall Time
0	SMPTE ST 424 & SMPTE ST 292 compliant
1	SMPTE ST 259 compliant
Floating	SMPTE ST 259 compliant

4.2.5 Output Amplitude (R_{SET})

The output amplitude of the GS3490 can be adjusted by changing the value of the R_{SET} resistor as shown in Table 4-5. For an 800mV_{pp} output with a nominal ±7% tolerance, a value of 750Ω is required. A ±1% SMT resistor should be used.

The R_{SET} resistor is part of an internal DC feedback loop in the GS3490. The resistor should be placed as close as possible to the RSET pin, and connected directly to the VCC plane with more than one via to minimize inductance (traces/wires may cause instability).

Note: Care should be taken when considering layout of the R_{SET} resistor. Please refer to Section 5.2 for more details.

Table 4-5: Typical R_{SET} Values

Output Swing (mV_{pp})	R_{SET} (Ω)	R_{TERM} (Ω)	V_{TERM} (V)
1040	576	75	3.3
800	750	75	3.3
500	1210	75	3.3

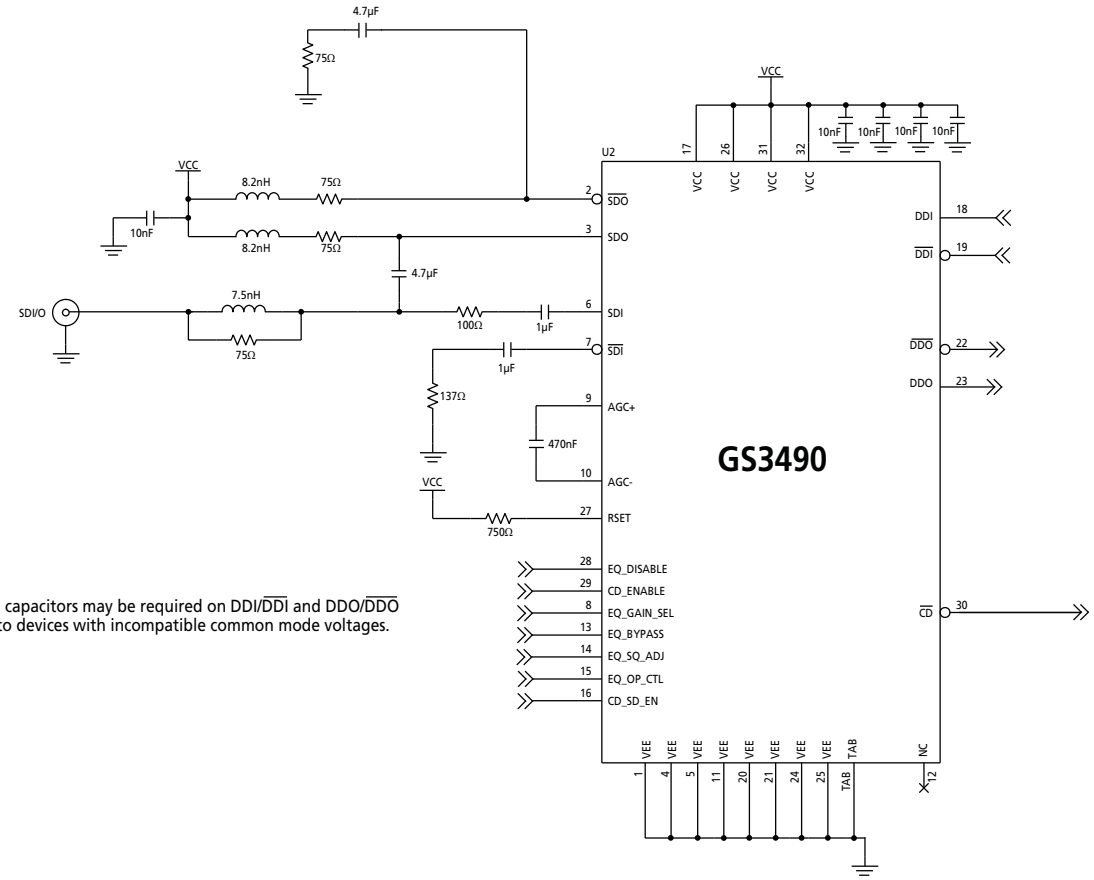
Note 1: Actual swing values may vary based on layout.

Note 2: R_{SET} is the resistor connected from pin 27 to VCC (refer to Figure 5-1).

Note 3: R_{TERM} is the SDO/$\overline{\text{SDO}}$ pull up resistor.

5. Application Information

5.1 Typical Application Circuit



Note: AC-coupling capacitors may be required on DDI/$\overline{\text{DDI}}$ and DDO/$\overline{\text{DDO}}$ when interfacing to devices with incompatible common mode voltages.

Figure 5-1: GS3490 Typical Application Circuit

5.2 PCB Layout

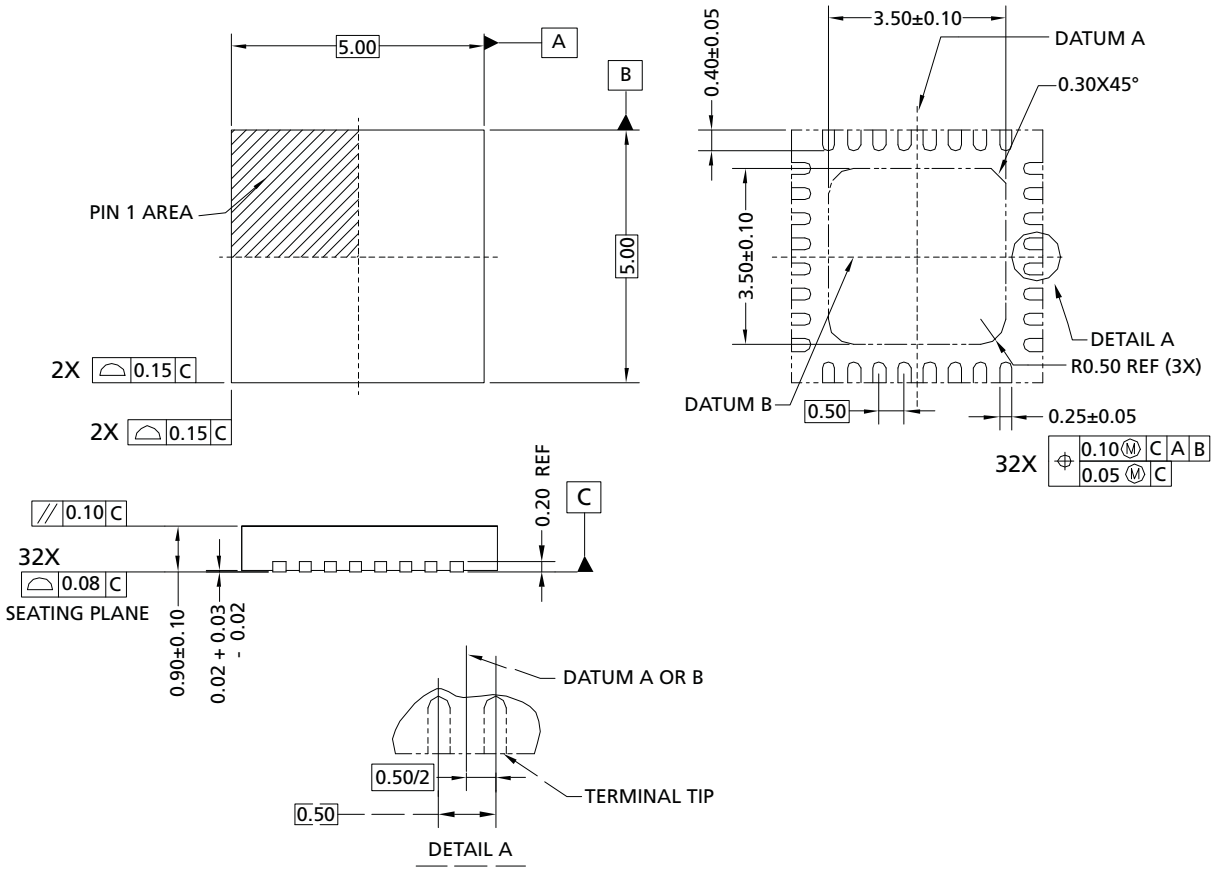
Special attention must be paid to component layout when designing Serial Digital Interfaces for HDTV. A FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for 3Gb/s rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- High-speed traces are curved to minimize impedance changes.

Cutouts in the inner layers should be used under the GS3490 input and output components to minimize parasitic capacitance. For more detail on this and other layout recommendations, please refer to A Guide For Designing With Semtech's 3G-SDI Equalizers (Doc ID: GENDOC-055280).

6. Package & Ordering Information

6.1 Package Dimensions



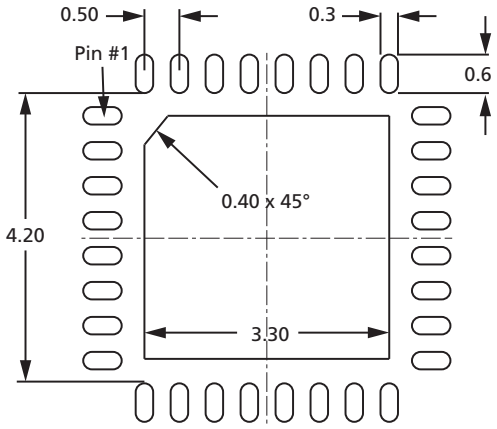
Note: All DIMENSIONS IN MM, ANGLES IN DEGREES
DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5 1994

Figure 6-1: Packaging Dimensions

6.2 Packaging Data

Parameter	Value
Package Type	32-pin QFN / 5mm x 5mm / 0.5mm pad pitch
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	17.8°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	26.4°C/W
Psi (ψ) =Junction-to-Top (of Package) Characterization Parameter	0.4°C/W
Pb-free and RoHS compliant	Yes

6.3 Recommended PCB Footprint



Notes:
1. All dimensions in mm.
2. Drawing not to scale.
3. 16 thermal VIAs, evenly spaced on centre paddle connected to ground plane.

Figure 6-2: Recommended PCB Footprint

6.4 Marking Diagram

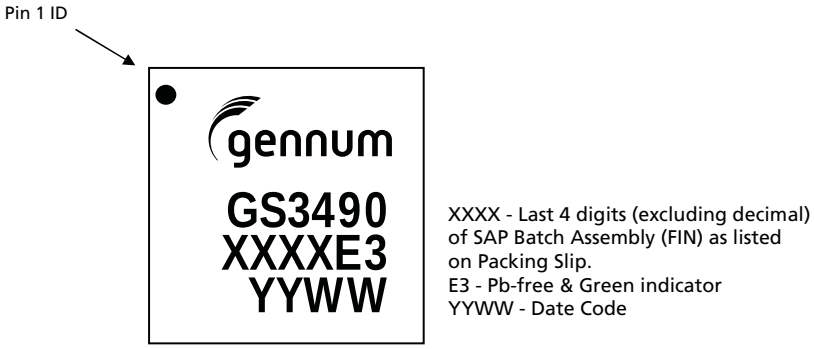


Figure 6-3: Marking Diagram

6.5 Solder Reflow Profiles

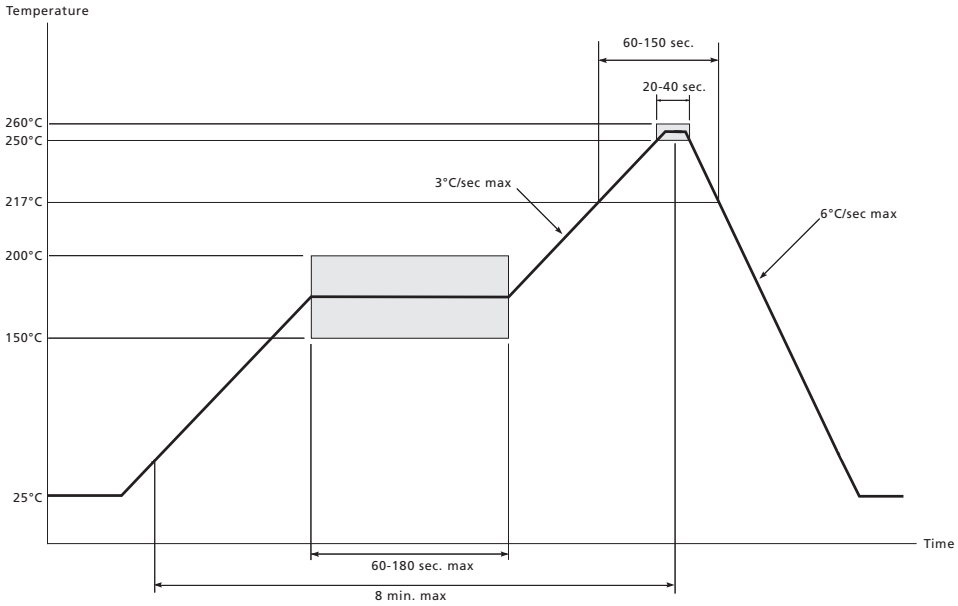


Figure 6-4: Maximum Pb-free Solder Reflow Profile

6.6 Ordering Information

Part	Part Number	Package	Temperature Range
GS3490	GS3490-INE3	32-pin QFN	-40°C to 85°C

DOCUMENT IDENTIFICATION
FINAL DATA SHEET
The product is in production. Semtech reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

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