

GS5484

24V, 3A, 340KHz Synchronous Step-Down DC/DC Converter

Product Description

The GS5484 is a synchronous step-down DC/DC converter that provides wide 4.5V to 24V input voltage range and 3A continuous load current capability.

Fault protection includes cycle-by-cycle current limit, input UVLO, output over voltage protection and thermal shutdown. Besides, adjustable soft-start function prevents inrush current at turn-on. This device uses current mode control scheme that provides fast transient response. In shutdown mode, the supply current is about 10uA.

The GS5484 is available in an 8-pin SOIC package, provides a very compact system solution and good thermal conductance.

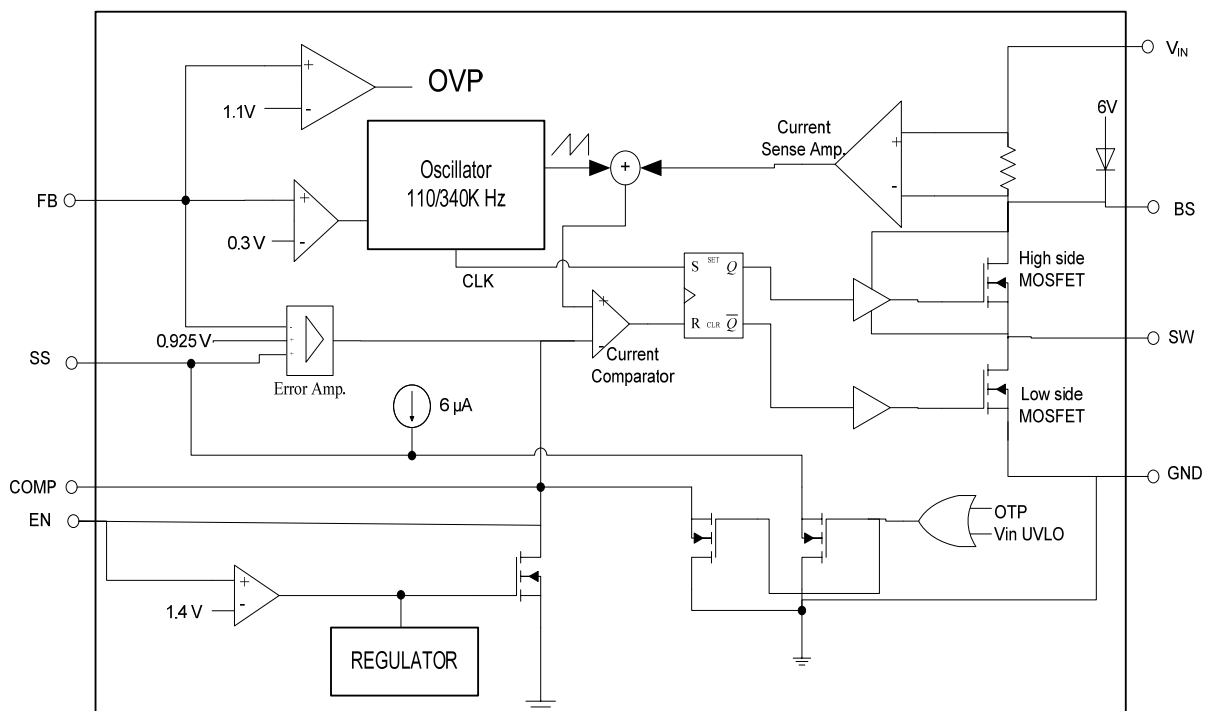
Features

- Wide Input Voltage from 4.5V to 24V
- 3A Output Current
- Adjustable Output Voltage from 0.925V to 20V
- 150mΩ integrated Power MOSFET
- High Efficiency Up to 92%
- Fixed 340KHz Switching Frequency
- Current Mode Operation
- Adjustable Soft-Start
- Cycle-by-Cycle current limit
- Input Under Voltage Lockout
- Over-Temperature Protection
- 10uA Shutdown Current
- Thermal Enhanced PSOP-8 Package
- RoHS Compliant, 100%Pb & Halogen Free

Applications

- Set-Top-Box
- DVD, LCD Displays
- OLPC, Netbook
- Distributed Power System
- Datacom, XDSL

Functional Block Diagram



Typical Applications

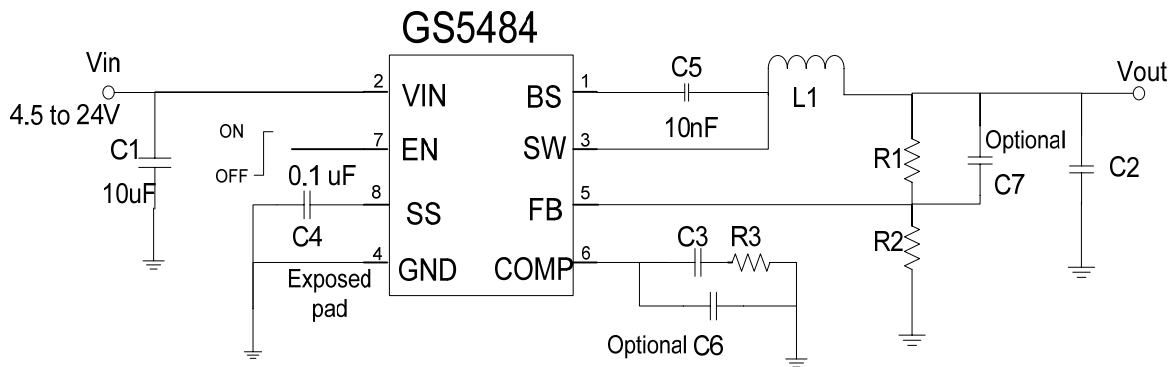
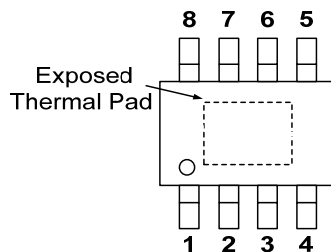


Table 1 recommended Component Selection

V _{OUT}	R1	R2	R3	C3	L1	C2
5.0V	66K	15K	12K	3.3nF	10 μ H	22 μ Fx2
3.3V	25.9K	10K	7.5K	3.3nF	10 μ H	22 μ Fx2
2.5V	17K	10K	6.8K	3.3nF	6.8 μ H	22 μ Fx2
1.8V	9.4K	10K	5.6K	3.3nF	6.8 μ H	22 μ Fx2
1.2V	3.9K	10K	3.9K	3.3nF	4.7 μ H	22 μ Fx2
1.0V	1.3K	15K	3.3K	3.3nF	3.3 μ H	22 μ Fx2

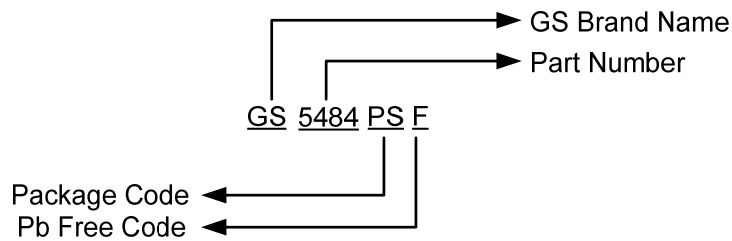
Packages & Pin Assignments

GS5484PSF (PSOP-8)



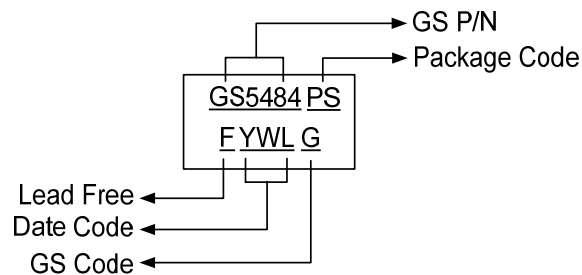
Name	No.	Description
BS	1	High Side Gate Drive Boost Input. A 10nF or greater capacitor must be connected from this pin to SW. It can boost the gate drive to fully turn on the internal high side NMOS.
V _{IN}	2	Power Supply Input Pin. Drive 4.5V to 24V voltage to this pin to power on this chip. Connecting a 10uF ceramic bypass capacitor between V _{IN} and GND to eliminate noise.
SW	3	Power Switching Output. It is the output pin that internal high side NMOS switching to supply power.
GND	4	Ground Pin. Connecting this pin to exposed pad.
FB	5	Voltage Feedback Input Pin. Connecting FB and V _{OUT} with a resistive voltage divider. This IC senses feedback voltage via FB and regulate it at 0.925V.
COMP	6	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a series RC network from COMP pin to GND.
EN	7	Enable Input Pin. This pin provides a digital control to turn the converter on or off. Connect to V _{IN} with a 100K Ω resistor for self-startup.
SS	8	Soft-Start Input Pin. This pin controls the soft-start period. Connect a capacitor from SS to GND to set the soft start period.

Ordering Information



Order Number	Package Code	Package	Quantity
GS5484PSF	PS	PSOP-8	4000 PCS/Tape & Reel

Marking Information



Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Max	Units
Input Supply Voltage	V_{IN}	-0.3 to +26	V
SW Voltage	V_{SW}	-1 ~ ($V_{IN} + 0.3$)	V
Boost Voltage	V_{BS}	($V_{SW} - 0.3$) ~ ($V_{SW} + 6$)	V
All Other Pins Voltage		-0.3 to +6	V
Maximum Junction Temperature		150	°C
Storage Temperature		-65~150	°C
Lead Temperature (Soldering 10 sec)		260	°C
ESD Rating (Human Body Mode)	HBM	2	KV

Recommended Operating Conditions (Note 2)

Parameter	Symbol	Max	Units
Input Supply Voltage	V_{IN}	4.5 to +24	V
Output Voltage	V_{OUT}	0.925~20	V
Ambient Temperature	T_A	-40~85	°C
SOP-8 (Exposed Pad)	θ_{JA}	75	°C/W
SOP-8 (Exposed Pad)	θ_{JC}	15	°C/W

Note 1: Stresses exceed those ratings may damage the device.

Note 2: If out of its operation conditions, the device is not guaranteed to function.

Electrical Characteristics

($V_{IN}=12V$, $T_A=25^{\circ}C$, unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Units
V_{IN} Input Supply Voltage (Note 3)		4.5		24	V
V_{IN} Supply Current	$V_{EN}=1.8V$		1.1		mA
V_{IN} Shutdown Supply Current	$V_{EN}=0V$		10	15	μA
Feedback Voltage	$4.5V \leq V_{IN} \leq 24V$	0.9	0.925	0.95	V
Feedback OVP Threshold Voltage			1.1		V
High-Side MOSFET $R_{DS(ON)}$ (Note 4)			100		m Ω
Low-Side MOSFET $R_{DS(ON)}$ (Note 4)			85		m Ω
High-Side MOSFET Leakage Current	$V_{EN} = 0V$ $V_{SW} = 0V$			10	μA
High-Side MOSFET Current Limit (Note 4)	Minimum Duty	4	5		A
Low-Side MOSFET Current Limit (Note 4)			3		A
COMP to Current sense Transconductance (Note 4)			5.2		A/V
Error Amplifier Transconductance (Note 4)	$\Delta I_{COMP} = \pm 10\mu A$		800		$\mu A/V$
Error Amplifier Voltage Gain (Note 4)			400		V/V
Oscillation frequency		280	340	380	KHz
Short Circuit Oscillation Frequency	$V_{FB} = 0V$		110		KHz
Maximum Duty Cycle	$V_{FB} = 0.8V$		90		%
Minimum On Time (Note 4)			220		ns
Input UVLO Threshold	V_{IN} Rising		4.4		V
Under Voltage Lockout Threshold Hysteresis			400		mV
Soft-Start Current	$V_{COMP} = 0V$ $V_{SS} = 0V$		6		μA
Soft-Start Period	$C_{SS} = 0.1\mu F$		15		ms
EN Input Threshold Voltage	Logic-High	2.0			V
	Logic-Low			0.4	
Thermal Shutdown Threshold (Note 4)			145		$^{\circ}C$

Note 3: When $V_{IN} = 4.5V$, $V_{OUT} = 3.3V$, only load 1.2A.

Note 4: Not production tested.

Typical Operating Characteristics

C1 = 10uF , C2 = 22uF x 2, L1 = 10uH, C4 = 0.1uF, T_A = +25°C, unless otherwise noted.

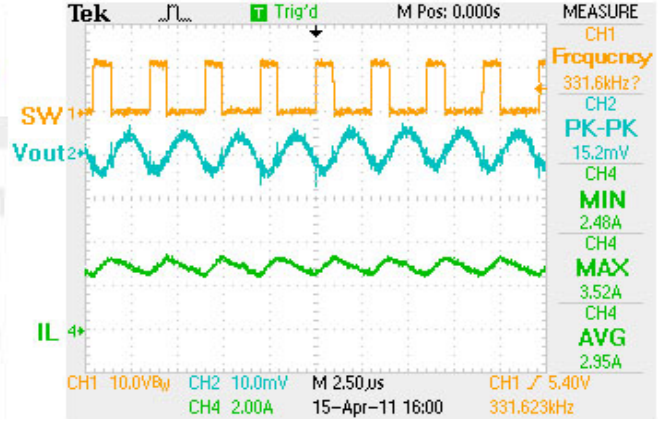
Steady State (no load)

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0A



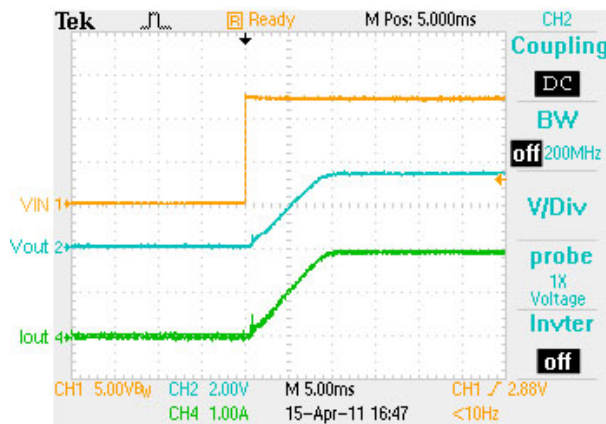
Steady State (heavy load)

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A



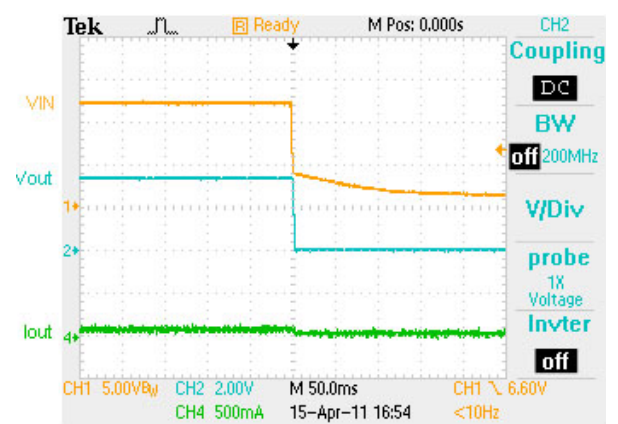
Power On

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=2A



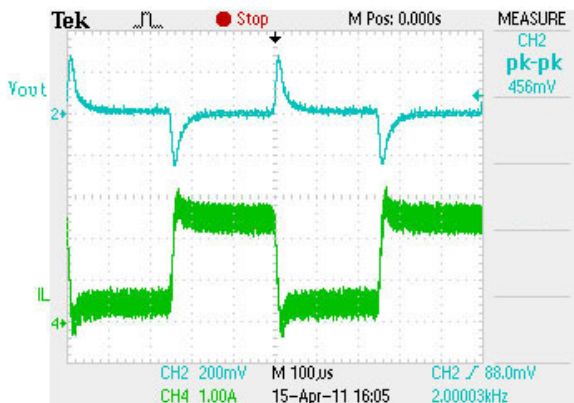
Shut down

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0.05A



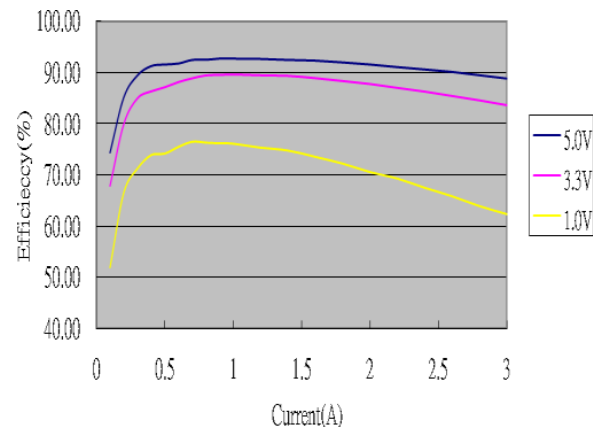
Dynamic loading

V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0.5A to 2.5A



Efficiency

V_{IN}=12V



Function Description

The GS5484 is a constant frequency current mode step-down synchronous DC/DC converter. It regulates input voltage from 4.5V to 24V, down to an output voltage as low as 0.925V, and can provide 3A of continuous load current.

Control Loop

During normal operation, the output voltage is sensed at FB pin through a resistive voltage divider and amplified through the error amplifier. The voltage of error amplifier output pin – COMP is compared to the switch current to controls the RS latch. At each cycle, the high side NMOS would be turned on when the oscillator sets the RS latch and would be turned off when current comparator resets the RS latch. When the load current increases, the FB pin voltage drops below 0.925V, it causes the COMP voltage increase until average inductor current arrive at new load current.

Enable

The GS5484 EN pin provides digital control to turn on/turn off the regulator. When the voltage of EN exceeds the threshold voltage, the regulator starts the soft start function. If the EN pin voltage is below than the threshold voltage, only the bandgap voltage is alive. If the EN pin voltage is below than the shutdown threshold voltage, the regulator will be disable and into the shutdown mode.

Maximum Load Current

The maximum load current decreases at lower input voltage because of large IR drop on the high side switch and low side switch. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%.

Output Over Voltage Protection

When the FB pin voltage exceeds 20% of the regulation voltage, the output over voltage protection function will discharge the COMP pin and the SS pin to GND, turning the high side MOSFET off.

Input Under Voltage Lockout

When the GS5484 power on, the internal circuits are held inactive until V_{IN} exceeds the input UVLO threshold voltage. And the regulator will be disabled when V_{IN} below the input UVLO threshold voltage. The hysteric of the UVLO comparator is 400 mV.

Short Circuit Protection

The GS5484 provides short circuit protection function to prevent the device damage from short condition. When the output short to ground, the oscillator frequency is reduced to prevent the inductor current increasing beyond the current limit. In the meantime, the current limit is also reduced to lower the short current. Once the short condition is removed, the frequency and current limit will return to normal.

Over Temperature Protection

The GS5484 incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown.

Compensation

The stability of the feedback circuit is controlled through COMP pin. The compensation value of the application circuit is optimized for particular requirements. If different conversions are requires, some of the components may need to be changes to ensure stability.

Application Information

Output Voltage Setting

The output voltage V_{OUT} is set using a resistive divider from the output to FB. The FB pin regulated voltage is 0.925V. Thus the output voltage is:

$$V_{OUT} = 0.925 \times \left(1 + \frac{R1}{R2} \right) V$$

R2 recommended value is 10k Ω , so R1 is determined by:

$$R1 = 10.81 \times (V_{OUT} - 0.925) \text{ k}\Omega$$

Table 1 lists recommended values of R1 and R2 for most used output voltage.

Table 2 Recommended Resistance Values

V_{OUT}	R1	R2
12V	121k Ω	10k Ω
5V	66.0k Ω	15k Ω
3.3V	25.9k Ω	10k Ω
2.5V	17.0k Ω	10k Ω
1.8V	9.40k Ω	10k Ω

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

The use of the input capacitor is controlling the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 times to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

Where D is the duty cycle of the power MOSFET.

A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1uF ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. Low ESR capacitors are preferred. Ceramic, tantalum or low ESR electrolytic capacitors can be used, depends on the output ripple requirement. Add a 100uF or 470uF Low ESR electrolytic capacitor when operated in high input voltage range ($V_{IN} > 20V$). It can improve the device's stability. The output ripple voltage ΔV_{OUT} is described as:

$$\Delta I = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{out}}{V_{in}}\right)$$

$$\Delta V_{OUT} = \Delta I \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{out}} \right)$$

Where ΔI is the peak-to-peak inductor ripple current, F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, V_{OUT} is the output voltage, R_{ESR} is the equivalent series resistance value of the output capacitor, and the C_{OUT} is the output capacitor. When using the ceramic capacitors, the R_{ESR} can be ignored and the output ripple voltage ΔV_{OUT} is shown as:

$$\Delta V_{OUT} = \frac{\Delta I}{8 \times F_{OSC} \times C_{OUT}}$$

When using tantalum or electrolytic capacitors, typically 90% of the output voltage ripple is contributed by the ESR of output capacitors. the output ripple voltage ΔV_{OUT} can be estimated as:

$$\Delta V_{OUT} = \Delta I \times R_{ESR}$$

Output Inductor Selection

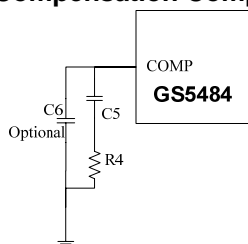
The output inductor is used for store energy and filter output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode. That will lower ripple current and results in lower output ripple voltage. A good rule for determining the inductance is set the peak-to-peak inductor ripple current ΔI almost equal to 30% of the maximum load current. Then the minimum inductance can be calculated with the following equation:

$$\Delta I = 0.3 \times I_{OUT(max)}$$

$$L \geq (V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{F_{OSC} \times \Delta I \times V_{IN}} \right)$$

Where V_{IN} is the maximum input voltage.

Compensation Components Selection



Selecting the appropriate compensation value by following procedure:

1. Calculate the R4 value with the following equation:

$$R4 < \frac{2\pi \times C_{OUT} \times 0.1 \times F_{OSC} \times V_{OUT}}{G_{EA} \times G_{CS} \times V_{REF}}$$

where G_{EA} is the error amplifier voltage gain, and G_{CS} is the current sense gain.

2. Calculate the C5 value with the following equation:

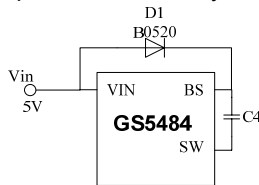
$$C5 > \frac{4}{2\pi \times R4 \times 0.1 \times F_{OSC}}$$

3. If the C_{OUT} ESR zero is less than half of the switching frequency, use C6 to cancel the ESR zero:

$$C6 = \frac{C_{OUT} \times R_{ESR}}{R4}$$

External Boost Diode Selection

For 5V input or 5V output applications, it is recommended that an external boost diode be added. This helps improve the efficiency. The boost diode can be a low cost one such as B0520.

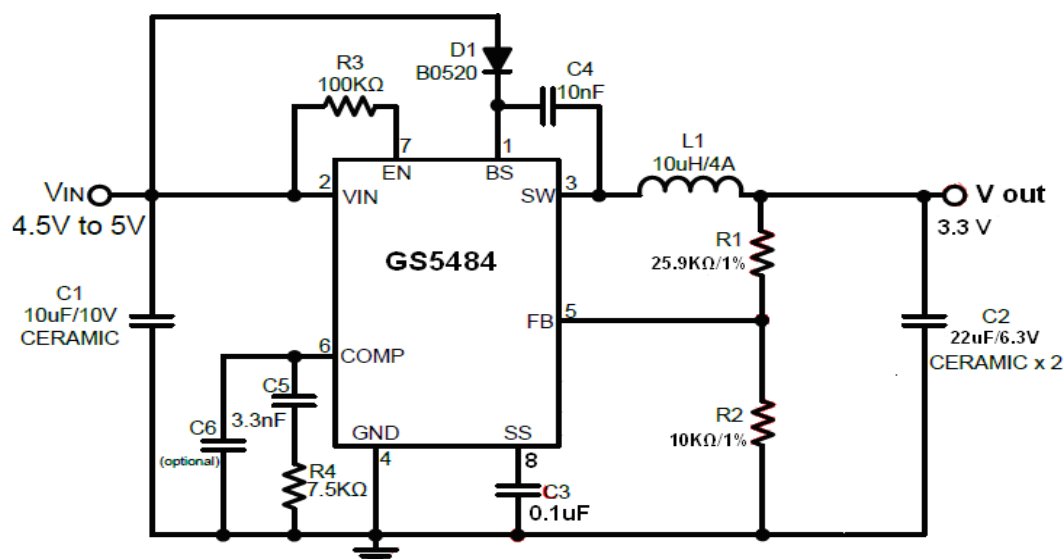


PCB Layout Recommendation

The device's performance and stability is dramatically affected by PCB layout. It is recommended to follow these general guidelines show below:

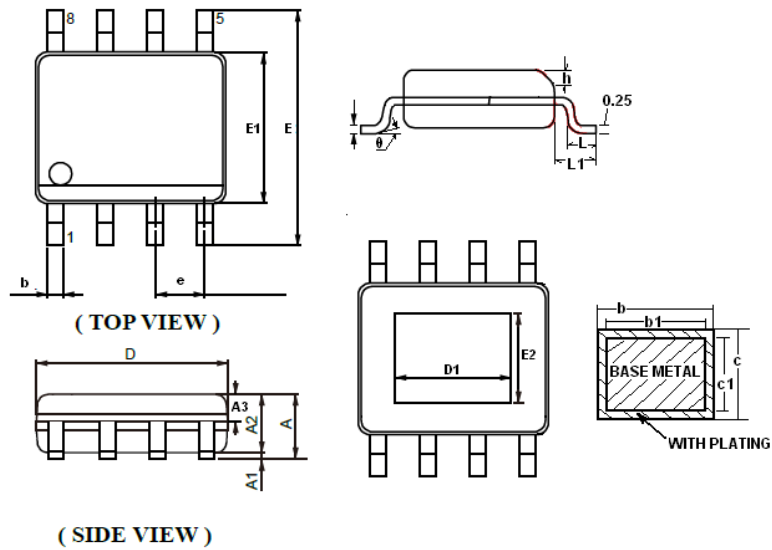
1. Place the input capacitors, output capacitors as close to the device as possible. Trace to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{IN} bypass capacitors close to the V_{IN} pin.
3. Place feedback resistors close to the FB pin.
4. Place compensation components close to the COMP pin.
5. Keep the sensitive signal (FB, COMP) away from the switching signal (SW).
6. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connects to the exposed pad should be maximized to improve thermal performance.
7. Multi-layer PCB design is recommended.

Typical Application Circuit



Package Dimension

PSOP-8 PLASTIC PACKAGE











Dimensions						
SYMBOL	Millimeters			Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.75	-	-	0.069
A1	0.05	-	0.15	0.002	-	0.006
A2	1.3	1.4	1.5	0.051	0.055	0.059
A3	0.6	0.65	0.7	0.024	0.026	0.028
b	0.39	-	0.48	0.015	-	0.019
b1	0.38	0.41	0.43	0.015	0.016	0.017
c	0.21	-	0.26	0.008	-	0.010
c1	0.19	0.2	0.21	0.007	0.008	0.008
D	4.84	-	5.025	0.189	-	0.196
D1	2.8	2.90	3.0	0.102	0.114	0.118
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.7	3.9	4.1	0.146	0.154	0.161
E2	1.9	2.0	2.1	0.075	0.079	0.083
e	1.27BSC.			0.050		
h	0.25	-	0.5	0.010	-	0.020
L	0.5	-	0.8	0.020	-	0.031
L1	1.05 BSC			0.041		
θ	0	-	8	0	-	8

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