

## Features

- Maximum 2A Low-Dropout Voltage Regulator
- Ultra Low Dropout Voltage  
Typically 220mV at 2A Output Current
- High Output Accuracy over Line, Load and Temperature
- Build-In Soft-Start
- Excellent startup under load from 0 to 2A
- Power-On-Reset Monitoring on Both  $V_{DD}$  and  $V_{IN}$  Pins
- Power-OK Output function
- Foldback over Current Protection and Thermal shutdown
- 0.1 $\mu$ A (typ) Shutdown Supply Current
- Low ESR Output Capacitor(Multi-layer Chip Capacitors (MLCC)) Applicable
- Vout Pull Low Resistance when Disable
- PSOP-8, TDFN10-3x3
- Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

## Applications

- Notebook PC Applications
- Motherboard Applications
- Low Voltage Logic Supplies
- Microprocessor and Chipset Supplies
- Graphic Cards
- Cordless phones

## General Description

The GS7105 can deliver up to 2A of continuous output current with a typical dropout voltage of only 220mV using internal n-channel MOSFETs. The linear regulator uses a separate VDD supply to power the control circuitry and drive the Internal n-channel MOSFETs. The output voltage is adjustable from 0.8V to the voltage that is very close to  $V_{IN}$ .

The GS7105 allows the use of low-ESR ceramic capacitor as low as 10 $\mu$ F. Moreover the IC provide good performance on both line transient response and load transient response.

The GS7105 provides foldback over current limit and thermal shutdown to prevent the linear regulator from damage. Built-in soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. During start-up, POK remain low until the output reaches 92% of its rating value.

The GS7105 is available in PSOP-8 package or TDFN10- 3x3 package.

**Typical Application**

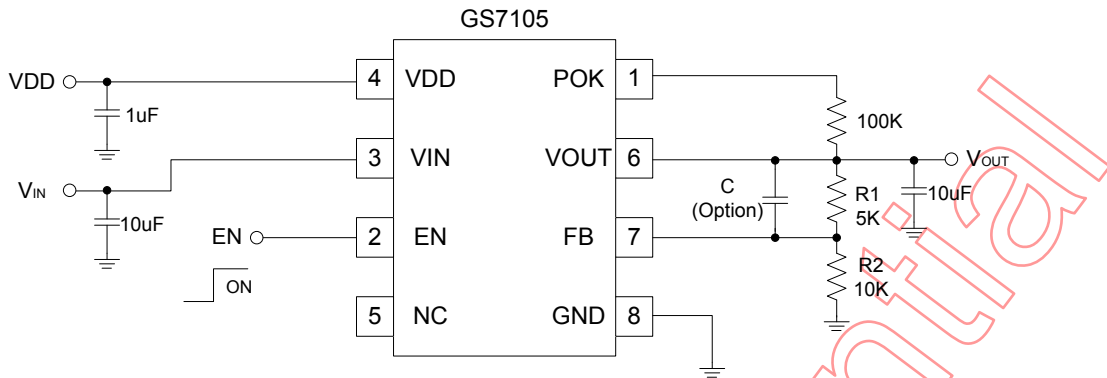


Figure1 Typical Application of GS7105

**Function Block Diagram**

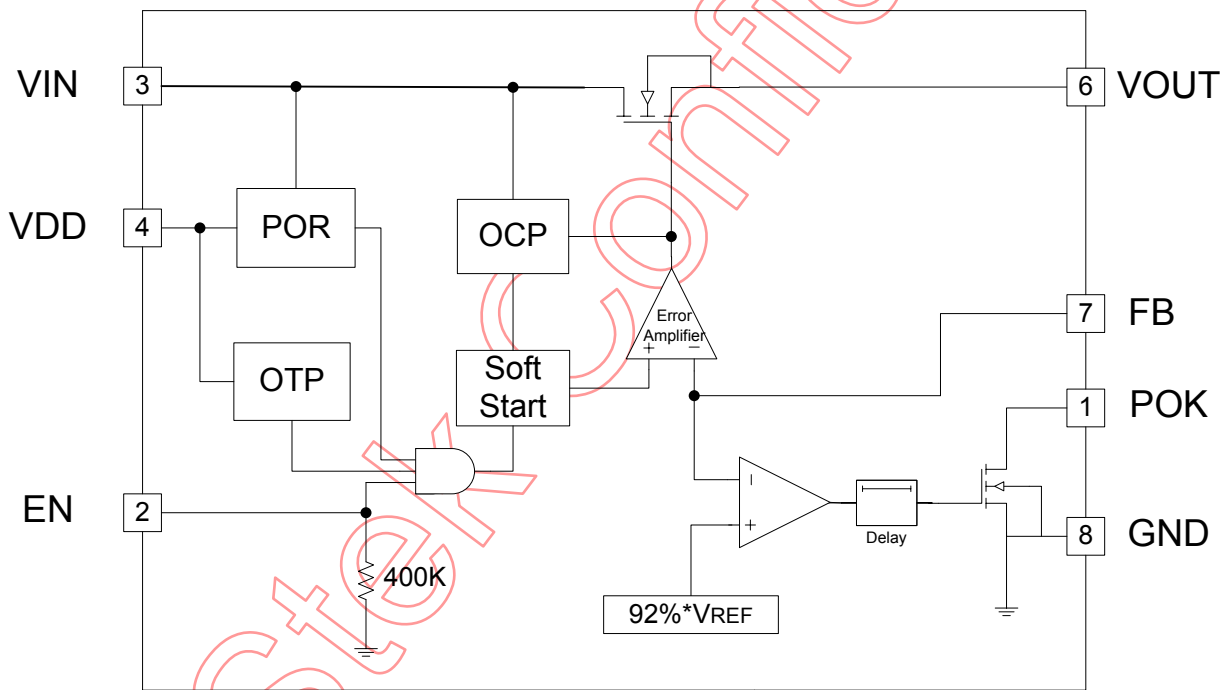
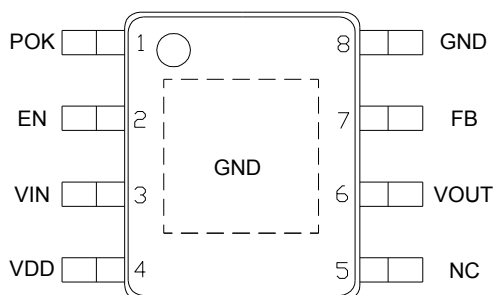
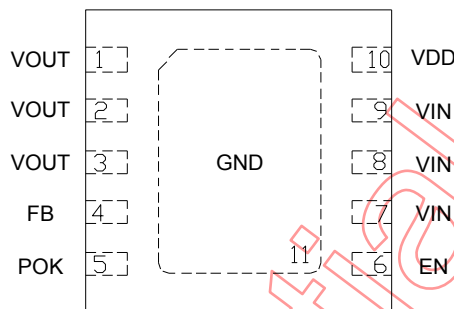


Figure 2 Function Block Diagram

**Pin Configuration**



PSOP-8



TDFN10-3x3

**Pin Descriptions**

Pin No.		Name	I/O type	Pin Function
PSOP8	TDFN10-3x3			
1	5	POK	O	Open drain output. Setting high impedance once V <sub>OUT</sub> reaches 92% of its rating voltage
2	6	EN	I	Chip Enable (active high). The device will be shutdown if this pin is left open.
3	7,8,9	VIN	I	Input Voltage. Large bulk capacitance should be placed closely to this pin. A 10μF ceramic capacitor is recommended at this pin.
4	10	VDD	I	Supply voltage for control circuit. A 3V to 5V supply voltage for control circuit is recommended and supply voltage should be 1.5V higher than the output voltage.
5		NC		Not connected
6	1,2,3	VOUT	O	Output Voltage. The power output of the device.
7	4	FB	I	Feedback Voltage. This pin is connected to the center tap of an external resistor divider network to set the output voltage as $V_{OUT} = 0.8(R1+R2)/R2$ .
8	11	GND	I	Ground.

**Ordering Information**

**GS7105PP-R**

1. Package ← → 2. Shipping

No	Item	Contents
1	Package	SO: PSOP-8(B) TD: TDFN10-3x3
2	Shipping	R: Tape & Reel

Example: GS7105 PSOP-8(B) Tape & Reel ordering information is “GS7105SO-R”

## Absolute Maximum Rating (Note 1)

Parameter	Symbol	Limits	Units
Supply Voltage	$V_{IN}$	$-0.3 < V_{IN} < 6$	V
Control Voltage	$V_{DD}$	$-0.3 < V_{DD} < 6$	V
Output Voltage	$V_{OUT}$	$-0.3 < V_{OUT} < 5$	V
EN, FB, POK		$-0.3 < (V_{EN}, V_{FB}, V_{POK}) < 6$	V
Package Power Dissipation at $T_A \leq 25^\circ\text{C}$	$P_{D\_PSOP-8}$	1333	mW
Package Power Dissipation at $T_A \leq 25^\circ\text{C}$	$P_{D\_TDFN10-3x3}$	1670	mW
Junction Temperature	$T_J$	- 45 ~ 150	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	- 65 ~ 150	$^\circ\text{C}$
Lead Temperature (Soldering) 10S	$T_{LEAD}$	260	$^\circ\text{C}$
ESD (Human Body Mode) (Note 2)	$V_{ESD\_HBM}$	2K	V
ESD (Machine Mode) (Note 2)	$V_{ESD\_MM}$	200	V

## Thermal Information (Note 3)

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	$\theta_{JA\_PSOP-8}$	75	$^\circ\text{C/W}$
Thermal Resistance Junction to Case	$\theta_{JC\_PSOP-8}$	12	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$\theta_{JA\_TDFN10-3x3}$	60	$^\circ\text{C/W}$
Thermal Resistance Junction to Case	$\theta_{JC\_TDFN10-3x3}$	5	$^\circ\text{C/W}$

## Recommend Operating Condition (Note 4)

Parameter	Symbol	Limits	Units
Supply Voltage	$V_{IN}$	$1.0 < V_{IN} < \text{Min}\{5.2, V_{DD}\}$	V
Control Voltage	$V_{DD}$	$3.0 < V_{DD} < 5.5$	V
Junction Temperature	$T_J$	- 40 ~ 125	$^\circ\text{C}$

### Electrical Characteristics

( $V_{IN} = V_{OUT} + 0.5V$ ,  $V_{EN} = V_{DD} = 5V$ ,  $C_{IN} = C_{OUT} = 10\mu F$ ,  $T_A = T_J = 25^\circ C$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
<b>Supply Voltage Section</b>						
$V_{DD}$ Operation Voltage Range	$V_{DD}$	$V_{DD}$ Input Range, $V_{OUT} = V_{REF}$	3.0		5.5	V
$V_{IN}$ Operation Voltage Range	$V_{IN}$	$V_{IN}$ Input Range, $V_{OUT} = V_{REF}$	1.0		Min{5.2, $V_{DD}$ }	V
Quiescent current	$I_Q$	$V_{DD} = V_{IN} = V_{EN} = 5V$ , $I_{OUT} = 0A$ , $V_{OUT} = V_{REF}$		1.0	1.5	mA
$V_{DD}$ Input current	$I_{VDD}$	$V_{DD} = V_{IN} = V_{EN} = 5V$ , $I_{OUT} = 0A$ , $V_{OUT} = V_{REF}$		1.0	1.5	mA
Control Input Current in Shutdown	$I_{VDD\_SD}$	$V_{DD} = V_{IN} = 5.0V$ , $I_{OUT} = 0A$ , $V_{EN} = 0V$		0.1	2	$\mu A$
$V_{DD}$ POR Threshold	$V_{DDRTH}$		2.4	2.7	3	V
$V_{DD}$ POR Hysteresis			0.15	0.2		V
$V_{IN}$ POR Threshold	$V_{INRTH}$		0.55	0.75	0.95	V
$V_{IN}$ POR Hysteresis			0.13	0.20		V
<b>Output Voltage</b>						
Reference Voltage	$V_{REF}$	$I_{OUT} = 1mA$ , $V_{OUT} = V_{REF}$	0.784	0.8	0.816	V
Output Voltage Accuracy			-2.0		+2.0	%
Line Regulation ( $V_{DD}$ )	$\Delta V_{LINE\_VDD}$	$V_{DD} = 4V$ to $5V$ , $I_{OUT} = 1mA$ , $V_{OUT} = V_{REF}$ , $V_{IN} = 2V$		0.03	0.2	%
Line Regulation ( $V_{IN}$ )	$\Delta V_{LINE\_IN}$	$V_{IN} = 1.2V$ to $5V$ , $I_{OUT} = 1mA$ , $V_{OUT} = V_{REF}$		0.01	0.1	%
Load Regulation (Note 5)	$\Delta V_{LOAD}$	$I_{OUT} = 1mA$ to $3A$ , $V_{OUT} = V_{REF}$		0.1	1.5	%
$V_{OUT}$ Pull Low Resistance		$V_{DD} = V_{IN} = 5.0V$ , $V_{EN} = 0V$		130		$\Omega$
<b>Dropout Voltage</b>						
Dropout Voltage (Note 6)	$V_{DROP}$	$V_{OUT} = V_{REF}$ , $I_{OUT} = 1A$		110	210	mV
		$V_{OUT} = V_{REF}$ , $I_{OUT} = 2A$		220	320	mV
<b>Protection</b>						
Current Limit	$I_{LIM}$	$V_{DD} = V_{IN} = V_{EN} = 5V$ , $V_{OUT} = V_{REF}$		3.5		A
Short Circuit Current	$I_{FOLDBACK}$	$V_{OUT} < 0.2V$		100		mA
Thermal Shutdown Temperature	$T_{SD}$	$T_J$ Rising		160		$^\circ C$

Thermal Shutdown Returned Temperature					110		°C
<b>Enable</b>							
EN Threshold	Logic-Low Voltage		$V_{DD}=5V$			0.6	V
	Logic-High Voltage		$V_{DD}=5V$	1.4			V
EN Input Bias Current		$I_{EN}$	$V_{EN}=5V$		12	20	uA
<b>Power OK</b>							
POK Rising Threshold			$V_{REF}$ Rising		92		%
POK Hysteresis			$V_{REF}$ falling		8		%
POK Sink Capability			$I_{PGOOD}=1mA$		0.2	0.4	V
POK Delay			-40°C ~125°C		1.3		mS

**Note 1.** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.**  $\theta_{JA}$  is measured in the natural convection at  $T_A=25^\circ C$  on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of  $\theta_{JC}$  is on the expose pad for PSOP-8 package.

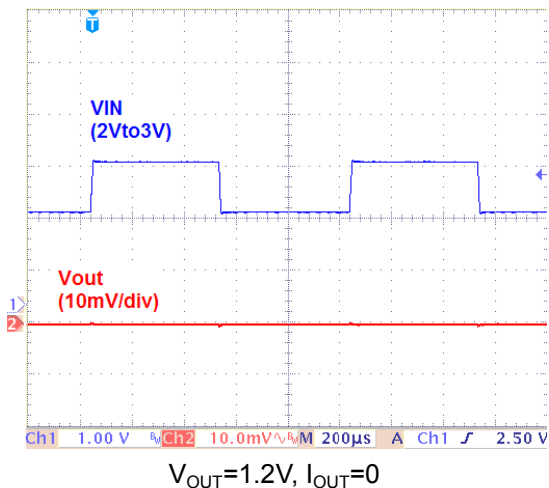
**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 1mA to 2A.

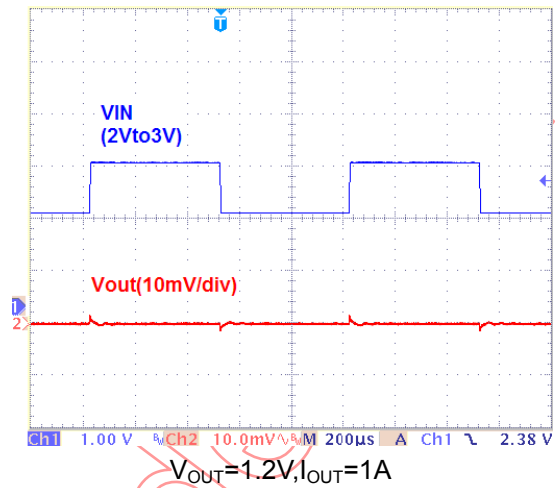
**Note 6.** The Dropout voltage is defined as  $V_{IN}-V_{OUT}$ , which is measured when  $V_{OUT}$  is  $0.98 * V_{OUT(NORMAL)}$ . The Dropout voltage is measured at constant junction temperature by using a 2ms current pulse.

Typical Characteristics

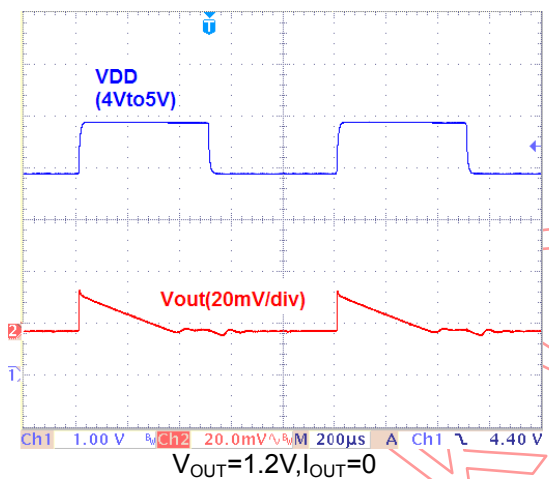
V<sub>IN</sub> Line Transient Response



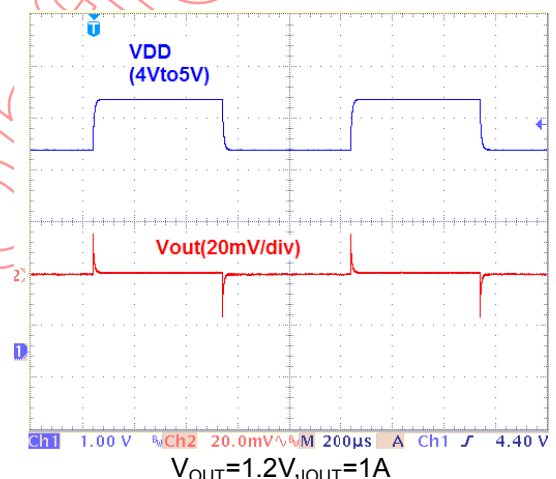
V<sub>IN</sub> Line Transient Response



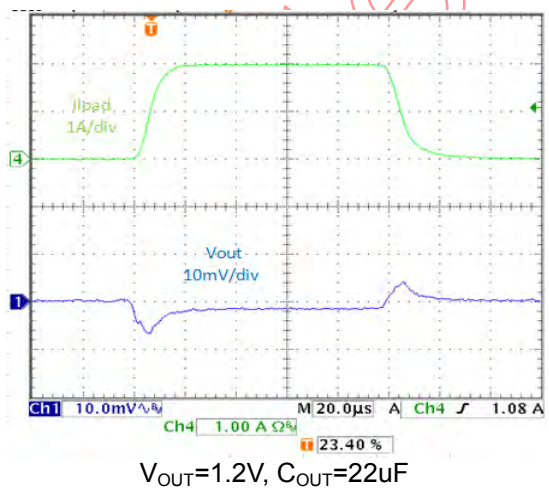
V<sub>DD</sub> Line Transient Response



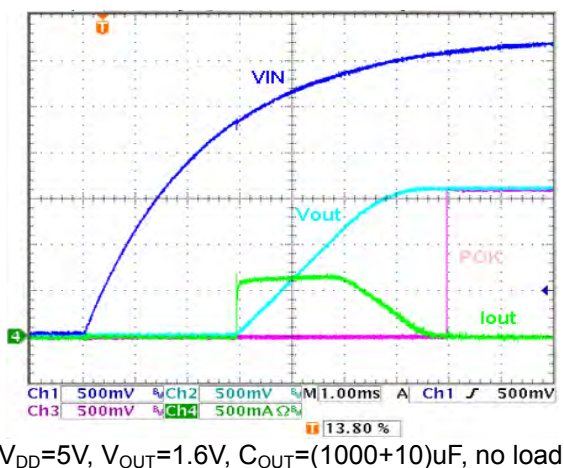
V<sub>DD</sub> Line Transient Response



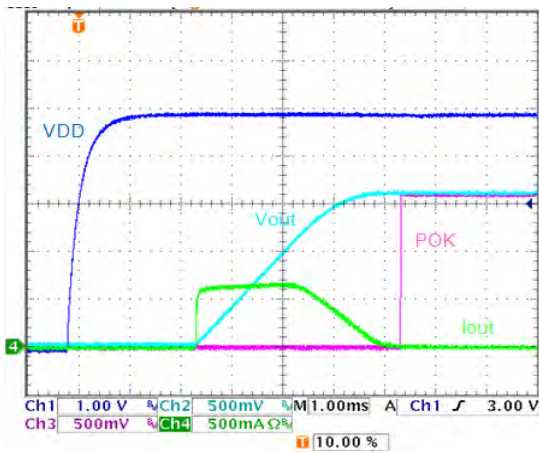
Load Transient Response



Power On from VIN

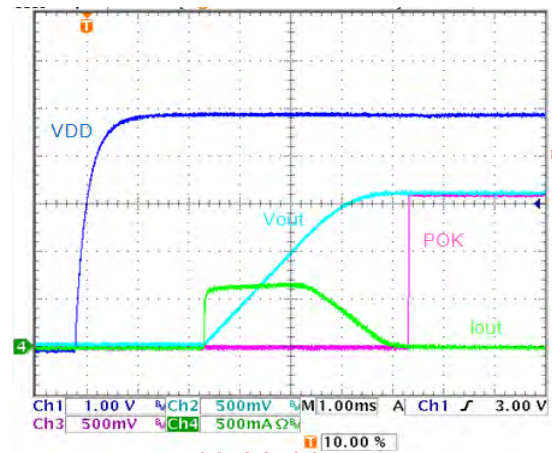


### Power On from V<sub>DD</sub>



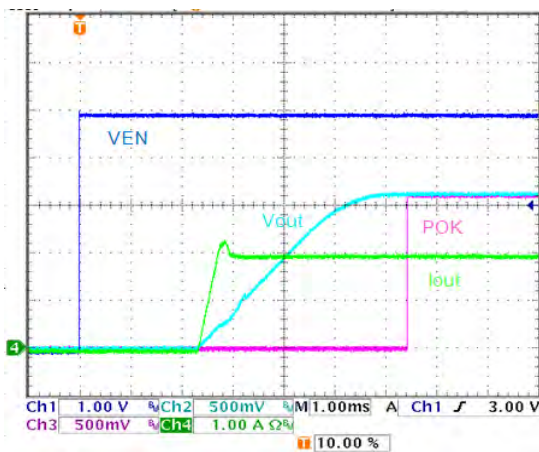
V<sub>DD</sub>=5V, V<sub>OUT</sub>=1.6V, C<sub>OUT</sub>=(1000+10)uF, no load

### Turn On from EN



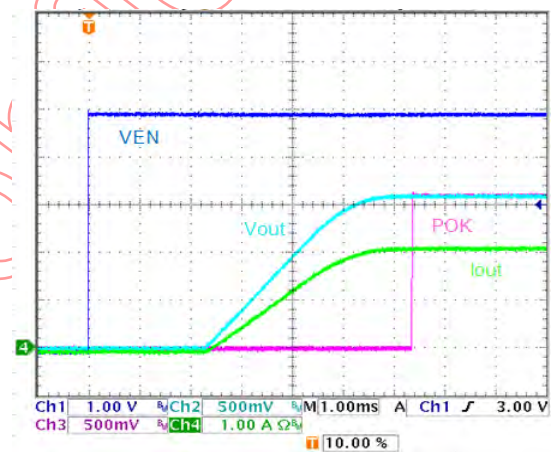
V<sub>EN</sub>=5V, V<sub>OUT</sub>=1.6V, C<sub>OUT</sub>=(1000+10)uF, no load

### Turn On from EN



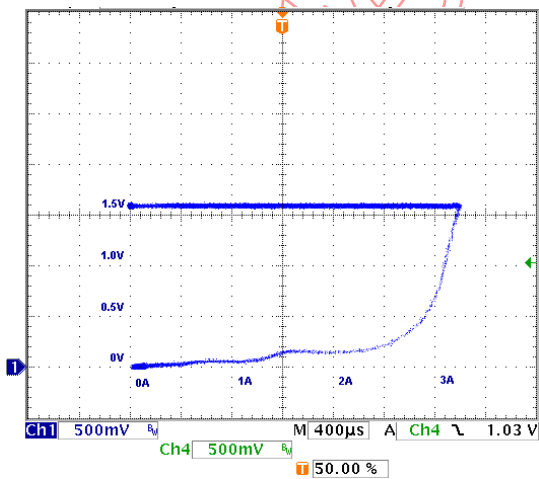
V<sub>EN</sub>=5V, V<sub>OUT</sub>=1.6V, C<sub>OUT</sub>=10uF, I<sub>load</sub>=2A

### Turn On from EN

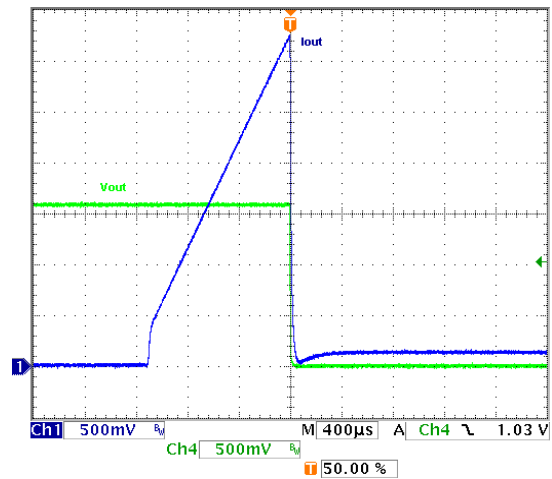


V<sub>EN</sub>=5V, V<sub>OUT</sub>=1.6V, C<sub>OUT</sub>=10uF, R<sub>load</sub>=0.8Ω

### Output Short Current

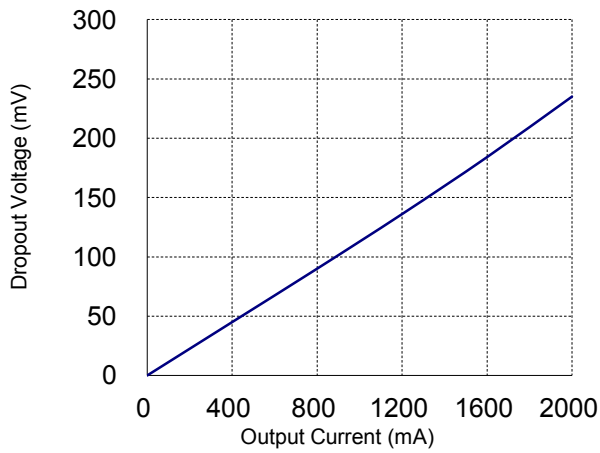


### Output Short Current

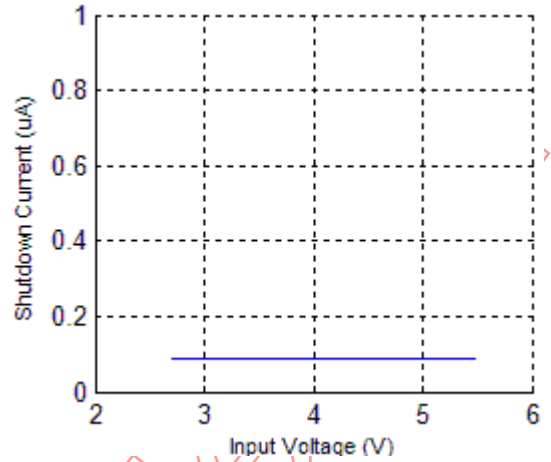




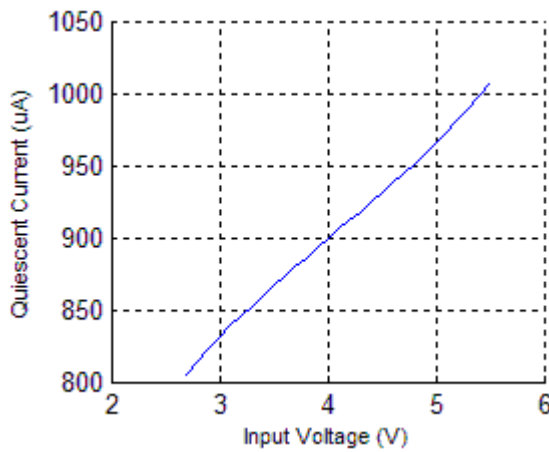
Dropout Voltage vs. Output Current



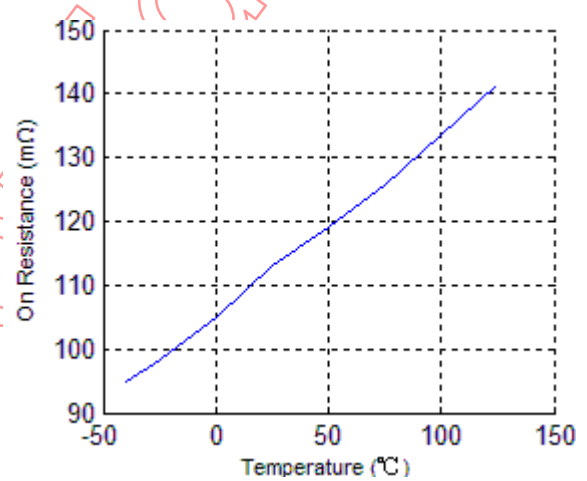
Shutdown Current vs. Input Voltage



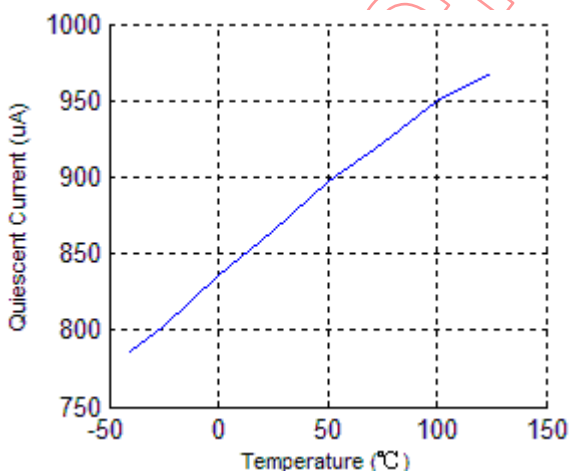
Quiescent Current vs. Input Voltage



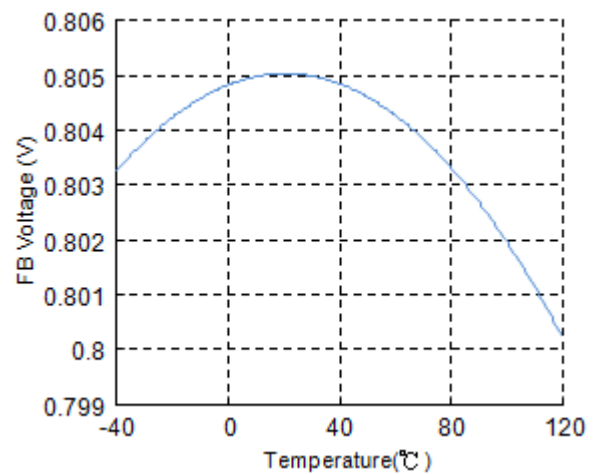
On Resistance vs. Temperature



Quiescent Current vs. Temperature



FB Voltage vs. Temperature



## Application Information

### Enable

The GS7105 has a dedicated enable pin(EN). When the EN pin is in the logic low ( $V_{EN}<0.6V$ ), the regulator will be turned off, reducing the supply current to less than 1uA.

When the EN pin is in the logic high ( $V_{EN}>1.4V$ ), the regulator will be turned on and undergoes a new soft-start cycle. Left open, the EN pin is pulled down by a internal resistor to shut down the regulator.

### Power-on-Reset

The GS7105 features a power-on-reset control through monitor both input voltages to prevent wrong operations. Only after the two supply voltages exceed their rising POR threshold voltages, the regulator is to be initiated and starts up.

### POK

The POK pin is an open-drain output, and can be connects to  $V_{OUT}$  or other rail through an external pull-up resistor. As the output voltage arrives 92% of normal output voltage, an internal delay function starts to perform a delay time and then output the POK pin high to indicate the output is OK. As the output voltage falls below the falling Power-OK threshold or one of the two supply voltages falls below it's falling POR threshold, the POK pin will output low immediately without a delay time.

### Build-In Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 1.5mS.

### Current Limit

The GS7105 contains a foldback over current protection function. It allows the output current to reach the maximum value of 3.5A. Then further decreases in the load resistance reduce both the load current and the load voltage. The main advantage of foldback limiting is less power dissipation in the pass transistor under shorted-load conditions. During startup, the current limit value is set to a high value, thus GS7105 can operate in full load condition. After startup, the current limit value is set to a normal value, so the pass transistor can be protected well.

### Thermal-Shutdown Protection

Thermal Shutdown protects GS7105 from excessive power dissipation. If the die temperature exceeds 160°C, the pass transistor is shut off. 50°C of hysteresis prevents the regulator from turning on until the die temperature drops to 110°C.

### Output Capacitor selection

The GS7105 is designed to employ ceramic output capacitors as low as 10uF; if employ EL output capacitor as large as 1000uF, feedback resistance( $R_{bottom}$ ) should be larger than 100K ohm(Table 2). Place the capacitors physically as close as possible to the device with wide and direct PCB traces. Capacitor ESR should be less than 50mohm.

	Cout	Rbottom
Ceramic	$\geq 10\mu F$	$\geq 0.1K\Omega$
EL	1000uF	$\geq 100K\Omega$

Table 1 Cout capacitor vs. Rbottom resistance

**Feedback Network**

Figure 3 shows the feedback network. The suggested design procedure is to choose  $R2=10K\Omega$  and then calculate  $R1$  using the following formula:  $R1=(V_{OUT}/V_{REF}-1)*R2$ .

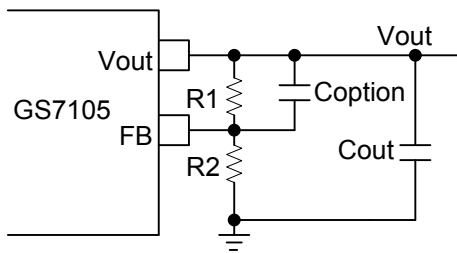


Figure 3. Feedback Network

$C_{OPTION}$  can improve transient response, and recommend value as follow:

$V_{OUT}$	R1	$C_{OPTION}$
0.8V ~ 1.6V	0 ~ 10 K $\Omega$	470pF~1nF
1.6V ~ 2.4V	10 K $\Omega$ ~ 20 K $\Omega$	100pF~500pF
2.4V ~ 3.6V	20 K $\Omega$ ~ 30 K $\Omega$	20pF~300pF

Table 2 R1 vs.  $C_{OPTION}$

**Input Capacitor selection**

Bypass  $V_{IN}$  to ground with a 10uF or greater capacitor. Bypass  $V_{DD}$  to ground with a 1uF capacitor for normal operation in most applications. Ceramic, tantalum or aluminum electrolytic capacitors may be selected for input capacitor. However ceramic capacitors are recommended due to their significant cost and space savings. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

**Power Dissipation and Layout Considerations**

Although internal thermal limiting function is integrated in GS7105, continuously keeping the junction near the thermal shutdown temperature may possibly affect device reliability. For continuous operation, it is highly recommended to

keep the junction temperature below the maximum operation junction temperature 125°C for maximum reliability.

The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{DD} \times I_Q$$

The maximum power dissipation can be calculated as:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where  $T_{J(MAX)}$  is the maximum operation junction temperature 125°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance.

The thermal resistance  $\theta_{JA}$  for PSOP-8 package is 75°C/W on the standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The copper thickness is 2oz. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (75^\circ\text{C/W}) = 1.33\text{W}$$

(SOP-8 Exposed Pad on the minimum layout)

The thermal resistance  $\theta_{JA}$  for TDFN10-3x3 package is 60°C/W on the standard JEDEC 51-7 (4 layers, 2S2P) thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (60^\circ\text{C/W}) = 1.67\text{W}$$

The thermal resistance  $\theta_{JA}$  of PSOP-8 is determined by the package design and the PCB design. Copper plane under the exposed pad is an effective heat sink and is useful for improving thermal conductivity. As shown in Figure 3, the amount of copper area to which the PSOP-8 is mounted affects thermal performance. When mounted to the standard PSOP-8 pad (Figure 3.a),  $\theta_{JA}$  is 75°C/W. Adding copper area of pad under the PSOP-8 Figure 3.b) reduces the  $\theta_{JA}$  to 54°C/W. Even further, increasing the copper area

of pad to 70mm<sup>2</sup> (Figure 3.c) reduces the  $\theta_{JA}$  to 49°C/W.

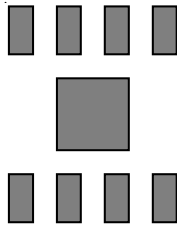


Figure 3 (a). Minimum Footprint,  $\theta_{JA} = 75^\circ\text{C/W}$

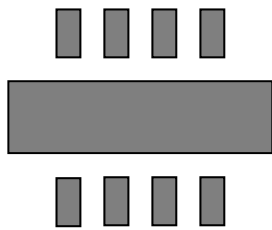


Figure 3 (b). Copper Area = 30mm<sup>2</sup>,  $\theta_{JA} = 54^\circ\text{C/W}$

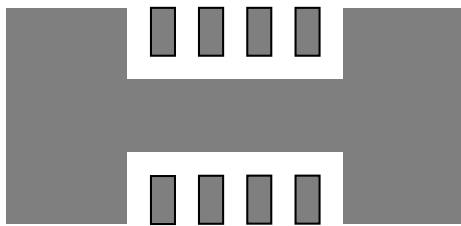


Figure 3 (c). Copper Area = 70mm<sup>2</sup>,  $\theta_{JA} = 49^\circ\text{C/W}$

Figure 3.  $\theta_{JA}$  vs. Different Cooper Area Layout Design And Figure 4 shows a curve for the  $\theta_{JA}$  of the PSOP-8 package for different copper area sizes using a typical PCB with 2oz copper in still air.

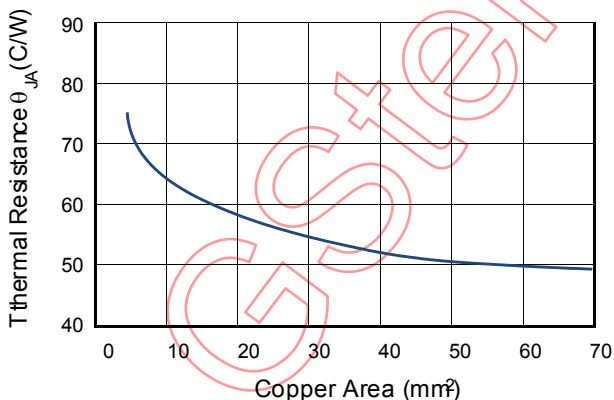


Figure 4  $\theta_{JA}$  vs. Copper Area

The maximum power dissipation depends on operating ambient temperature or fixed  $T_{J(\text{MAX})}$

and thermal resistance  $\theta_{JA}$ . For GS7105 packages, the Figure 5 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

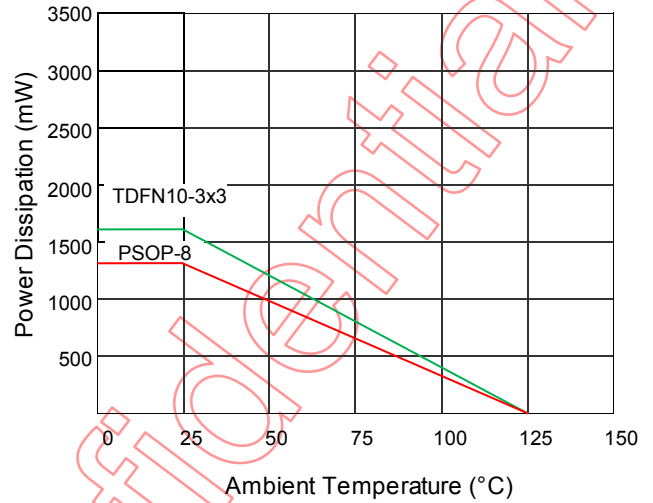
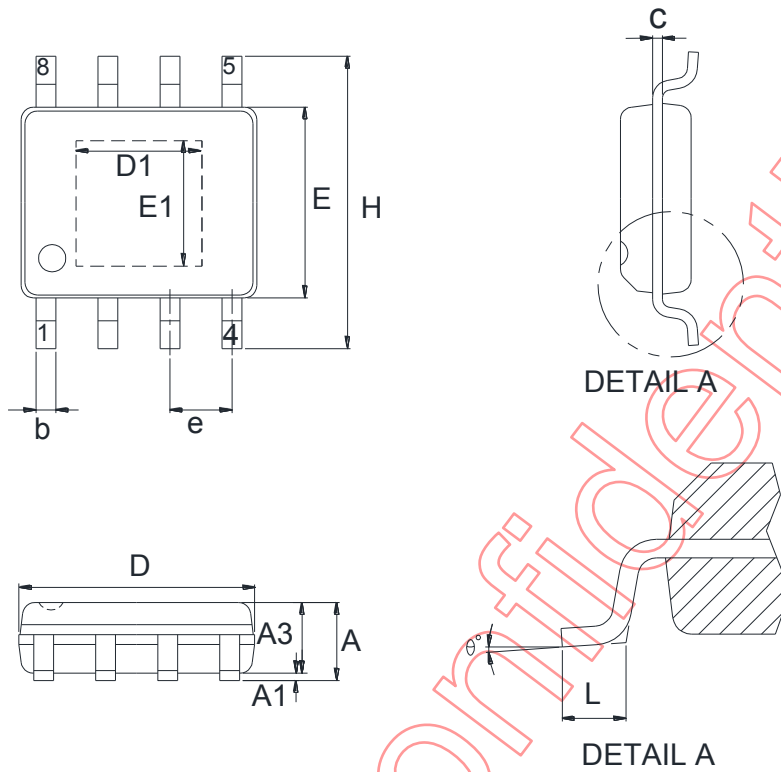


Figure 5 Derating Curve for Packages

GStek Confidential

**Package Dimensions, PSOP-8(B)**

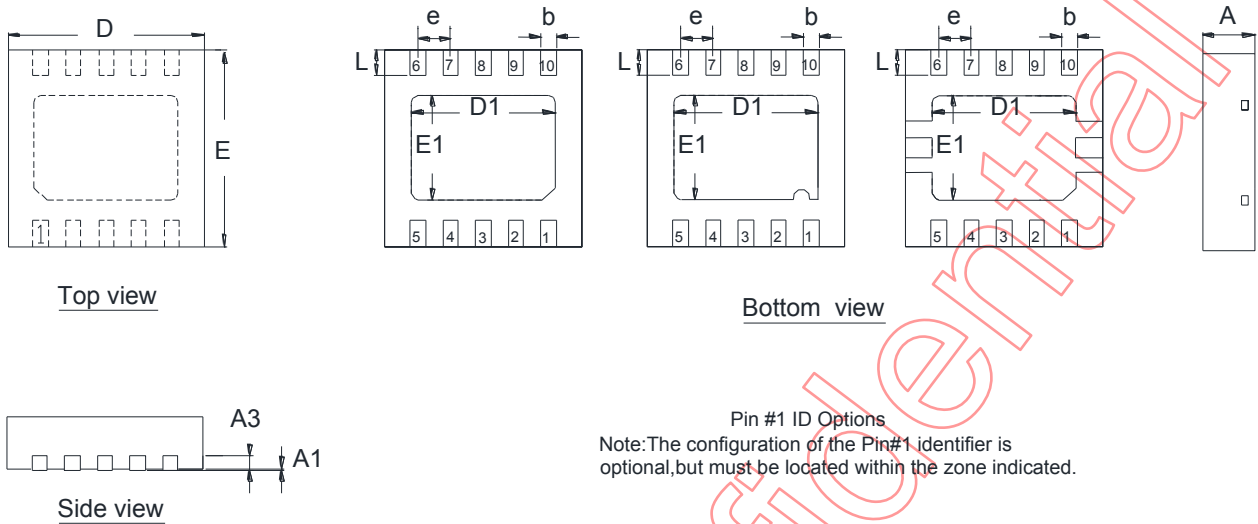


Symbol	Dimensions in Millimeters	
	Min.	Max.
A	1.30	1.80
A1	-	0.15
A3	1.25	-
b	0.31	0.51
c	0.17	0.25
e	1.27 REF.	
D	4.70	5.10
E	3.80	4.00
D1	3.1 REF.	
E1	2.3 REF.	
H	5.80	6.20
L	0.40	1.27
$\theta$	0°	8°

**Note:**

- 1. Min.: Minimum dimension specified.
- 2. Max.: Maximum dimension specified.
- 3. REF.: Reference. Normal/Regular dimension specified for reference.

### Package Dimensions, TDFN10-3x3



#### Pin #1 ID Options

Note: The configuration of the Pin#1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.70	0.80
A1	0.00	0.05
A3	0.203 REF.	
b	0.18	0.30
e	0.50 REF.	
D	2.90	3.10
E	2.90	3.10
D1	2.30 REF.	
E1	1.65 REF.	
L	0.30	0.50

#### Note:

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

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