

Features

- Maximum 1A Low-Dropout Voltage Regulator
- Ultra Low Dropout Voltage
Typically 100mV at 1A Output Current
- High Output Accuracy over Line, Load and Temperature
- Build-In Soft-Start
- Excellent startup under load from 0 to 1A
- Power-On-Reset Monitoring on Both V_{DD} and V_{IN} Pins
- Power-OK Output function
- Foldback over Current Protection and Thermal shutdown
- 0.1 μ A (typ) Shutdown Supply Current
- Low ESR Output Capacitor(Multi-layer Chip Capacitors (MLCC)) Applicable
- Vout Pull Low Resistance when Disable
- SOT-23-6,PSOP-8,TQFN9-1.5x1.5 and TDFN6-2x1.8 package.
- Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

Applications

- Notebook PC Applications
- Motherboard Applications
- Low Voltage Logic Supplies
- Microprocessor and Chipset Supplies
- Graphic Cards
- Cordless phones

General Description

The GS7135 can deliver up to 1A of continuous output current with a typical dropout voltage of only 100mV using internal n-channel MOSFETs. The linear regulator uses a separate VDD supply to power the control circuitry and drive the Internal n-channel MOSFETs. The output voltage is adjustable from 0.8V to the voltage that is very close to V_{IN} .

The GS7135 allows the use of low-ESR ceramic capacitor as low as 10 μ F. Moreover the IC provides good performance on both line transient response and load transient response.

The GS7135 provides foldback over current limit and thermal shutdown to prevent the linear regulator from damage. Built-in soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. During start-up, POK remain low until the output reaches 92% of its rating value.

The GS7135 is available in SOT-23-6,PSOP-8, TQFN9-1.5x1.5 and TDFN6-2x1.8 package.

Typical Application

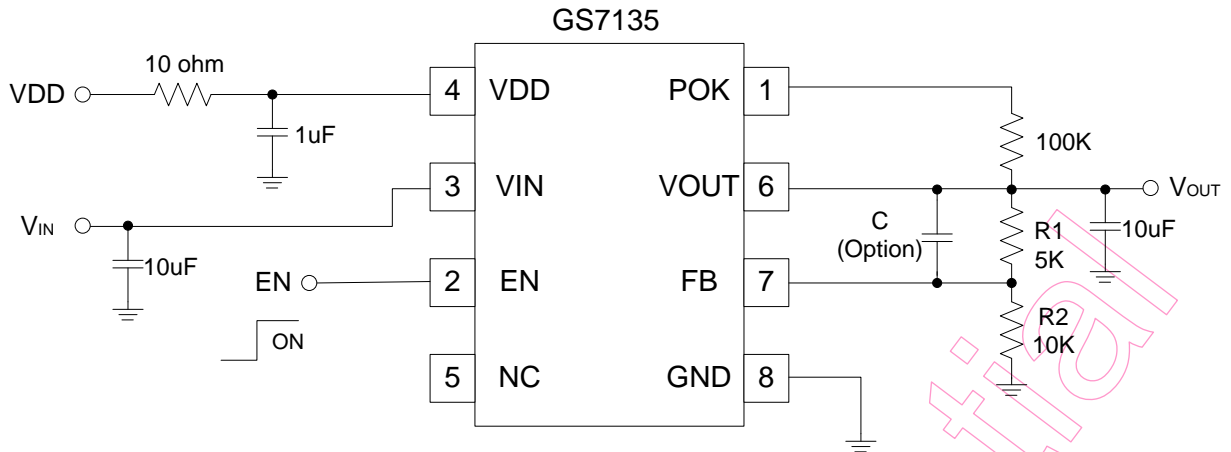


Figure1, Typical Application of GS7135 (PSOP-8 Package)

Function Block Diagram

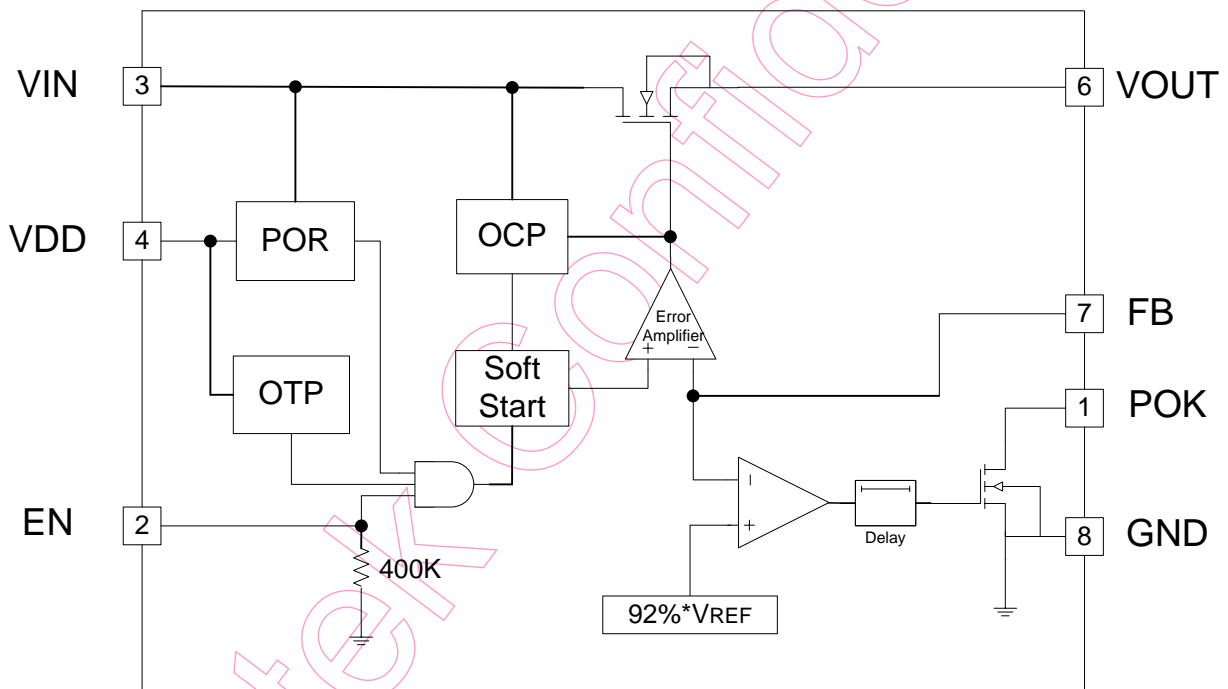


Figure 2 Function Block Diagram (PSOP-8 Package)

Pin Configuration

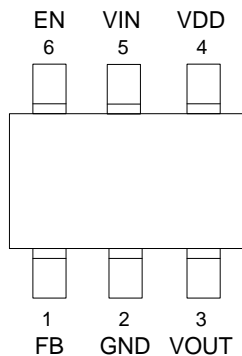


Figure 3a, SOT-23-6(ST) package

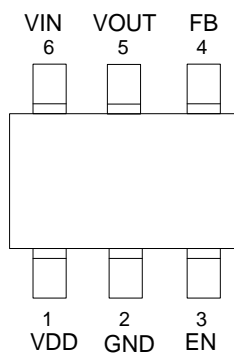


Figure 3b, SOT-23-6(S6) package

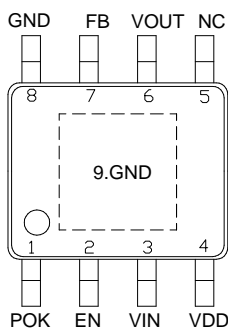


Figure 3c, PSOP-8 package

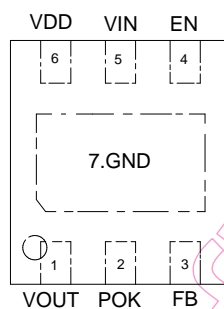


Figure 3d, TDFN6-1.8x2 package

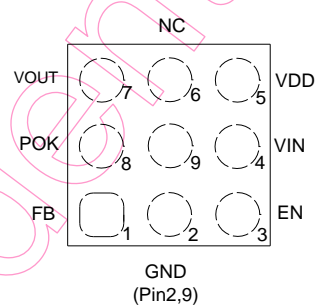


Figure 3e, TQFN9-1.5x1.5 package

Pin Descriptions

Pin No.				Name	I/O type	Pin Function	
PSOP-8	SOT-23-6	TQFN9-1.5x1.5	TDFN6-2x1.8				
2	6	3	3	4	EN	I	Chip Enable (active high). The device will be shutdown if this pin is left open.
3	5	6	4	5	VIN	I	Input Voltage. Large bulk capacitance should be placed closely to this pin. A 10µF ceramic capacitor is recommended at this pin.
4	4	1	5	6	VDD	I	Supply voltage for control circuit. VDD is recommend from 3V to 5V and should be 1.5V higher than the output voltage.
6	3	5	7	1	VOUT	O	Output Voltage. The power output of the device.
7	1	4	1	3	FB	I	Feedback Voltage. This pin is connected to the center tap of an external resistor divider network to set the output voltage as $V_{OUT} = 0.8(R1+R2)/R2$.
8,9	2	2	2,9	7	GND	I	Ground.
1			8	2	POK	O	Open drain output. Setting high impedance once V_{OUT} reaches 92% of its rating voltage
5			6		NC		

Ordering Information

GS7135PP- R

1. Package ← → 2. Shipping

No	Item	Contents
1	Package	ST: SOT-23-6 S6: SOT-23-6 TD: TDFN6-1.8x2 TQ: TQFN9-1.5x1.5 SO: PSOP-8
2	Shipping	R: Tape & Reel

Example: GS7135 PSOP-8 Tape & Reel ordering information is "GS7135SO-R"

Absolute Maximum Rating (Note 1)

Parameter	Symbol	Limits	Units
Supply Voltage	V_{IN}	$1 < V_{IN} < 6$	V
Control Voltage	V_{DD}	$3 < V_{DD} < 6$	V
Output Voltage	V_{OUT}	$0.8 < V_{OUT} < 5$	V
EN, FB, POK		$-0.3 < (V_{EN}, V_{FB}, V_{POK}) < 6$	V
Package Power Dissipation at $T_A \leq 25^\circ\text{C}$	P_{D_PSOP-8}	1333	mW
Package Power Dissipation at $T_A \leq 25^\circ\text{C}$	$P_{D_SOT-23-6}$	420	mW
Package Power Dissipation at $T_A \leq 25^\circ\text{C}$	$P_{D_TDFN6-1.8x2}$	880	mW
Package Power Dissipation at $T_A \leq 25^\circ\text{C}$	$P_{D_TQFN9-1.5x1.5}$	250	mW
Junction Temperature	T_J	- 45 ~ 150	$^\circ\text{C}$
Storage Temperature	T_{STG}	- 65 ~ 150	$^\circ\text{C}$
Lead Temperature (Soldering) 10S	T_{LEAD}	260	$^\circ\text{C}$
ESD (Human Body Mode) (Note 2)	V_{ESD_HBM}	2K	V
ESD (Machine Mode) (Note 2)	V_{ESD_MM}	200	V

Thermal Information (Note 3)

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	θ_{JA_PSOP-8}	75	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$\theta_{JA_SOT-23-6}$	238	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$\theta_{JA_TDFN6-1.8x2}$	114	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient	$\theta_{JA_TQFN9-1.5x1.5}$	400	$^\circ\text{C/W}$

Recommend Operating Condition (Note 4)

Parameter	Symbol	Limits	Units
Supply Voltage	V_{IN}	$1.0 < V_{IN} < \min\{5.2V, V_{DD}\}$	V
Control Voltage (Note 5)	V_{DD}	$3.0 < V_{DD} < 5.5$	V
Junction Temperature	T_J	- 40 ~ 125	°C
Ambient Temperature	T_A	- 40 ~ 85	°C

Electrical Characteristics

($V_{IN} = V_{OUT} + 0.5V$, $V_{EN} = V_{DD} = 5V$, $C_{IN} = C_{OUT} = 10\mu F$, $T_A = T_J = 25^\circ C$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage Section						
V_{DD} Operation Voltage Range	V_{DD}	V_{DD} Input Range, $V_{OUT} = V_{REF}$	3.0		5.5	V
V_{IN} Operation Voltage Range	V_{IN}	V_{IN} Input Range, $V_{OUT} = V_{REF}$	1.0		$\min\{5.2V, V_{DD}\}$	V
Quiescent current	I_Q	$V_{DD} = V_{IN} = V_{EN} = 5V$, $I_{OUT} = 0A$, $V_{OUT} = V_{REF}$		1.0	1.5	mA
V_{DD} Input current	I_{VDD}	$V_{DD} = V_{IN} = V_{EN} = 5V$, $I_{OUT} = 0A$, $V_{OUT} = V_{REF}$		1.0	1.5	mA
Control Input Current in Shutdown	I_{VDD_SD}	$V_{DD} = V_{IN} = 5.0V$, $I_{OUT} = 0A$, $V_{EN} = 0V$		0.1	1	uA
V_{DD} POR Threshold	V_{DDRTH}		2.4	2.7	3	V
V_{DD} POR Hysteresis			0.15	0.2		V
V_{IN} POR Threshold	V_{INRTH}		0.55	0.75	0.95	V
V_{IN} POR Hysteresis			0.13	0.20		V
Output Voltage						
Reference Voltage	V_{REF}	$I_{OUT} = 1mA$, $V_{OUT} = V_{REF}$	0.784	0.8	0.816	V
Output Voltage Accuracy			-2.0		+2.0	%
Line Regulation (V_{DD})	ΔV_{LINE_VDD}	$V_{DD} = 4V$ to $5V$, $I_{OUT} = 1mA$, $V_{OUT} = V_{REF}$, $V_{IN} = 2V$		0.03	0.2	%
Line Regulation (V_{IN})	ΔV_{LINE_IN}	$V_{IN} = 1.2V$ to $5V$, $I_{OUT} = 1mA$, $V_{OUT} = V_{REF}$		0.01	0.1	%
Load Regulation (Note6)	ΔV_{LOAD}	$I_{OUT} = 1mA$ to $1A$, $V_{OUT} = V_{REF}$		0.1	1.5	%
V_{OUT} Pull Low Resistance		$V_{DD} = V_{IN} = 5.0V$, $V_{EN} = 0V$		130		Ω
Dropout Voltage						
Dropout Voltage (Note 7)	V_{DROP}	$V_{OUT} = V_{REF}$, $I_{OUT} = 1A$		100	200	mV

Protection							
Current Limit	ILIM	$V_{DD}=V_{IN}=V_{EN}=5V, V_{OUT}=V_{REF}$		1.8			A
Short Circuit Current	$I_{FOLDBACK}$	$V_{OUT}<0.2V$		30			mA
Thermal Shutdown Temperature	T_{SD}	T_J Rising		160			°C
Thermal Shutdown Returned Temperature				110			°C
Enable							
EN Threshold	Logic-Low Voltage		$V_{DD}=5V$			0.6	V
	Logic-High Voltage		$V_{DD}=5V$	1.2			V
EN Input Bias Current	I_{EN}	$V_{EN}=5V$		12	20		uA
Power OK							
POK Rising Threshold		V_{REF} Rising		92			%
POK Hysteresis		V_{REF} falling		8			%
POK Sink Capability		$I_{PGOOD}=1mA$		0.04	0.1		V
POK Delay		$-40^{\circ}C \sim 125^{\circ}C$		1.7			mS

Note 1. Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at $T_A=25^{\circ}C$ on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for PSOP-8 package.

Note 4. The device is not guaranteed to function outside its operating conditions.

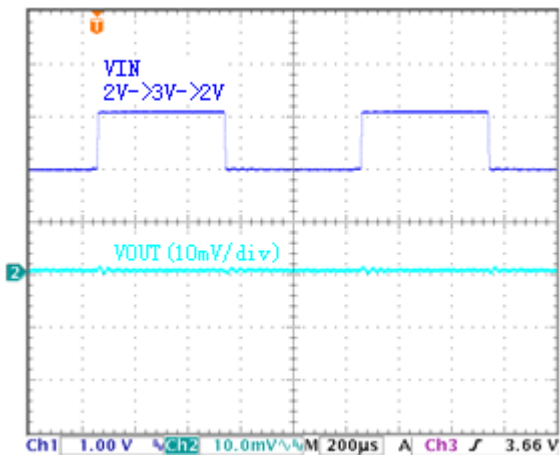
Note 5. V_{DD} should be 1.5V higher than the output voltage, $V_{DD}> 1.5V+V_{out}$

Note 6. Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 1mA to 1A.

Note 7. The Dropout voltage is defined as $V_{IN}-V_{OUT}$, which is measured when V_{OUT} is $0.98*V_{OUT(NORMAL)}$. The dropout voltage is measured at constant junction temperature by using a 2ms current pulse.

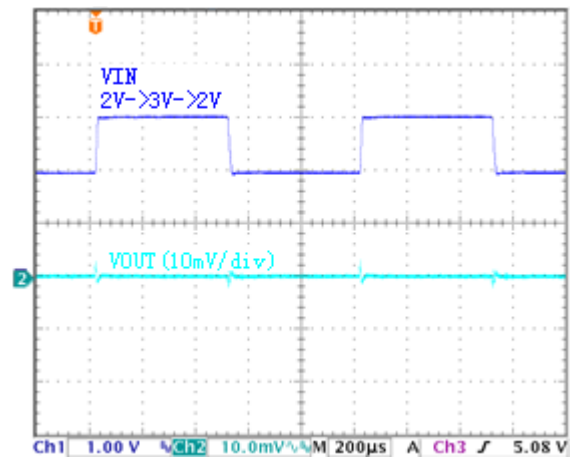
Typical Characteristics

V_{IN} Line Transient Response



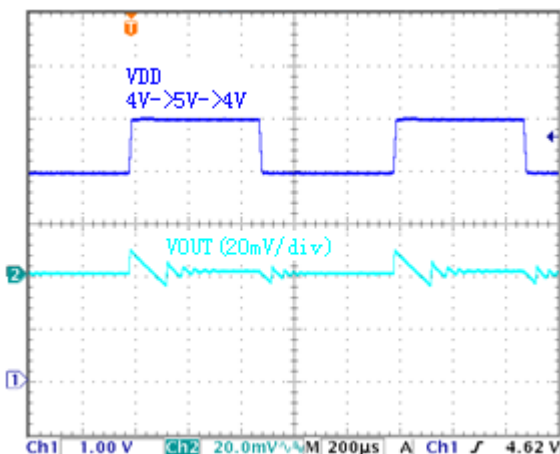
V_{OUT}=1.2V, I_{OUT}=0

V_{IN} Line Transient Response



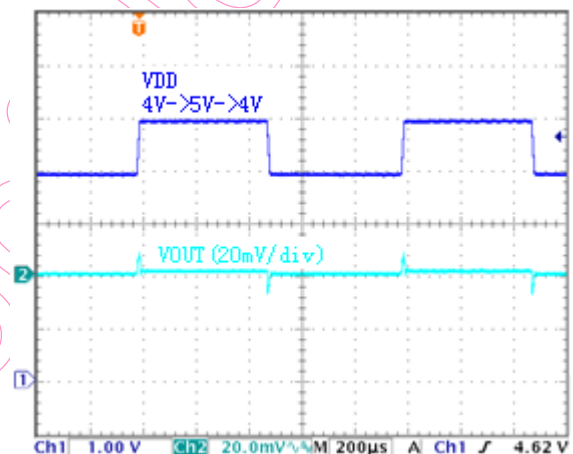
V_{OUT}=1.2V, I_{OUT}=1A

V_{DD} Line Transient Response



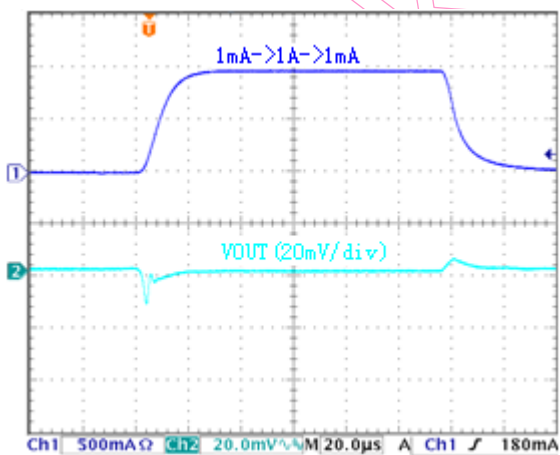
V_{OUT}=1.2V, I_{OUT}=0

V_{DD} Line Transient Response



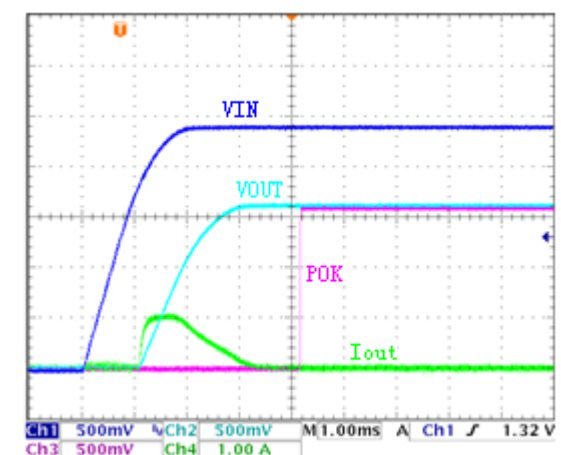
V_{OUT}=1.2V, I_{OUT}=1A

Load Transient Response



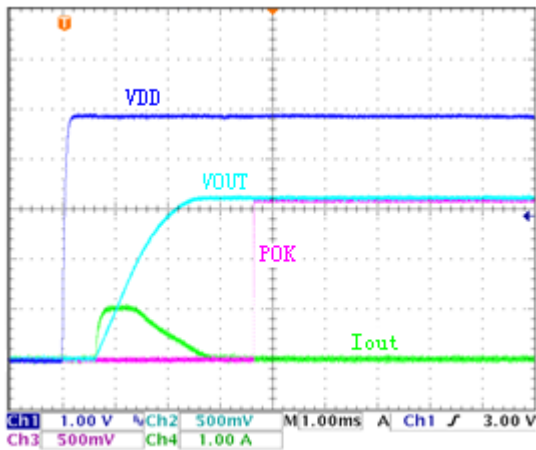
V_{OUT}=1.2V, C_{OUT}=22µF

Power On from VIN



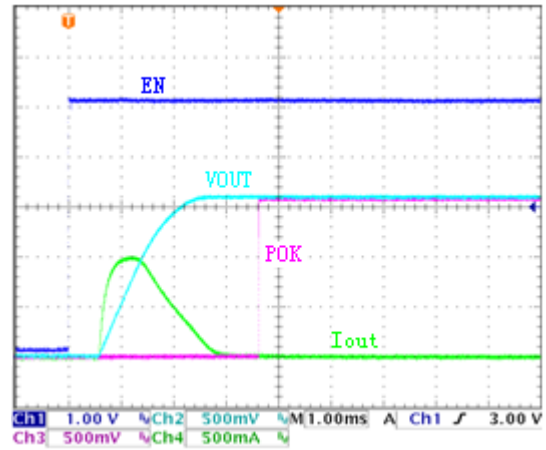
V_{DD}=5V, V_{IN}=2.4V, V_{OUT}=1.6V, C_{OUT}=1000µF, no load

Power On from V_{DD}



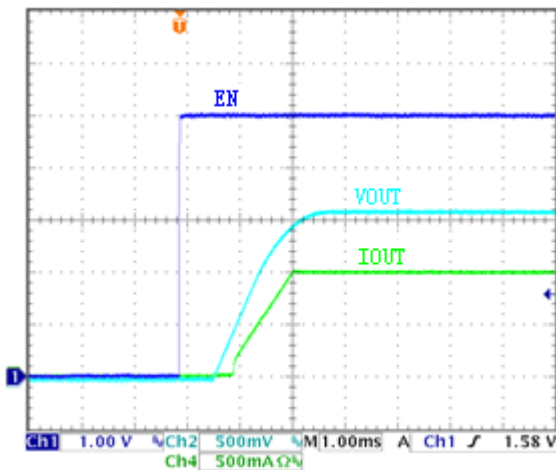
V_{DD}=5V, V_{OUT}=1.6V, C_{OUT}=1000uF, no load

Turn On from EN



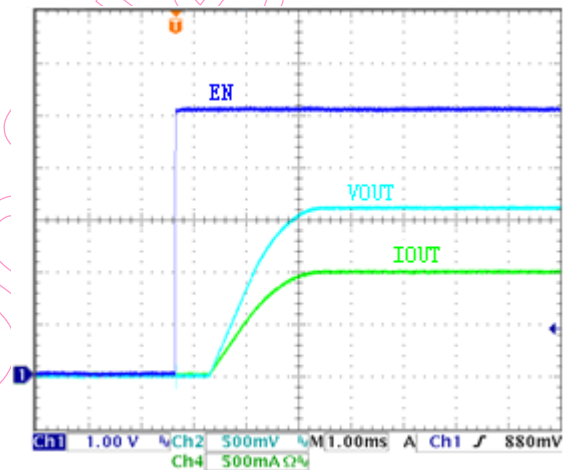
V_{EN}=5V, V_{OUT}=1.6V, C_{OUT}=1000uF, no load

Turn On from EN



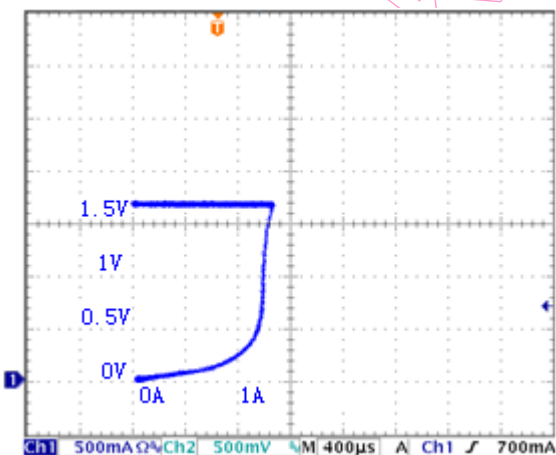
V_{EN}=5V, V_{OUT}=1.6V, C_{OUT}=10uF, I_{load}=1A

Turn On from EN

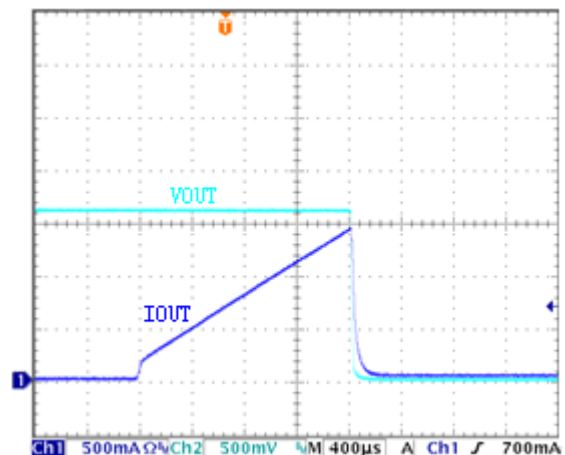


V_{EN}=5V, V_{OUT}=1.6V, C_{OUT}=10uF, R_{load}=0.8

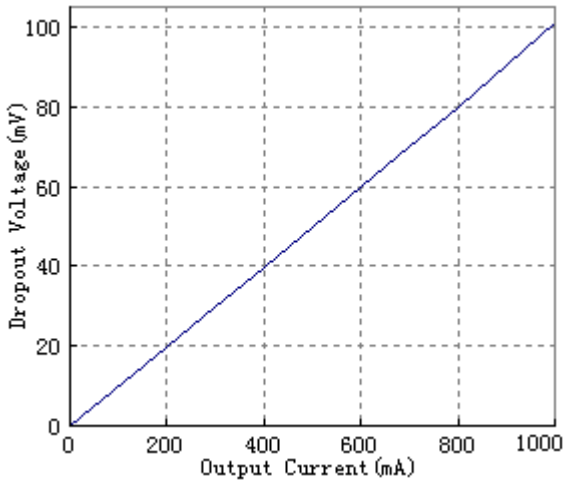
Output Short Current



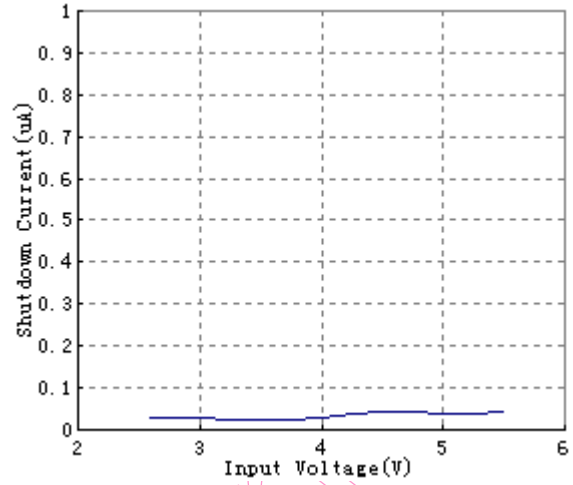
Output Short Current



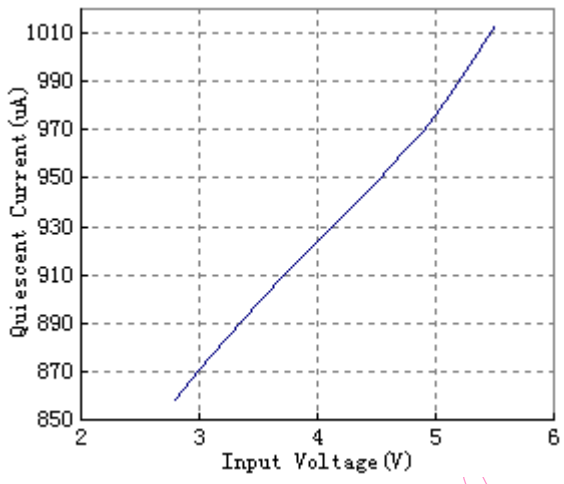
Dropout Voltage vs. Output Current



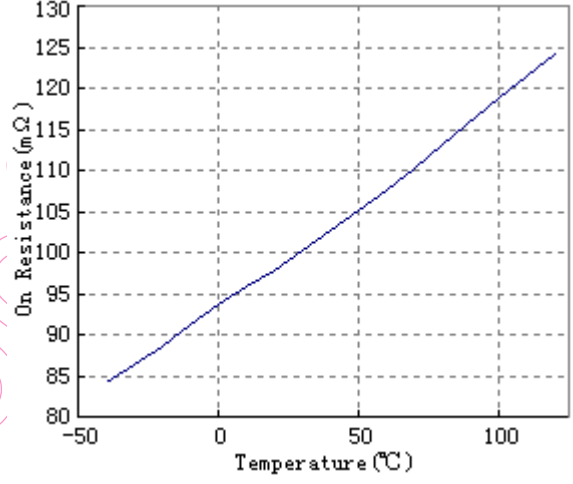
Shutdown Current vs. Input Voltage



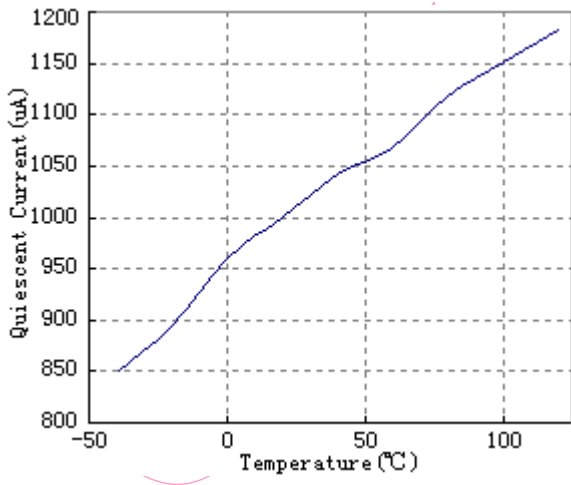
Quiescent Current vs. Input Voltage



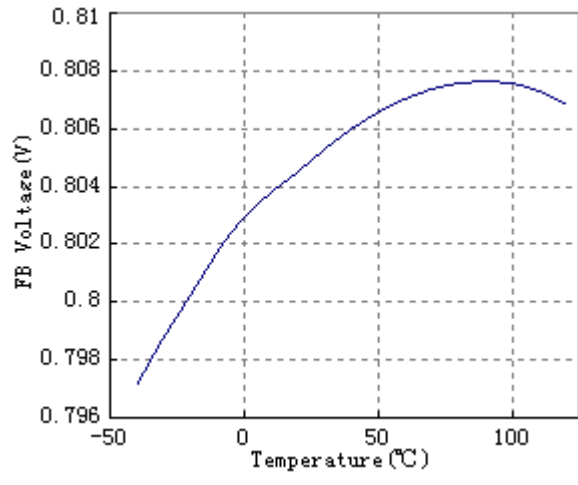
On Resistance vs. Temperature



Quiescent Current vs. Temperature



FB Voltage vs. Temperature



Application Information

Enable

The GS7135 has a dedicated enable pin(EN). When the EN pin is in the logic low ($V_{EN}<0.6V$), the regulator will be turned off, reducing the supply current to less than 1uA.

When the EN pin is in the logic high ($V_{EN}>1.2V$), the regulator will be turned on and undergoes a new soft-start cycle. Left open, the EN pin is pulled down by a internal resistor to shut down the regulator.

Power-on-Reset

The GS7135 features a power-on-reset control through monitor both input voltages to prevent wrong operations. Only after the two supply voltages exceed their rising POR threshold voltages, the regulator is to be initiated and starts up.

POK

The POK pin is an open-drain output, and can be connects to V_{OUT} or other rail through an external pull-up resistor. As the output voltage arrives 92% of normal output voltage, an internal delay function starts to perform a delay time and then output the POK pin high to indicate the output is OK. As the output voltage falls below the falling Power-OK threshold or one of the two supply voltages falls below it's falling POR threshold, the POK pin will output low immediately without a delay time.

Build-In Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 1.5mS.

Current Limit

The GS7135 contains a foldback over current protection function. It allows the output current to

reach the value of 1.8A. Then further decreases in the load resistance reduce both the load current and the load voltage. The main advantage of foldback limiting is less power dissipation in the pass transistor under shorted-load conditions. During startup, the current limit value is set to a high value, thus GS7135 can operate in full load condition. After startup, the current limit value is set to a normal value, so the pass transistor can be protected well.

Thermal-Shutdown Protection

Thermal Shutdown protects GS7135 from excessive power dissipation. If the die temperature exceeds 160°C, the pass transistor is shut off. 50°C of hysteresis prevents the regulator from turning on until the die temperature drops to 110°C.

Output Capacitor selection

The GS7135 is specifically designed to employ ceramic output capacitors as low as 10uF. Place the capacitors physically as close as possible to the device with wide and direct PCB traces. Capacitor ESR should be less than 50mohm.

Feedback Network

Figure 4 shows the feedback network. The suggested design procedure is to choose $R1=10K\Omega$ and then calculate $R2$ using the following formula: $R1=(V_{OUT}/V_{REF}-1)*R2$.

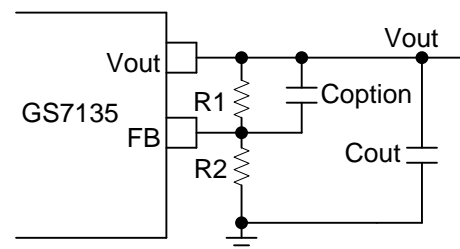


Figure 4 Feedback Network

C_{OPTION} can improve transient response, and recommend value as follow:

V _{OUT}	R1	C _{OPTION}
0.8V ~ 1.6V	0 ~ 10 KΩ	470pF~1nF
1.6V ~ 2.4V	10 KΩ ~ 20 KΩ	100pF~500pF
2.4V ~ 3.6V	20 KΩ ~ 30 KΩ	20pF~300pF

Input Capacitor selection

Bypass VIN to ground with a 10uF or greater capacitor. Bypass VDD to ground with a 1uF capacitor for normal operation in most applications. Ceramic, tantalum or aluminum electrolytic capacitors may be selected for input capacitor. However ceramic capacitors are recommended due to their significant cost and space savings. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

Power Dissipation and Layout Considerations

Although internal thermal limiting function is integrated in GS7135, continuously keeping the junction near the thermal shutdown temperature may possibly affect device reliability. For continuous operation, it is highly recommended to keep the junction temperature below the maximum operation junction temperature 125°C for maximum reliability.

The power dissipation definition in device is:

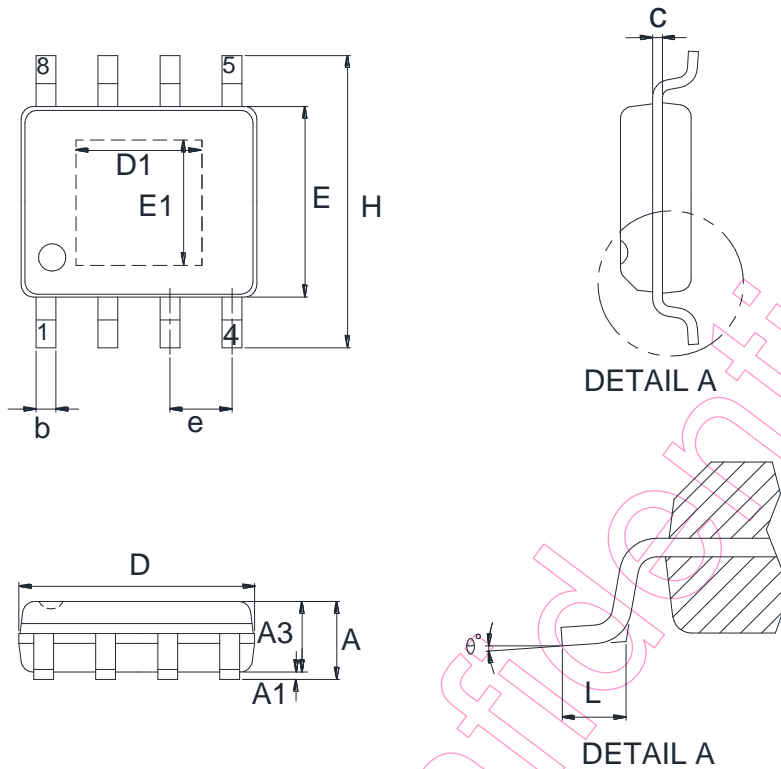
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{DD} \times I_Q$$

The maximum power dissipation can be calculated as:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where T_{J(MAX)} is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

Package Dimensions, PSOP-8(B)

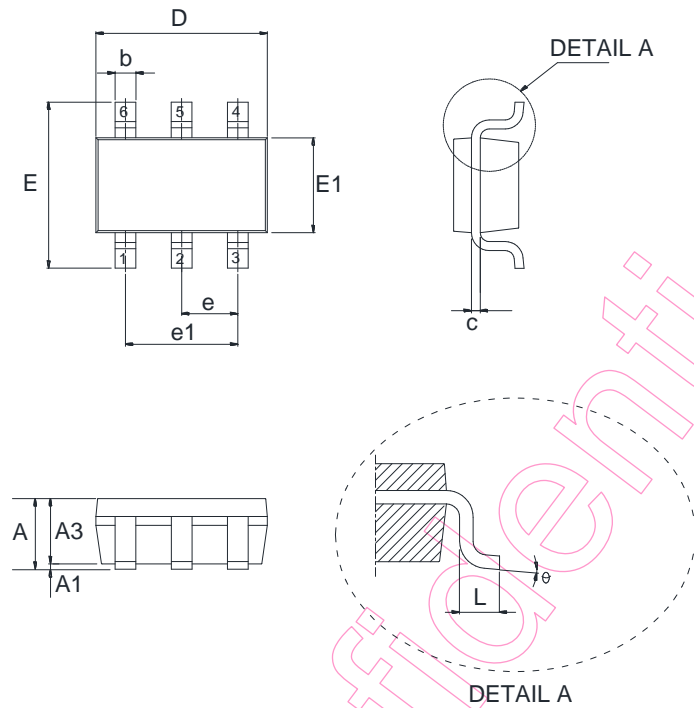


Symbol	Dimensions in Millimeters	
	Min.	Max.
A	1.30	1.80
A1	-	0.15
A3	1.25	-
b	0.31	0.51
c	0.17	0.25
e	1.27 REF.	
D	4.70	5.10
E	3.80	4.00
D1	3.1 REF.	
E1	2.3 REF.	
H	5.80	6.20
L	0.40	1.27
θ	0°	8°

Note:

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, SOT-23-6

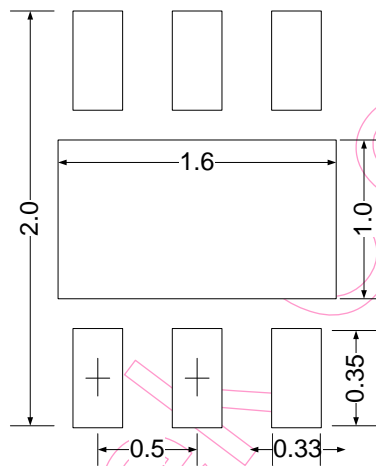
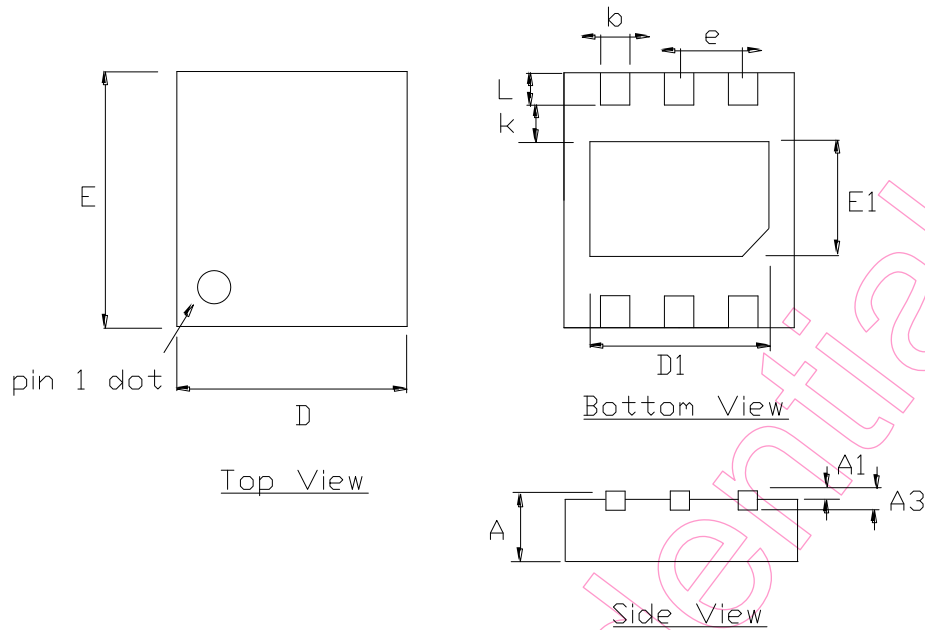


Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
A3	0.90	1.30
b	0.30	0.50
c	0.08	0.25
e	0.95 REF.	
e1	1.90 REF.	
D	2.90 REF.	
E	2.80 REF.	
E1	1.60 REF.	
L	0.30	0.60
θ	0°	8°

Note

- 1.Min.: Minimum dimension specified.
- 2.Max.: Maximum dimension specified.
- 3.REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, TDFN6-1.8x2



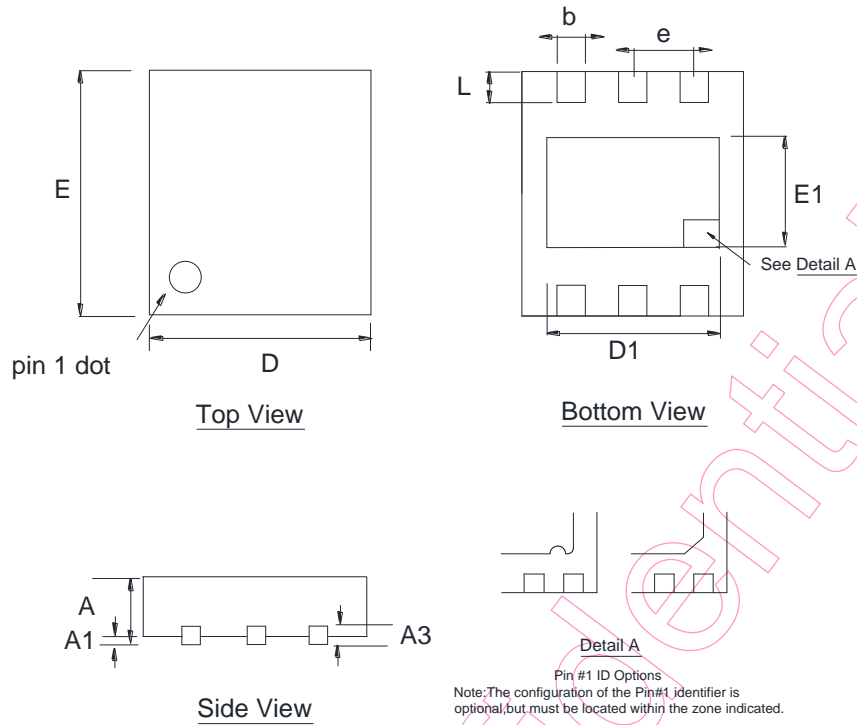
Unit: mm

Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.45	0.55
A1	0.00	0.05
A3	0.15 REF.	
D	1.72	1.88
D1	1.30	1.50
E	1.92	2.08
E1	0.80	1.00
k	0.20 Min.	
b	0.18	0.30
e	0.50 REF.	
L	0.17	0.33

Note

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, TDFN6-1.8x2

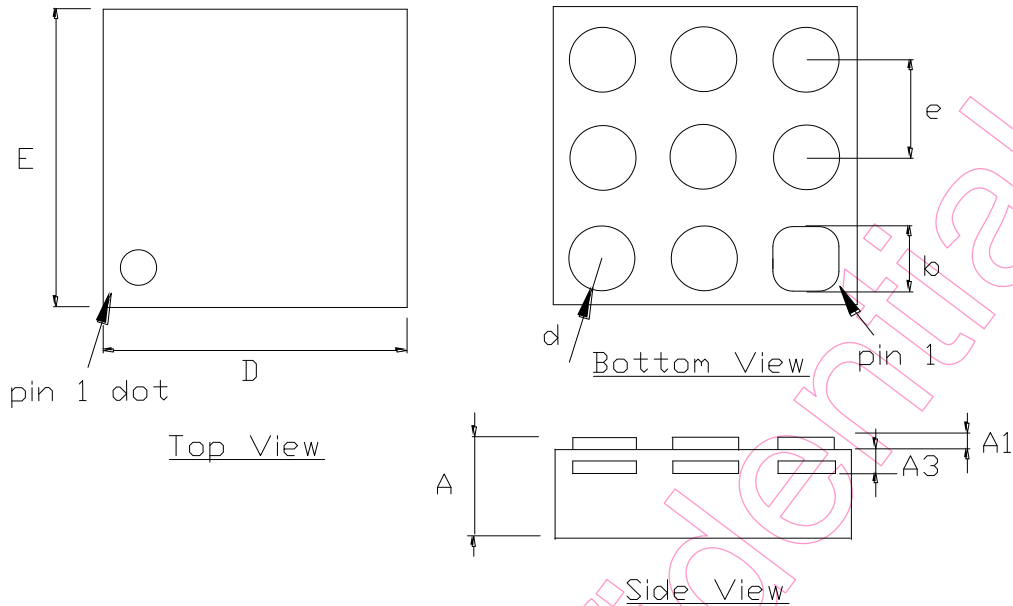


Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.45	0.60
A1	0.00	0.05
A3	0.15 REF.	
b	0.15	0.28
e	0.50 REF.	
D	1.70	1.90
E	1.90	2.10
D1	1.45 REF.	
E1	0.95 REF.	
L	0.17	0.33

Note:

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, TQFN9-1.5x1.5



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.45	0.55
A1	0.00	0.05
A3	0.15 REF.	
D	1.42	1.58
E	1.42	1.58
b	0.17	0.33
e	0.50 REF.	
d	0.17	0.33

Note

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

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