

### Features

- Maximum 3A Low-Dropout Voltage Regulator
- Ultra Low Dropout Voltage  
Typically 170mV at 3A Output Current
- High Output Accuracy over Line, Load and Temperature
- Build-In Soft-Start
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Power-OK Output function
- Low ESR Output Capacitor(Multi-layer Chip Capacitors (MLCC)) Applicable
- Vout Pull Low Resistance when Disable
- TDFN10-3x3 package.
- Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

### Applications

- Notebook PC Applications
- Motherboard Applications
- Low Voltage Logic Supplies
- Microprocessor and Chipset Supplies
- Graphic Cards
- Cordless phones

### General Description

The GS7163 can deliver up to 3A of continuous output current with a typical dropout voltage of only 170mV using internal n-channel MOSFETs. The linear regulator uses a separate VCNTL supply to power the control circuitry and drive the internal n-channel MOSFETs. The output voltage is adjustable from 1.05V to the voltage that is very close to VIN.

The GS7163 allows the use of low-ESR ceramic capacitor as low as 10uF. Moreover the IC provides good performance on both line transient response and load transient response.

The GS7163 provides current limit, short current protection and thermal shutdown to prevent the linear regulator from damage. Built-in soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. During start-up, POK remain low until the output reaches 92% of its rating value.

The GS7163 is available in TDFN10-3x3 package.

**Typical Application**

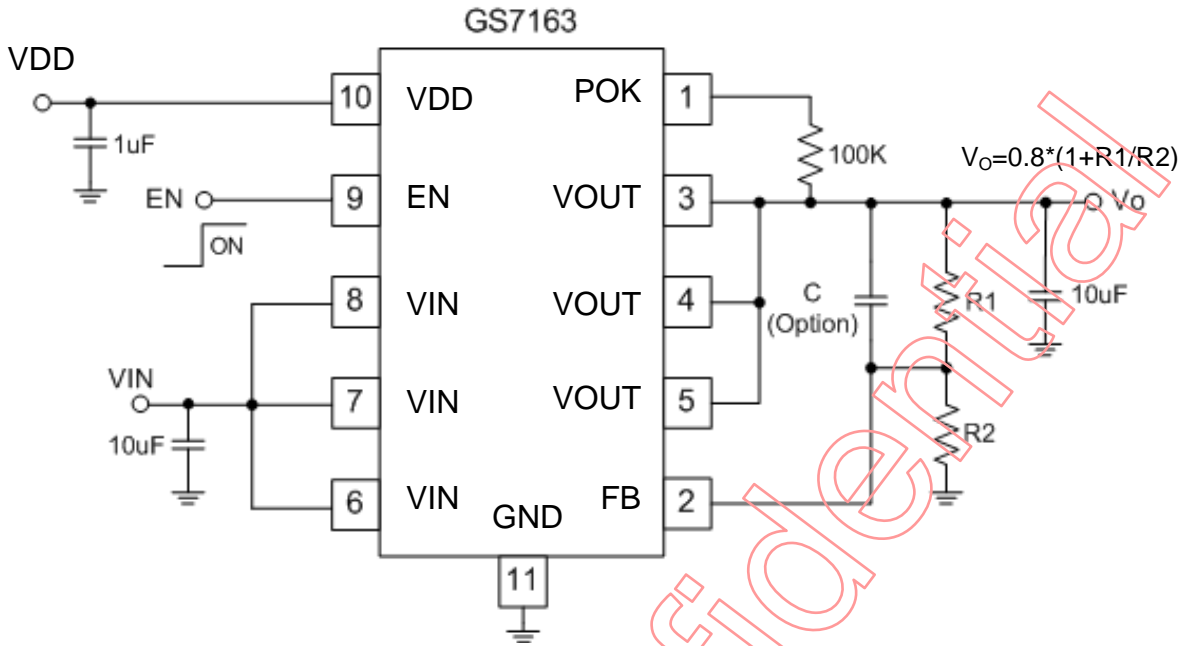


Figure 1 Typical Application of GS7163

**Function Block Diagram**

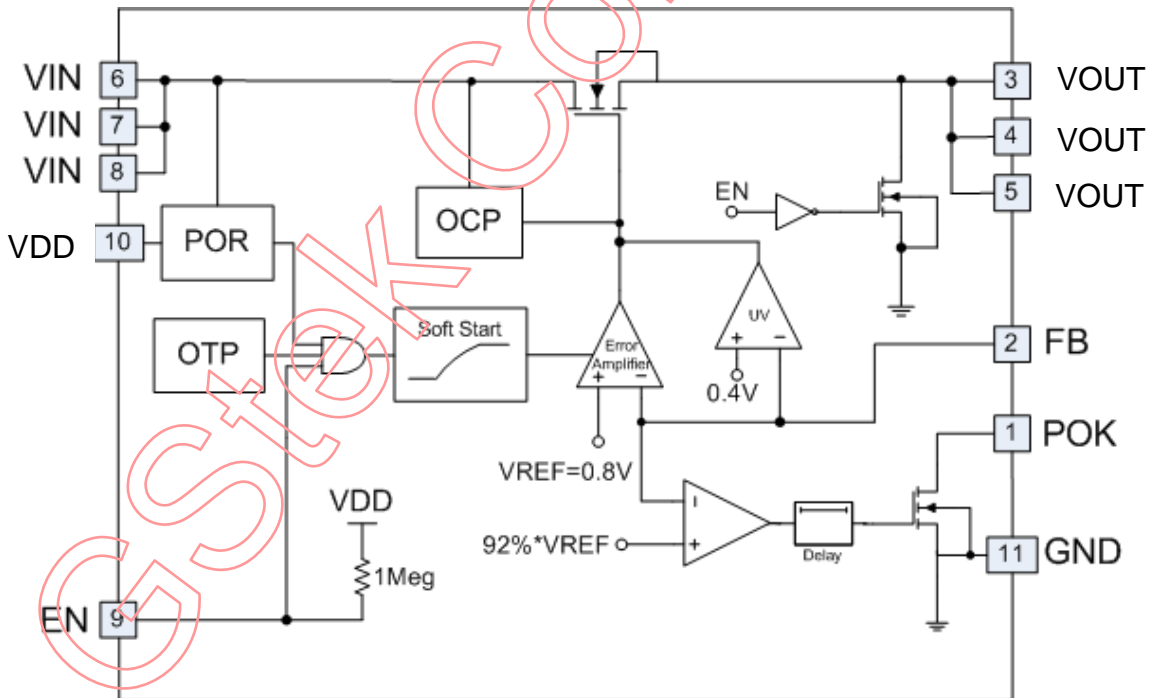
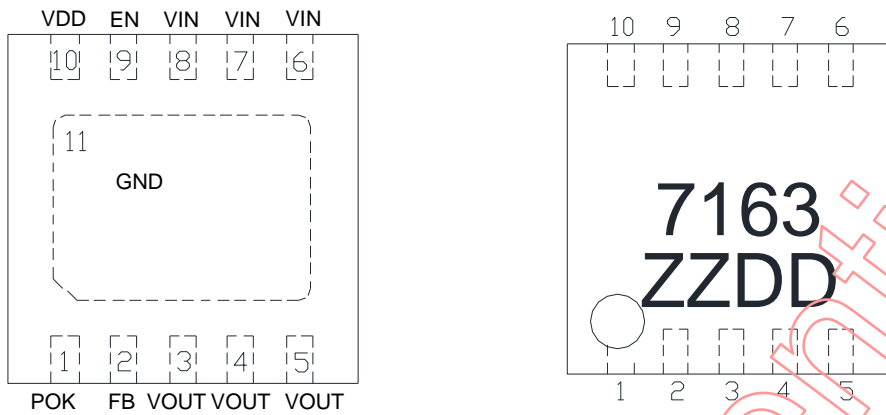


Figure 2 Function Block Diagram

**Pin Configuration**



TDFN10-3x3  
( Top view)

**Pin Descriptions**

Pin No.	Name	I/O type	Pin Function
TDFN10-3x3			
1	POK	O	Open drain output. Setting high impedance once $V_{OUT}$ reaches 92% of its rating voltage
2	FB	I	Feedback Voltage. This pin is connected to the center tap of an external resistor divider network to set the output voltage as $V_{OUT} = 0.8(R1+R2)/R2$ .
3, 4, 5	VOUT	O	Output Voltage. The power output of the device.
6, 7, 8	VIN	I	Input Voltage. Large bulk capacitance should be placed closely to this pin. A 10 $\mu$ F ceramic capacitor is recommended at this pin.
9	EN	I	Chip Enable (active high). This pin is internal pull high to VDD. The device will be shutdown if this pin is pull low.
10	VDD	I	Supply voltage for control circuit. This pin provides bias voltage to the control circuit and driver for the pass transistor. For better current capability, A 3V to 5V supply voltage for control circuit is recommended and supply voltage should be 1.5V higher than the output voltage.
11	GND	I/O	Ground.

**Ordering Information**

**GS7163PP-R**

1. Package ← → 2. Shipping

No	Item	Contents
1	Package	TD:TDFN10-3x3
2	Shipping	R: Tape & Reel

Example: GS7163 TDFN10-3x3 Tape & Reel ordering information is “GS7163TD-R”

**Absolute Maximum Rating (Note 1)**

Parameter	Symbol	Limits	Units
Supply Voltage	V <sub>IN</sub>	1 < V <sub>IN</sub> < 6	V
Control Voltage	V <sub>CNTL</sub>	3 < V <sub>CNTL</sub> < 6	V
Output Voltage	V <sub>O</sub>	0.8 < V <sub>O</sub> < 5	V
Package Power Dissipation at T <sub>A</sub> ≤ 25°C	P <sub>D,TDFN10-3x3</sub>	1670	mW
Junction Temperature	T <sub>J</sub>	- 45 ~ 150	°C
Storage Temperature	T <sub>STG</sub>	- 65 ~ 150	°C
Lead Temperature (Soldering) 10S	T <sub>LEAD</sub>	260	°C
ESD (Human Body Mode) (Note 2)	V <sub>ESD_HBM</sub>	2K	V
ESD (Machine Mode) (Note 2)	V <sub>ESD_MM</sub>	200	V

**Thermal Information (Note 3)**

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	θ <sub>JA,TDFN10-3x3</sub>	60	°C/W
Thermal Resistance Junction to Case	θ <sub>JC,TDFN10-3x3</sub>	5	°C/W

**Recommend Operating Condition (Note 4)**

Parameter	Symbol	Limits	Units
Supply Voltage	V <sub>IN</sub>	1.05 < V <sub>IN</sub> < Min{V <sub>CNTL</sub> +0.3V,5.5}	V
Control Voltage	V <sub>DD</sub>	3.0 < V <sub>CNTL</sub> < 5.5	V
Junction Temperature	T <sub>J</sub>	- 40 ~ 125	°C
Ambient Temperature	T <sub>A</sub>	-40 ~ 85	°C

**Electrical Characteristics**

( $V_{IN} = V_O + 0.5V$ ,  $V_{EN} = V_{CNTL} = 5V$ ,  $C_{IN} = C_O = 10\mu F$ ,  $T_A = T_J = 25^\circ C$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
<b>Supply Voltage Section</b>						
$V_{CNTL}$ Operation Voltage Range	$V_{CNTL}$	$V_{CNTL}$ Input Range, $V_O = V_{REF}$	3.0		5.5	V
$V_{IN}$ Operation Voltage Range	$V_{IN}$	$V_{IN}$ Input Range, $V_O = V_{REF}$	1.05		Min{ $V_{CNTL} + 0.3V, 5.5$ }	V
$V_{CNTL}$ Input current	$I_{CNTL}$	$V_{CNTL} = V_{IN} = V_{EN} = 5V$ , $I_O = 0A$ , $V_O = V_{REF}$		1.0	1.5	mA
Control Input Current in Shutdown	$I_{SD}$	$V_{CNTL} = V_{IN} = 5.0V$ , $I_O = 0A$ , $V_{EN} = 0V$		0.1	30	$\mu A$
$V_{CNTL}$ POR Threshold	$V_{CNTLTH}$		2.5	2.7	2.9	V
$V_{CNTL}$ POR Hysteresis				0.4		V
$V_{IN}$ POR Threshold	$V_{INTH}$		0.8	0.9	1.0	V
$V_{IN}$ POR Hysteresis			0.2	0.35	0.5	V
$V_{IN}$ POR Falling Delay Time				100		$\mu s$
<b>Output Voltage</b>						
Reference Voltage	$V_{REF}$	$V_{CNTL} = V_{IN} = V_{EN} = 5V$ , $I_O = 1mA$	0.792	0.8	0.808	V
Line Regulation ( $V_{CNTL}$ )	$\Delta V_{LINE\_CNTL}$	$V_{CNTL} = 4V$ to $5V$ , $I_O = 1mA$ , $V_O = V_{REF}$ , $V_{IN} = 2V$		0.03	0.2	%
Line Regulation ( $V_{IN}$ )	$\Delta V_{LINE\_IN}$	$V_{IN} = 1.2V$ to $5V$ , $I_O = 1mA$ , $V_O = V_{REF}$		0.01	0.1	%
Load Regulation (Note 5)	$\Delta V_{LOAD}$	$V_{CNTL} = V_{EN} = 5V$ , $V_{IN} = 2V$ , $I_O = 1mA$ to $3A$ , $V_O = V_{REF}$		0.1	1.5	%
$V_O$ Pull Low Resistance		$V_{CNTL} = V_{IN} = 5.0V$ , $V_{EN} = 0V$		100	150	$\Omega$
<b>Dropout Voltage</b>						
Dropout Voltage (Note 6)	$V_{DROP}$	$V_{CNTL} = 5V$ , $V_O = 1.2V$ , $I_O = 2A$		110	170	mV
		$V_{CNTL} = 5V$ , $V_O = 1.2V$ , $I_O = 3A$		170	250	mV
<b>Protection</b>						
Current Limit (OCP)	$I_{LIM}$	$V_{CNTL} = V_{IN} = V_{EN} = 5V$ , $V_O = V_{REF}$		4.5	6	A
OCP trip mode		OCP Re-try, ON:OFF=1:5		1:5		
$V_{FB}$ Under Voltage Threshold	$UVP_{FB}$	$V_{FB}$ Falling		0.4		V
Thermal Shutdown Temperature	$T_{SD}$	$T_J$ Rising		160		$^\circ C$

Thermal Shutdown Hysteresis					40		°C
<b>Enable</b>							
EN Threshold	Logic-Low Voltage		$V_{CNTL}=5V$			0.3	V
	Logic-High Voltage		$V_{CNTL}=5V$	1.1			V
EN Internal Impedance			EN to $V_{CNTL}$ Impedance	0.5	1		MegΩ
EN Input Bias Current		$I_{EN}$	$V_{EN}=0V$		5	10	uA
Soft Start Time		$T_{SS}$	From 10%*Vo to 90%*Vo	0.6	1	2	mS
<b>Power OK</b>							
POK Threshold Voltage for Power OK		$V_{POK}$	$V_{FB}$ Rising	90	92	94	%
POK Threshold Voltage for Power NOT OK		$V_{PNOK}$	$V_{FB}$ falling	80	82	84	%
POK Sink Capability			$I_{POK}=5mA$			0.4	V
POK Delay time		$T_{DELAY}$		1	2	4	mS

**Note 1.** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.**  $\theta_{JA}$  is measured in the natural convection at  $T_A=25^\circ C$  on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard. The case point of  $\theta_{JC}$  is on the expose pad for PSOP-8 package.

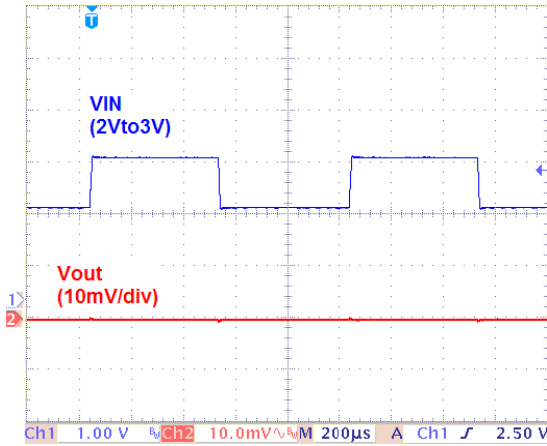
**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 1mA to 3A.

**Note 6.** The Dropout voltage is defined as  $V_{IN}-V_{OUT}$ , which is measured when  $V_{OUT}$  is  $0.98*V_{OUT(NORMAL)}$ . The Dropout voltage is measured at constant junction temperature by using a 2ms current pulse.

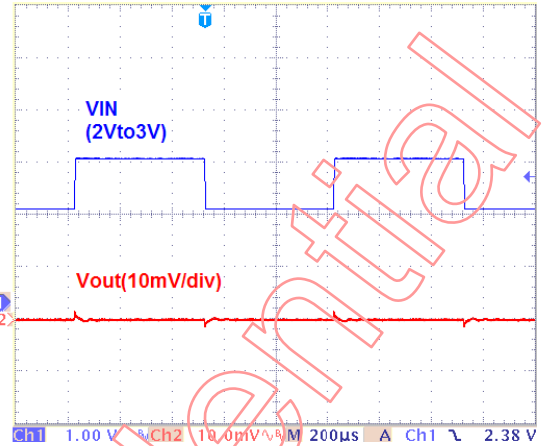
Typical Characteristics

V<sub>IN</sub> Line Transient Response



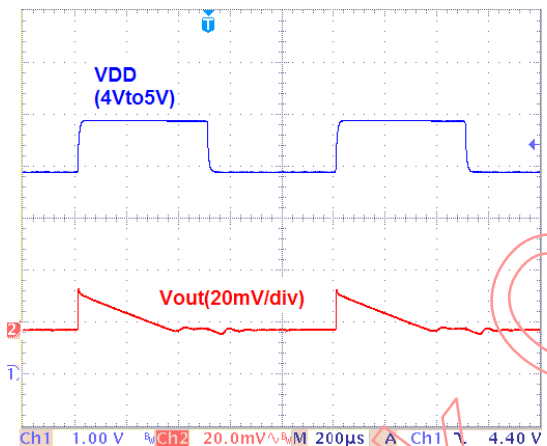
V<sub>O</sub>=1.2V, I<sub>OUT</sub>=0

V<sub>IN</sub> Line Transient Response



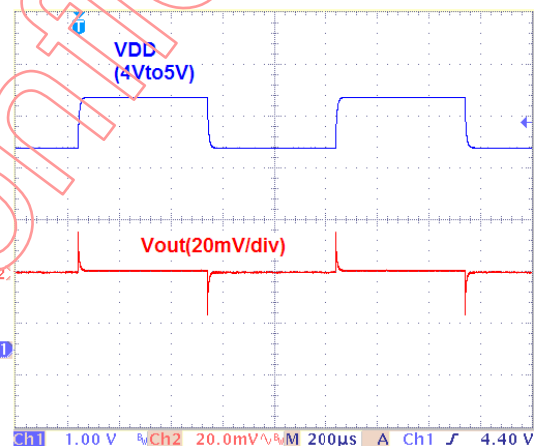
V<sub>O</sub>=1.2V, I<sub>OUT</sub>=1A

V<sub>CNTL</sub> Line Transient Response



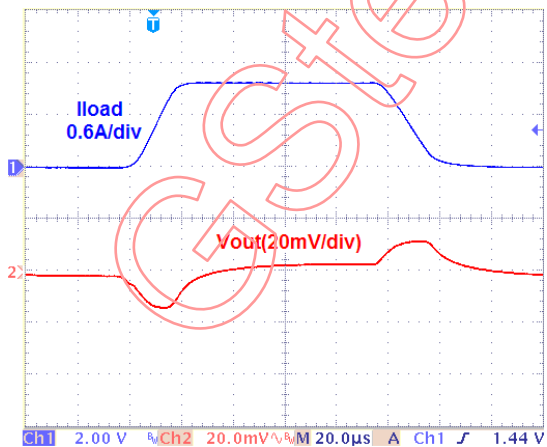
V<sub>O</sub>=1.2V, I<sub>OUT</sub>=0

V<sub>CNTL</sub> Line Transient Response



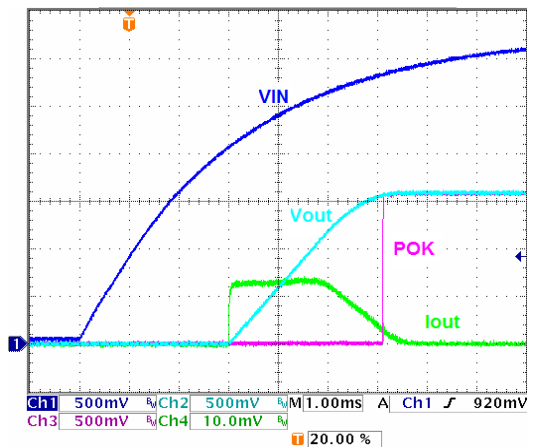
V<sub>O</sub>=1.2V, I<sub>OUT</sub>=1A

Load Transient Response



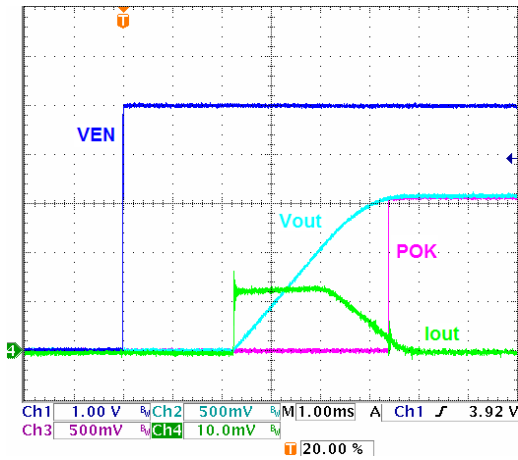
V<sub>O</sub>=1.2V, C<sub>OUT</sub>=22uF

Power On from V<sub>IN</sub>



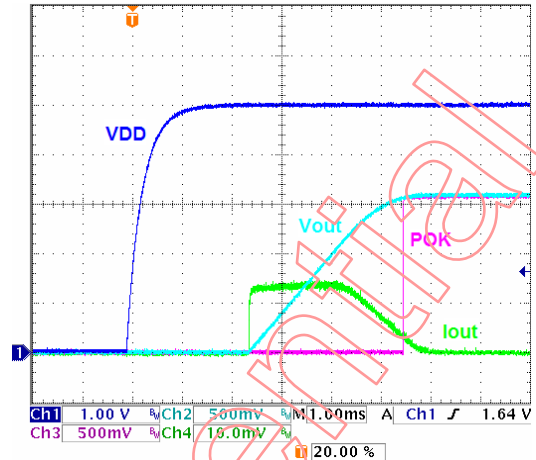
V<sub>CNTL</sub>=5V, V<sub>IN</sub>=3.3V, V<sub>O</sub>=1.6V, C<sub>O</sub>=2200uF, no load

**Turn On from EN**



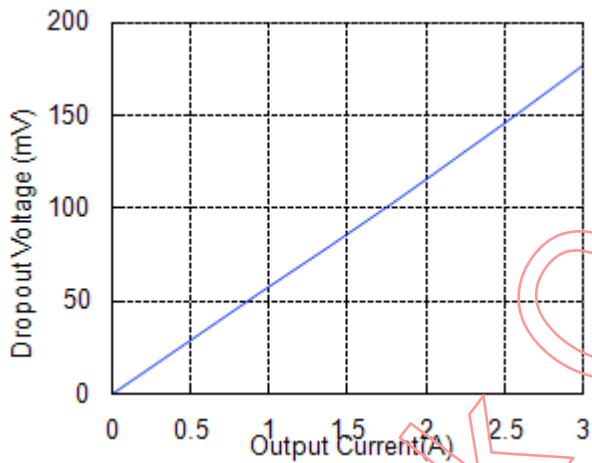
$V_{EN}=5V, V_O=1.6V, C_O=2200\mu F, \text{no load}$

**Power On from  $V_{CNTL}$**

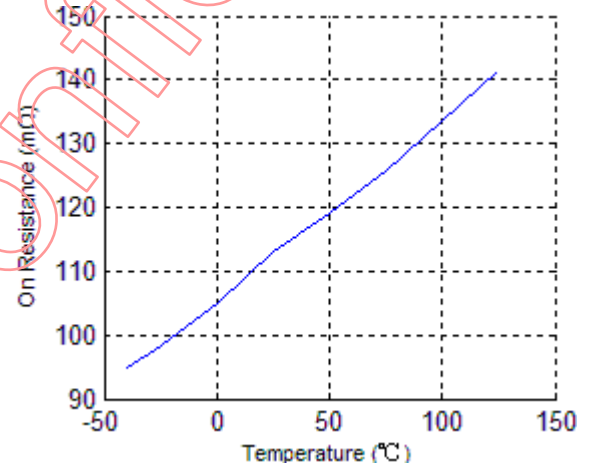


$V_{CNTL}=5V, V_{IN}=3.3V, V_O=1.6V, C_O=2200\mu F, \text{no load}$

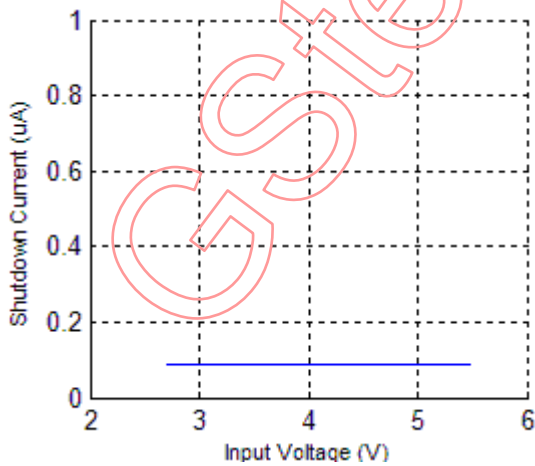
**Dropout Voltage vs. Output Current**



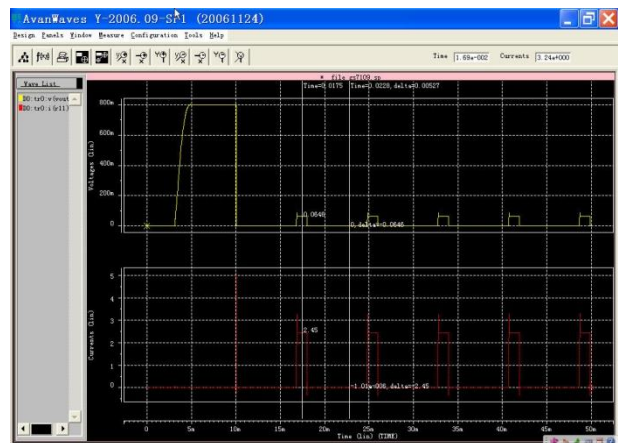
**On Resistance vs. Temperature**



**Shutdown Current vs. Input Voltage**

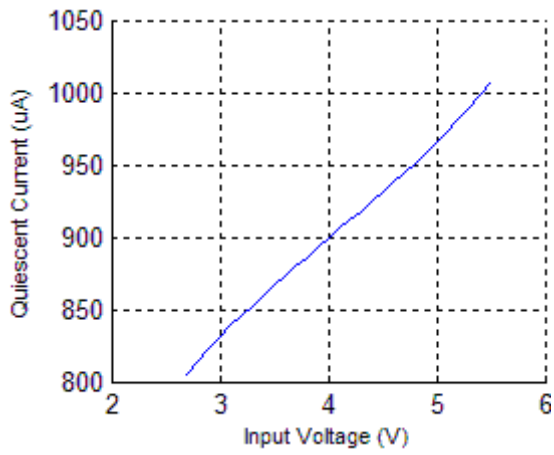


**Output Short Current**

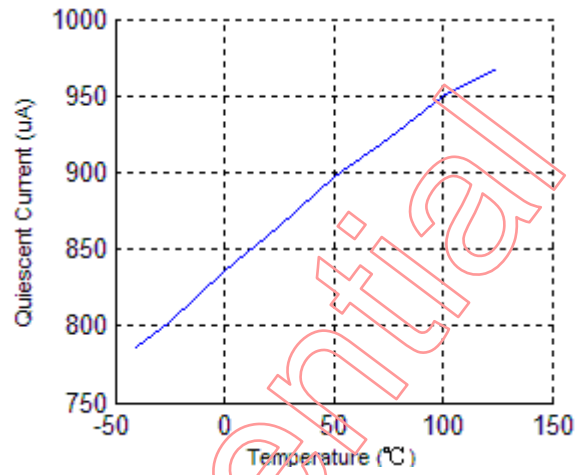




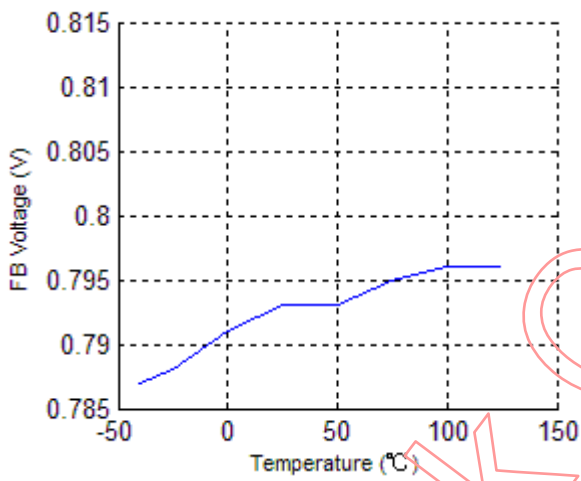
### Quiescent Current vs. Input Voltage



### Quiescent Current vs. Temperature



### FB Voltage vs. Temperature



## Application Information

### Enable

The GS7163 has a dedicated enable pin(EN). When the EN pin is in the logic low ( $V_{EN} < 0.3V$ ), the regulator will be turned off, reducing the supply current to less than 1uA.

When the EN pin is in the logic high ( $V_{EN} > 1.1V$ ), the regulator will be turned on and undergoes a new soft-start cycle. Left open, the EN pin is pulled up by an internal resistor to turn on the regulator.

### Power-on-Reset

The GS7163 features a power-on-reset control through monitor both input voltages to prevent wrong operations. Only after the two supply voltages exceed their rising POR threshold voltages, the regulator is to be initiated and starts up.

### POK

The POK pin is an open-drain output, and can be connects to  $V_{OUT}$  or other rail through an external pull-up resistor. As the output voltage arrives 92% of normal output voltage, an internal delay function starts to perform a delay time and then output the POK pin high to indicate the output is OK. As the output voltage falls below the falling Power-OK threshold or one of the two supply voltages falls below it's falling POR threshold, the POK pin will output low immediately without a delay time.

### Build-In Soft-Start

An internal soft-start function controls rise rate of the output voltage to limit the current surge at start-up. The typical soft-start interval is about 1mS.

### Current Limit

The GS7163 contains over current protection

function. It allows the output current to reach the maximum value of 4.5A. Then further decreases in the load resistance reduce both the load current and the load voltage.

### Thermal-Shutdown Protection

Thermal Shutdown protects GS7163 from excessive power dissipation. If the die temperature exceeds 160°C, the pass transistor is shut off. 40°C of hysteresis prevents the regulator from turning on until the die temperature drops to 120°C.

### Output Capacitor selection

The GS7163 is designed to employ ceramic output capacitors as low as 10uF; if employ EL output capacitor as large as 1000uF, feedback resistance ( $R_{bottom}$ ) should be larger than 100K ohm(Table 1). Place the capacitors physically as close as possible to the device with wide and direct PCB traces. Capacitor ESR should be less than 50mohm.

	Cout	Rbottom
Ceramic	$\geq 10\mu F$	$\geq 0.1K \Omega$
EL	1000uF	$\geq 100K \Omega$

Table 1 Cout capacitor vs. Rbottom resistance

### Input Capacitor selection

Bypass VIN to ground with a 10uF or greater capacitor. Bypass VCNTL to ground with a 1uF capacitor for normal operation in most applications. Ceramic, tantalum or aluminum electrolytic capacitors may be selected for input capacitor. However ceramic capacitors are recommended due to their significant cost and space savings. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

**Power Dissipation and Layout Considerations**

Although internal thermal limiting function is integrated in GS7163, continuously keeping the junction near the thermal shutdown temperature may possibly affect device reliability. For continuous operation, it is highly recommended to keep the junction temperature below the maximum operation junction temperature 125°C for maximum reliability.

The power dissipation definition in device is:

$$P_D = (V_{IN} - V_O) \times I_O + VCNTL \times I_Q$$

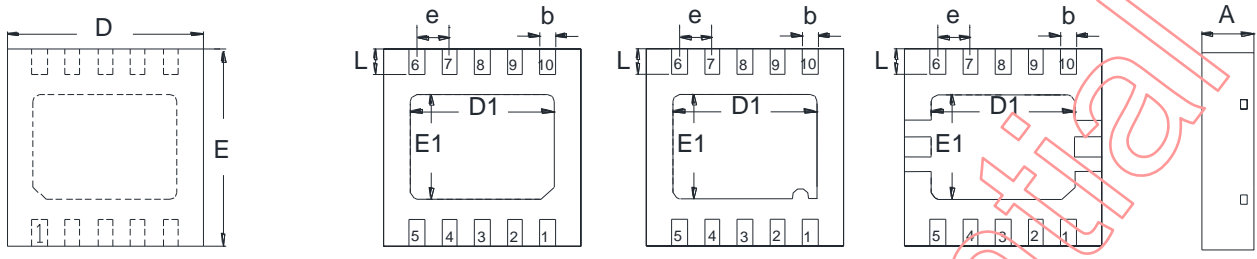
The maximum power dissipation can be calculated as:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where  $T_{J(MAX)}$  is the maximum operation junction temperature 125°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance.

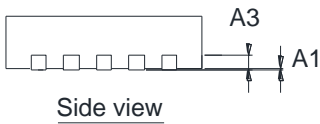
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Package Dimensions, TDFN10-3x3



Top view

Bottom view



Side view

Pin #1 ID Options

Note: The configuration of the Pin#1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.70	0.80
A1	0.00	0.05
A3	0.203 REF.	
b	0.18	0.30
e	0.50 REF.	
D	2.90	3.10
E	2.90	3.10
D1	2.30 REF.	
E1	1.65 REF.	
L	0.30	0.50

Note:

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

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