BGA
Commercial Temp
Industrial Temp

256K x 32
8Mb Asynchronous SRAM

10, 12, 15ns
3.3V V_{DD}

Features

- Fast access time: 10, 12, 15ns.
- CMOS low power operation: 340/290/260/220mA at min. cycle time.
- Single 3.3V ± 0.3V power supply.
- All inputs and outputs are TTL compatible.
- Byte control.
- Fully static operation.
- Industrial Temperature Option: -40° to 85°C.
- 14mm x 22mm, 119 Bump, 1.27mm Pitch Ball Grid Array package.

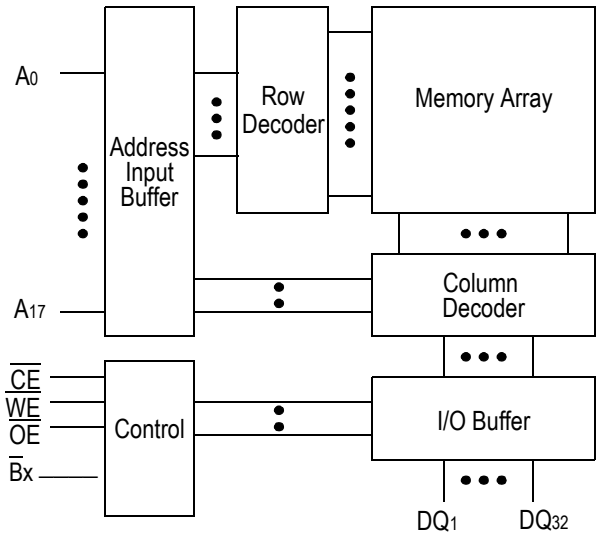
Description

The GS78132 is a high speed CMOS static RAM organized as 262,144-words by 32-bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3V power supply and all inputs and outputs are TTL compatible. The GS78132 is available in 14mm x 22mm BGA package.

Pin Descriptions

Symbol	Description
A_0 to A_{17}	Address input
$\overline{CE}$	Chip enable input
DQ_{A1} TO DQ_{A8}	Byte A Data input/output
DQ_{B1} TO DQ_{B8}	Byte B Data input/output
DQ_{C1} TO DQ_{C8}	Byte C Data input/output
DQ_{D1} TO DQ_{D8}	Byte D Data input/output
$\overline{B}_A$	Byte A Byte enable input
$\overline{B}_B$	Byte B Byte enable input
$\overline{B}_C$	Byte C Byte enable input
$\overline{B}_D$	Byte D Byte enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{DD}	+3.3V power supply
V_{SS}	Ground
NC	No connect

Block Diagram



256K x 32 Async SRAM in 119 Bump, 14x22mmBGA

Top View

	1	2	3	4	5	6	7
A	NC	A_{15}	A_{14}	A_{16}	A_{13}	A_{12}	NC
B	$\overline{B}_C$	A_{11}	A_{10}	$\overline{CE}$	A_9	A_8	$\overline{B}_B$
C	DQ_{C6}	NC	V_{DD}, NC	A_{17}	V_{SS}, NC	NC	DQ_{B6}
D	DQ_{C5}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{B5}
E	DQ_{C4}	DQ_{C8}	V_{DD}	V_{SS}	V_{DD}	DQ_{B8}	DQ_{B4}
F	DQ_{C3}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{B3}
G	DQ_{C2}	DQ_{C7}	V_{DD}	V_{SS}	V_{DD}	DQ_{B7}	DQ_{B2}
H	DQ_{C1}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{B1}
J	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	V_{DD}
K	DQ_{D1}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{A1}
L	DQ_{D2}	DQ_{D7}	V_{DD}	V_{SS}	V_{DD}	DQ_{A7}	DQ_{A2}
M	DQ_{D3}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{A3}
N	DQ_{D4}	DQ_{D8}	V_{DD}	V_{SS}	V_{DD}	DQ_{A8}	DQ_{A4}
P	DQ_{D5}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	DQ_{A5}
R	DQ_{D6}	NC	NC	NC	NC	NC	DQ_{A6}
T	$\overline{B}_D$	A_7	A_6	$\overline{WE}$	A_5	A_4	$\overline{B}_A$
U	NC	A_3	A_2	$\overline{OE}$	A_1	A_0	NC

Note: Bumps 3C and 5C are actually NC's but should be wired 3C = V_{DD} and 5C = V_{ss} to assure compatibility with future versions.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	DQ_{A1-8}	DQ_{B1-8}	DQ_{C1-8}	DQ_{D1-8}	Supply Current
H	X	X	X	X	X	X	Not Selected	Not Selected	Not Selected	Not Selected	ISB1, ISB2
L	L	H	L	L	L	L	Read	Read	Read	Read	I_{DD}
			H	L	L	L	High Z	Read	Read	Read	
			L	H	L	L	Read	High Z	Read	Read	
			L	L	H	L	Read	Read	High Z	Read	
			L	L	L	H	Read	Read	Read	High Z	
L	X	L	L	L	L	L	Write	Write	Write	Write	
			H	L	L	L	High Z	Write	Write	Write	
			L	H	L	L	Write	High Z	Write	Write	
			L	L	H	L	Write	Write	High Z	Write	
			L	L	L	H	Write	Write	Write	High	
L	H	H	X	X	X	X	High Z	High Z	High Z	High Z	
L	X	X	H	H	H	H	High Z	High Z	High Z	High Z	

Note: X: “H” or “L”

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.5 to +4.6	V
Input Voltage	V_{IN}	-0.5 to V_{DD}+0.5 (≤ 4.6V max.)	V
Output Voltage	V_{OUT}	-0.5 to V_{DD}+0.5 (≤ 4.6V max.)	V
Allowable power dissipation	PD	1.5	W
Storage temperature	T_{STG}	-55 to 150	°C

Note:
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -10/12/15	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	-	V_{DD}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	-	70	°C
Ambient Temperature, Industrial Range	T_{Ai}	-40	-	85	°C

Note:
1. Input overshoot voltage should be less than VDD+2V and not exceed 20ns.
2. Input undershoot voltage should be greater than -2V and not exceed 20ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	10	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	7	pF

Notes:
1. Tested at T_A=25°C, f=1MHz
2. These parameters are sampled and are not 100% tested

DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	V_{IN} = 0 to V_{DD}	-2uA	2uA
Output Leakage Current	I_{OL}	Output High Z, V_{OUT} = 0 to V_{DD}	-1uA	1uA
Output High Voltage	V_{OH}	I_{OH} = - 4mA	2.4	
Output Low Voltage	V_{OL}	I_{OL} = + 4mA		0.4V

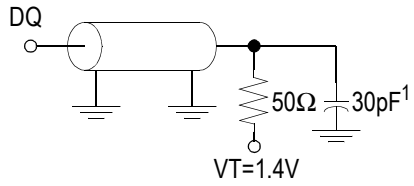
Power Supply Currents

Parameter	Symbol	Test Conditions	0 to 70°C			-40 to 85°C		
			10ns	12ns	15ns	10ns	12ns	15ns
Operating Supply Current	I_{DD}	$\overline{E} \le V_{IL}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time I_{OUT} = 0 mA	290mA	260mA	220mA	310mA	280mA	240mA
Standby Current	I_{SB1}	$\overline{E} \ge V_{IH}$ All other inputs $\ge V_{IH}$ or $\le V_{IL}$ Min. cycle time	130mA	120mA	110mA	150mA	140mA	130mA
Standby Current	I_{SB2}	$E \ge V_{DD}$ - 0.2V All other inputs $\ge V_{DD}$ - 0.2V or $\le$ 0.2V	60mA			80mA		

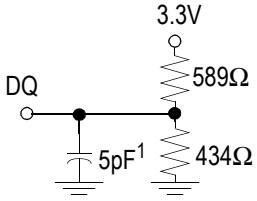
AC Test Conditions

Parameter	Conditions
Input high level	V_{IH}=2.4V
Input low level	V_{IL}=0.4V
Input rise time	tr=1V/ns
Input fall time	tf=1V/ns
Input reference level	1.4V
Output reference level	1.4V
Output load	Fig. 1& 2

Output Load 1



Output Load 2



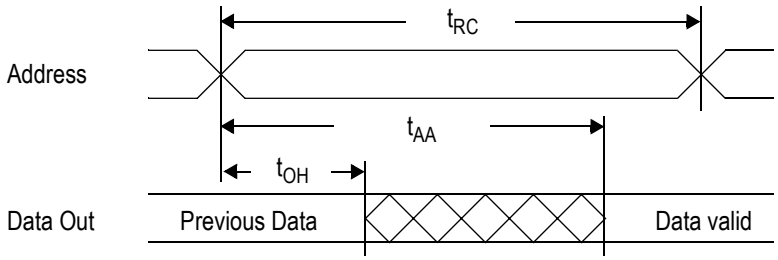
Note:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
3. Output load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}.

AC Characteristics

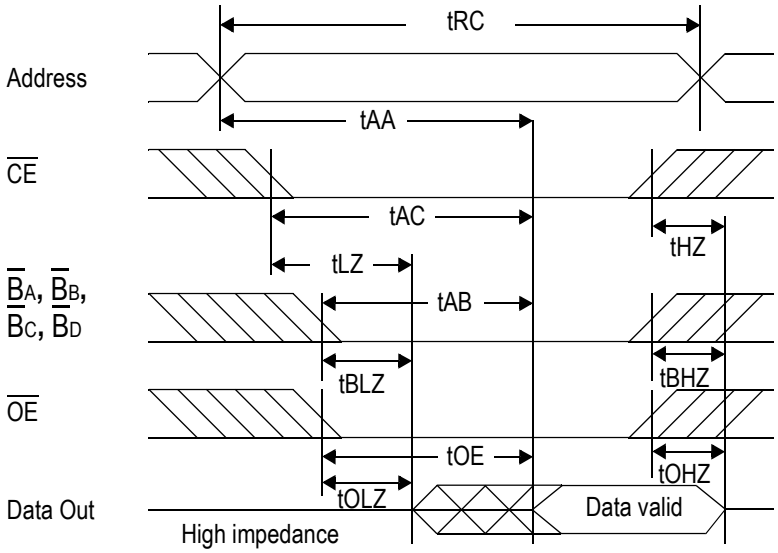
Read Cycle

Parameter	Symbol	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	10	---	12	---	15	---	ns
Address access time	t_{AA}	---	10	---	12	---	15	ns
Chip enable access time ($\overline{CE}$)	t_{AC}	---	10	---	12	---	15	ns
Byte enable access time	t_{AB}	---	4	---	5	---	6	ns
Output enable to output valid ($\overline{OE}$)	t_{OE}	---	4	---	5	---	6	ns
Output hold from address change	t_{OH}	3	---	3	---	3	---	ns
Chip enable to output in low Z ($\overline{CE}$)	t_{LZ}*	3	---	3	---	3	---	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	---	0	---	0	---	ns
Byte enable to output in low Z	t_{BLZ}*	0	---	0	---	0	---	ns
Chip disable to output in High Z ($\overline{CE}$)	t_{HZ}*	---	5	---	6	---	7	ns
Output disable to output in High Z ($\overline{OE}$)	t_{OHZ}*	---	4	---	5	---	6	ns
Byte disable to output in High Z	t_{BHZ}*	---	4	---	5	---	6	ns

Read Cycle 1: $\overline{CE}$ = $\overline{OE}$ = V_{IL} , $\overline{WE}$ = V_{IH}, $\overline{B}_A$ = $\overline{B}_B$ = $\overline{B}_C$ = $\overline{B}_D$ = V_{IL}



Read Cycle 2: $\overline{WE}$ = V_{IH}

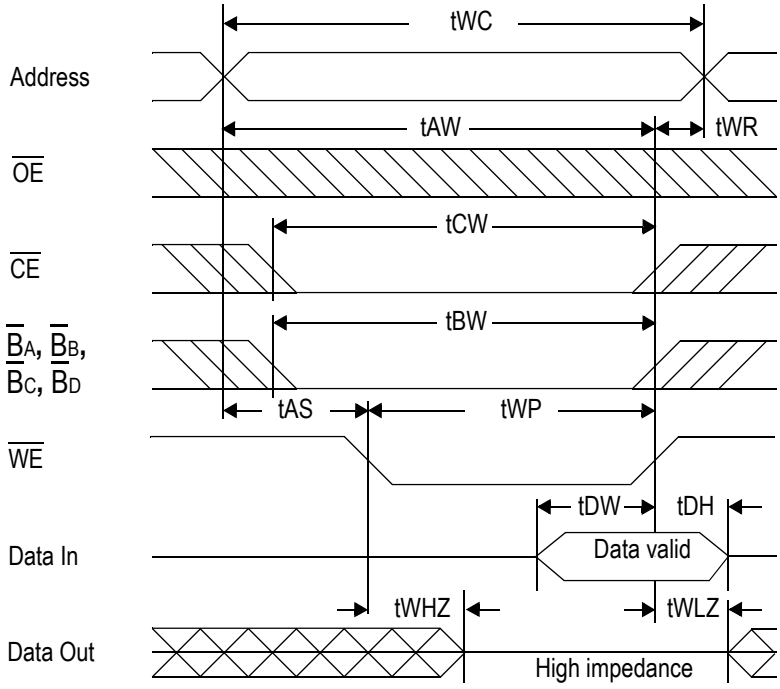


Write Cycle

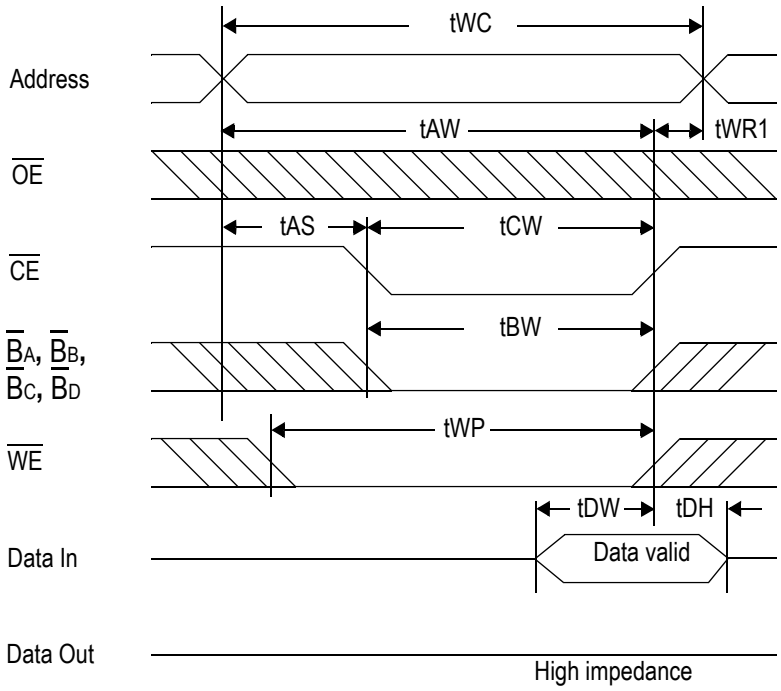
Parameter	Symbol	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	tWC	10	---	12	---	15	---	ns
Address valid to end of write	tAW	7	---	8	---	10	---	ns
Chip enable to end of write	tCW	7	---	8	---	10	---	ns
Byte enable to end of write	tBW	7	---	8	---	10	---	ns
Data set up time	tDW	5	---	6	---	7	---	ns
Data hold time	tDH	0	---	0	---	0	---	ns
Write pulse width	tWP	7	---	8	---	10	---	ns
Address set up time	tAS	0	---	0	---	0	---	ns
Write recovery time ($\overline{WE}$)	tWR	0	---	0	---	0	---	ns
Write recovery time ($\overline{CE}$)	tWR1	0	---	0	---	0	---	ns
Output Low Z from end of write	tWLZ*	3	---	3	---	3	---	ns
Write to output in High Z	tWHZ*	---	4	---	5	---	6	ns

* These parameters are sampled and are not 100% tested

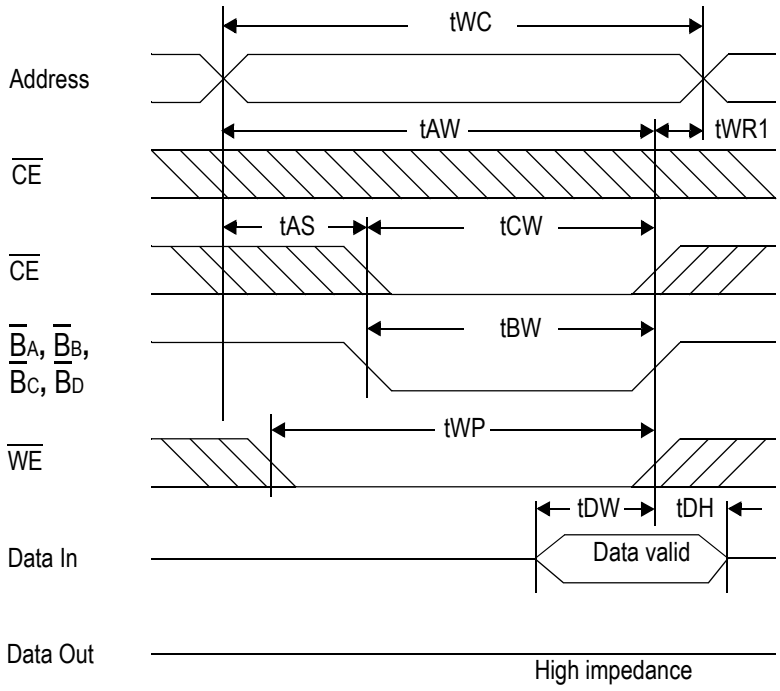
Write Cycle 1: $\overline{WE}$ Controlled



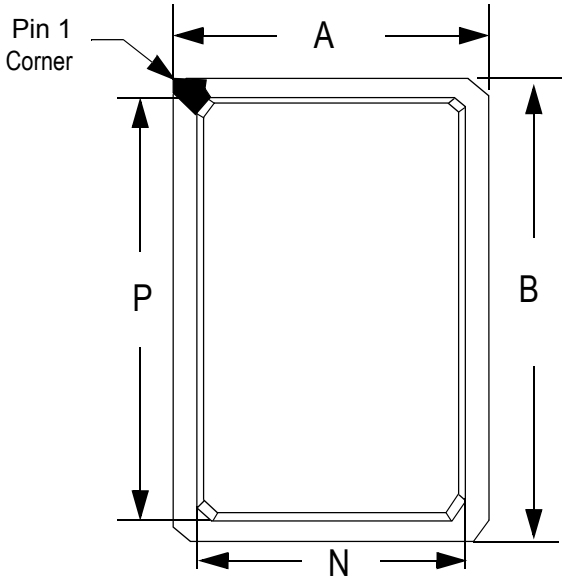
Write Cycle 2: $\overline{CE}$ Controlled



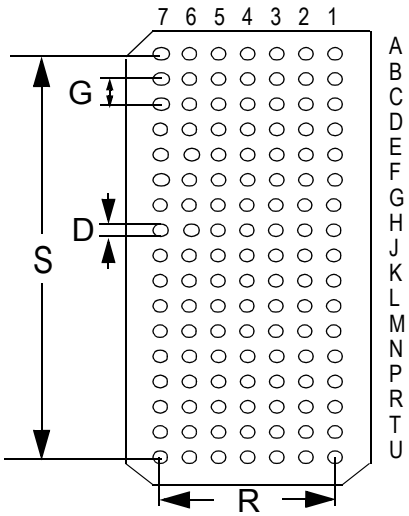
Write Cycle 3: Byte Enable Controlled



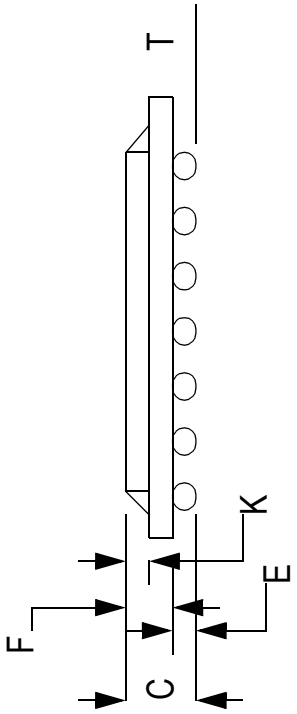
Package Dimensions - 119 Pin PBGA



Top View



Bottom View



Side View

Package Dimensions - 119 Pin PBGA

Symbol	Description	Min.	Nom.	Max
A	Width	13.8	14.0	14.2
B	Length	21.8	22.0	22.2
C	Package Height (including ball)	-		2.40
D	Ball Size	0.60	0.75	0.90
E	Ball Height	0.50	0.60	0.70
F	Package Height (excluding balls)		1.46	1.70
G	Width between Balls		1.27	
K	Package Height above board	0.80	0.90	1.00
N	Cut-out Package Width		12.00	
P	Foot Length		19.50	
R	Width of package between balls		7.62	
S	Length of package between balls		20.32	
T	Variance of Ball Height		0.15	

Unit: mm

BPR 1999.05.18

Ordering Information

Part Number*	Package	Access Time	Temp. Range	Status
GS78132B-10	BGA	10 ns	Commercial	
GS78132B-12	BGA	12 ns	Commercial	
GS78132B-15	BGA	15 ns	Commercial	
GS78132B-10I	BGA	10 ns	Industrial	
GS78132B-12I	BGA	12 ns	Industrial	
GS78132B-15I	BGA	15 ns	Industrial	

* Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS78132B-12T

Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
GS78132Rev0.01a 5/1999; 1.00 X/1999	Format/Typos	• p.2/Changed 12x22 to 14x22/Typo • p.2/Changed $\overline{E}$ to $\overline{CE}$/consistency.
	Content	• p.2/Changed Pin T1 from $\overline{B}_A$ to $\overline{B}_D$/Correction
GS78132Rev 1.0010/1999A;Rev 1.01 2/2000FormatB		• Added GSI Logo