

100-Pin TQFP & 165-Bump BGA 1M x 18, 512K x 36, 512K x 36
Commercial Temp
Industrial Temp
18Mb Sync Burst SRAMs
250 MHz–150 MHz
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- \overline{FT} pin for user-configurable flow through or pipeline operation
- Dual Cycle Deselect (DCD) operation
- IEEE 1149.1 JTAG-compatible Boundary Scan
- 2.5 V or 3.3 V +10%/–10% core power supply
- 2.5 V or 3.3 V I/O supply
- \overline{LBO} pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to Interleaved Pipeline mode
- Byte Write (\overline{BW}) and/or Global Write (\overline{GW}) operation
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC-standard 100-lead TQFP package
- RoHS-compliant 100-lead TQFP and 165-bump BGA packages available

Functional Description

Applications

The GS8161E18B(T/D)/GS8161E32B(D)/GS8161E36B(T/D) is a 18,874,368-bit high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enable ($\overline{E1}$), address burst control inputs (\overline{ADSP} , \overline{ADSC} , \overline{ADV}) and write control inputs (\overline{Bx} , \overline{BW} , \overline{GW}) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable (\overline{G}) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either \overline{ADSP} or \overline{ADSC} inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by \overline{ADV} . The burst address counter may be configured to count in either linear or interleave order with the

Linear Burst Order (\overline{LBO}) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the \overline{FT} mode pin (Pin 14). Holding the \overline{FT} mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding \overline{FT} high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

DCD Pipelined Reads

The GS8161E18B(T/D)/GS8161E32B(D)/GS8161E36B(T/D) is a DCD (Dual Cycle Deselect) pipelined synchronous SRAM. SCD (Single Cycle Deselect) versions are also available. DCD SRAMs pipeline disable commands to the same degree as read commands. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable (\overline{BW}) input combined with one or more individual byte write signals (\overline{Bx}). In addition, Global Write (\overline{GW}) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

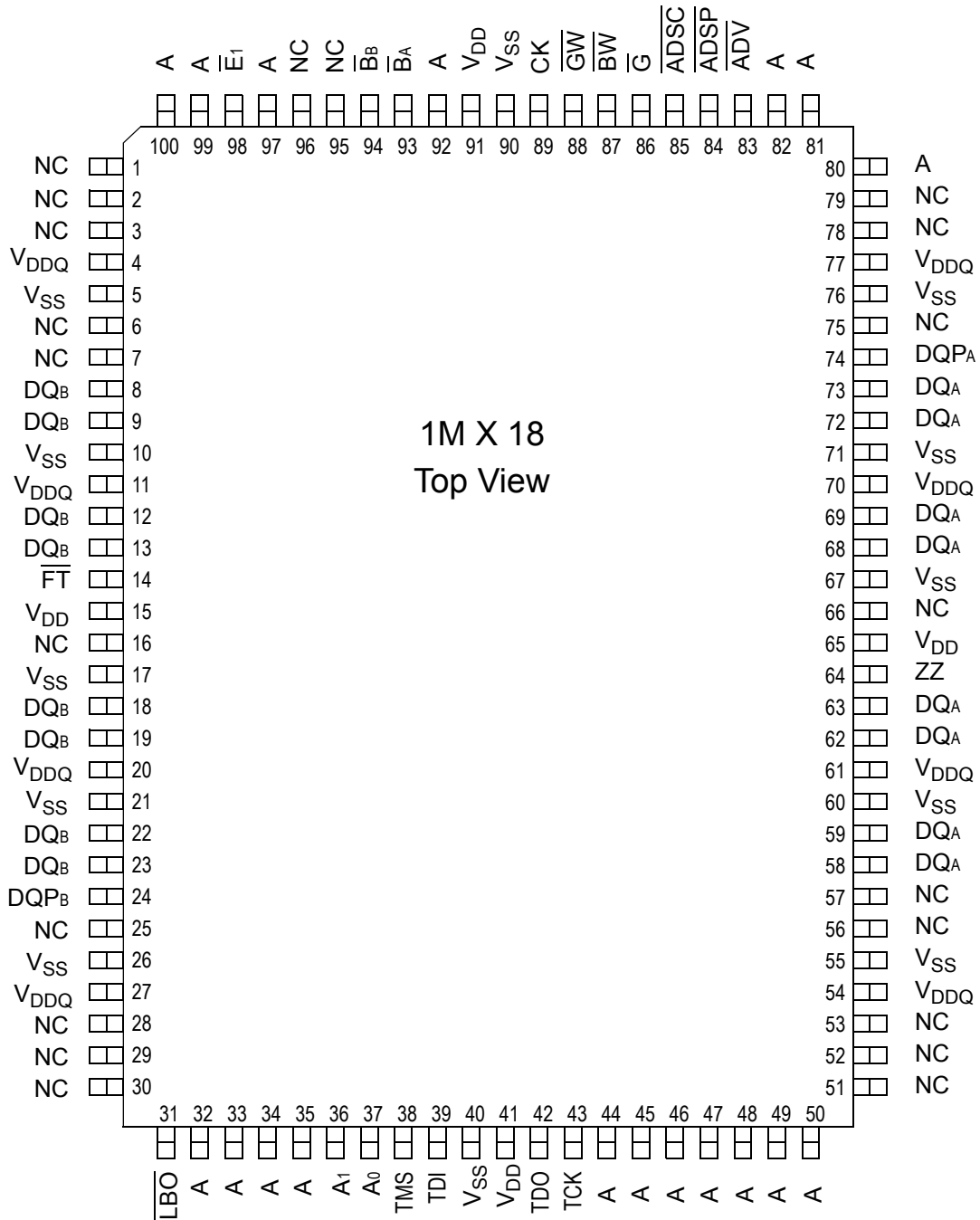
Core and Interface Voltages

The GS8161E18B(T/D)/GS8161E32B(D)/GS8161E36B(T/D) operates on a 2.5 V or 3.3 V power supply. All input are 3.3 V and 2.5 V compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuits and are 3.3 V and 2.5 V compatible.

Parameter Synopsis

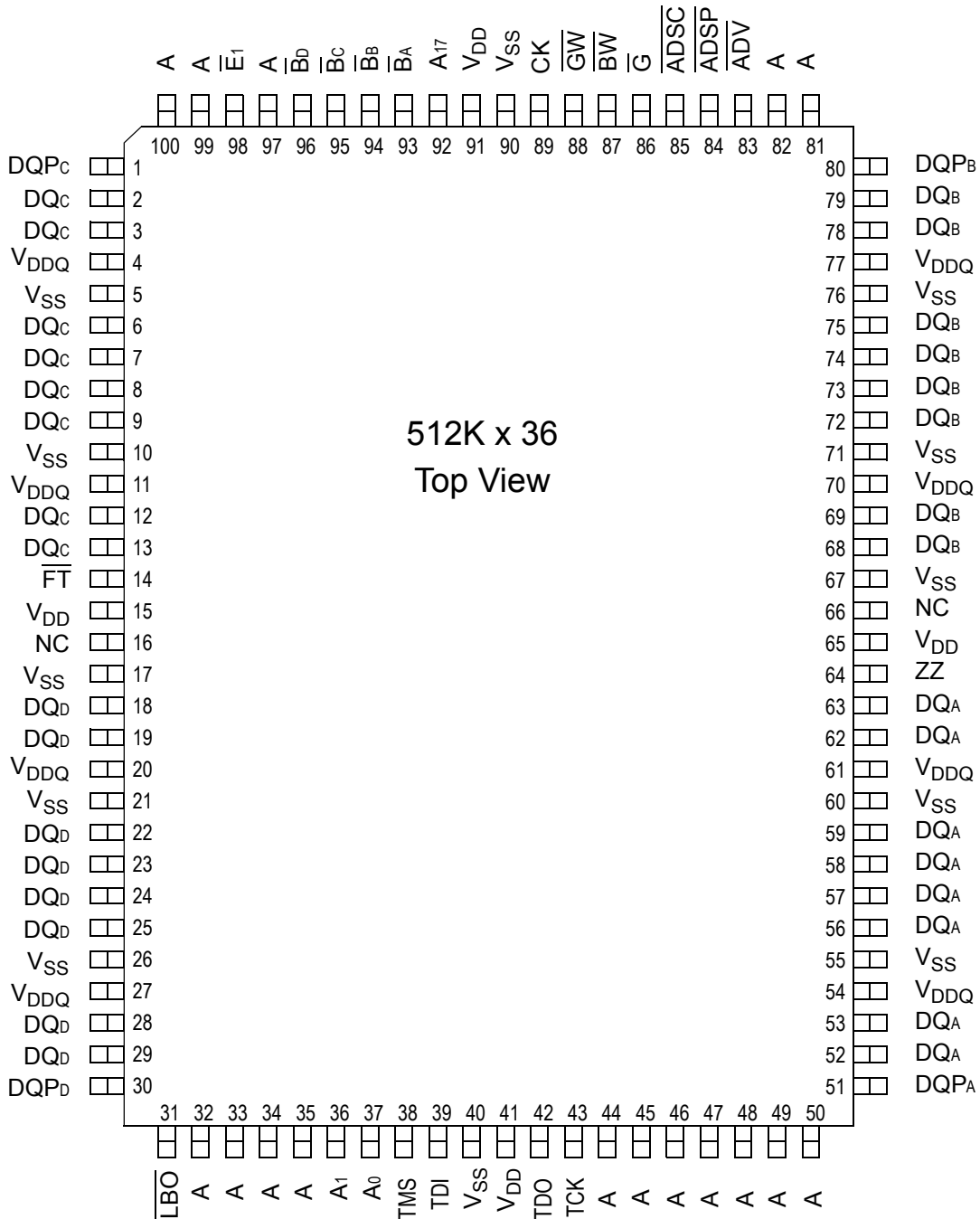
		-250	-200	-150	Unit
Pipeline 3-1-1-1	t _{kQ}	2.5	3.0	3.8	ns
	t _{Cycle}	4.0	5.0	6.7	ns
	Curr (x18)	295	245	200	mA
	Curr (x32/x36)	345	285	225	mA
Flow Through 2-1-1-1	t _{kQ}	5.5	6.5	7.5	ns
	t _{Cycle}	5.5	6.5	7.5	ns
	Curr (x18)	225	200	185	mA
	Curr (x32/x36)	255	220	205	mA

GS8161E18B 100-Pin TQFP Pinout



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GS8161E36B 100-Pin TQFP Pinout



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TQFP Pin Description

Symbol	Type	Description
A ₀ , A ₁	I	Address field LSBs and Address Counter preset Inputs
A	I	Address Inputs
DQ _A DQ _B DQ _C DQ _D	I/O	Data Input and Output pins
NC	—	No Connect
\overline{BW}	I	Byte Write—Writes all enabled bytes; active low
\overline{BA} , \overline{BB} , \overline{BC} , \overline{BD}	I	Byte Write Enable for DQ _A , DQ _B Data I/Os; active low
CK	I	Clock Input Signal; active high
\overline{GW}	I	Global Write Enable—Writes all bytes; active low
\overline{E}_1	I	Chip Enable; active low
\overline{G}	I	Output Enable; active low
\overline{ADV}	I	Burst address counter advance enable; active low
\overline{ADSP} , \overline{ADSC}	I	Address Strobe (Processor, Cache Controller); active low
ZZ	I	Sleep Mode control; active high
\overline{LBO}	I	Linear Burst Order mode; active low
TMS	I	Scan Test Mode Select
TDI	I	Scan Test Data In
TDO	O	Scan Test Data Out
TCK	I	Scan Test Clock
V _{DD}	I	Core power supply
V _{SS}	I	I/O and Core Ground
V _{DDQ}	I	Output driver power supply

165 Bump BGA—x18 Commom I/O—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	\overline{BB}	NC	$\overline{E3}$	\overline{BW}	\overline{ADSC}	\overline{ADV}	A	A	A
B	NC	A	E2	NC	\overline{BA}	CK	\overline{GW}	\overline{G}	\overline{ADSP}	A	NC	B
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	$DQPA$	C
D	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	D
E	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	E
F	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	F
G	NC	DQB	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQA	G
H	\overline{FT}	MCL	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ	H
J	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	J
K	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	K
L	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	L
M	DQB	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	NC	M
N	$DQPB$	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	NC	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	A	P
R	\overline{LBO}	NC	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13mm x 15 mm Body—1.0 mm Bump Pitch

165 Bump BGA—x32 Common I/O—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	\overline{BC}	\overline{BB}	$\overline{E3}$	\overline{BW}	\overline{ADSC}	\overline{ADV}	A	NC	A
B	NC	A	E2	\overline{BD}	\overline{BA}	CK	\overline{GW}	\overline{G}	\overline{ADSP}	A	NC	B
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	C
D	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	D
E	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	E
F	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	F
G	DQC	DQC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQB	DQB	G
H	\overline{FT}	MCL	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ	H
J	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	J
K	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	K
L	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	L
M	DQD	DQD	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQA	DQA	M
N	NC	NC	V_{DDQ}	V_{SS}	NC	A	NC	V_{SS}	V_{DDQ}	NC	NC	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	A	P
R	\overline{LBO}	NC	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13mm x 15 mm Body—1.0 mm Bump Pitch

165 Bump BGA—x36 Common I/O—Top View (Package D)

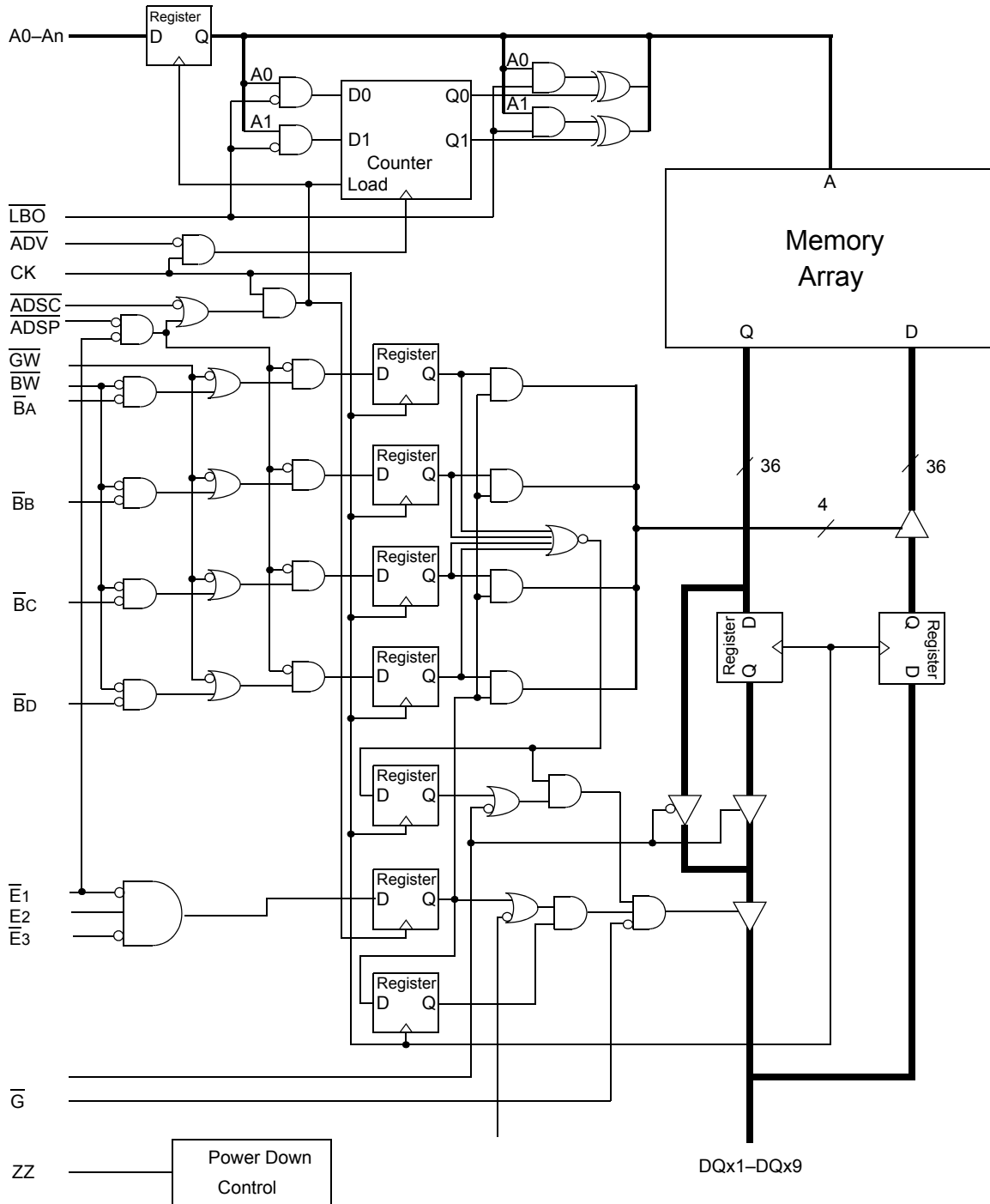
	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	\overline{BC}	\overline{BB}	$\overline{E3}$	\overline{BW}	\overline{ADSC}	\overline{ADV}	A	NC	A
B	NC	A	E2	\overline{BD}	\overline{BA}	CK	\overline{GW}	\overline{G}	\overline{ADSP}	A	NC	B
C	DQPC	NC	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	DQPB	C
D	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	D
E	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	E
F	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	F
G	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	G
H	\overline{FT}	MCL	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC	NC	ZZ	H
J	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	J
K	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	K
L	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	L
M	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	M
N	DQPD	NC	V _{DDQ}	V _{SS}	NC	A	NC	V _{SS}	V _{DDQ}	NC	DQPA	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	A	P
R	\overline{LBO}	NC	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13mm x 15 mm Body—1.0 mm Bump Pitch

GS8161E18/32/36BD 165-Bump BGA Pin Description

Symbol	Type	Description
A ₀ , A ₁	I	Address field LSBs and Address Counter Preset Inputs
A	I	Address Inputs
DQ _A DQ _B DQ _C DQ _D	I/O	Data Input and Output pins
$\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$	I	Byte Write Enable for DQ _A , DQ _B , DQ _C , DQ _D I/Os; active low
NC	—	No Connect
CK	I	Clock Input Signal; active high
$\overline{B_W}$	I	Byte Write—Writes all enabled bytes; active low
$\overline{G_W}$	I	Global Write Enable—Writes all bytes; active low
$\overline{E_1}$	I	Chip Enable; active low
$\overline{E_3}$	I	Chip Enable; active low
E ₂	I	Chip Enable; active high
\overline{G}	I	Output Enable; active low
$\overline{A_{DV}}$	I	Burst address counter advance enable; active low
$\overline{A_{DSC}}$, $\overline{A_{DSP}}$	I	Address Strobe (Processor, Cache Controller); active low
$\overline{Z_Z}$	I	Sleep mode control; active high
$\overline{F_T}$	I	Flow Through or Pipeline mode; active low
$\overline{L_{B_O}}$	I	Linear Burst Order mode; active low
TMS	I	Scan Test Mode Select
TDI	I	Scan Test Data In
TDO	O	Scan Test Data Out
TCK	I	Scan Test Clock
MCL	—	Must Connect Low
V _{DD}	I	Core power supply
V _{SS}	I	I/O and Core Ground
V _{DDQ}	I	Output driver power supply

GS8161E18/32/36B Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:

There are pull-up devices on the $\overline{\text{FT}}$ pin and a pull-down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:

The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:

The burst counter wraps to initial state on the 5th clock.

Byte Write Truth Table

Function	\overline{GW}	\overline{BW}	\overline{BA}	\overline{BB}	\overline{BC}	\overline{BD}	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs \overline{BA} , \overline{BB} , \overline{BC} and/or \overline{BD} may be used in any combination with \overline{BW} to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "c" and "d" are only available on the x36 version.

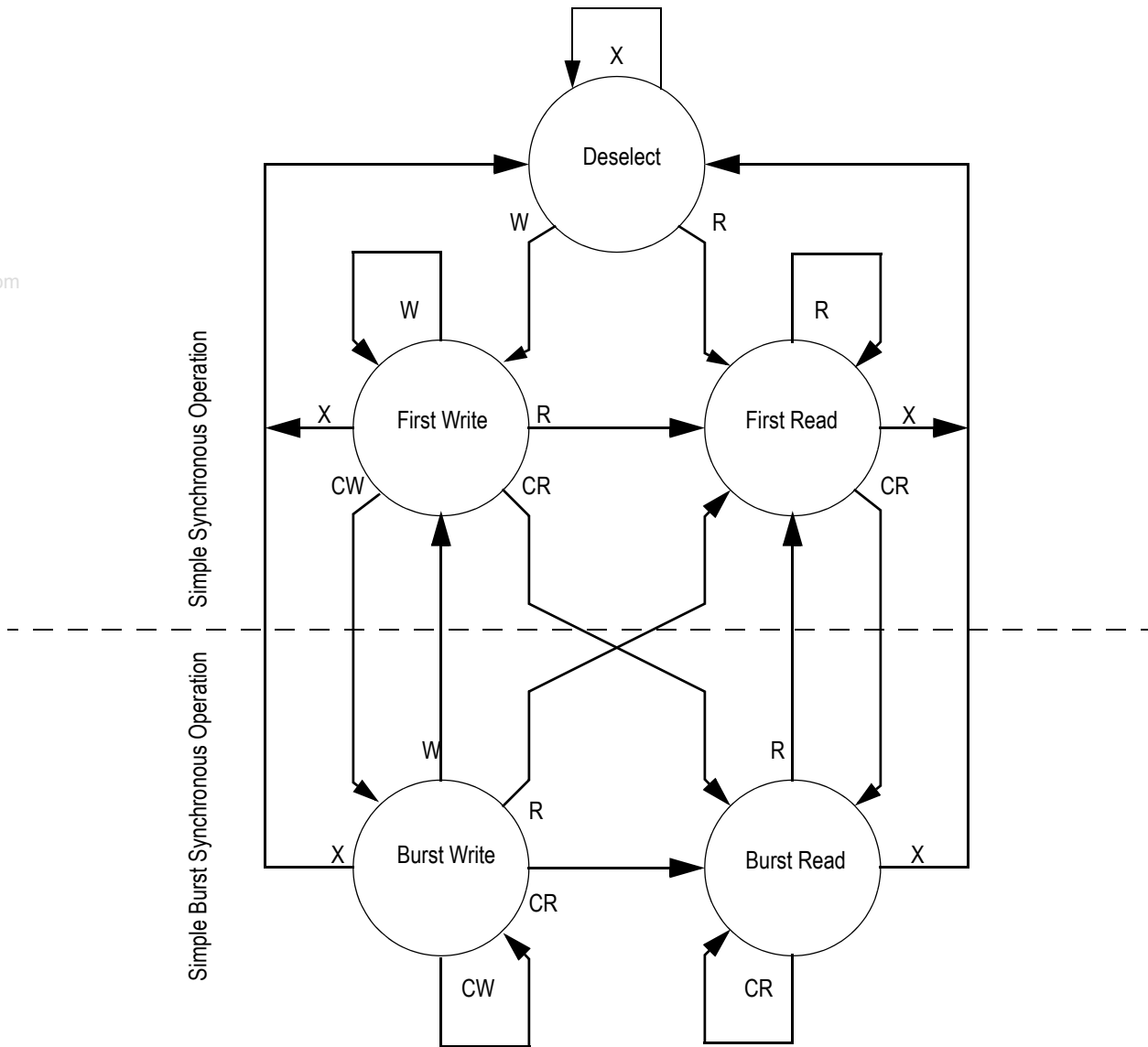
Synchronous Truth Table

Operation	Address Used	State Diagram Key ⁵	\bar{E}_1	E^2	\overline{ADSP}	\overline{ADSC}	\overline{ADV}	\bar{W}^3	DQ ⁴
Deselect Cycle, Power Down	None	X	H	X	X	L	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	None	X	L	F	H	L	X	X	High-Z
<i>Read Cycle, Begin Burst</i>	<i>External</i>	<i>R</i>	<i>L</i>	<i>T</i>	<i>L</i>	<i>X</i>	<i>X</i>	<i>X</i>	<i>Q</i>
Read Cycle, Begin Burst	External	R	L	T	H	L	X	F	Q
Write Cycle, Begin Burst	External	W	L	T	H	L	X	T	D
<i>Read Cycle, Continue Burst</i>	<i>Next</i>	<i>CR</i>	<i>X</i>	<i>X</i>	<i>H</i>	<i>H</i>	<i>L</i>	<i>F</i>	<i>Q</i>
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
<i>Write Cycle, Continue Burst</i>	<i>Next</i>	<i>CW</i>	<i>X</i>	<i>X</i>	<i>H</i>	<i>H</i>	<i>L</i>	<i>T</i>	<i>D</i>
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current			X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current			X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current			X	H	H	H	T	D
Write Cycle, Suspend Burst	Current			X	X	H	H	T	D

Notes:

1. X = Don't Care, H = High, L = Low
2. E = T (True) if $E_2 = 1$; E = F (False) if $E_2 = 0$
3. $\bar{W} = T$ (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. \bar{G} is an asynchronous input. \bar{G} can be driven high at any time to disable active output drivers. \bar{G} low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying \overline{ADSP} high and \overline{ADSC} low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying \overline{ADSP} high and \overline{ADV} low while using \overline{ADSC} to load new addresses allows simple burst operations. See *ITALIC* items above.

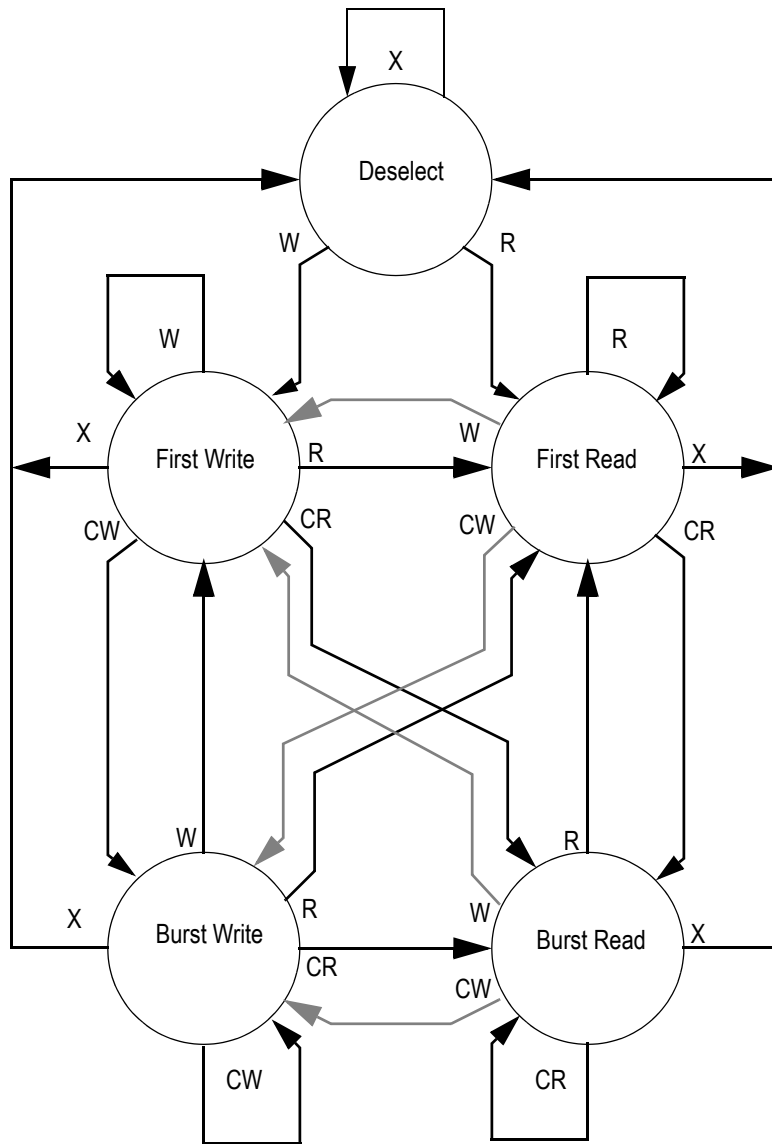
Simplified State Diagram



Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes \overline{G} is tied low.
2. The upper portion of the diagram assumes active use of only the Enable ($\overline{E1}$) and Write (\overline{BA} , \overline{BB} , \overline{BC} , \overline{BD} , \overline{BW} , and \overline{GW}) control inputs, and that \overline{ADSP} is tied high and \overline{ADSC} is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and \overline{ADSC} control inputs, and assumes \overline{ADSP} is tied high and \overline{ADV} is tied low.

Simplified State Diagram with \overline{G}



Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of \overline{G} .
2. Use of "Dummy Reads" (Read Cycles with \overline{G} High) may be used to make the transition from read cycles to write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in gray tone assume \overline{G} has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

 (All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	-0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	-0.5 to 4.6	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to $V_{DDQ} + 0.5$	V
V_{IN}	Voltage on Other Input Pins	-0.5 to $V_{DD} + 0.5$	V
I_{IN}	Input Current on Any Pin	+/-20	mA
I_{OUT}	Output Current on Any I/O Pin	+/-20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	-55 to 125	°C
T_{BIAS}	Temperature Under Bias	-55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V	
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V	
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V	
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V	

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 1.5\text{ V}$ maximum, with a pulse width not to exceed 50% tKC.

V_{DDQ3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V _{DD} Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V	1
V _{DD} Input Low Voltage	V _{IL}	-0.3	—	0.8	V	1
V _{DDQ} I/O Input High Voltage	V _{IHQ}	2.0	—	V _{DDQ} + 0.3	V	1,3
V _{DDQ} I/O Input Low Voltage	V _{ILQ}	-0.3	—	0.8	V	1,3

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 1.5\text{ V}$ maximum, with a pulse width not to exceed 50% t_{KC}.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

V_{DDQ2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V _{DD} Input High Voltage	V _{IH}	0.6*V _{DD}	—	V _{DD} + 0.3	V	1
V _{DD} Input Low Voltage	V _{IL}	-0.3	—	0.3*V _{DD}	V	1
V _{DDQ} I/O Input High Voltage	V _{IHQ}	0.6*V _{DD}	—	V _{DDQ} + 0.3	V	1,3
V _{DDQ} I/O Input Low Voltage	V _{ILQ}	-0.3	—	0.3*V _{DD}	V	1,3

Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 1.5\text{ V}$ maximum, with a pulse width not to exceed 50% t_{KC}.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

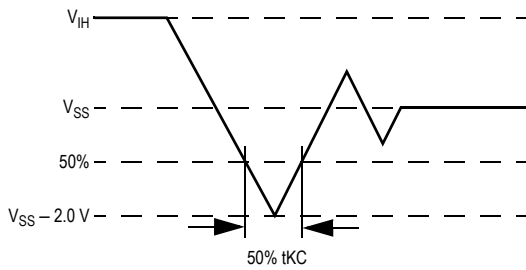
Recommended Operating Temperatures

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature (Commercial Range Versions)	T _A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T _A	-40	25	85	°C	2

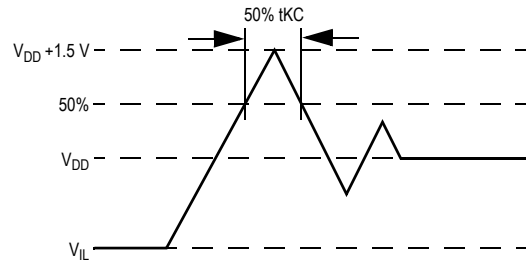
Notes:

1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 1.5\text{ V}$ maximum, with a pulse width not to exceed 50% t_{KC}.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



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Capacitance

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 2.5\text{ V}$)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0\text{ V}$	4	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0\text{ V}$	6	7	pF

Note:

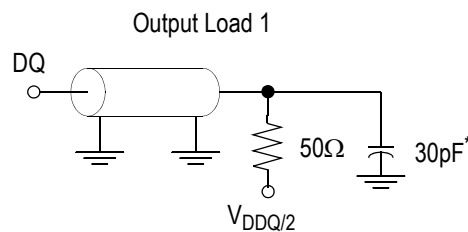
These parameters are sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	$V_{DD} - 0.2\text{ V}$
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DDQ}/2$
Output load	Fig. 1

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	$V_{IN} = 0$ to V_{DD}	-1 μ A	1 μ A
ZZ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0 \text{ V} \leq V_{IN} \leq V_{IH}$	-1 μ A -1 μ A	1 μ A 100 μ A
\overline{FT} Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0 \text{ V} \leq V_{IN} \leq V_{IL}$	-100 μ A -1 μ A	1 μ A 1 μ A
Output Leakage Current	I_{OL}	Output Disable, $V_{OUT} = 0$ to V_{DD}	-1 μ A	1 μ A
Output High Voltage	V_{OH2}	$I_{OH} = -8 \text{ mA}$, $V_{DDQ} = 2.375 \text{ V}$	1.7 V	—
Output High Voltage	V_{OH3}	$I_{OH} = -8 \text{ mA}$, $V_{DDQ} = 3.135 \text{ V}$	2.4 V	—
Output Low Voltage	V_{OL}	$I_{OL} = 8 \text{ mA}$	—	0.4 V

Operating Currents

Parameter	Test Conditions	Mode	Symbol	-250		-200		-150		Unit	
				0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C		
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x32/ x36)	Pipeline	I_{DD} I_{DDQ}	305 40	315 40	255 30	265 30	205 20	215 20	mA
			Flow Through	I_{DD} I_{DDQ}	235 20	245 20	205 15	215 15	190 15	200 15	mA
		(x18)	Pipeline	I_{DD} I_{DDQ}	275 20	285 20	230 15	240 15	185 15	195 15	mA
			Flow Through	I_{DD} I_{DDQ}	215 10	225 10	190 10	200 10	175 10	185 10	mA
Standby Current	$ZZ \geq V_{DD} - 0.2 V$	—	Pipeline	I_{SB}	40	50	40	50	40	50	mA
			Flow Through	I_{SB}	40	50	40	50	40	50	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	Pipeline	I_{DD}	85	90	75	80	60	65	mA
			Flow Through	I_{DD}	60	65	50	55	50	55	mA

Notes:

- I_{DD} and I_{DDQ} apply to any combination of V_{DD3} , V_{DD2} , V_{DDQ3} , and V_{DDQ2} operation.
- All parameters listed are worst case scenario.

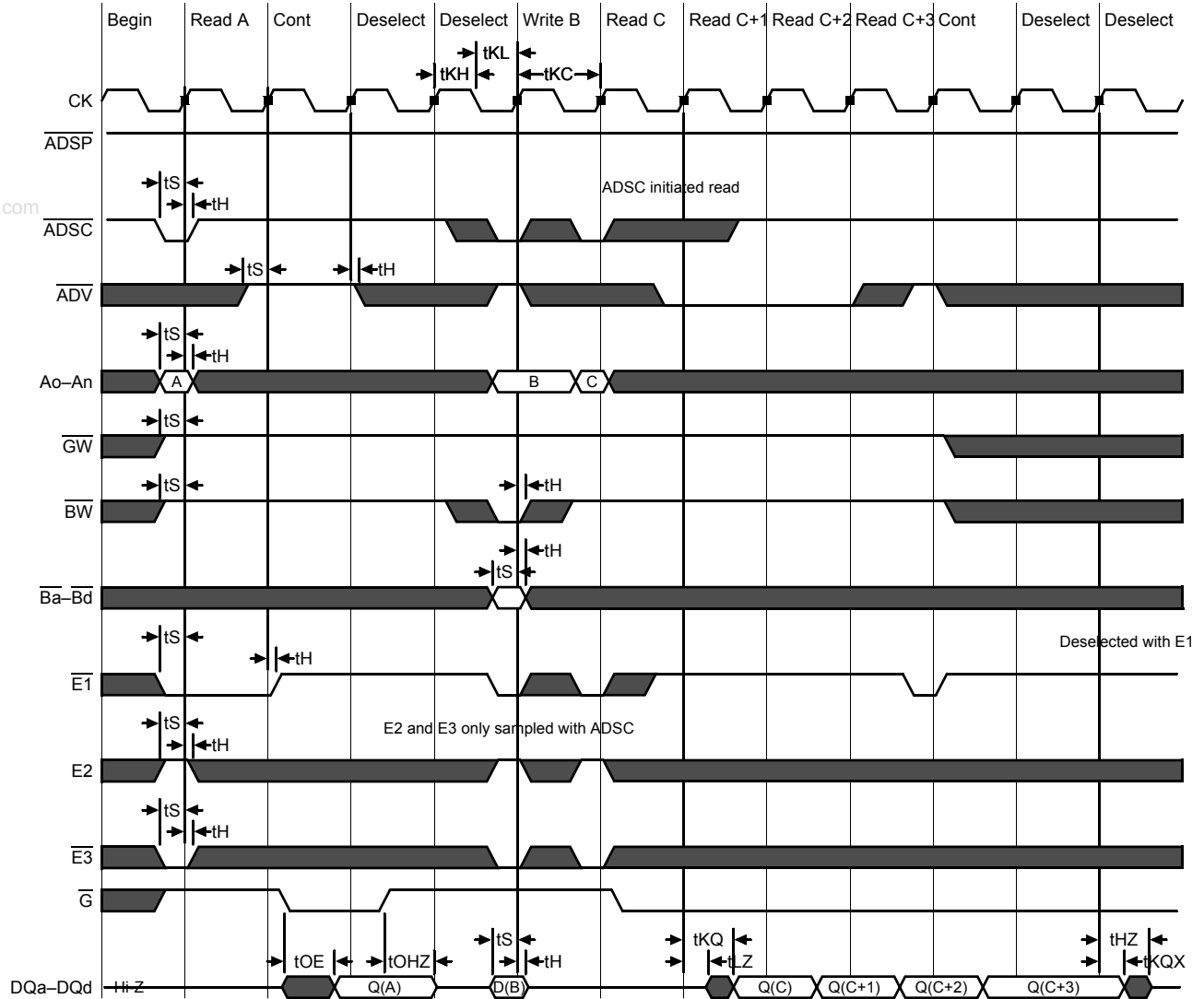
AC Electrical Characteristics

	Parameter	Symbol	-250		-200		-150		Unit
			Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	t _{KC}	4.0	—	5.0	—	6.7	—	ns
	Clock to Output Valid	t _{KQ}	—	2.5	—	3.0	—	3.8	ns
	Clock to Output Invalid	t _{KQX}	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	t _{LZ} ¹	1.5	—	1.5	—	1.5	—	ns
	Setup time	t _S	1.2	—	1.4	—	1.5	—	ns
	Hold time	t _H	0.2	—	0.4	—	0.5	—	ns
Flow Through	Clock Cycle Time	t _{KC}	5.5	—	6.5	—	7.5	—	ns
	Clock to Output Valid	t _{KQ}	—	5.5	—	6.5	—	7.5	ns
	Clock to Output Invalid	t _{KQX}	2.0	—	2.0	—	2.0	—	ns
	Clock to Output in Low-Z	t _{LZ} ¹	2.0	—	2.0	—	2.0	—	ns
	Setup time	t _S	1.5	—	1.5	—	1.5	—	ns
	Hold time	t _H	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	t _{KH}	1.3	—	1.3	—	1.5	—	ns
	Clock LOW Time	t _{KL}	1.5	—	1.5	—	1.7	—	ns
	Clock to Output in High-Z	t _{HZ} ¹	1.5	2.5	1.5	3.0	1.5	3.0	ns
	\bar{G} to Output Valid	t _{OE}	—	2.5	—	3.0	—	3.8	ns
	\bar{G} to output in Low-Z	t _{OLZ} ¹	0	—	0	—	0	—	ns
	\bar{G} to output in High-Z	t _{OHZ} ¹	—	2.5	—	3.0	—	3.8	ns
	ZZ setup time	t _{ZZS} ²	5	—	5	—	5	—	ns
	ZZ hold time	t _{ZZH} ²	1	—	1	—	1	—	ns
	ZZ recovery	t _{ZZR}	20	—	20	—	20	—	ns

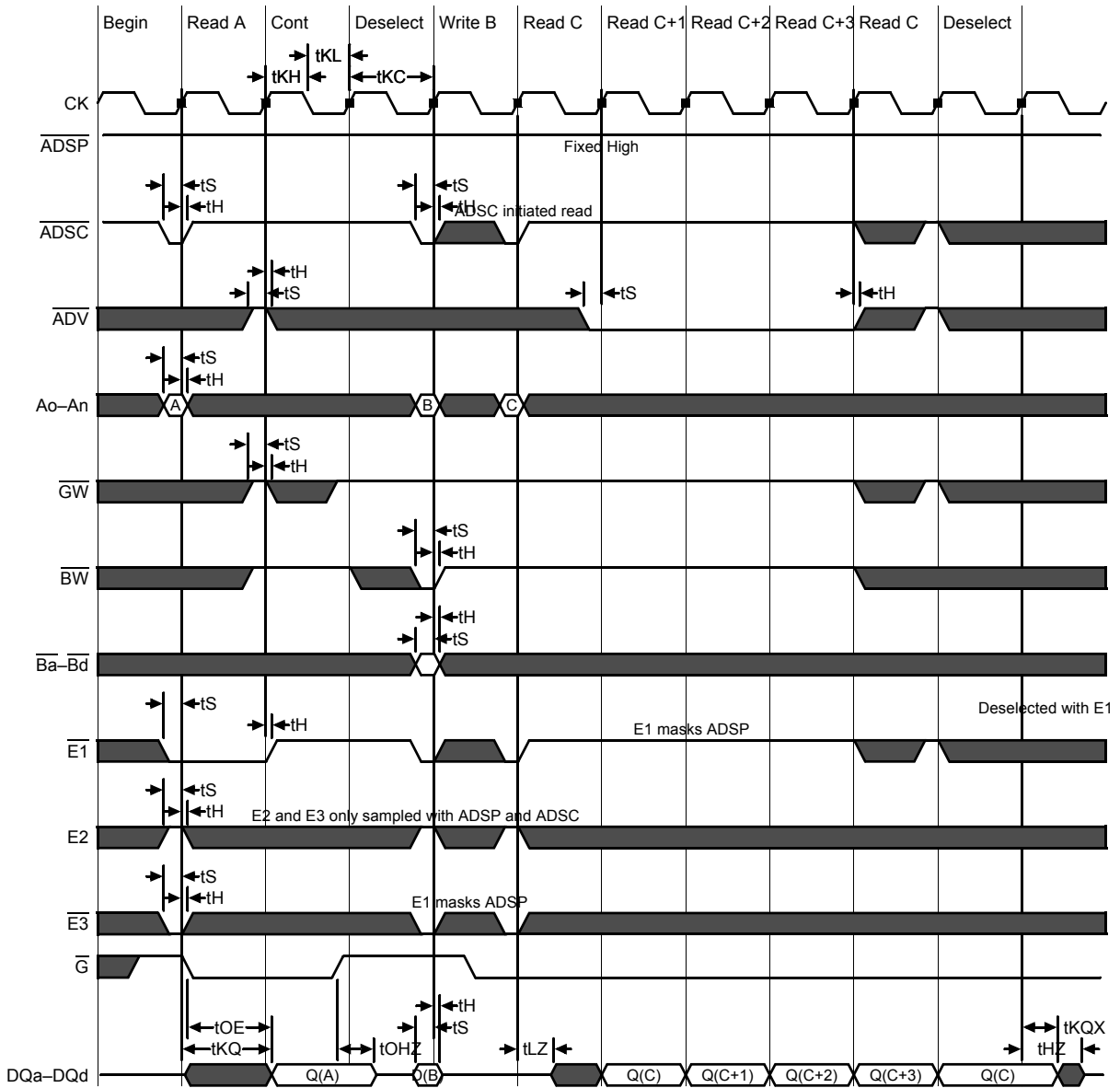
Notes:

1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

Pipeline Mode Timing (DCD)



Flow Through Mode Timing (DCD)



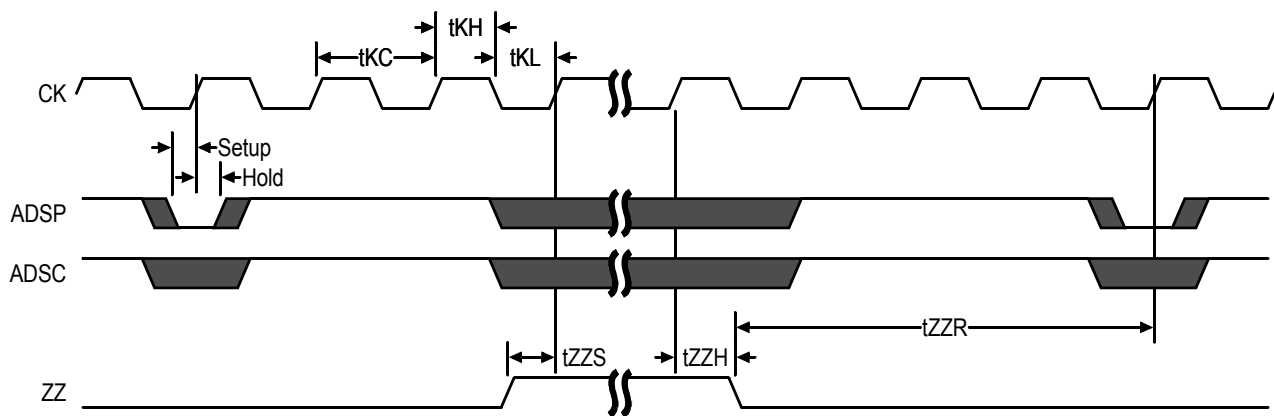
Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after ZZ recovery time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z. The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, I_{SB2} is guaranteed after the time t_{ZZI} is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during t_{ZZR} , only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

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Sleep Mode Timing



Application Tips

Single and Dual Cycle Deselect

SCD devices force the use of “dummy read cycles” (read cycles that are launched normally but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs (like this one) do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings) but greater care must be exercised to avoid excessive bus contention.

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD} . The JTAG output drivers are powered by V_{DDQ} .

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS} . TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automatically at power-up.

JTAG Port Registers

Overview

The various JTAG registers, referred to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

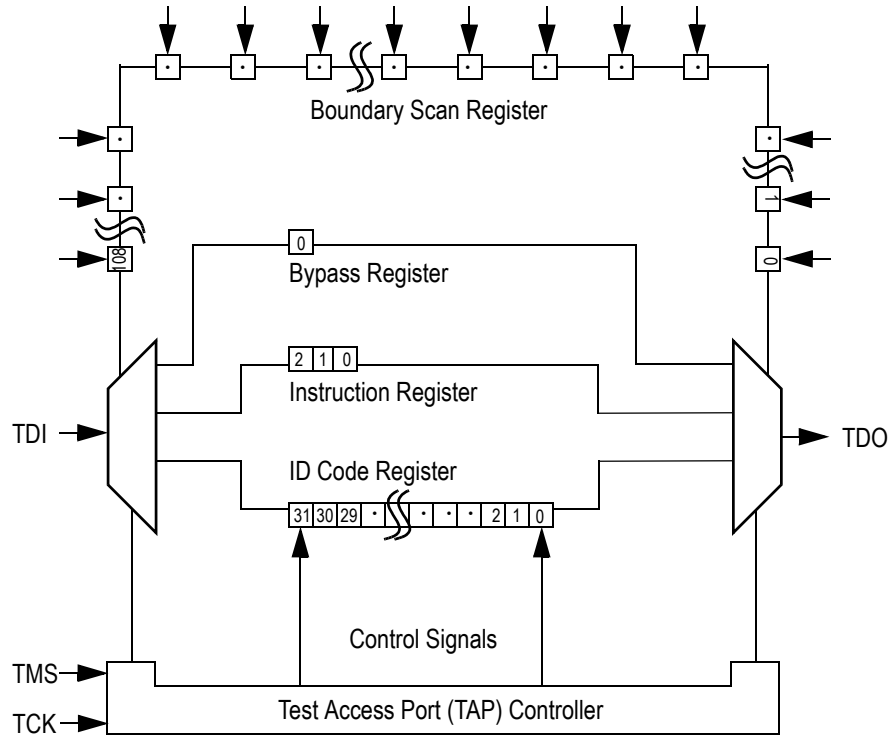
Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code								Presence Register			
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x36	X	X	X	X	0	0	0	X	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1
x18	X	X	X	X	0	0	0	X	1	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	1

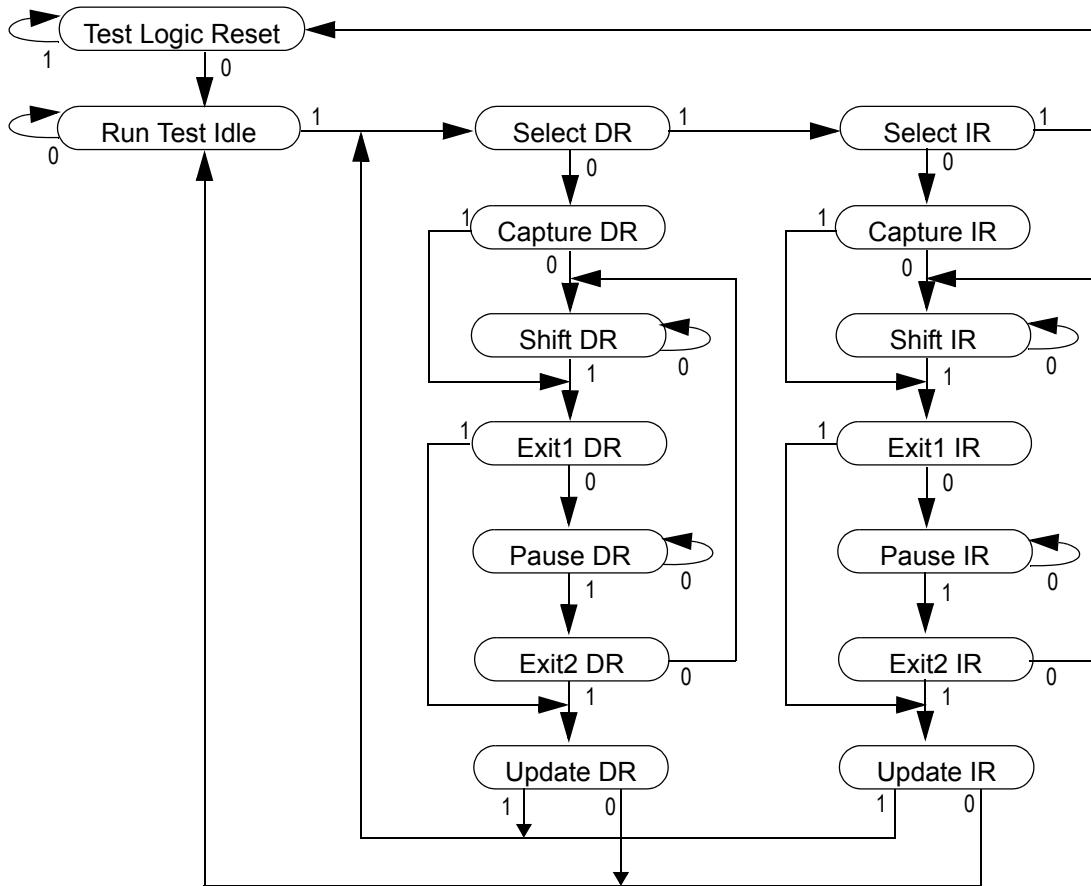
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the state of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:

1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
3.3 V Test Port Input High Voltage	V_{IHJ3}	2.0	$V_{DD3} + 0.3$	V	1
3.3 V Test Port Input Low Voltage	V_{ILJ3}	-0.3	0.8	V	1
2.5 V Test Port Input High Voltage	V_{IHJ2}	$0.6 * V_{DD2}$	$V_{DD2} + 0.3$	V	1
2.5 V Test Port Input Low Voltage	V_{ILJ2}	-0.3	$0.3 * V_{DD2}$	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	-300	1	μ A	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	-1	100	μ A	3
TDO Output Leakage Current	I_{OLJ}	-1	1	μ A	4
Test Port Output High Voltage	V_{OHJ}	1.7	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.4	V	5, 7
Test Port Output CMOS High	V_{OHJC}	$V_{DDQ} - 100$ mV	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	100 mV	V	5, 9

Notes:

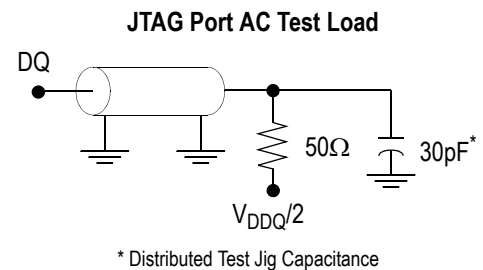
- Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 1.5\text{ V}$ maximum, with a pulse width not to exceed 50% tTKC.
- $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
- $0\text{ V} \leq V_{IN} \leq V_{ILJn}$
- Output Disable, $V_{OUT} = 0$ to V_{DDn}
- The TDO output driver is served by the V_{DDQ} supply.
- $I_{OHJ} = -4\text{ mA}$
- $I_{OLJ} = +4\text{ mA}$
- $I_{OHJC} = -100\text{ }\mu\text{A}$
- $I_{OHJC} = +100\text{ }\mu\text{A}$

JTAG Port AC Test Conditions

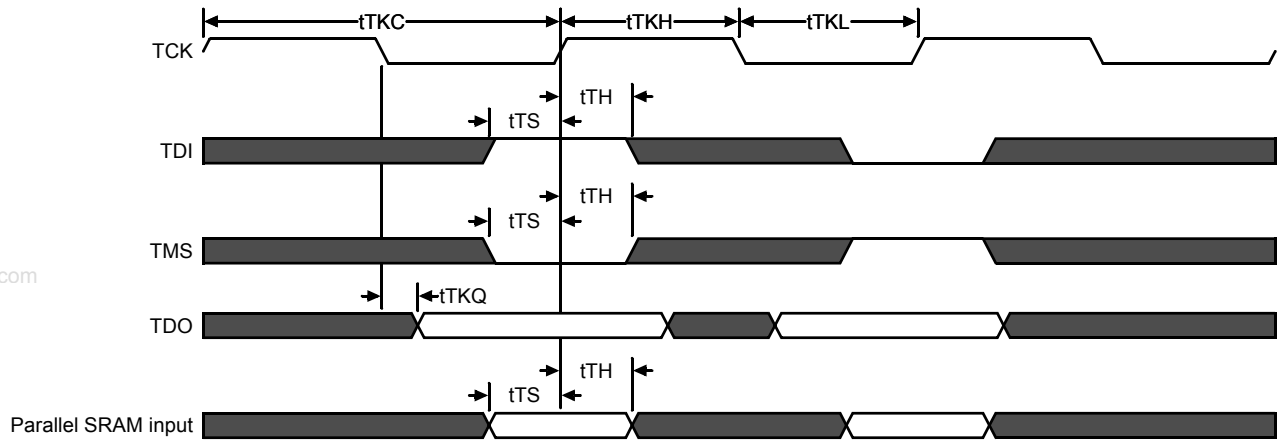
Parameter	Conditions
Input high level	$V_{DD} - 0.2\text{ V}$
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

Notes:

- Include scope and jig capacitance.
- Test conditions as shown unless otherwise noted.



JTAG Port Timing Diagram



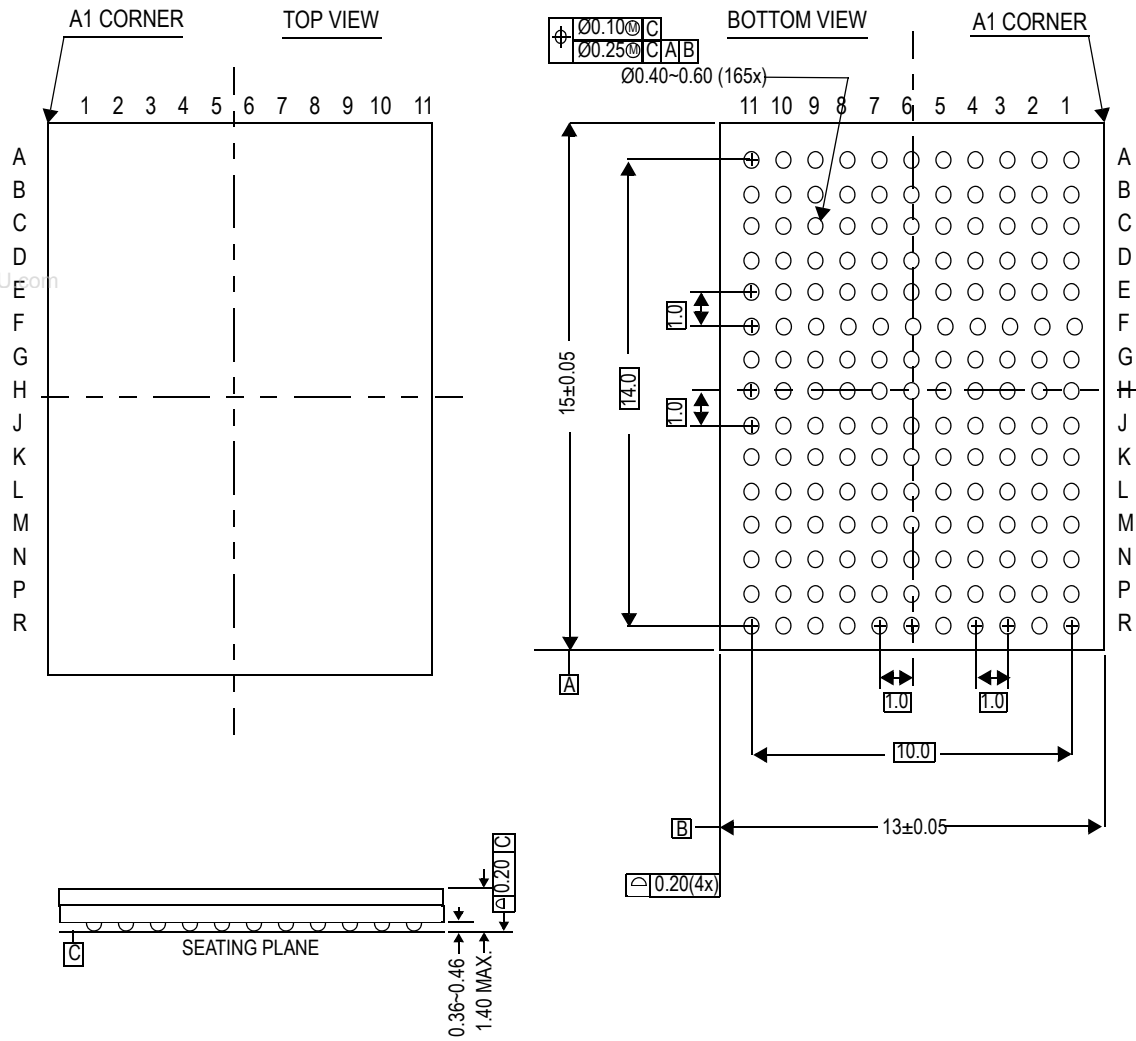
JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	t_{TKC}	50	—	ns
TCK Low to TDO Valid	t_{TKQ}	—	20	ns
TCK High Pulse Width	t_{TKH}	20	—	ns
TCK Low Pulse Width	t_{TKL}	20	—	ns
TDI & TMS Set Up Time	t_{TS}	10	—	ns
TDI & TMS Hold Time	t_{TH}	10	—	ns

Boundary Scan (BSDL Files)

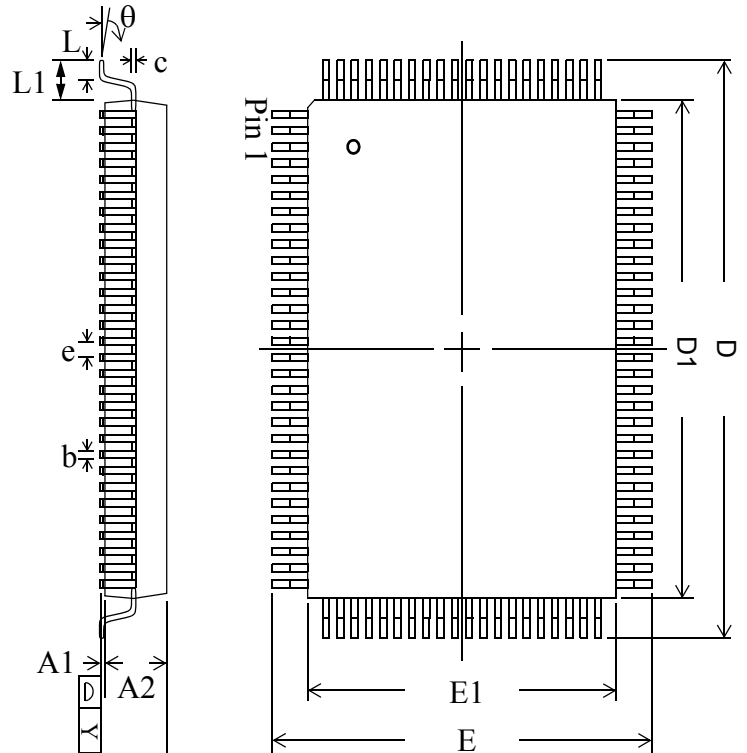
For information regarding the Boundary Scan Chain, or to obtain BSDL files for this part, please contact our Applications Engineering Department at: apps@gsitechnology.com.

Package Dimensions—165-Bump FPBGA (Package D)



TQFP Package Drawing (Package T)

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°



Notes:

1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number ¹	Type	Package	Speed ² (MHz/ns)	T _A ³	Status
1M x 18	GS8161E18BT-250	DCD Pipeline/Flow Through	TQFP	250/5.5	C	MP
1M x 18	GS8161E18BT-200	DCD Pipeline/Flow Through	TQFP	200/6.5	C	MP
1M x 18	GS8161E18BT-150	DCD Pipeline/Flow Through	TQFP	150/7.5	C	MP
1M x 18	GS8161E18BGT-250	DCD Pipeline/Flow Through	RoHS-compliant TQFP	250/5.5	C	PQ
1M x 18	GS8161E18BGT-200	DCD Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	C	PQ
1M x 18	GS8161E18BGT-150	DCD Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	C	PQ
1M x 18	GS8161E18BD-250	DCD Pipeline/Flow Through	165 BGA	250/5.5	C	MP
1M x 18	GS8161E18BD-200	DCD Pipeline/Flow Through	165 BGA	200/6.5	C	MP
1M x 18	GS8161E18BD-150	DCD Pipeline/Flow Through	165 BGA	150/7.5	C	MP
512K x 32	GS8161E32BD-250	DCD Pipeline/Flow Through	165 BGA	250/5.5	C	MP
512K x 32	GS8161E32BD-200	DCD Pipeline/Flow Through	165 BGA	200/6.5	C	MP
512K x 32	GS8161E32BD-150	DCD Pipeline/Flow Through	165 BGA	150/7.5	C	MP
1M x 18	GS8161E18BGD-250	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	250/5.5	C	PQ
1M x 18	GS8161E18BGD-200	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	200/6.5	C	PQ
1M x 18	GS8161E18BGD-150	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	150/7.5	C	PQ
512K x 32	GS8161E32BGD-250	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	250/5.5	C	PQ
512K x 32	GS8161E32BGD-200	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	200/6.5	C	PQ
512K x 32	GS8161E32BGD-150	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	150/7.5	C	PQ
512K x 36	GS8161E36BT-250	DCD Pipeline/Flow Through	TQFP	250/5.5	C	MP
512K x 36	GS8161E36BT-200	DCD Pipeline/Flow Through	TQFP	200/6.5	C	MP
512K x 36	GS8161E36BT-150	DCD Pipeline/Flow Through	TQFP	150/7.5	C	MP
512K x 36	GS8161E36BGT-250	DCD Pipeline/Flow Through	RoHS-compliant TQFP	250/5.5	C	PQ
512K x 36	GS8161E36BGT-200	DCD Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	C	PQ
512K x 36	GS8161E36BGT-150	DCD Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	C	PQ
512K x 36	GS8161E36BD-250	DCD Pipeline/Flow Through	165 BGA	250/5.5	C	MP
512K x 36	GS8161E36BD-200	DCD Pipeline/Flow Through	165 BGA	200/6.5	C	MP
512K x 36	GS8161E36BD-150	DCD Pipeline/Flow Through	165 BGA	150/7.5	C	MP
512K x 36	GS8161E36BGD-250	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	250/5.5	C	PQ
512K x 36	GS8161E36BGD-200	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	200/6.5	C	PQ
512K x 36	GS8161E36BGD-150	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	150/7.5	C	PQ

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number.
- The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
- T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
- GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsistechnology.com) for a complete listing of current offerings.

Ordering Information for GSI Synchronous Burst RAMs (Continued)

Org	Part Number ¹	Type	Package	Speed ² (MHz/ns)	T _A ³	Status
1M x 18	GS8161E18BT-250I	DCD Pipeline/Flow Through	TQFP	250/5.5	I	MP
1M x 18	GS8161E18BT-200I	DCD Pipeline/Flow Through	TQFP	200/6.5	I	MP
1M x 18	GS8161E18BT-150I	DCD Pipeline/Flow Through	TQFP	150/7.5	I	MP
1M x 18	GS8161E18BGT-250I	DCD Pipeline/Flow Through	RoHS-compliant TQFP	250/5.5	I	PQ
1M x 18	GS8161E18BGT-200I	DCD Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	I	PQ
1M x 18	GS8161E18BGT-150I	DCD Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	I	PQ
1M x 18	GS8161E18BD-250I	DCD Pipeline/Flow Through	165 BGA	250/5.5	I	MP
1M x 18	GS8161E18BD-200I	DCD Pipeline/Flow Through	165 BGA	200/6.5	I	MP
1M x 18	GS8161E18BD-150I	DCD Pipeline/Flow Through	165 BGA	150/7.5	I	MP
512K x 32	GS8161E32BD-250I	DCD Pipeline/Flow Through	165 BGA	250/5.5	I	MP
512K x 32	GS8161E32BD-200I	DCD Pipeline/Flow Through	165 BGA	200/6.5	I	MP
512K x 32	GS8161E32BD-150I	DCD Pipeline/Flow Through	165 BGA	150/7.5	I	MP
1M x 18	GS8161E18BGD-250I	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	250/5.5	I	PQ
1M x 18	GS8161E18BGD-200I	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	200/6.5	I	PQ
1M x 18	GS8161E18BGD-150I	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	150/7.5	I	PQ
512K x 32	GS8161E32BGD-250I	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	250/5.5	I	PQ
512K x 32	GS8161E32BGD-200I	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	200/6.5	I	PQ
512K x 32	GS8161E32BGD-150I	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	150/7.5	I	PQ
512K x 36	GS8161E36BT-250I	DCD Pipeline/Flow Through	TQFP	250/5.5	I	MP
512K x 36	GS8161E36BT-200I	DCD Pipeline/Flow Through	TQFP	200/6.5	I	MP
512K x 36	GS8161E36BT-150I	DCD Pipeline/Flow Through	TQFP	150/7.5	I	MP
512K x 36	GS8161E36BGT-250I	DCD Pipeline/Flow Through	RoHS-compliant TQFP	250/5.5	I	PQ
512K x 36	GS8161E36BGT-200I	DCD Pipeline/Flow Through	RoHS-compliant TQFP	200/6.5	I	PQ
512K x 36	GS8161E36BGT-150I	DCD Pipeline/Flow Through	RoHS-compliant TQFP	150/7.5	I	PQ
512K x 36	GS8161E36BD-250I	DCD Pipeline/Flow Through	165 BGA	250/5.5	I	MP
512K x 36	GS8161E36BD-200I	DCD Pipeline/Flow Through	165 BGA	200/6.5	I	MP
512K x 36	GS8161E36BD-150I	DCD Pipeline/Flow Through	165 BGA	150/7.5	I	MP
512K x 36	GS8161E36BGD-250I	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	250/5.5	I	PQ
512K x 36	GS8161E36BGD-200I	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	200/6.5	I	PQ
512K x 36	GS8161E36BGD-150I	DCD Pipeline/Flow Through	RoHS-compliant 165 BGA	150/7.5	I	PQ

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number.
- The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
- T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
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18Mb Sync SRAM Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
8161ExxB_r1		• Creation of new datasheet
8161ExxB_r1; 8161ExxB_r1_01	Content	• Updated overshoot/undershoot information
8161ExxB_r1_01; 8161ExxB_r1_02	Content	<ul style="list-style-type: none"> • Added 300 MHz speed bin • Added Pb-Free information for 165 BGA • Corrected block diagram (added E2 & E3 references) • Corrected truth table (added E2 & E3 references)
8161ExxB_r1_02; 8161ExxB_r1_03	Content	<ul style="list-style-type: none"> • Removed 300 MHz speed bin • Changed Pb-Free to RoHS-compliant • Added Status column to Ordering Information table