

165-Bump BGA  
Commercial Temp  
Industrial Temp

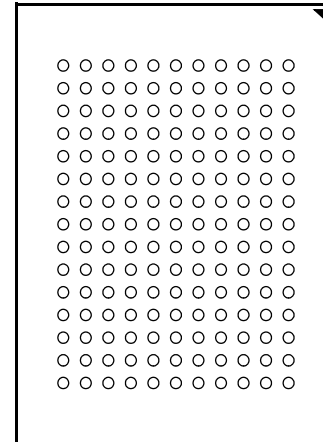


## 18Mb Burst of 2 DDR SigmaSIO-II SRAM

267 MHz–167 MHz  
1.8 V  $V_{DD}$   
1.8 V and 1.5 V I/O

### Features

- Simultaneous Read and Write SigmaQuad™ Interface
- JEDEC-standard pinout and package
- Dual Double Data Rate interface
- Byte Write controls sampled at data-in time
- DLL circuitry for wide output data valid window and future frequency scaling
- Burst of 2 Read and Write
- 1.8 V +150/–100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ mode pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 165-bump, 13 mm x 15 mm, 1 mm bump pitch BGA package
- RoHS-compliant 165-bump BGA package available
- Pin-compatible with future 36Mb, 72Mb, and 144Mb devices



**Bottom View**

**165-Bump, 13 mm x 15 mm BGA**  
**1 mm Bump Pitch, 11 x 15 Bump Array**  
**JEDEC Std. MO-216, Variation CAB-1**

### SigmaRAM™ Family Overview

GS8182S18 are built in compliance with the SigmaSIO-II SRAM pinout standard for Separate I/O synchronous SRAMs. They are 18,874,368-bit (18Mb) SRAMs. These are the first in a family of wide, very low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

### Clocking and Addressing Schemes

A Burst of 2 SigmaSIO-II SRAM is a synchronous device. It employs dual input register clock inputs, K and  $\bar{K}$ . The device also allows the user to manipulate the output register clock input quasi independently with dual output register clock inputs, C and  $\bar{C}$ . If the C clocks are tied high, the K clocks are

routed internally to fire the output registers instead. Each Burst of 2 SigmaSIO-II SRAM also supplies Echo Clock outputs, CQ and  $\bar{CQ}$ , which are synchronized with read data output. When used in a source synchronous clocking scheme, the Echo Clock outputs can be used to fire input registers at the data's destination.

Because Separate I/O Burst of 2 RAMs always transfer data in two packets, A0 is internally set to 0 for the first read or write transfer, and automatically incremented by 1 for the next transfer. Because the LSB is tied off internally, the address field of a Burst of 2 RAM is always one address pin less than the advertised index depth (e.g., the 1M x 18 has a 512K addressable index).

### Parameter Synopsis

	-267	-250	-200	-167
tKHKH	3.75 ns	4.0 ns	5.0 ns	6.0 ns
tKHQV	0.45 ns	0.45 ns	0.45 ns	0.5 ns

## 1M x 18 SigmaQuad SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	V <sub>SS</sub> /SA (144Mb)	NC/SA (36Mb)	R $\overline{\text{W}}$	$\overline{\text{BW1}}$	$\overline{\text{K}}$	NC	$\overline{\text{LD}}$	SA	V <sub>SS</sub> /SA (72Mb)	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{\text{BW0}}$	SA	NC	NC	Q8
C	NC	NC	D10	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	NC	Q7	D8
D	NC	D11	Q10	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	D7
E	NC	NC	Q11	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	D6	Q6
F	NC	Q12	D12	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	Q5
G	NC	D13	Q13	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	D5
H	$\overline{\text{D}}_{\text{OFF}}$	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	NC	NC	D14	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	Q4	D4
K	NC	NC	Q14	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	D3	Q3
L	NC	Q15	D15	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC	Q2
M	NC	NC	D16	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	Q1	D2
N	NC	D17	Q16	V <sub>SS</sub>	SA	SA	SA	V <sub>SS</sub>	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

 11 x 15 Bump BGA—13 x 15 mm<sup>2</sup> Body—1 mm Bump Pitch

**Notes:**

- Expansion addresses: A3 for 36Mb, A10 for 72Mb, A2 for 144Mb
- $\overline{\text{BW0}}$  controls writes to D0:D8.  $\overline{\text{BW1}}$  controls writes to D9:D17.
- It is recommended that H1 be tied low for compatibility with future devices.

## Pin Description Table

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
NC	No Connect	—	—
R/W	Synchronous Read/Write	Input	
$\overline{\text{BW0}}\text{--}\overline{\text{BW1}}$	Synchronous Byte Writes	Input	Active Low
K	Input Clock	Input	Active High
C	Output Clock	Input	Active High
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V <sub>REF</sub>	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
$\overline{\text{K}}$	Input Clock	Input	Active Low
$\overline{\text{C}}$	Output Clock	Output	Active Low
$\overline{\text{D}}_{\text{OFF}}$	DLL Disable	—	Active Low
$\overline{\text{LD}}$	Synchronous Load Pin	—	Active Low
$\overline{\text{CQ}}$	Output Echo Clock	Output	Active Low
CQ	Output Echo Clock	Output	Active High
D	Synchronous Data Inputs	Input	
Q	Synchronous Data Outputs	Output	
V <sub>DD</sub>	Power Supply	Supply	1.8 V Nominal
V <sub>DDQ</sub>	Isolated Output Buffer Supply	Supply	1.8 or 1.5 V Nominal
V <sub>SS</sub>	Power Supply: Ground	Supply	—

### Notes:

1. C,  $\overline{\text{C}}$ , K, or  $\overline{\text{K}}$  cannot be set to V<sub>REF</sub> voltage.
2. When ZQ pin is directly connected to V<sub>DD</sub>, output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. NC = Not Connected to die or any other pin

## Background

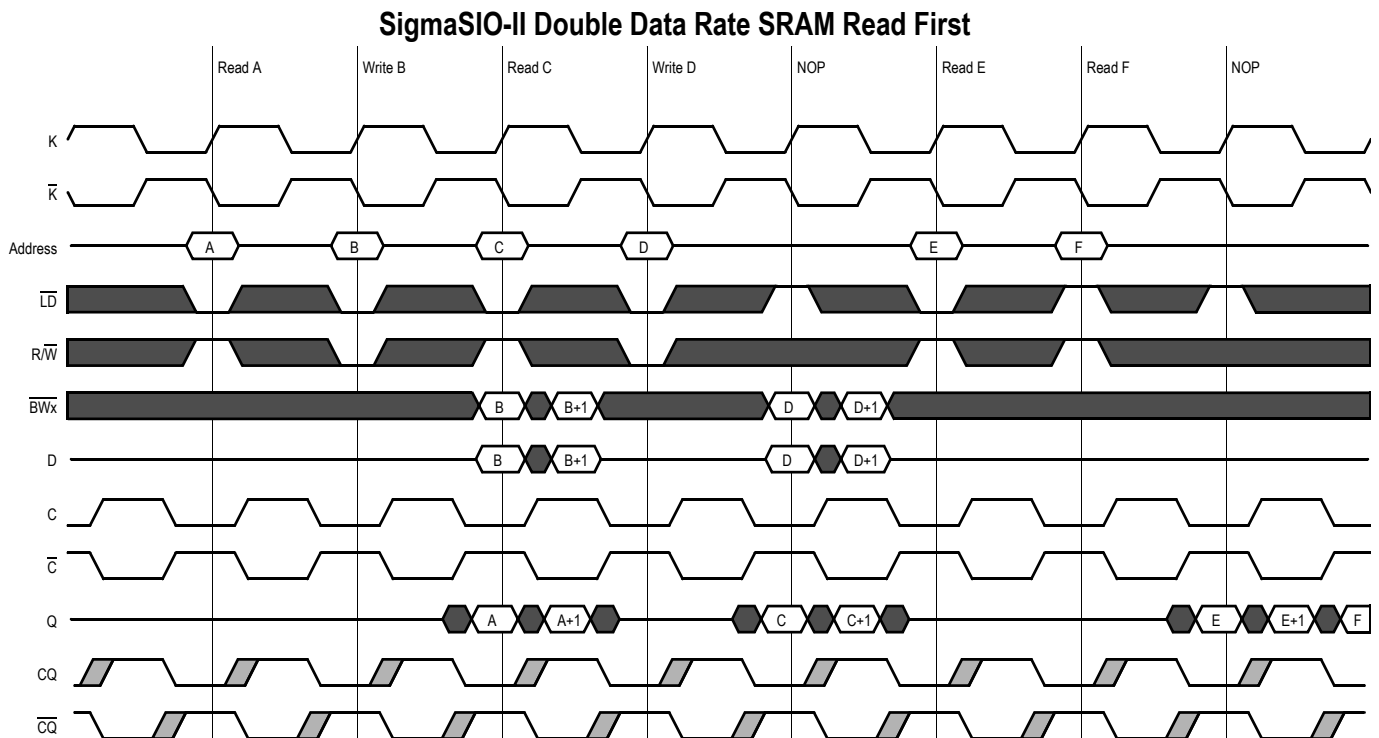
Separate I/O SRAMs, like SigmaQuad SRAMs, are attractive in applications where alternating reads and writes are needed. On the other hand, Common I/O SRAMs like the SigmaCIO family are popular in applications where bursts of read or write traffic are needed. The SigmaSIO SRAM is a hybrid of these two devices. Like the SigmaQuad family devices, the SigmaSIO features a separate I/O data path, offering the user independent Data In and Data Out pins. However, the SigmaSIO devices offer a control protocol like that offered on the SigmaCIO devices. Therefore, while SigmaQuad SRAMs allow a user to operate both data ports at the same time, they force alternating loads of read and write addresses. SigmaSIO SRAMs allow continuous loads of read or write addresses like SigmaCIO SRAMs, but in a separate I/O configuration.

Like a SigmaQuad SRAM, a SigmaSIO-II SRAM can execute an alternating sequence of reads and writes. However, doing so results in the Data In port and the Data Out port stalling with nothing to do on alternate transfers. A SigmaQuad device would keep both ports running at capacity full time. On the other hand, the SigmaSIO device can accept a continuous stream of read commands and read data or a continuous stream of write commands and write data. The SigmaQuad device, by contrast, restricts the user from loading a continuous stream of read or write addresses. The advantage of the SigmaSIO device is that it allows twice the random address bandwidth for either reads or writes than could be achieved with a SigmaQuad version of the device. SigmaCIO SRAMs offer this same advantage, but do not have the separate Data In and Data Out pins offered on the SigmaSIO SRAMs. Therefore, SigmaSIO devices are useful in pseudo dual port SRAM applications where communication of burst traffic between two electrically independent busses is desired.

Each of the three SigmaQuad Family SRAMs—SigmaQuad, SigmaCIO, and SigmaSIO—supports similar address rates because random address rate is determined by the internal performance of the RAM. In addition, all three SigmaQuad Family SRAMs are based on the same internal circuits. Differences between the truth tables of the different devices proceed from differences in how the RAM’s interface is contrived to interact with the rest of the system. Each mode of operation has its own advantages and disadvantages. The user should consider the nature of the work to be done by the RAM to evaluate which version is best suited to the application at hand.

**Burst of 2 SigmaSIO-II SRAM DDR Read**

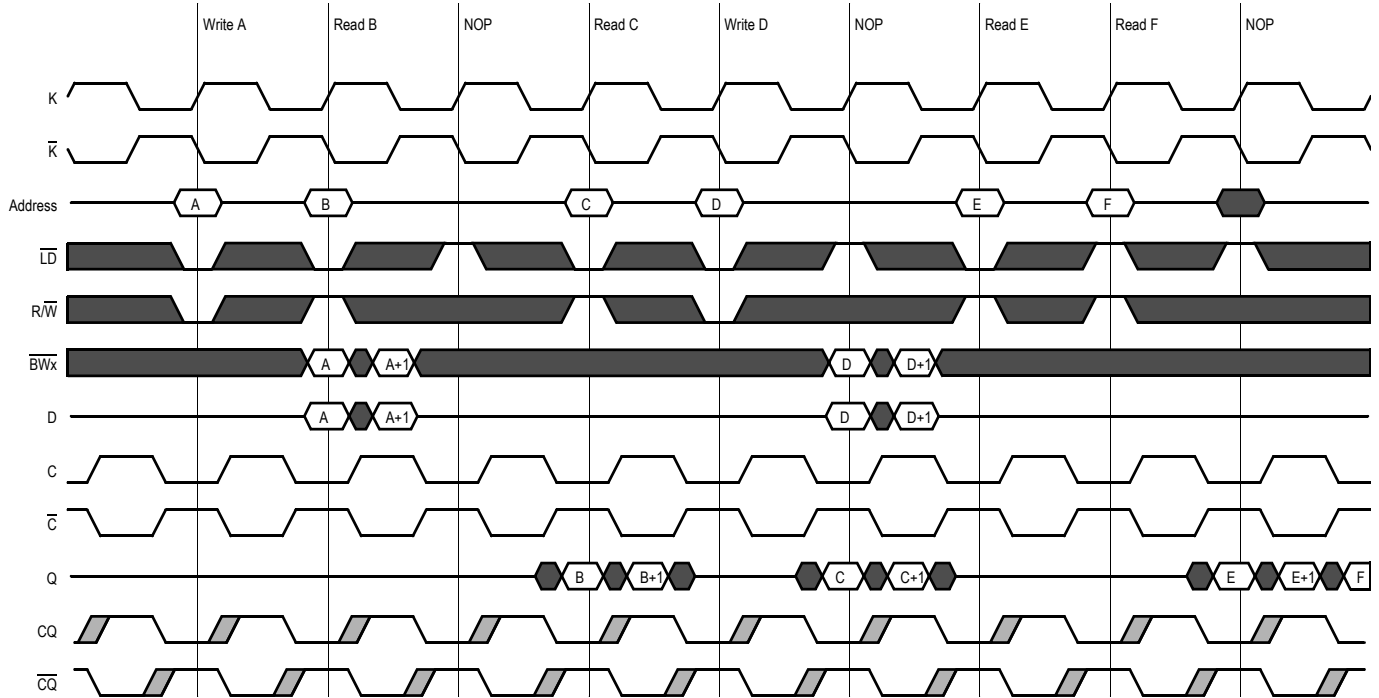
The status of the Address Input, R/W, and LD pins are sampled at each rising edge of K. LD high causes chip disable. A high on the R/W pin begins a read cycle. Data can be clocked out after the next rising edge of K with a rising edge of C (or by K if C and C are tied high), and after the following rising edge of K with a rising edge of C (or by K if C and C are tied high).



**Burst of 2 SigmaSIO-II SRAM DDR Write**

The status of the Address Input,  $R/\overline{W}$ , and  $\overline{LD}$  pins are sampled at each rising edge of  $K$ .  $\overline{LD}$  high causes chip disable. A low on the  $R/\overline{W}$  pin, begins a write cycle. Data is clocked in by the next rising edge of  $K$  and then the rising edge of  $\overline{K}$ .

**SigmaSIO-II Double Data Rate SRAM Write First**



## Special Functions

### Byte Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g.,  $\overline{BW0}$  controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven high or low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 2 beat data transfer. The x18 version of the RAM, for example, may write 36 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

### Example x18 RAM Write Sequence using Byte Write Enables

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
Beat 1	0	1	Data In	Don't Care
Beat 2	1	0	Don't Care	Data In

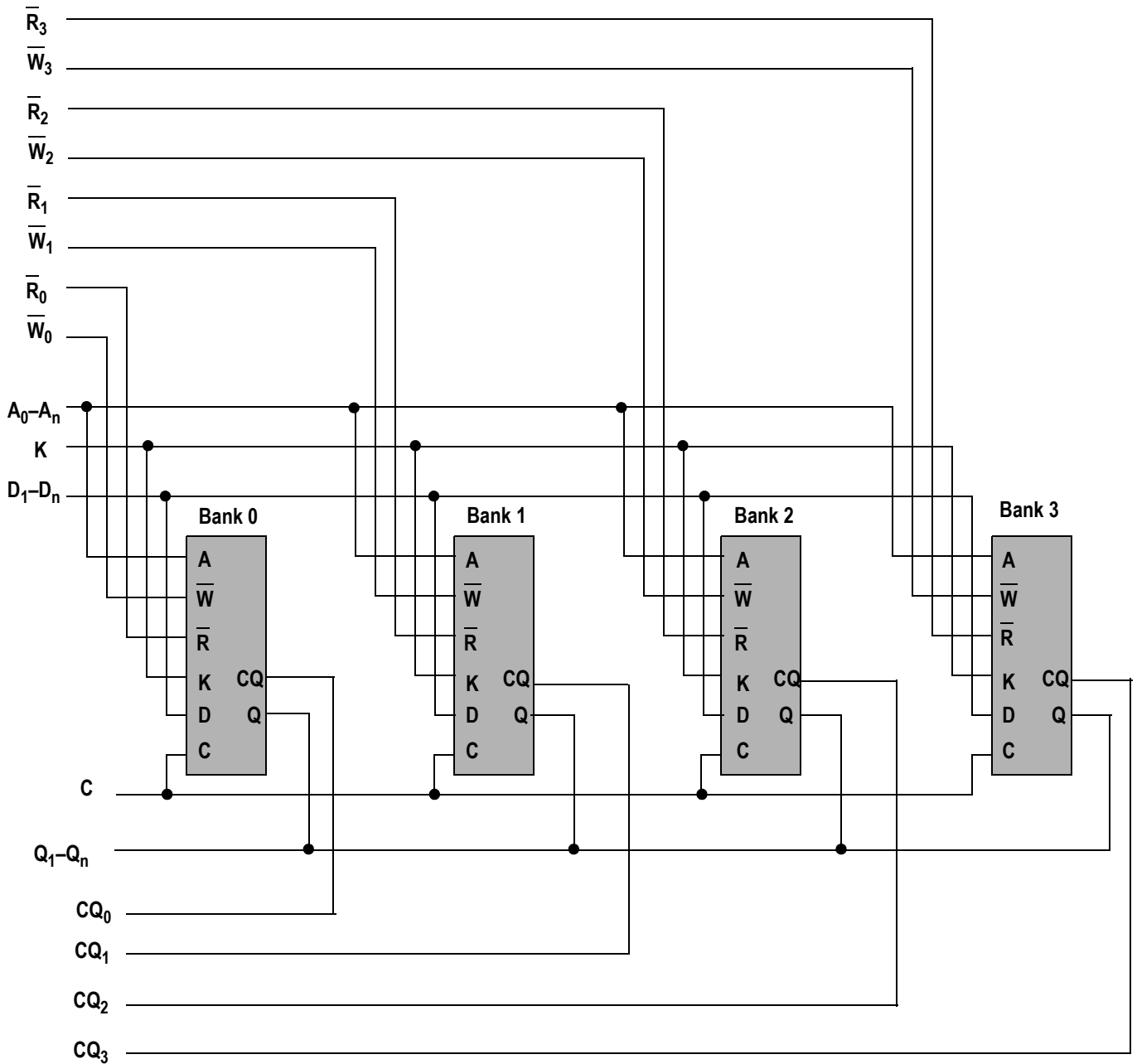
### Resulting Write Operation

Beat 1		Beat 2	
D0–D8	D9–D17	D0–D8	D9–D17
Written	Unchanged	Unchanged	Written

### Output Register Control

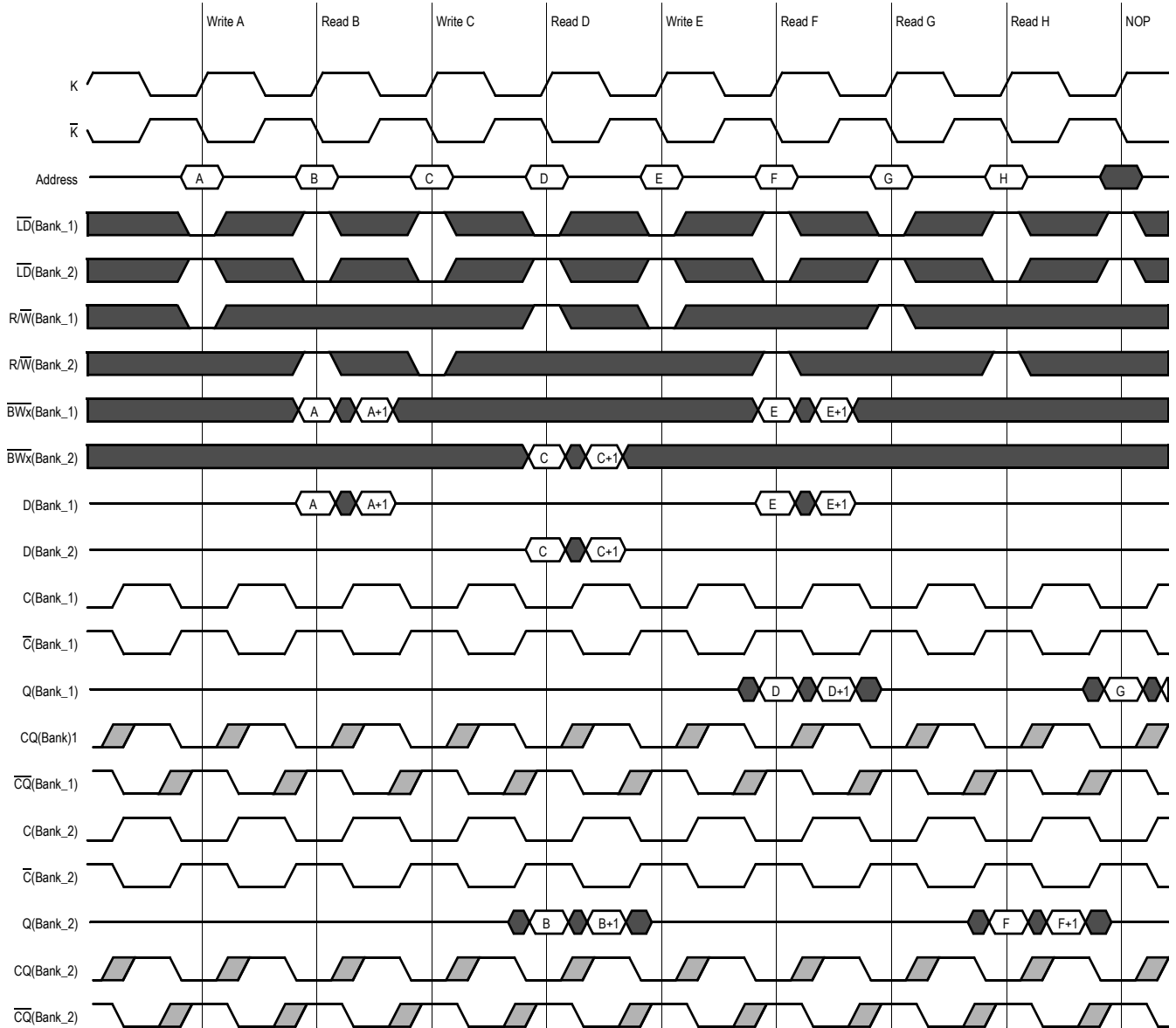
SigmaSIO-II SRAMs offer two mechanisms for controlling the output data registers. Typically, control is handled by the Output Register Clock inputs, C and  $\overline{C}$ . The Output Register Clock inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K and  $\overline{K}$  clocks. If the C and  $\overline{C}$  clock inputs are tied high, the RAM reverts to K and  $\overline{K}$  control of the outputs.

Example Four Bank Depth Expansion Schematic



**Note:**  
For simplicity  $\overline{BWN}$  is not shown.

**Burst of 2 SigmaSIO-II SRAM Depth Expansion**



**FLXDrive-II Output Driver Impedance Control**

HSTL I/O SigmaSIO-II SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to  $V_{SS}$  via an external resistor,  $R_Q$ , to allow the SRAM to monitor and adjust its output driver impedance. The value of  $R_Q$  must be 5X the value of the intended line impedance driven by the SRAM. The allowable range of  $R_Q$  to guarantee impedance matching with a vendor-specified tolerance is between  $150\Omega$  and  $300\Omega$ . Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. The SRAM's output impedance circuitry compensates for drifts in supply voltage and temperature every 1024 cycles. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.



**Separate I/O Burst of 2 SigmaSIO-II SRAM Truth Table**

A	$\overline{\text{LD}}$	$\text{R}/\overline{\text{W}}$	Current Operation	D	D	Q	Q
$\text{K} \uparrow$ ( $t_n$ )	$\text{K} \uparrow$ ( $t_n$ )	$\text{K} \uparrow$ ( $t_n$ )	$\text{K} \uparrow$ ( $t_n$ )	$\text{K} \uparrow$ ( $t_{n+1}$ )	$\overline{\text{K}} \uparrow$ ( $t_{n+1}$ )	$\text{K} \uparrow$ ( $t_{n+1}$ )	$\overline{\text{K}} \uparrow$ ( $t_{n+1}$ )
X	1	X	Deselect	X	—	Hi-Z	—
V	0	1	Read	X	—	Q0	Q1
V	0	0	Write	D0	D1	Hi-Z	—

**Notes:**

1. "1" = input "high"; "0" = input "low"; "V" = input "valid"; "X" = input "don't care"
2. "—" indicates that the input requirement or output state is determined by the next operation.
3. Q0 and Q1 indicate the first and second pieces of output data transferred during Read operations.
4. D0 and D1 indicate the first and second pieces of input data transferred during Write operations.
5. Qs are tristated for one cycle in response to Deselect and Write commands, one cycle after the command is sampled, except when preceded by a Read command.
6. CQ is never tristated.
7. Users should not clock in metastable addresses.

**x18 Byte Write Clock Truth Table**

$\overline{BW}$	$\overline{BW}$	Current Operation	D	D
$K \uparrow$ ( $t_{n+1}$ )	$K \uparrow$ ( $t_{n+2}$ )	$K \uparrow$ ( $t_n$ )	$K \uparrow$ ( $t_{n+1}$ )	$K \uparrow$ ( $t_{n+2}$ )
T	T	Write Dx stored if $\overline{BWn} = 0$ in both data transfers	D1	D2
T	F	Write Dx stored if $\overline{BWn} = 0$ in 1st data transfer only	D1	X
F	T	Write Dx stored if $\overline{BWn} = 0$ in 2nd data transfer only	X	D2
F	F	Write Abort No Dx stored in either data transfer	X	X

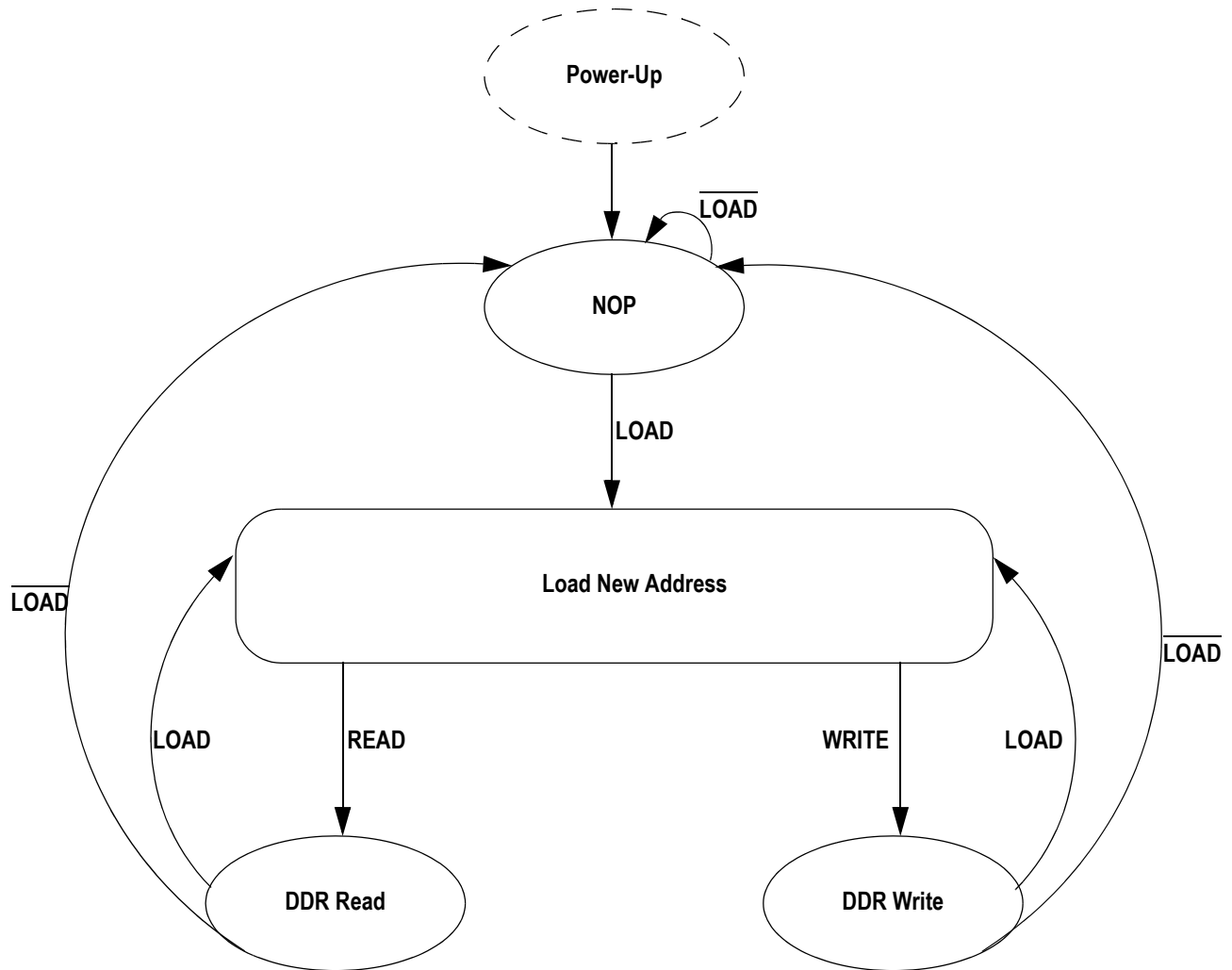
**Notes:**

1. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
2. If one or more  $\overline{BWn} = 0$ , then  $\overline{BW} = "T"$ , else  $\overline{BW} = "F"$ .

**x18 Byte Write Enable ( $\overline{BWn}$ ) Truth Table**

$\overline{BW1}$	$\overline{BW0}$	D9–D17	D0–D8
1	1	Don't Care	Don't Care
0	1	Don't Care	Data In
1	0	Data In	Don't Care
0	0	Data In	Data In

State Diagram



## Absolute Maximum Ratings

(All voltages reference to  $V_{SS}$ )

Symbol	Description	Value	Unit
$V_{DD}$	Voltage on $V_{DD}$ Pins	-0.5 to 2.9	V
$V_{DDQ}$	Voltage in $V_{DDQ}$ Pins	-0.5 to $V_{DD}$	V
$V_{REF}$	Voltage in $V_{REF}$ Pins	-0.5 to $V_{DDQ}$	V
$V_{I/O}$	Voltage on I/O Pins	-0.5 to $V_{DDQ} + 0.3$ ( $\leq 2.9$ V max.)	V
$V_{IN}$	Voltage on Other Input Pins	-0.5 to $V_{DDQ} + 0.3$ ( $\leq 2.9$ V max.)	V
$I_{IN}$	Input Current on Any Pin	+/-100	mA dc
$I_{OUT}$	Output Current on Any I/O Pin	+/-100	mA dc
$T_J$	Maximum Junction Temperature	125	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature	-55 to 125	$^{\circ}\text{C}$
$T_{SUB}$	Storage Under Bias	-50 to 100	$^{\circ}\text{C}$

### Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

## Recommended Operating Conditions

### Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	$V_{DD}$	1.7	1.8	1.95	V	
1.5 V I/O Supply Voltage	$V_{DDQ}$	1.4	1.5	1.65	V	1
1.8 V I/O Supply Voltage	$V_{DDQ}$	1.7	1.8	1.95	V	1
Reference Voltage	$V_{REF}$	0.68	—	0.95	V	1

### Notes:

- Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both  $1.4\text{ V} \leq V_{DDQ} \leq 1.6\text{ V}$  (i.e., 1.5 V I/O) and  $1.7\text{ V} \leq V_{DDQ} \leq 1.95\text{ V}$  (i.e., 1.8 V I/O) and quoted at whichever condition is worst case.
- The power supplies need to be powered up simultaneously or in the following sequence:  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$ , followed by signal inputs. The power down sequence must be the reverse.  $V_{DDQ}$  must not exceed  $V_{DD}$ .

## Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature (Commercial Range Versions)	$T_A$	0	25	70	$^{\circ}\text{C}$	2
Ambient Temperature (Industrial Range Versions)	$T_A$	-40	25	85	$^{\circ}\text{C}$	2

### HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
DC Input Logic High	$V_{IH} (dc)$	$V_{REF} + 0.1$	$V_{DDQ} + 0.3$	mV	1
DC Input Logic Low	$V_{IL} (dc)$	-0.3	$V_{REF} - 0.1$	mV	1

**Note:**

Compatible with both 1.8 V and 1.5 V I/O drivers

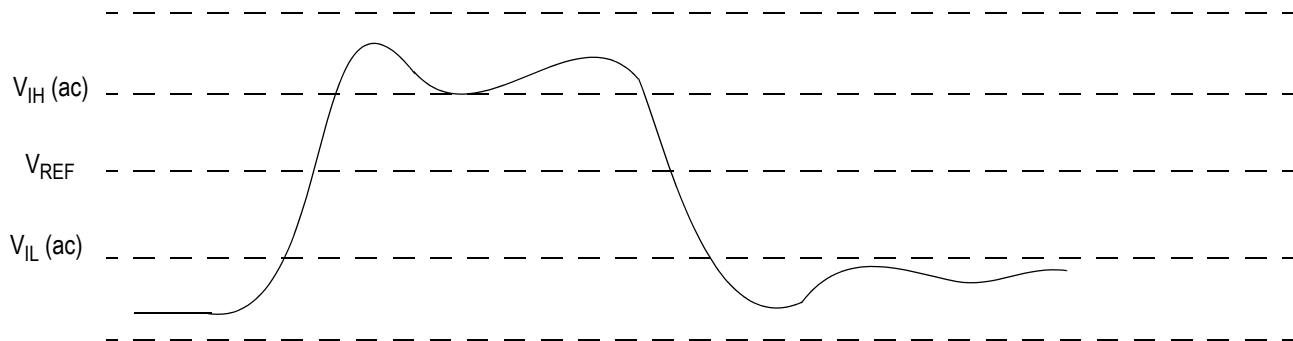
### HSTL I/O AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	$V_{IH} (ac)$	$V_{REF} + 0.2$	—	mV	3,4
AC Input Logic Low	$V_{IL} (ac)$	—	$V_{REF} - 0.2$	mV	3,4
$V_{REF}$ Peak to Peak AC Voltage	$V_{REF} (ac)$	—	5% $V_{REF} (DC)$	mV	1

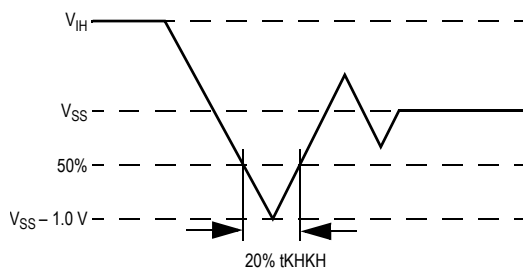
**Notes:**

1. The peak to peak AC component superimposed on  $V_{REF}$  may not exceed 5% of the DC component of  $V_{REF}$ .
2. To guarantee AC characteristics,  $V_{IH}, V_{IL}, Trise,$  and  $Tfall$  of inputs and clocks must be within 10% of each other.
3. For devices supplied with HSTL I/O input buffers. Compatible with both 1.8 V and 1.5 V I/O drivers.
4. See AC Input Definition drawing below.

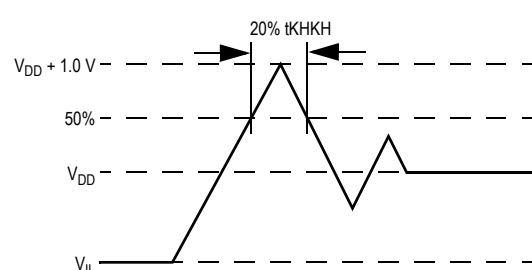
### HSTL I/O AC Input Definitions



### Undershoot Measurement and Timing



### Overshoot Measurement and Timing



## Capacitance

( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{DD} = 3.3\text{ V}$ )

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$	4	5	pF
Output Capacitance	$C_{OUT}$	$V_{OUT} = 0\text{ V}$	6	7	pF

**Note:**

This parameter is sample tested.

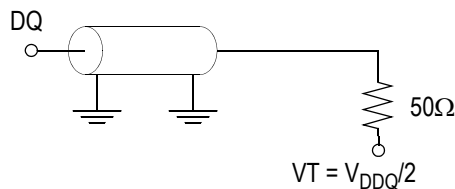
## AC Test Conditions

Parameter	Conditions
Input high level	$V_{DDQ}$
Input low level	0 V
Max. input slew rate	2 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$

**Note:**

Test conditions as specified with output loading as shown unless otherwise noted.

## AC Test Load Diagram



$$R_Q = 250\ \Omega \text{ (HSTL I/O)}$$

$$V_{REF} = 0.75\text{ V}$$

## Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max	Notes
Input Leakage Current (except mode pins)	$I_{IL}$	$V_{IN} = 0\text{ to }V_{DD}$	-2 $\mu\text{A}$	2 $\mu\text{A}$	
Output Leakage Current	$I_{OL}$	Output Disable, $V_{OUT} = 0\text{ to }V_{DDQ}$	-2 $\mu\text{A}$	2 $\mu\text{A}$	

**Programmable Impedance HSTL Output Driver DC Electrical Characteristics**

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	$V_{OH1}$	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	1, 3
Output Low Voltage	$V_{OL1}$	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	2, 3
Output High Voltage	$V_{OH2}$	$V_{DDQ} - 0.2$	$V_{DDQ}$	V	4, 5
Output Low Voltage	$V_{OL2}$	$V_{SS}$	0.2	V	4, 6

**Notes:**

- $I_{OH} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$  @  $V_{OH} = V_{DDQ}/2$  (for:  $175\Omega \leq RQ \leq 350\Omega$ ).
- $I_{OL} = (V_{DDQ}/2) / (RQ/5) \pm 15\%$  @  $V_{OL} = V_{DDQ}/2$  (for:  $175\Omega \leq RQ \leq 350\Omega$ ).
- Parameter tested with  $RQ = 250\Omega$  and  $V_{DDQ} = 1.5$  V or 1.8 V
- Minimum Impedance mode,  $ZQ = V_{SS}$
- $I_{OH} = -1.0$  mA
- $I_{OL} = 1.0$  mA

**Operating Currents**

Parameter	Org	Symbol	-267		-250		-200		-167		Test Conditions
			0°C to 70°C	-40°C to +85°C	0°C to 70°C	-40°C to +85°C	0°C to 70°C	-40°C to +85°C	0°C to 70°C	-40°C to +85°C	
Operating Current	x18	IDD	475 mA	485 mA	450 mA	460 mA	400 mA	410 mA	350 mA	360 mA	$V_{DD} = \text{max.}; I_{OUT} = 0$ mA; Cycle Time $\geq t_{KHKH}$ min.
Standby Current (NOP)	x18	ISB1	230 mA	235 mA	220 mA	225 mA	205 mA	210 mA	195 mA	200 mA	Device deselected; $I_{OUT} = 0$ mA; $f = \text{max.}$ ; All inputs $\leq 0.2$ V or $\geq V_{DD} - 0.2$ V

**Notes:**

- Power measured with output pins floating.
- All inputs (except ZQ,  $V_{REF}$ ) are held at either  $V_{IH}$  or  $V_{IL}$ .
- Operating supply currents are measured at 100% buss utilization.
- NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.

**AC Electrical Characteristics**

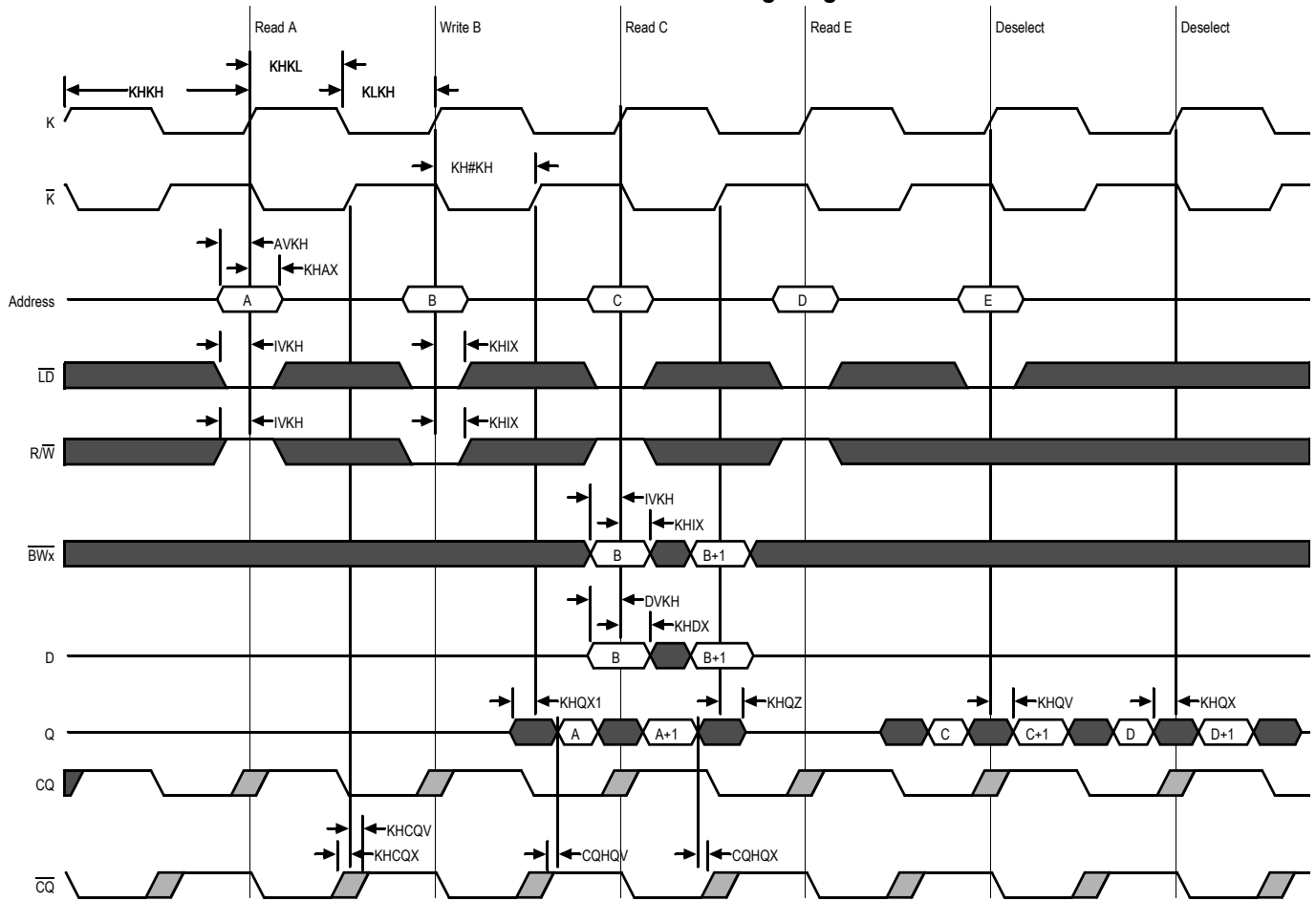
Parameter	Symbol	-267		-250		-200		-167		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
K Clock Cycle Time C Clock Cycle Time	$t_{KHKH}$ $t_{CHCH}$	3.75	6.3	4.0	6.3	5.0	7.88	6.0	8.4	ns	
K Clock High Pulse Width C Clock High Pulse Width	$t_{KHKL}$ $t_{CHCL}$	1.6	—	1.6	—	2.0	—	2.4	—	ns	
K Clock Low Pulse Width C Clock Low Pulse Width	$t_{KLKH}$ $t_{CLCH}$	1.6	—	1.6	—	2.0	—	2.4	—	ns	
Clock to $\overline{\text{Clock}}$ Delay	$t_{KH\overline{K}H}$ $t_{CH\overline{C}H}$	1.8	—	1.8	—	2.3	—	2.8	—	ns	
Address Input Setup Time	$t_{AVKH}$	0.5	—	0.5	—	0.6	—	0.7	—	ns	
Address Input Hold Time	$t_{KHAX}$	0.5	—	0.5	—	0.6	—	0.7	—	ns	
Control Input Setup Time	$t_{BVKH}$	0.5	—	0.5	—	0.6	—	0.7	—	ns	1
Control Input Hold Time	$t_{KH BX}$	0.5	—	0.5	—	0.6	—	0.7	—	ns	1
Data and Byte Write Input Setup Time	$t_{DVKH}$	0.35	—	0.35	—	0.4	—	0.5	—	ns	
Data and Byte Write Input Hold Time	$t_{KHDX}$	0.35	—	0.35	—	0.4	—	0.5	—	ns	
K Clock High to Data Output Valid C Clock High to Data Output Valid	$t_{KHQV}$ $t_{CHQV}$	—	0.45	—	0.45	—	0.45	—	0.5	ns	
K Clock High to Data Output Hold C Clock High to Data Output Hold	$t_{KHQX}$ $t_{CHQX}$	-0.45	—	-0.45	—	-0.45	—	-0.5	—	ns	2
K Clock High to Data Output Low-Z C Clock High to Data Output Low-Z	$t_{KHQX1}$ $t_{CHQX1}$	-0.45	—	-0.45	—	-0.45	—	-0.5	—	ns	2,3
K Clock High to Data Output High-Z C Clock High to Data Output High-Z	$t_{KHQZ}$ $t_{CHQZ}$	—	0.45	—	0.45	—	0.45	—	0.5	ns	2,3
K Clock High to CQ Clock High C Clock High to CQ Clock High	$t_{KHCQV}$ $t_{CHCQV}$	—	0.45	—	0.45	—	0.45	—	0.5	ns	
K Clock High to CQ Clock Hold C Clock High to CQ Clock Hold	$t_{KHCQX}$ $t_{CHCQX}$	-0.45	—	-0.45	—	-0.45	—	-0.5	—	ns	2
CQ Clock High to Data Output Valid	$t_{CQH QV}$	—	0.3	—	0.3	—	0.35	—	0.4	ns	2
CQ Clock High to Data Output Hold	$t_{CQH QX}$	-0.3	—	-0.3	—	-0.35	—	-0.4	—	ns	2

**Notes:**

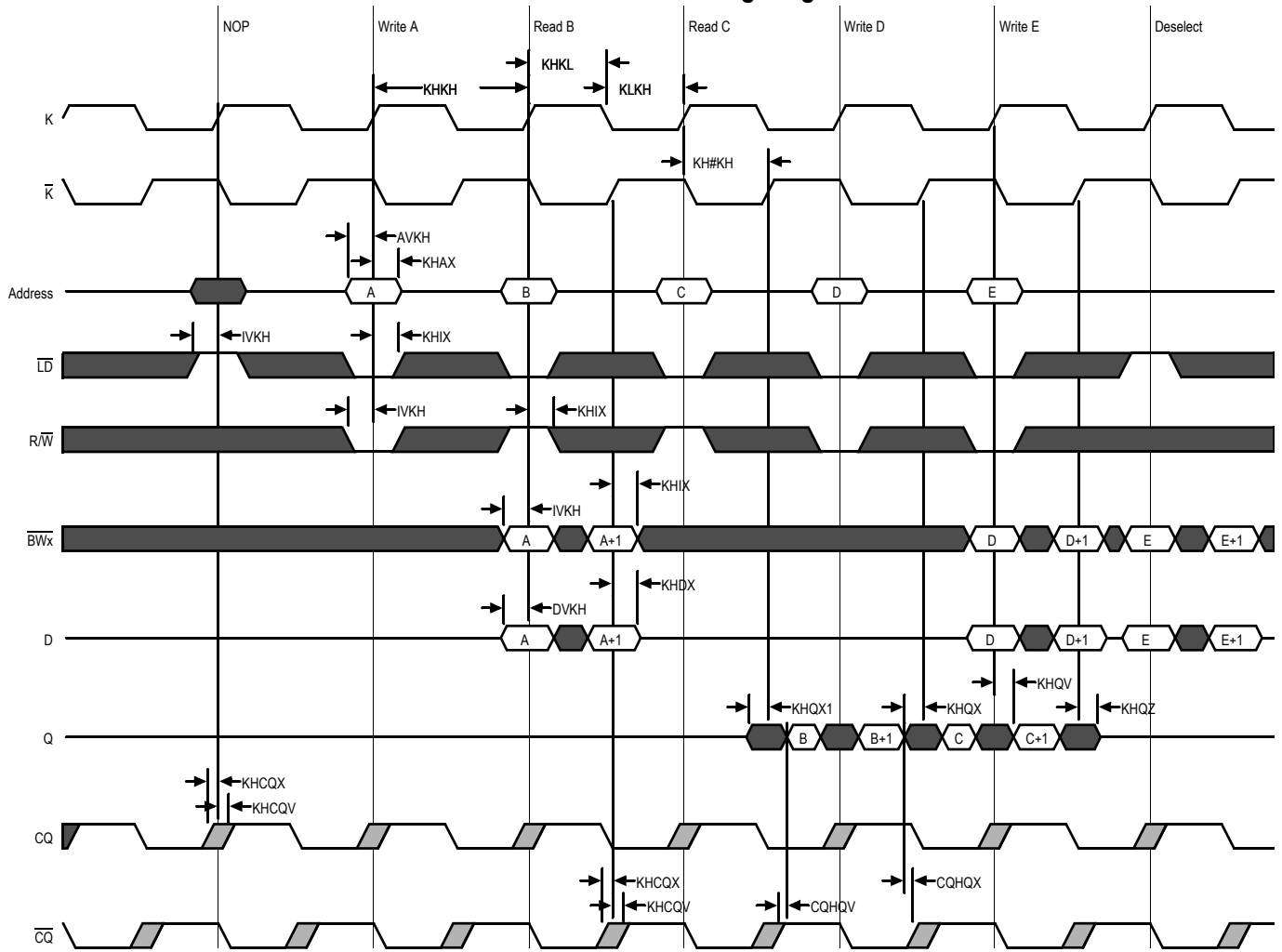
1. These parameters apply to control inputs  $\overline{R}$  and  $\overline{W}$ .
2. These parameters are guaranteed by design through extensive corner lot characterization.
3. These parameters are measured at  $\pm 50$  mV from steady state voltage.



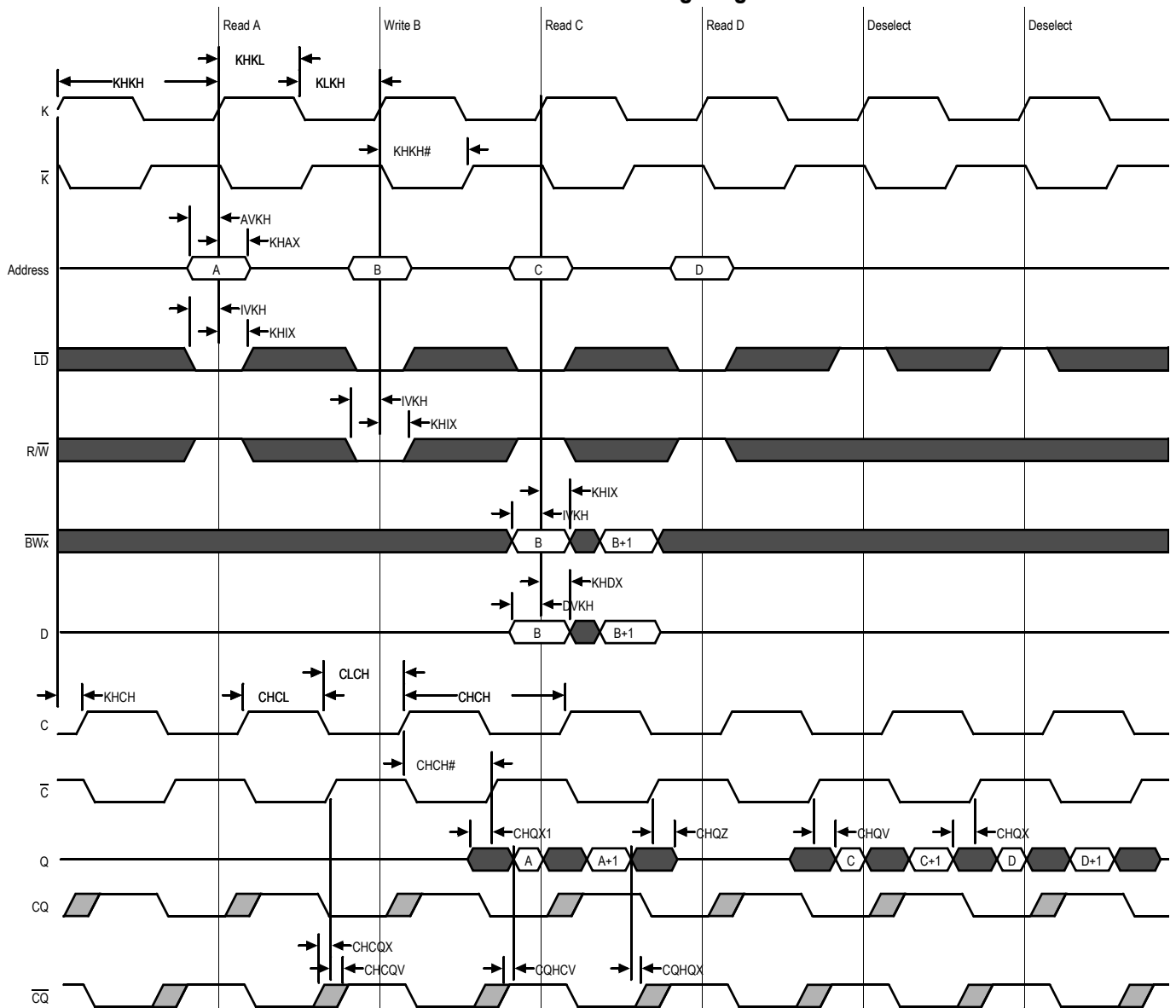
### K Controlled Read-First Timing Diagram



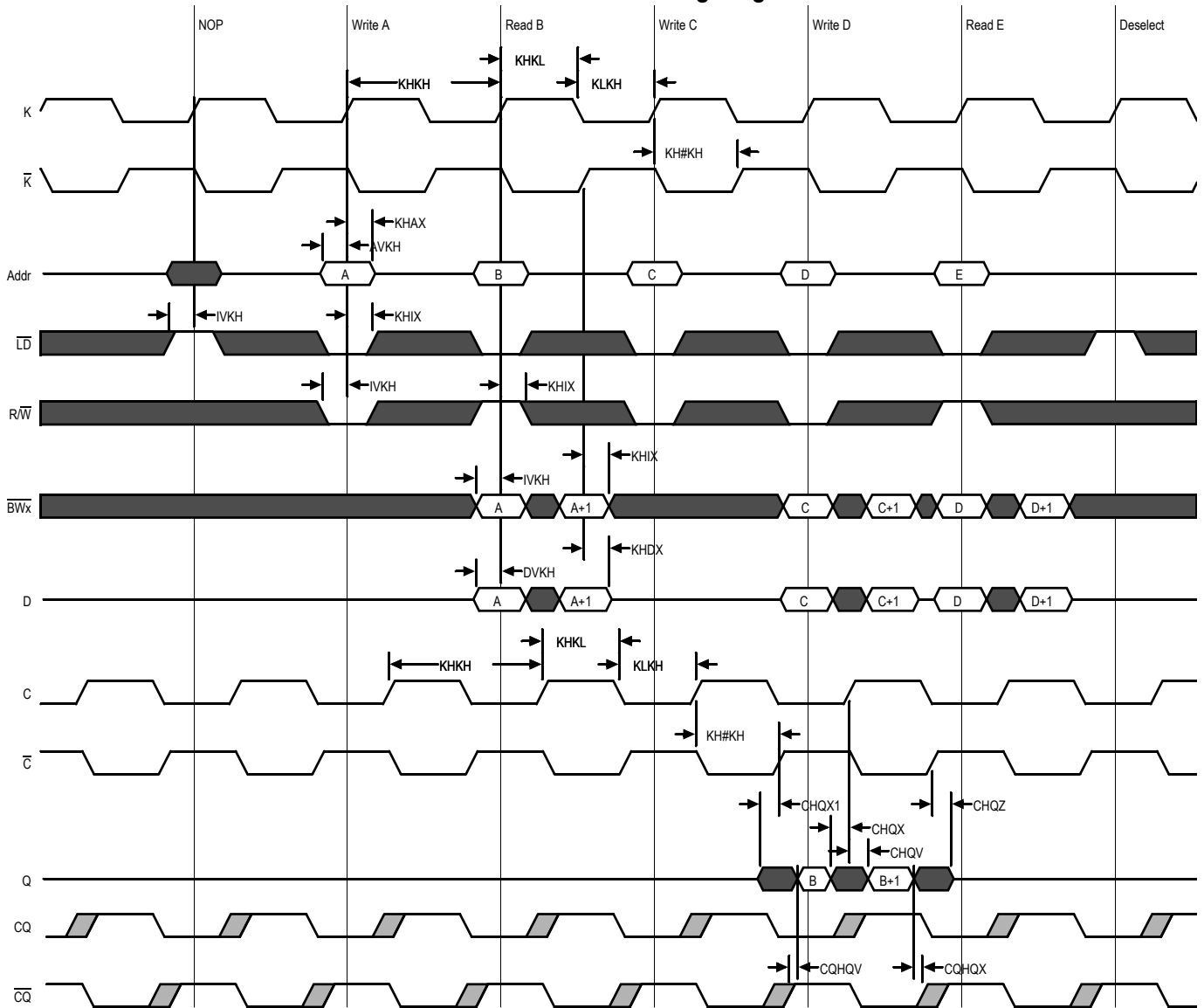
### K Controlled Write-First Timing Diagram



### C Controlled Read-First Timing Diagram



### C Controlled Write-First Timing Diagram



## JTAG Port Operation

### Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with  $V_{DD}$ . The JTAG output drivers are powered by  $V_{DDQ}$ .

### Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either  $V_{DD}$  or  $V_{SS}$ . TDO should be left unconnected.

## JTAG Port Registers

### JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

### Note:

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automatically at power-up.

### Overview

The various JTAG registers, referred to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

### Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

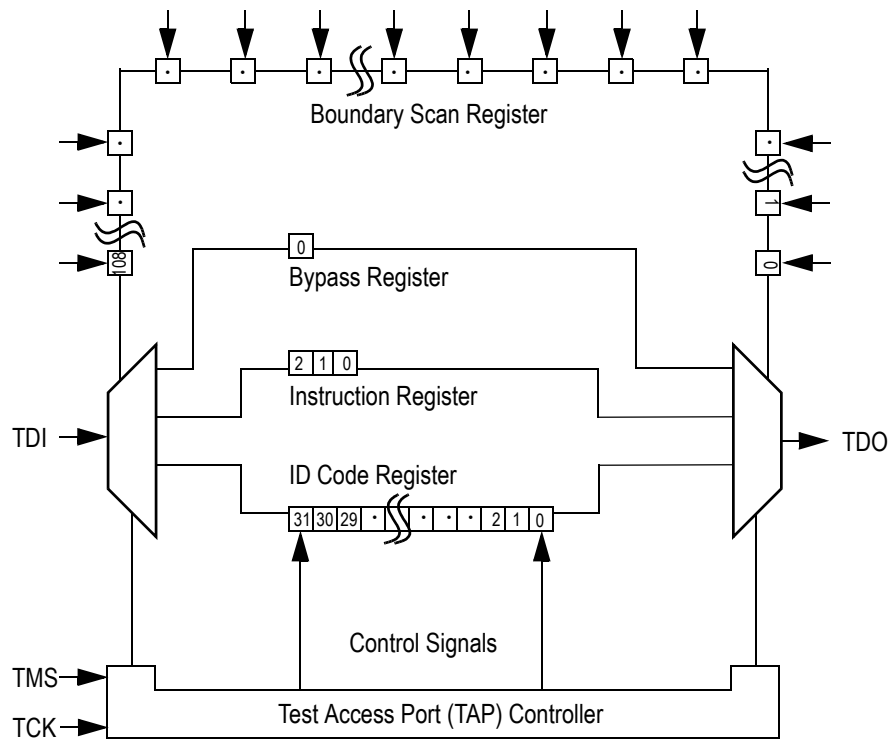
### Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

**Boundary Scan Register**

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

**JTAG TAP Block Diagram**



**Identification (ID) Register**

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents TBD for this part.

**Tap Controller Instruction Set  
ID Register Contents**

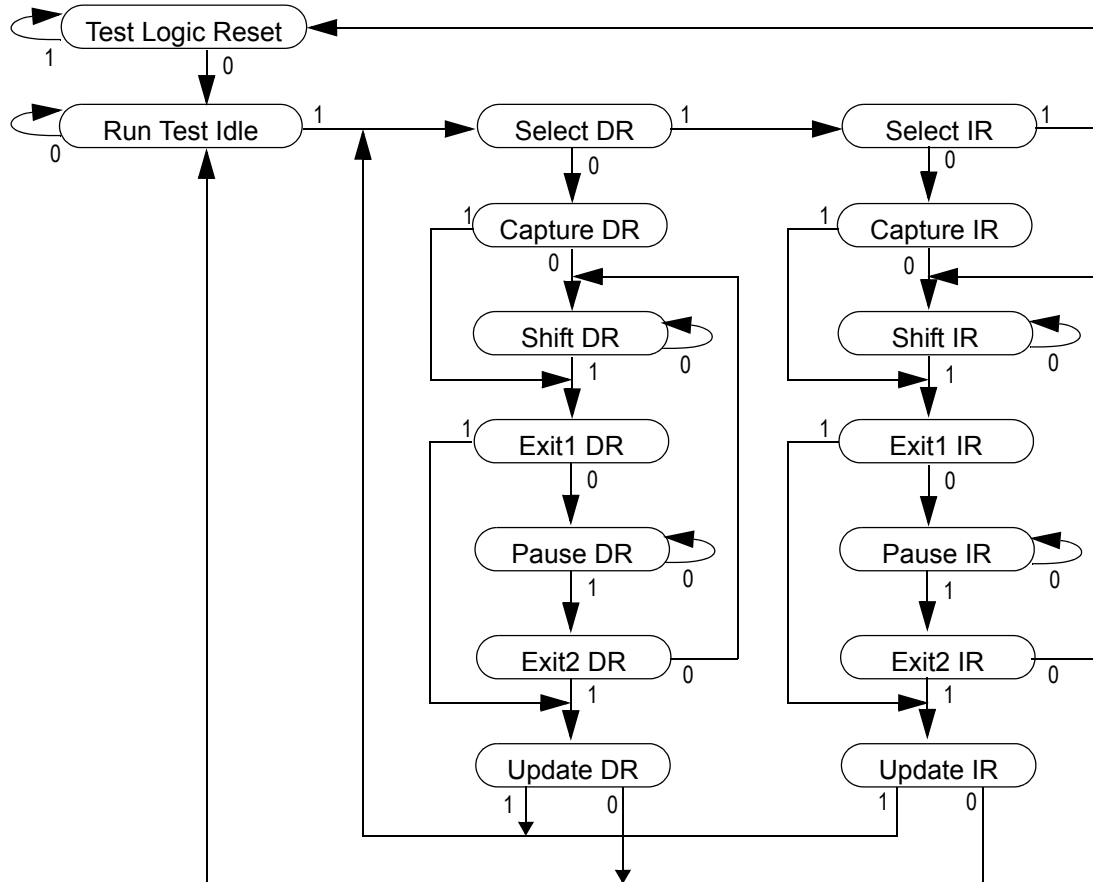
	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code								Presence Register			
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x18	X	X	X	X	0	0	0	X	1	0	0	0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	1

**Overview**

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

### JTAG Tap Controller State Diagram



#### Instruction Descriptions

##### BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

##### SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time ( $t_{TS}$  plus  $t_{TH}$ ). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

##### EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.



Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the state of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

#### **IDCODE**

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

#### **SAMPLE-Z**

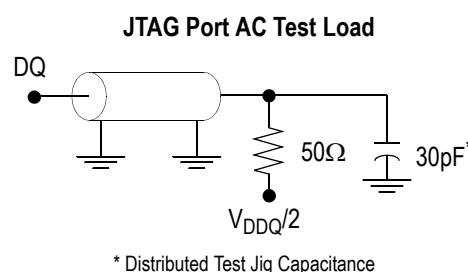
If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

#### **RFU**

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

**JTAG Port AC Test Conditions**

Parameter	Conditions
Input high level	$V_{DD} - 0.2 V$
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DDQ}/2$
Output reference level	$V_{DDQ}/2$


**Notes:**

1. Include scope and jig capacitance.
2. Test conditions as shown unless otherwise noted.

**JTAG TAP Instruction Set Summary**

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

**Notes:**

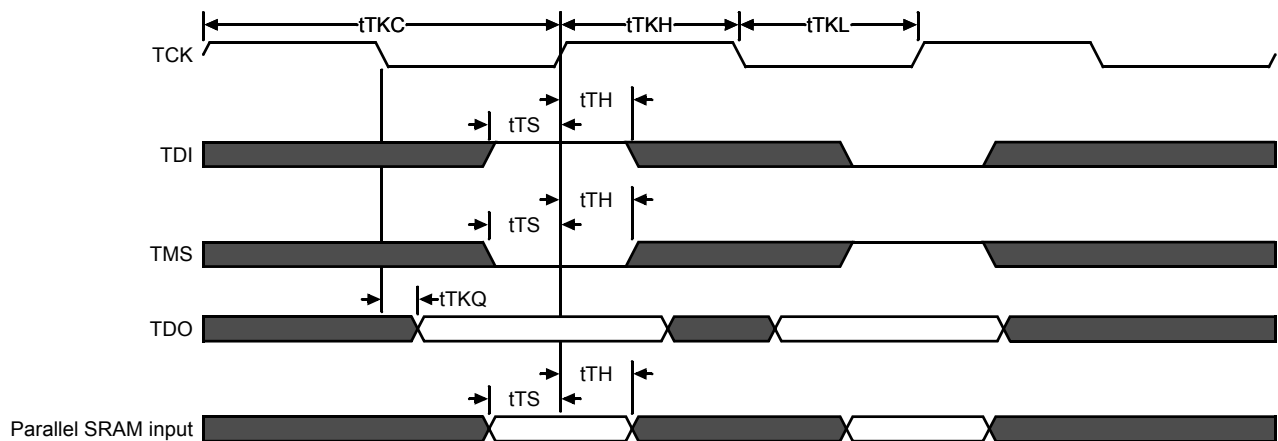
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

**JTAG Port Recommended Operating Conditions and DC Characteristics**

Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input High Voltage	$V_{IHJ}$	$0.6 * V_{DD}$	$V_{DD2} + 0.3$	V	1
Test Port Input Low Voltage	$V_{ILJ}$	-0.3	$0.3 * V_{DD}$	V	1
TMS, TCK and TDI Input Leakage Current	$I_{INHJ}$	-300	1	$\mu A$	2
TMS, TCK and TDI Input Leakage Current	$I_{INLJ}$	-1	100	$\mu A$	3
TDO Output Leakage Current	$I_{OLJ}$	-1	1	$\mu A$	4
Test Port Output High Voltage	$V_{OHJ}$	1.7	—	V	5, 6
Test Port Output Low Voltage	$V_{OLJ}$	—	0.4	V	5, 7
Test Port Output CMOS High	$V_{OHJC}$	$V_{DDQ} - 100 \text{ mV}$	—	V	5, 8
Test Port Output CMOS Low	$V_{OLJC}$	—	100 mV	V	5, 9

**Notes:**

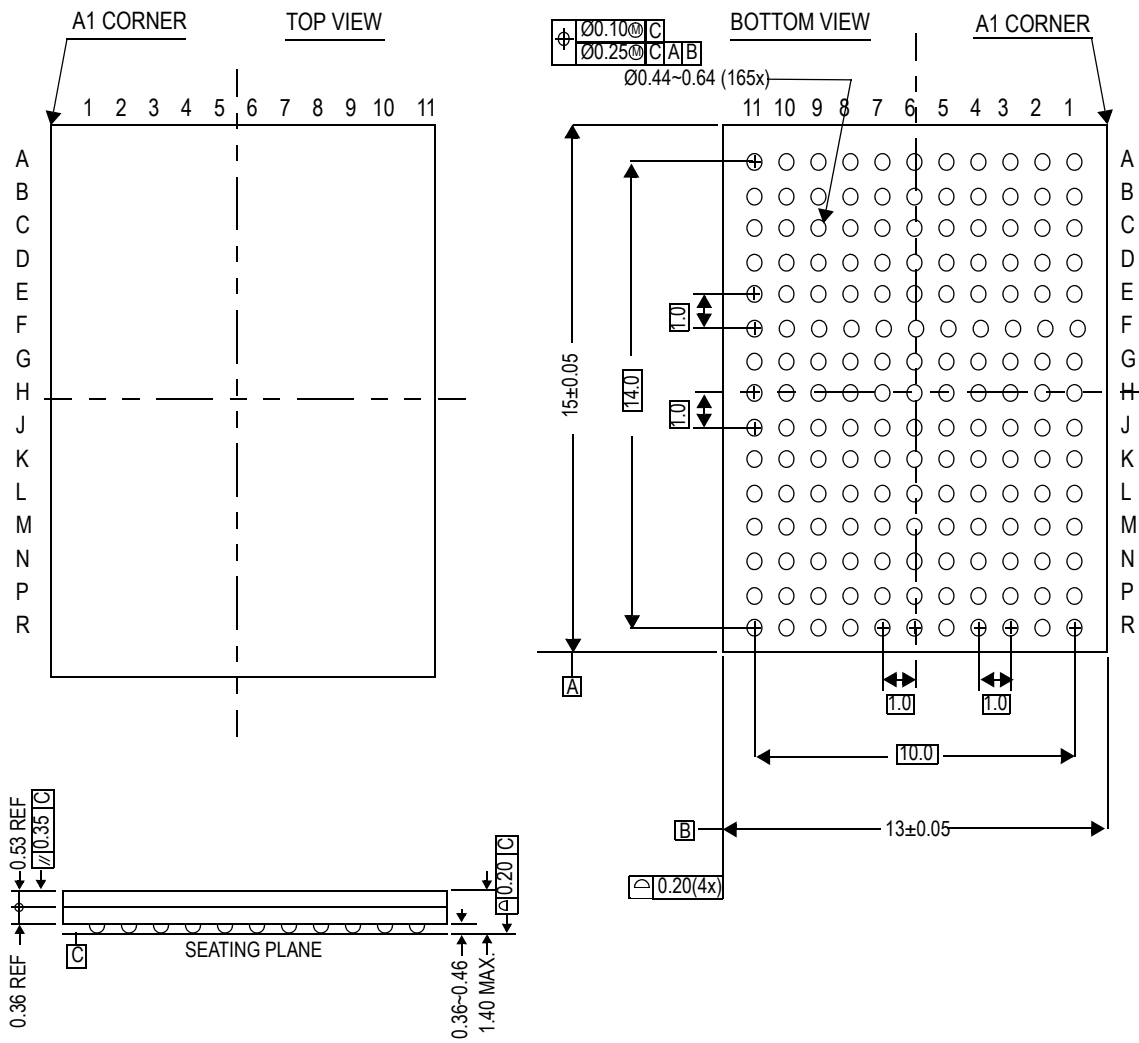
- Input Under/overshoot voltage must be  $-1 \text{ V} < V_i < V_{DD} + 1 \text{ V}$  not to exceed 2.9 V maximum, with a pulse width not to exceed 20% tTKC.
- $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
- $0 \text{ V} \leq V_{IN} \leq V_{ILJn}$
- Output Disable,  $V_{OUT} = 0$  to  $V_{DDn}$
- The TDO output driver is served by the  $V_{DDQ}$  supply.
- $I_{OHJ} = -4 \text{ mA}$
- $I_{OLJ} = +4 \text{ mA}$
- $I_{OHJC} = -100 \text{ }\mu A$
- $I_{OHJC} = +100 \text{ }\mu A$

**JTAG Port Timing Diagram**


**JTAG Port AC Electrical Characteristics**

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

Package Dimensions—165-Bump FPBGA (Package D; Variation 3)



**Ordering Information—GSI SigmaSIO-II SRAM**

Org	Part Number <sup>1</sup>	Type	Package	Speed (MHz)	T <sub>A</sub> <sup>3</sup>	Status
1M x 18	GS8182S18D-267	SigmaSIO-II SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	267	C	MP
1M x 18	GS8182S18D-250	SigmaSIO-II SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	250	C	MP
1M x 18	GS8182S18D-200	SigmaSIO-II SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	200	C	MP
1M x 18	GS8182S18D-167	SigmaSIO-II SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	167	C	MP
1M x 18	GS8182S18D-267I	SigmaSIO-II SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	267	I	MP
1M x 18	GS8182S18D-250I	SigmaSIO-II SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	250	I	MP
1M x 18	GS8182S18D-200I	SigmaSIO-II SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	200	I	MP
1M x 18	GS8182S18D-167I	SigmaSIO-II SRAM	1 mm Pitch, 165-Pin BGA (var. 3)	167	I	MP
1M x 18	GS8182S18GD-267	SigmaSIO-II SRAM	RoHS-compliant 1 mm Pitch, 165-Pin BGA (var. 3)	267	C	PQ
1M x 18	GS8182S18GD-250	SigmaSIO-II SRAM	RoHS-compliant 1 mm Pitch, 165-Pin BGA (var. 3)	250	C	PQ
1M x 18	GS8182S18GD-200	SigmaSIO-II SRAM	RoHS-compliant 1 mm Pitch, 165-Pin BGA (var. 3)	200	C	PQ
1M x 18	GS8182S18GD-167	SigmaSIO-II SRAM	RoHS-compliant 1 mm Pitch, 165-Pin BGA (var. 3)	167	C	PQ
1M x 18	GS8182S18GD-267I	SigmaSIO-II SRAM	RoHS-compliant 1 mm Pitch, 165-Pin BGA (var. 3)	267	I	PQ
1M x 18	GS8182S18GD-250I	SigmaSIO-II SRAM	RoHS-compliant 1 mm Pitch, 165-Pin BGA (var. 3)	250	I	PQ
1M x 18	GS8182S18GD-200I	SigmaSIO-II SRAM	RoHS-compliant 1 mm Pitch, 165-Pin BGA (var. 3)	200	I	PQ
1M x 18	GS8182S18GD-167I	SigmaSIO-II SRAM	RoHS-compliant 1 mm Pitch, 165-Pin BGA (var. 3)	167	I	PQ

**Notes:**

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS8182S18D-250T.
2. T<sub>A</sub> = C = Commercial Temperature Range. T<sub>A</sub> = I = Industrial Temperature Range.
3. MP = Mass Production. PQ = Pre-Qualification.

**SigmaSIO-II Revision History**

File Name	Format/Content	Description of changes
8182Sxx_r1		Creation of datasheet
8182Sxx_r1; 8182Sxx_r1_01	Content	<ul style="list-style-type: none"> <li>• Changed 330 MHz to 333MHz</li> <li>• Removed any references to 133 MHz or 100 MHz</li> </ul>
8182Sxx_r1_01; 8182Sxx_r1_02	Content	<ul style="list-style-type: none"> <li>• Updated AC spec information</li> </ul>
8182Sxx_r1_02; 8182Sxx_r1_03	Content	<ul style="list-style-type: none"> <li>• Comprehensive rewrite, including (but not limited to) tables, pinouts, and timing diagrams</li> </ul>
8182Sxx_r1_03; 8182Sxx_r1_04	Content	<ul style="list-style-type: none"> <li>• Removed x36 configuration</li> <li>• Removed 333 and 300 MHz speed bins</li> <li>• Updated format</li> </ul>
8182Sxx_r1_04; 8182Sxx_r1_05	Content	<ul style="list-style-type: none"> <li>• Updated timing diagrams</li> <li>• Corrected erroneous VDD information in pin description table</li> <li>• Deleted erroneous sentent in FLXDrive section</li> </ul>
8182Sxx_r1_05; 8182Sxx_r1_06	Content	<ul style="list-style-type: none"> <li>• Added 165 BGA Pb-Free information</li> <li>• Added Storage Under Bias information</li> <li>• Incorporated IDD information into Operating Currents table</li> <li>• Updated Test Conditions for Operating Currents table</li> <li>• Added max numbers for tKHKH and tCHCH in AC Char. table</li> <li>• Added Clock to /Clock Delay timing to AC Char. table</li> </ul>
8182Sxx_r1_06; 8182Sxx_r1_07	Content	<ul style="list-style-type: none"> <li>• Updated timing diagrams</li> </ul>
8182Sxx_r1_07; 8182Sxx_r1_08	Content	<ul style="list-style-type: none"> <li>• Added 267 MHz speed bin</li> </ul>