119-Bump BGA
Commercial Temp
Industrial Temp

512K x 18, 256K x 36 8Mb S/DCD Sync Burst SRAMs

200 MHz–133 MHz
3.3 V V_{DD}
3.3 V and 2.5 V I/O

Features

- FT pin for user-configurable flow through or pipelined operation
- Single/Dual Cycle Deselect Selectable
- ZQ mode pin for user-selectable high/low output drive strength
- 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- LBO pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to SCD x18/x36 Interleaved Pipeline mode
- Byte Write (BW) and/or Global Write (GW) operation
- Common data inputs and data outputs
- Clock Control, registered, address, data, and control
- Internal self-timed write cycle
- Automatic power-down for portable applications
- 119-bump BGA package

		-200	-180	-166	-150	-133	Unit
Pipeline 3-1-1-1	tCycle	5.0	5. 5	6.0	6.7	7.5	ns
	t_{KQ}	3.0	3.2	3.5	3.8	4.0	ns
	I_{DD}	450	410	380	350	340	mA
Flow Through 2-1-1-1	t_{KQ}	7.5	8	8.5	9.0	9.5	ns
	tCycle	10	10	10	10	10	ns
	I_{DD}	270	270	250	240	220	mA

Functional Description

Applications

The GS88418/36B is a 9,437,184-bit high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enables (E1, in x18 version, E1 and E2 in x36 version), address burst control inputs (ADSP, ADSC, ADV), and write control inputs (Bx, BW, GW) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable (G) and power-down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either ADSP or ADSC inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by ADV. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order (LBO) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the FT mode bump (Bump 5R). Holding the FT mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding FT high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

SCD and DCD Pipelined Reads

The GS88436B is a SCD (Single Cycle Deselect) and DCD (Dual Cycle Deselect) pipelined synchronous SRAM. DCD SRAMs pipeline disable commands to the same degree as read commands. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock. The user may configure this SRAM for either mode of operation using the SCD mode input on Bump 4L.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable (BW) input combined with one or more individual byte write signals (Bx). In addition, Global Write (GW) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

FLXDrive™

The ZQ pin allows selection between high drive strength (ZQ low) for multi-drop bus applications and normal drive strength (ZQ floating or high) point-to-point applications. See the Output Driver Characteristics chart for details.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

Core and Interface Voltages

The GS884B operates on a 3.3 V power supply and all inputs/outputs are 3.3 V- and 2.5 V-compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuit.

GS88436 Pad Out

119-Bump BGA—Top View

	1	2	3	4	5	6	7
A	V_{DDQ}	A_6	A_7	$\overline{ADSP}$	A_8	A_9	V_{DDQ}
B	NC	E_2	A_4	$\overline{ADSC}$	A_{15}	A_{17}	NC
C	NC	A_5	A_3	V_{DD}	A_{14}	A_{16}	NC
D	DQ_{C4}	DQ_{PC9}	V_{SS}	ZQ	V_{SS}	DQ_{PB9}	DQ_{B4}
E	DQ_{C3}	DQ_{C8}	V_{SS}	$\overline{E}_1$	V_{SS}	DQ_{B8}	DQ_{B3}
F	V_{DDQ}	DQ_{C7}	V_{SS}	$\overline{G}$	V_{SS}	DQ_{B7}	V_{DDQ}
G	DQ_{C2}	DQ_{C6}	$\overline{B}_C$	$\overline{ADV}$	$\overline{B}_B$	DQ_{B6}	DQ_{B2}
H	DQ_{C1}	DQ_{C5}	V_{SS}	$\overline{GW}$	V_{SS}	DQ_{B5}	DQ_{B1}
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	DQ_{D1}	DQ_{D5}	V_{SS}	CK	V_{SS}	DQ_{A5}	DQ_{A1}
L	DQ_{D2}	DQ_{D6}	$\overline{B}_D$	SCD	$\overline{B}_A$	DQ_{A6}	DQ_{A2}
M	V_{DDQ}	DQ_{D7}	V_{SS}	$\overline{BW}$	V_{SS}	DQ_{A7}	V_{DDQ}
N	DQ_{D3}	DQ_{D8}	V_{SS}	A_1	V_{SS}	DQ_{A8}	DQ_{A3}
P	DQ_{D4}	DQ_{PD9}	V_{SS}	A_0	V_{SS}	DQ_{PA9}	DQ_{A4}
R	NC	A_2	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A_{13}	NC
T	NC	NC	A_{10}	A_{11}	A_{12}	NC	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

GS88418 Pad Out

119-Bump BGA—Top View

	1	2	3	4	5	6	7
A	V_{DDQ}	A_6	A_7	$\overline{ADSP}$	A_8	A_9	V_{DDQ}
B	NC	NC	A_4	$\overline{ADSC}$	A_{15}	A_{17}	NC
C	NC	A_5	A_3	V_{DD}	A_{14}	A_{16}	NC
D	DQ_{B1}	NC	V_{SS}	ZQ	V_{SS}	DQ_{A9}	NC
E	NC	DQ_{B2}	V_{SS}	$\overline{E}_1$	V_{SS}	NC	DQ_{A8}
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQ_{A7}	V_{DDQ}
G	NC	DQ_{B3}	$\overline{B}_B$	$\overline{ADV}$	NC	NC	DQ_{A6}
H	DQ_{B4}	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_{A5}	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_{B5}	V_{SS}	CK	V_{SS}	NC	DQ_{A4}
L	DQ_{B6}	NC	NC	SCD	$\overline{B}_A$	DQ_{A3}	NC
M	V_{DDQ}	DQ_{B7}	V_{SS}	$\overline{BW}$	V_{SS}	NC	V_{DDQ}
N	DQ_{B8}	NC	V_{SS}	A_1	V_{SS}	DQ_{A2}	NC
P	NC	DQ_{B9}	V_{SS}	A_0	V_{SS}	NC	DQ_{A1}
R	NC	A_2	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A_{13}	NC
T	NC	A_{10}	A_{11}	NC	A_{12}	A_{18}	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

GS88418/36 BGA Pin Description

Pin Location	Symbol	Type	Description
P4, N4	A_0, A_1	I	Address field LSBs and Address Counter Preset Inputs
A2, A3, A5, A6, B3, B5, C2, C3, C5, C6, G4, R2, R6, T3, T5	An	I	Address Inputs
T4	An	I	Address Inputs (x36 Version)
T2, T6	NC	—	No Connect (x36 Version)
T2, T6	An	I	Address Inputs (x18 Version)
K7, L7, N7, P7, K6, L6, M6, N6, P6 H7, G7, E7, D7, H6, G6, F6, E6, D6 H1, G1, E1, D1, H2, G2, F2, E2, D2 K1, L1, N1, P1, K2, L2, M2, N2, P2	DQ_{A1}–DQ_{PA9} DQ_{B1}–DQ_{PB9} DQ_{C1}–DQ_{PC9} DQ_{D1}–DQ_{PD9}	I/O	Data Input and Output pins (x36 Version)
L5, G5, G3, L3	$\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_A, DQ_B, DQ_C, DQ_D I/Os; active low (x36 Version)
P7, N6, L6, K7, H6, G7, F6, E7, D6 D1, E2, G2, H1, K2, L1, M2, N1, P2	DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9}	I/O	Data Input and Output pins (x18 Version)
L5, G3	$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B Data I/Os; active low (x18 Version)
P6, N7, M6, L7, K6, H7, G6, E6, D7, D2, E1, F2, G1, H2, K1, L2, N2, P1, G5, L3, T4	NC	—	No Connect (x18 Version)
K4	CK	I	Clock Input Signal; active high
E4	$\overline{E}_1$	I	Chip Enable; active low
B2	E_2	I	Chip Enable; active high
F4	$\overline{G}$	I	Output Enable; active low
T7	ZZ	I	Sleep Mode control; active high
R5	$\overline{FT}$	I	Flow Through or Pipeline mode; active low
R3	$\overline{LBO}$	I	Linear Burst Order mode; active low
L4	SCD	I	Single Cycle Deselect/$\overline{\text{Dual Cycle Deselect}}$ Mode Control
D4	ZQ	I	FLXDrive Output Impedance Control (Low = Low Impedance [High Drive], High = High Impedance [Low Drive])
B1, C1, R1, T1, L4, B7, C7, U6, R7, J3,J5, U2, U3, U4, U5	NC	—	No Connect
J2, C4, J4, R4, J6	V_{DD}	I	Core power supply
D3, E3, F3, H3, K3, M3, N3, P3, D5, E5, F5, H5, K5, M5, N5, P5	V_{SS}	I	I/O and Core Ground
A1, F1, J1, M1, U1, A7, F7, J7, M7, U7	V_{DDQ}	I	Output driver power supply

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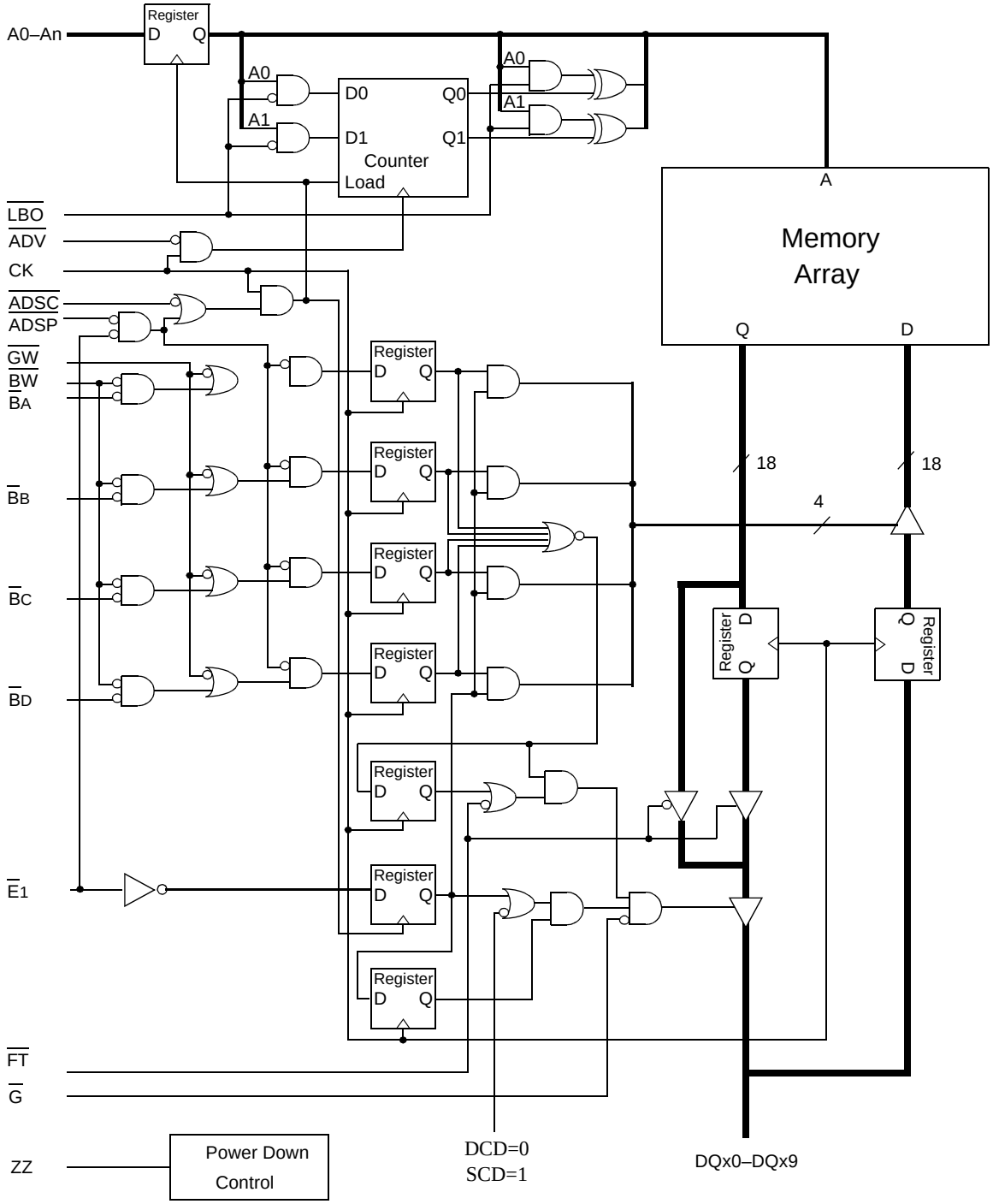
GS88418/36 Block Diagram



Note: Only x18 version shown for simplicity.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H or NC	Interleaved Burst
Output Register Control	$\overline{FT}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$
Single/Dual Cycle Deselect Control	SCD	L	Dual Cycle Deselect
		H or NC	Single Cycle Deselect
FLXDrive Output Impedance Control	ZQ	L	High Drive (Low Impedance)
		H	Low Drive (High Impedance)

Note:
There are pull-up devices on the $\overline{LBO}$, ZQ, SCD, and $\overline{FT}$ pins and a pull down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above table.

Enable / Disable Parity I/O Pins

This SRAM allows the user to configure the device to operate in Parity I/O active (x18 or x36) or in Parity I/O inactive (x16 or x32) mode. Holding the $\overline{PE}$ bump low or letting it float will activate the 9th I/O on each byte of the RAM. Tying $\overline{PE}$ high deactivates the 9th I/O of each byte, although the bit in each byte of the memory array remains active to store and recall parity bits generated and read into the ByteSafe parity circuits.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

BPR 1999.05.18

Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

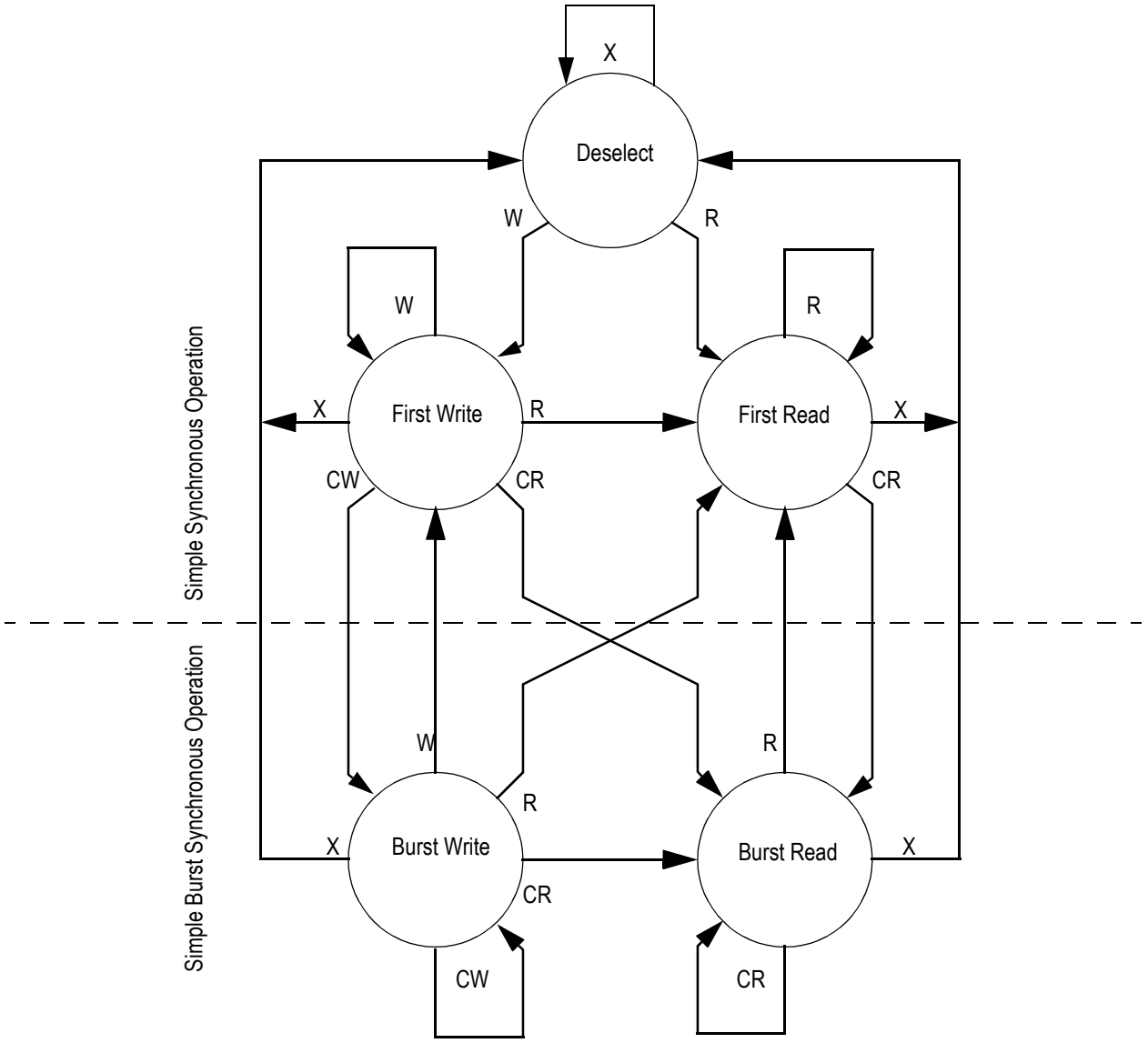
Notes:
1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, and/or $\overline{B}_D$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x36 version.

Synchronous Truth Table

Operation	Address Used	State Diagram Key[5]	$\overline{E1}$	E2[2] (x36only)	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	W[3]	DQ[4]
Deselect Cycle, Power Down	**None**	**X**	**H**	**X**	**X**	**L**	**X**	**X**	**High-Z**
Deselect Cycle, Power Down	None	X	L	F	L	X	X	X	High-Z
Deselect Cycle, Power Down	**None**	**X**	**L**	**F**	**H**	**L**	**X**	**X**	**High-Z**
Read Cycle, Begin Burst	External	R	L	T	L	X	X	X	Q
Read Cycle, Begin Burst	**External**	**R**	**L**	**T**	**H**	**L**	**X**	**F**	**Q**
Write Cycle, Begin Burst	**External**	**W**	**L**	**T**	**H**	**L**	**X**	**T**	**D**
Read Cycle, Continue Burst	*Next*	*CR*	*X*	*X*	*H*	*H*	*L*	*F*	*Q*
Read Cycle, Continue Burst	Next	CR	H	X	X	H	L	F	Q
Write Cycle, Continue Burst	*Next*	*CW*	*X*	*X*	*H*	*H*	*L*	*T*	*D*
Write Cycle, Continue Burst	Next	CW	H	X	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	X	H	H	T	D

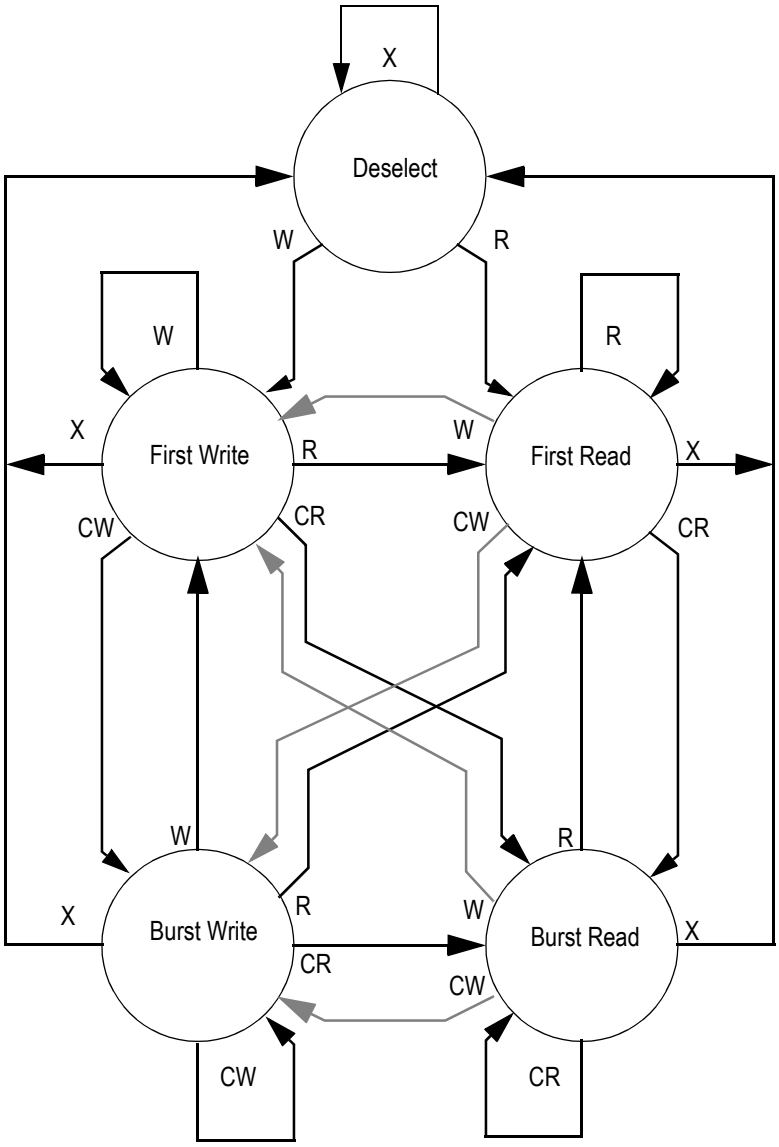
Notes:
1. X = Don't Care, H = High, L = Low.
2. For x36 Version, E = T (True) if E2 = 1; E = F (False) if E2 = 0.
3. $\overline{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding.
4. $\overline{G}$ is an asynchronous input. $\overline{G}$ can be driven high at any time to disable active output drivers. $\overline{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
5. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
6. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
7. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

Simplified State Diagram



Notes:
1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable (E1 and E2) and Write ($\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$, $\overline{BW}$, and $\overline{GW}$) control inputs, and that $\overline{ADSP}$ is tied high and $\overline{ADSC}$ is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{ADSC}$ control inputs, and assumes $\overline{ADSP}$ is tied high and $\overline{ADV}$ is tied low.

Simplified State Diagram with $\overline{G}$



Notes:
1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from read cycles to write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in gray tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
V_{CK}	Voltage on Clock Input Pin	–0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

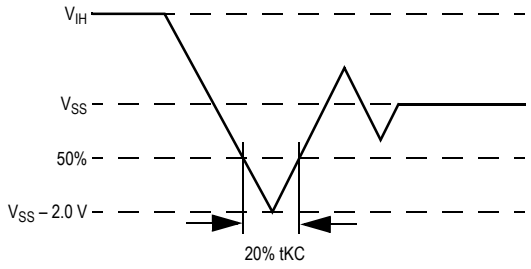
Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

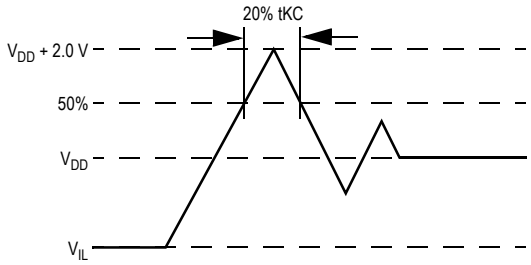
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V_{DD}	3.135	3.3	3.6	V	
I/O Supply Voltage	V_{DDQ}	2.375	2.5	V_{DD}	V	1
Input High Voltage	V_{IH}	1.7	—	V_{DD} +0.3	V	2
Input Low Voltage	V_{IL}	–0.3	—	0.8	V	2
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	3
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	3

Notes:
1. Unless otherwise noted, all performance specifications quoted are evaluated for worst case at both 2.75 V ≤ V_{DDQ} ≤ 2.375 V (i.e., 2.5 V I/O) and 3.6 V ≤ V_{DDQ} ≤ 3.135 V (i.e., 3.3 V I/O), and quoted at whichever condition is worst case.
2. This device features input buffers compatible with both 3.3 V and 2.5 V I/O drivers.
3. Most speed grades and configurations of this device are offered in both Commercial and Industrial Temperature ranges. The part number of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
4. Input Under/overshoot voltage must be –2 V > Vi < V_{DD} +2 V with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 3.3 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

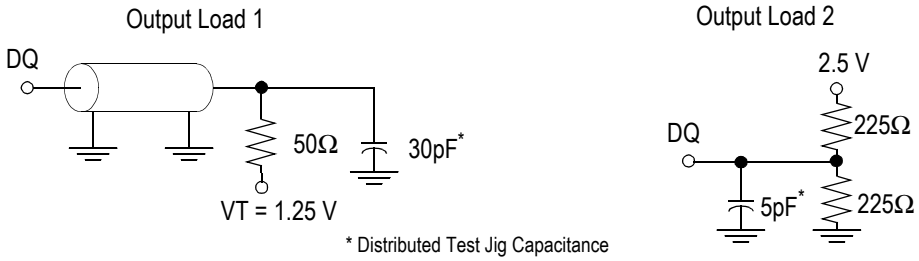
Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	9	°C/W	3

Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V
Output load	**Fig. 1& 2**

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output Load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}
4. Device is deselected as defined by the Truth Table.



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{INZZ}	$V_{DD} \geq V_{IN} \geq V_{IH}$ 0 V ≤ V_{IN} ≤ V_{IH}	–1 uA –1 uA	1 uA 300 uA
Mode Pin Input Current	I_{INM}	$V_{DD} \geq V_{IN} \geq V_{IL}$ 0 V ≤ V_{IN} ≤ V_{IL}	–300 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH}	I_{OH} = –4 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 4 mA	—	0.4 V

Operating Currents

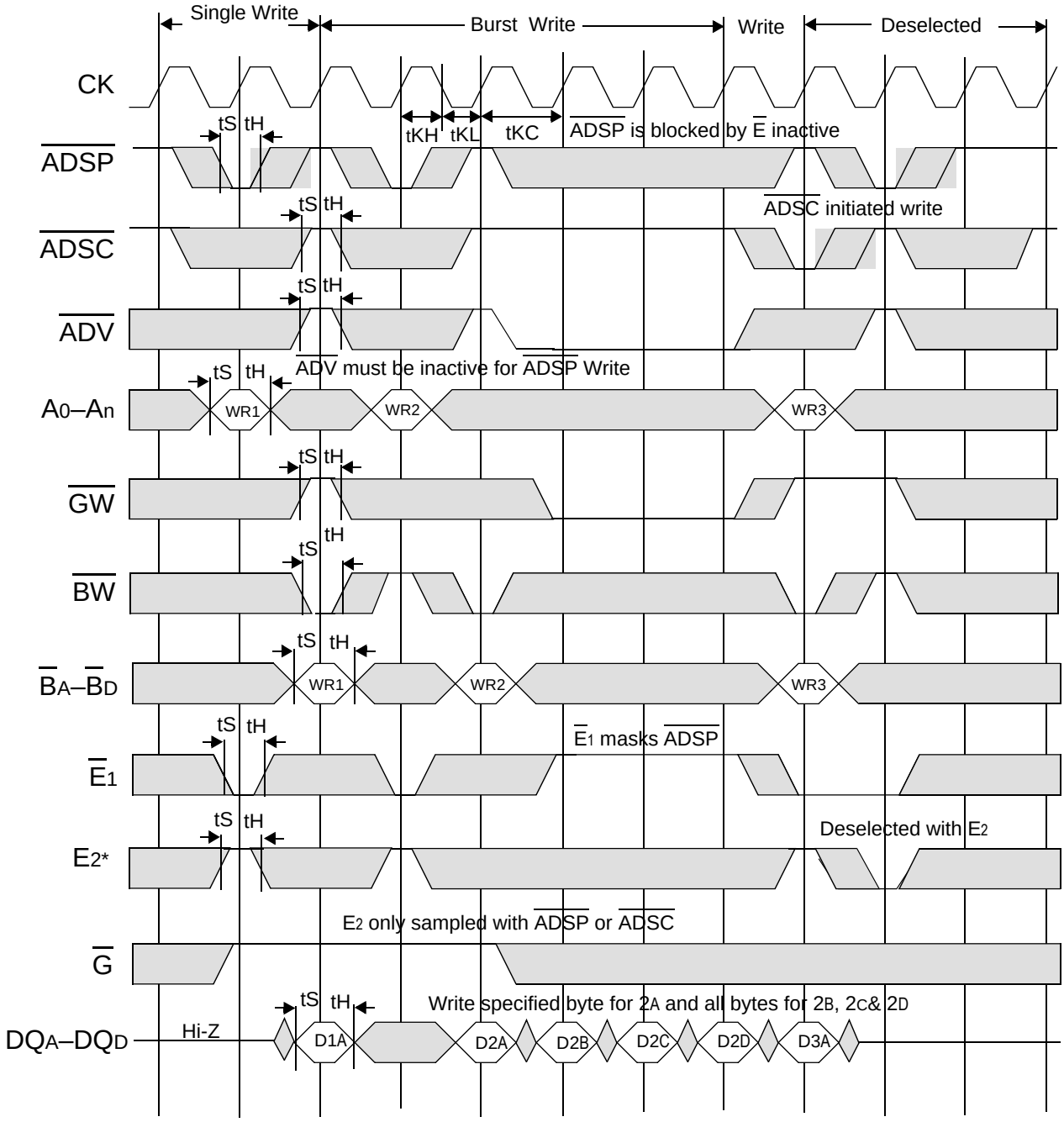
Parameter	Test Conditions	Symbol	-200		-180		-166		-150		-133		Unit
			0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	
Operating Current	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	I_{DD} Pipeline	450	470	410	430	380	400	350	370	340	360	mA
		I_{DD} Flow Through	270	290	270	290	250	270	240	250	220	240	mA
Standby Current	ZZ ≥ V_{DD} – 0.2 V	I_{SB} Pipeline	40	60	40	60	40	60	40	60	40	60	mA
		I_{SB} Flow Through	40	60	40	60	40	60	40	60	40	60	mA
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	I_{DD} Pipeline	120	140	110	130	100	120	100	120	90	110	mA
		I_{DD} Flow Through	90	110	80	100	80	100	70	90	70	90	mA

AC Electrical Characteristics

	Parameter	Symbol	-200		-180		-166		-150		-133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	5.0	—	5.5	—	6.0	—	6.7	—	7.5	—	ns
	Clock to Output Valid	tKQ	—	3.0	—	3.2	—	3.5	—	3.8	—	4.0	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Flow Through	Clock Cycle Time	tKC	10.0	—	10.0	—	10.0	—	10.0	—	10.0	—	ns
	Clock to Output Valid	tKQ	—	7.5	—	8.0	—	8.5	—	9.0	—	9.5	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock HIGH Time	tKH	1.3	—	1.3	—	1.3	—	1.3	—	1.3	—	ns
	Clock LOW Time	tKL	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	3.0	1.5	3.2	1.5	3.5	1.5	3.8	1.5	4.0	ns
	$\overline{G}$ to Output Valid	tOE	—	3.2	—	3.2	—	3.5	—	3.8	—	4.0	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	3.0	—	3.2	—	3.5	—	3.8	—	4.0	ns
	Setup time	tS	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	20	—	ns

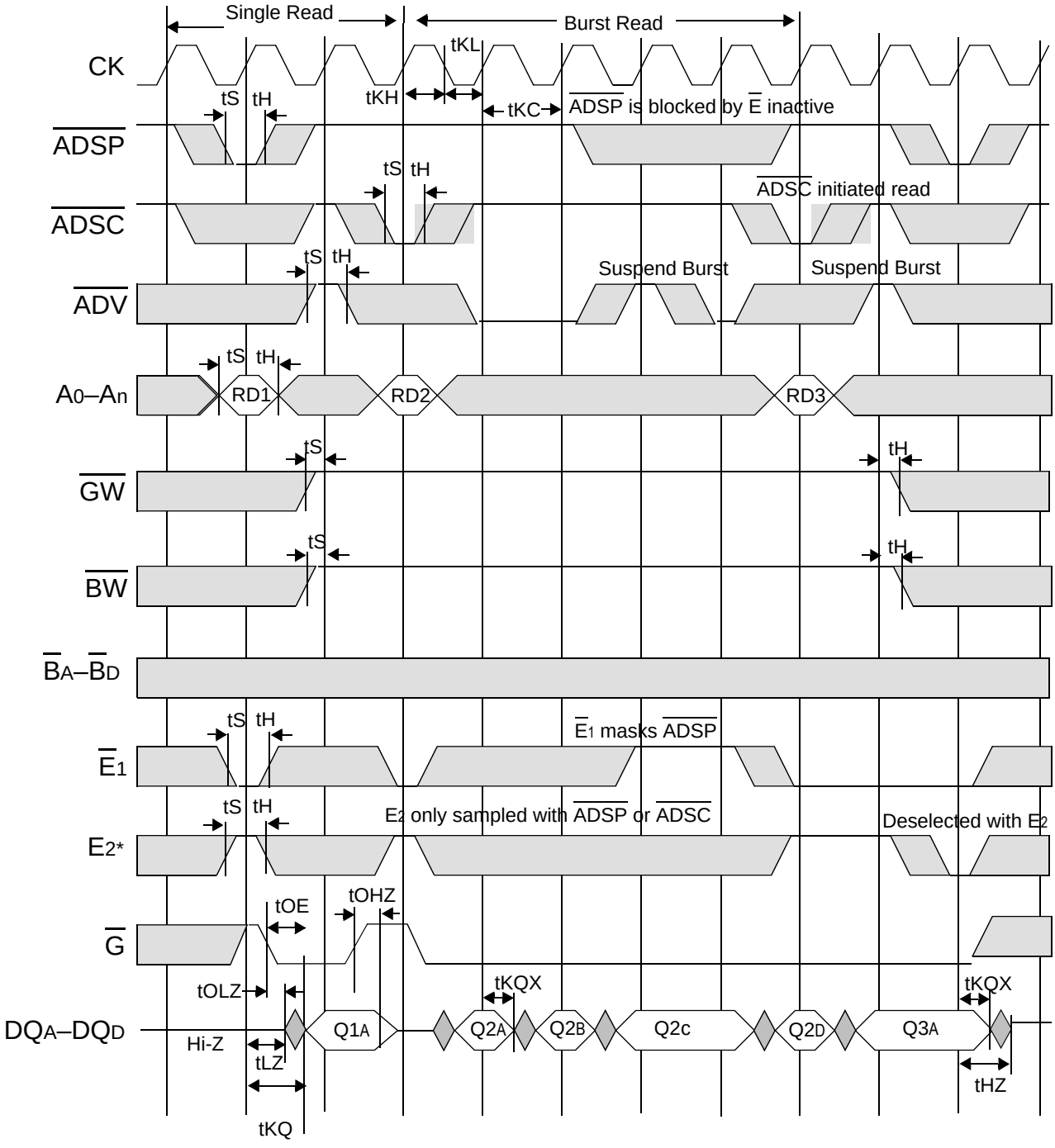
Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

Write Cycle Timing

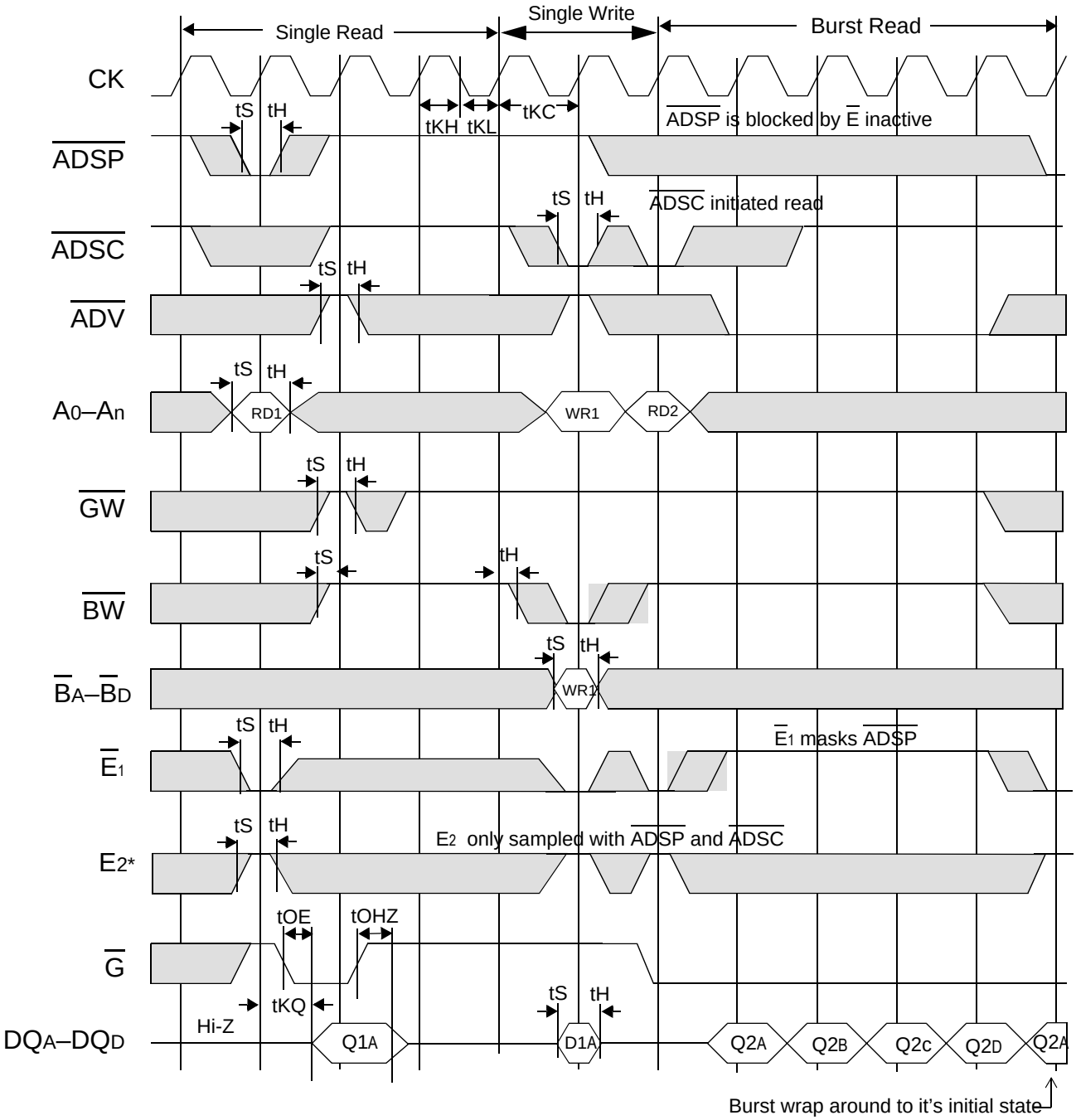


* Only in 88436B

Flow Through Read Cycle Timing

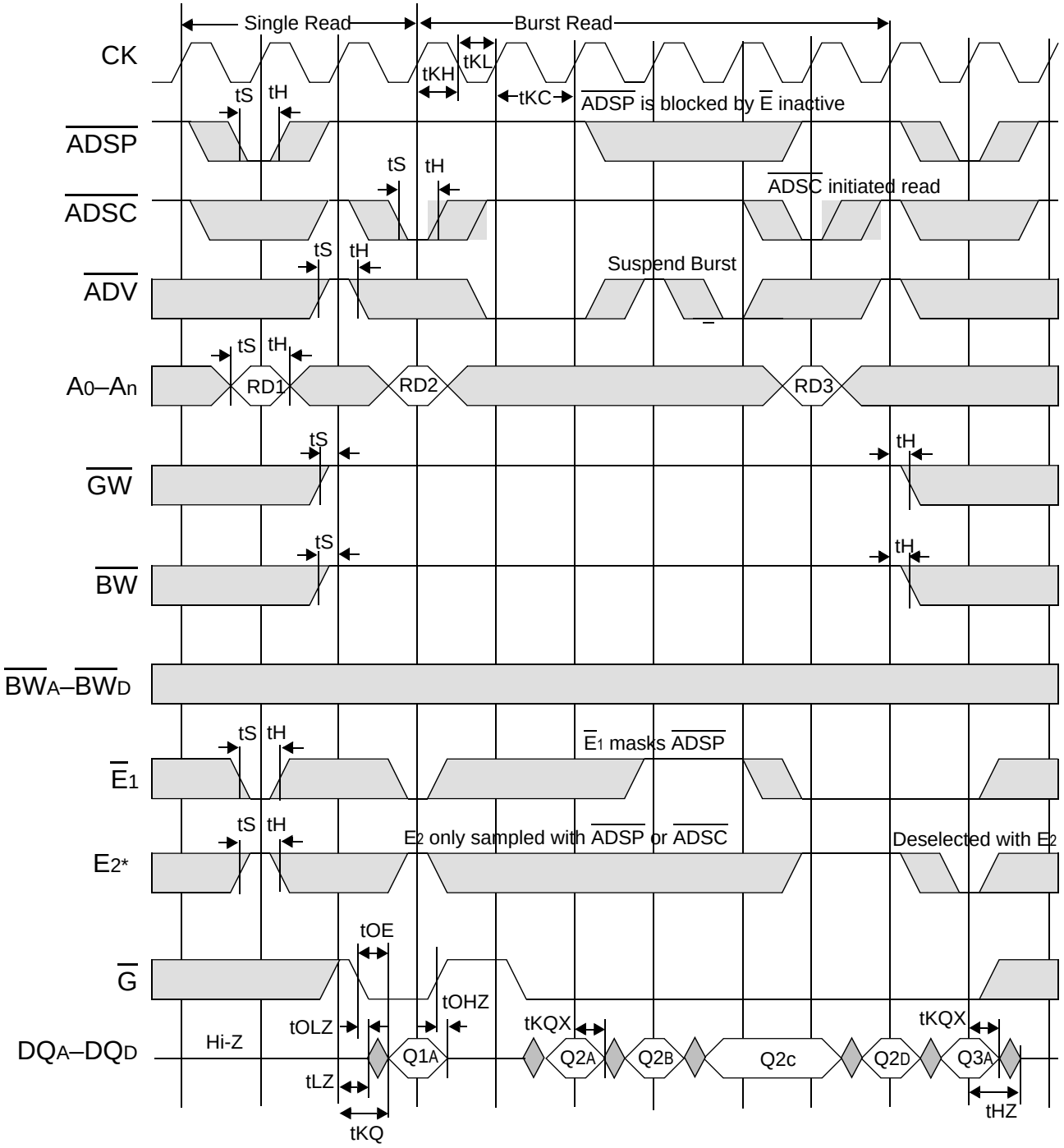


Flow Through Read-Write Cycle Timing



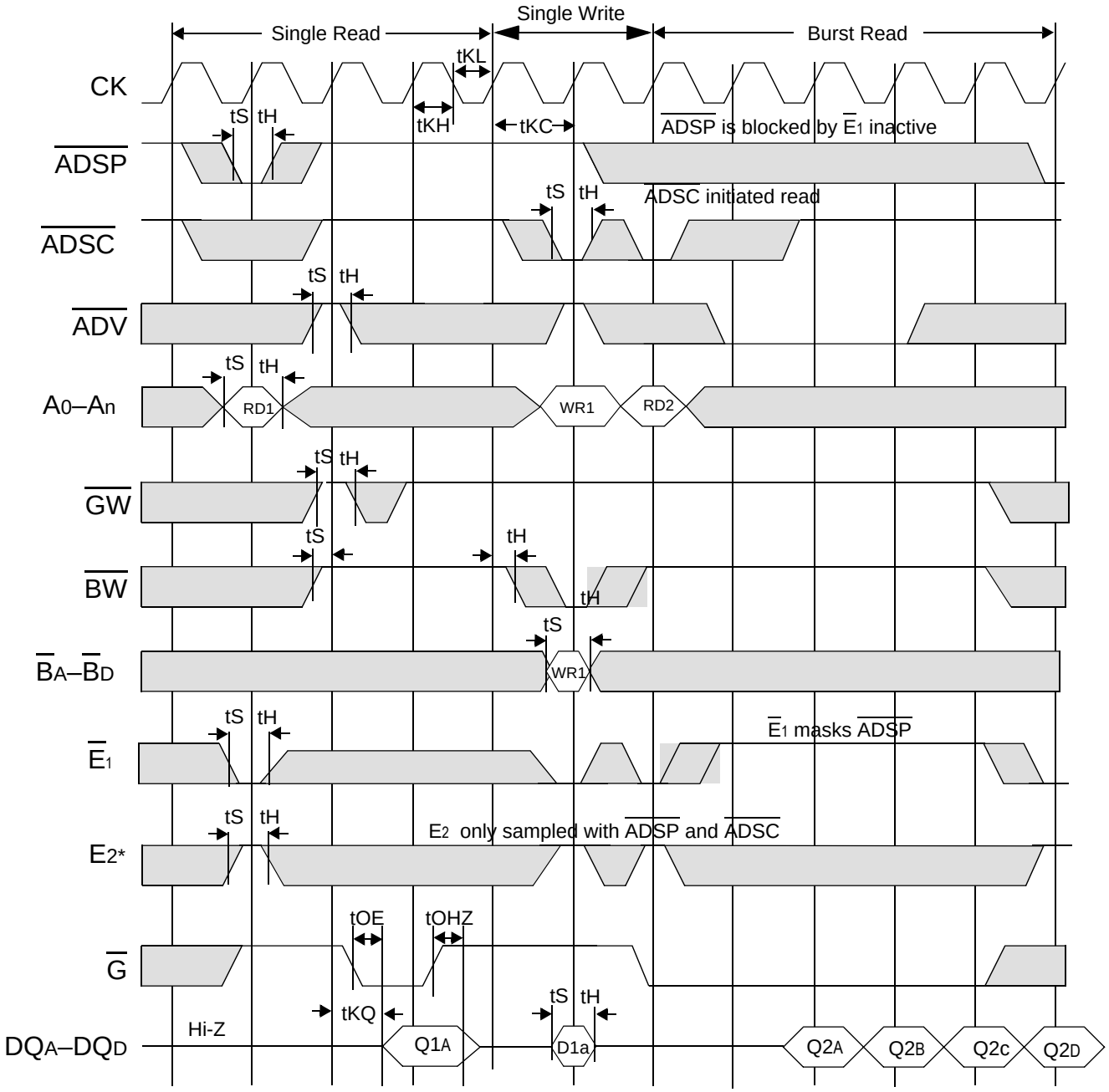
* Only in 88436B

Pipelined SCD Read Cycle Timing



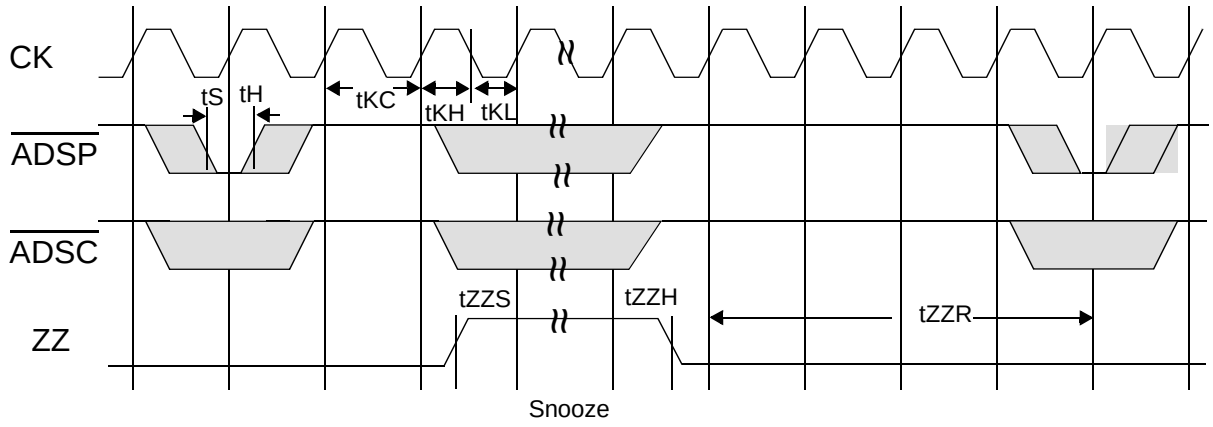
* Only in 88436B

Pipelined DCD Read-Write Cycle Timing



* Only in 88436B

Sleep Mode Timing Diagram

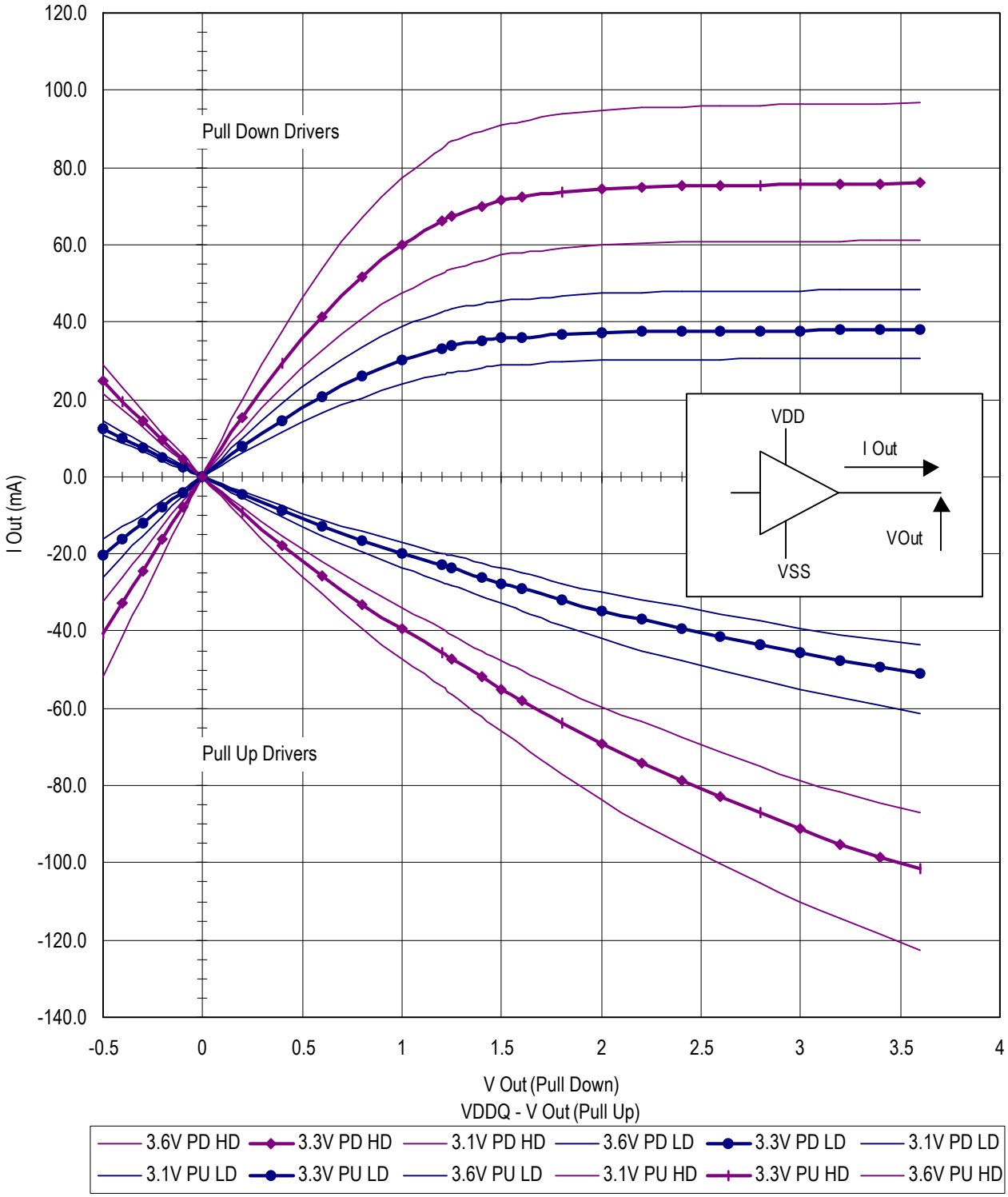


Application Tips

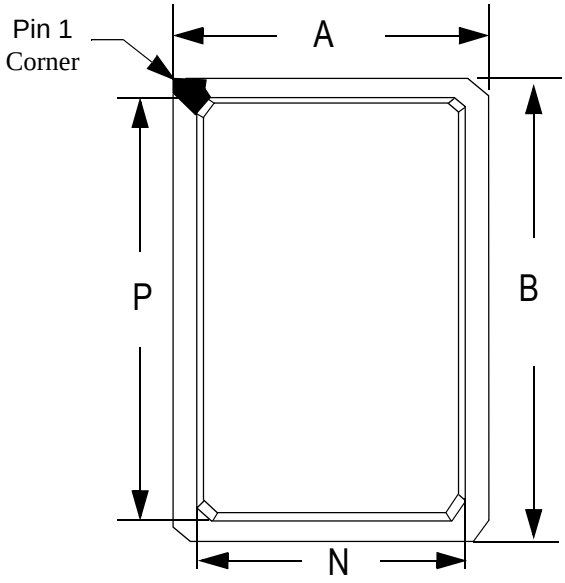
Single and Dual Cycle Deselect

SCD devices force the use of "dummy read cycles" (read cycles that are launched normally, but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance, but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings), but greater care must be exercised to avoid excessive bus contention.

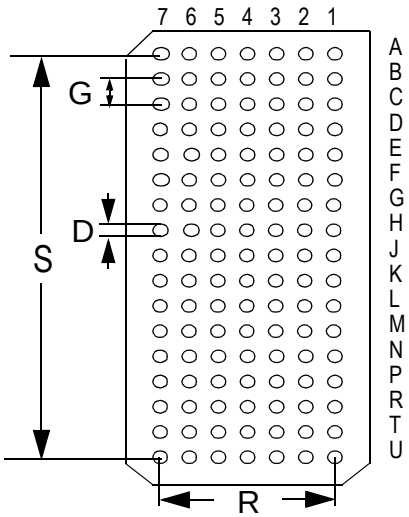
FLXDrive Output Driver Characteristics



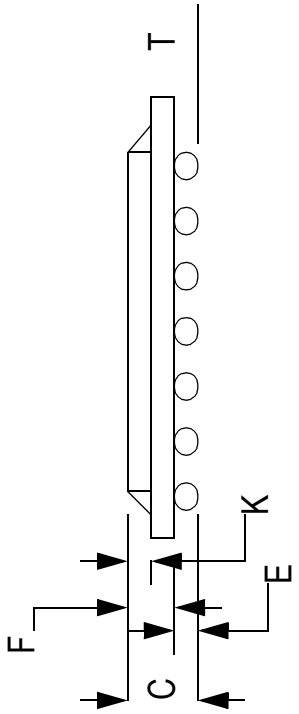
Package Dimensions—119-Pin BGA



Top View



Bottom View



Side View

Package Dimensions—119-Pin BGA

Symbol	Description	Min.	Nom.	Max
A	Width	13.8	14.0	14.2
B	Length	21.8	22.0	22.2
C	Package Height (including ball)	-		2.40
D	Ball Size	0.60	0.75	0.90
E	Ball Height	0.50	0.60	0.70
F	Package Height (excluding balls)		1.46	1.70
G	Width between Balls		1.27	
K	Package Height above board	0.80	0.90	1.00
N	Cut-out Package Width		12.00	
P	Foot Length		19.50	
R	Width of package between balls		7.62	
S	Length of package between balls		20.32	
T	Variance of Ball Height		0.15	

Unit: mm

Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
512K x 18	GS88418B-200	S/DCD Pipeline/Flow Through	BGA	200/7.5	C	
512K x 18	GS88418B-180	S/DCD Pipeline/Flow Through	BGA	180/8	C	
512K x 18	GS88418B-166	S/DCD Pipeline/Flow Through	BGA	166/8.5	C	
512K x 18	GS88418B-150	S/DCD Pipeline/Flow Through	BGA	150/9	C	
512K x 18	GS88418B-133	S/DCD Pipeline/Flow Through	BGA	133/9.5	C	
256K x 36	GS88436B-200	S/DCD Pipeline/Flow Through	BGA	200/7.5	C	
256K x 36	GS88436B-180	S/DCD Pipeline/Flow Through	BGA	180/8	C	
256K x 36	GS88436B-166	S/DCD Pipeline/Flow Through	BGA	166/8.5	C	
256K x 36	GS88436B-150	S/DCD Pipeline/Flow Through	BGA	150/9	C	
256K x 36	GS88436B-133	S/DCD Pipeline/Flow Through	BGA	133/9.5	C	
512K x 18	GS88418B-200I	S/DCD Pipeline/Flow Through	BGA	200/7.5	I	Not Available
512K x 18	GS88418B-180I	S/DCD Pipeline/Flow Through	BGA	180/8	I	
512K x 18	GS88418B-166I	S/DCD Pipeline/Flow Through	BGA	166/8.5	I	
512K x 18	GS88418B-150I	S/DCD Pipeline/Flow Through	BGA	150/9	I	
512K x 18	GS88418B-133I	S/DCD Pipeline/Flow Through	BGA	133/9.5	I	
512K x 36	GS88418B-200I	S/DCD Pipeline/Flow Through	BGA	200/7.5	I	Not Available
512K x 36	GS88418B-180I	S/DCD Pipeline/Flow Through	BGA	180/8	I	
256K x 36	GS88436B-166I	S/DCD Pipeline/Flow Through	BGA	166/8.5	I	
256K x 36	GS88436B-150I	S/DCD Pipeline/Flow Through	BGA	150/9	I	
256K x 36	GS88436B-133I	S/DCD Pipeline/Flow Through	BGA	133/9.5	I	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS88418BT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
GS8841836B Rev 1.00	First Release	•
88418_r1; 88418_r1_01	Content	• Updated BGA pinout to meet JEDEC standards
88418_r1_01; 88418_r1_02	Format	• Updated format to comply with Technical Publications standards
88418_r1_02; 88418_r1_03	Content	• Updated Capitance table—removed Input row and changed Output row to I/O
88418_r1_03; 88418_r1_04	Content	• Updated speed bin table on page 1 (Added 150 MHz and 133 MHz) • Updated pinouts on pages 2 & 3 (U2–U5 should all be NC) • Removed PE, DP, and QE from Pin Description table on page 4; added R7, J3, J5, U2, U3, U4, U5 to NC row • Added 150 MHz and 133 MHz to Operating Currents table on page 14 • Added 150 MHz and 133 MHz to Electrical Characteristics table on page 15 • Deleted BSR table on page 22
88418_r1_04; 88418_r1_05	Content	• Added references to 150 MHz and 133 MHz speed bins to headers and ordering information table

