# GS9020

## 2A Sink/Source Bus Termination Regulator

### Product Description

The GS9020 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements.

The regulator is capable of actively sinking or sourcing up to 2A while regulating an output voltage to within 40mV.

The output termination voltage can be tightly regulated to track 1/2VDDQ by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The GS9020 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection.

The GS9020 are available in the PSOP-8 (Exposed Pad) surface mount packages.

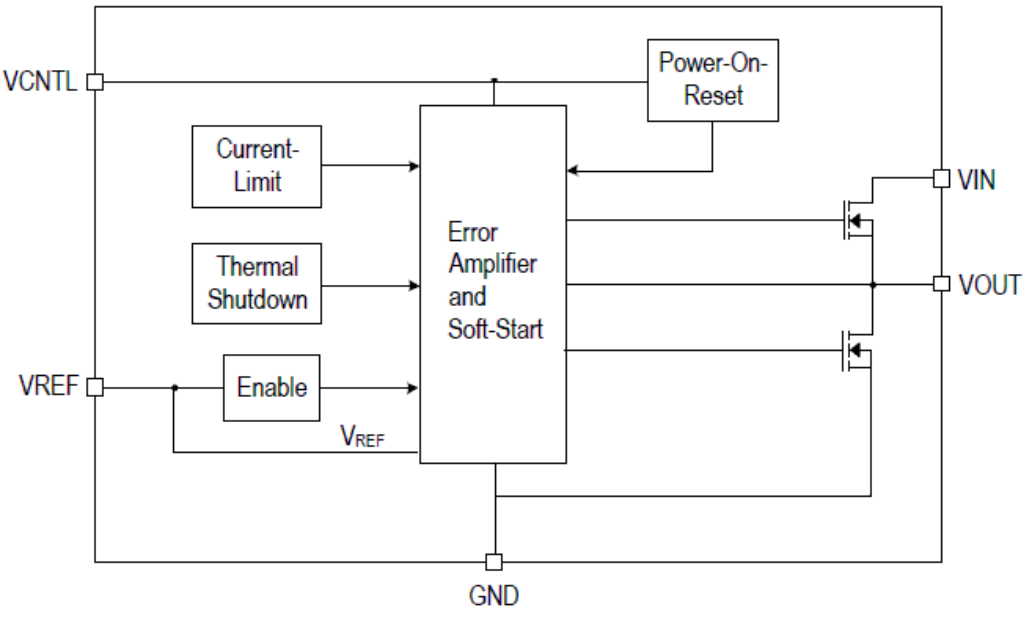
### Features

- Generate Termination Voltage for DDR Interface
- Sink and Source 2A Continuous Current
- Integrated Power MOSFETs
- Generates Termination Voltage for SSTL_2, SSTL_18, HSTL, SCSI-2 and SCSI-3 Interfaces
- High Accuracy Output Voltage at Full-Load
- Output Voltage traces REFEN Pin Voltage
- Low External Component Count
- Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
- Current Limiting Protection
- Thermal Shutdown Protection
- PSOP-8 with exposed pad Pb-Free Package
- RoHS Compliant, 100%Pb & Halogen Free

### Applications

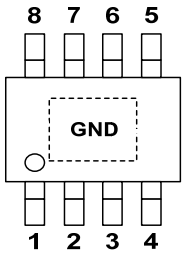
- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs, Printers
- Embedded Systems
- Active Termination Buses

### Block Diagram



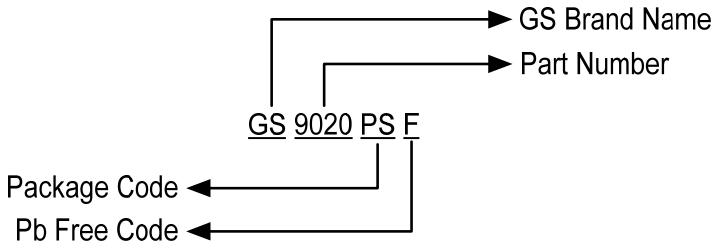
## Packages & Pin Assignments (Top View)

**GS9020PSF (PSOP-8)**

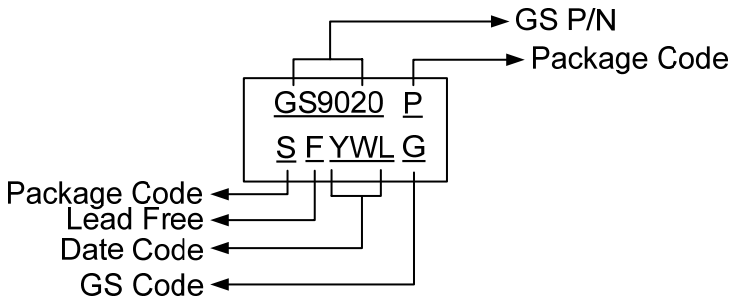



| Pin No. | Pin Name | Pin Function Description |
|---|---|---|
| 1 | $V_{IN}$ | Input Voltage pin |
| 2 | GND | Ground pin |
| 3 | $V_{REF}$ | Reference voltage input and chip enable pin |
| 4 | $V_{OUT}$ | Output Voltage pin |
| 5,7,8 | NC | No connect pin |
| 6 | $V_{CNTL}$ | Supply Input and Gate drive voltage pin |

## Ordering Information




## Marking Information



## Absolute Maximum Ratings (Note 1)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{IN}$ | Input Voltage | 6 | V |
| $V_{CNTL}$ | Control Voltage | 6 | V |
| $P_D$ | Power Dissipation | Internally Limited | -- |
| $T_{STG}$ | Storage Temperature Range | -40 to +150 | ºC |
| - | ESD (HBM) | 2000 | V |
| $\theta_{JC}$ | Thermal Resistance from Junction to case | 15 | ºC/W |
| $\theta_{JA}$ | Thermal Resistance from Junction to ambient (Note 2) | 40 | ºC/W |

Note 1: Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Note 2: $\theta_{JA}$ is measured with the PCB copper area (need connect to Exposed pad) of approximately in$1.5^2$.

## Recommended Operating Conditions

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{IN}$ | Input Voltage | 1.2 to $V_{CNTL}$ | V |
| $V_{CNTL}$ | Control Voltage | 5.0 or 3.3 | V |
| $V_{REF}$ | $V_{REF}$ Input Voltage | 0.6 ~ $V_{CNTL}$ - 2.2 | V |
| $T_A$ | Ambient Temperature | -40 to +85 | ºC |
| $T_J$ | Junction Temperature | -40 to +125 | ºC |

Note: $V_{OS}$ offset is the voltage measurement defined as $V_{OUT}$ subtracted from $V_{REFEN}$.

## Electrical Characteristics

$V_{IN}$ =2.5V/1.8V/1.5V, $V_{CNTL}$ =3.3V, $V_{REFEN}$ =1.25V/0.9V/0.75V, $C_{OUT}$ =10μF (Ceramic), $T_A$ =25°C, unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CNTL}$ | Gate Drive Voltage Range | - | - | 3.3 | 5.5 | V |
| $V_{CNTLRTH}$ | POR Threshold | - | - | 2.55 | - | V |
| $V_{CNTL}$ | POR Hysteresis | - | - | 0.1 | - | V |
| $V_{IN}$ | Input Voltage | - | 1.2 | - | $V_{CNTL}$ | V |
| $I_{CNTL}$ | Quiescent Current | $I_{OUT}$=0A | - | 1 | 3 | mA |
| $I_{STBY}$ | Standby Current | $I_{OUT}$=0A,$V_{REFEN}$=0V | - | 1 | 10 | μA |
| $V_{OS}$ | Output Offset Voltage(Note1) | $I_{OUT}$=0A | -20 | - | +20 | mV |
| $\Delta V_{LOAD}$ | Load Regulation(Note2) | $I_{OUT}$=±2.0A | - | 0.5 | +20 | % |
| $I_{CL-Source}$ | Current limit | Sourcing | 2.1 | - | - | A |
| $I_{CL-Sink}$ | | Sinking | 2.1 | - | - | A |
| $T_{SS}$ | Soft-Start Period | - | - | 0.4 | - | ms |
| $T_{SD}$ | Thermal Shutdown | - | - | 155 | - | ºC |
| $T_{SDH}$ | Thermal Shutdown Hysteresis | - | - | 30 | - | ºC |
| $V_{IH}$ | Shutdown Threshold | Enable, REFEN Rising | 0.6 | - | - | V |
| $V_{IL}$ | | Shutdown, REFEN Falling | - | - | 0.2 | |

Note 1: $V_{OS}$ offset is the voltage measurement defined as $V_{OUT}$ subtracted from $V_{REFEN}$.

Note 2: Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 2A.

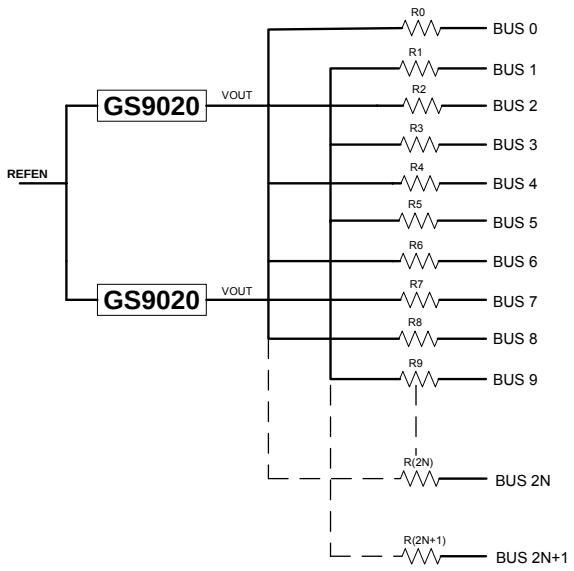
## Application Information

### Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the GS9020. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between GS9020 and the preceding power converter.

### Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on VREFEN is below 0.2V. In addition, the capacitor and voltage divider form the low-pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.




### Thermal Consideration

The GS9020 series can deliver a current of up to 2A over the full operating junction temperature range. However, the maximum output current must be dated at higher ambient temperature to ensure the junction temperature does not exceed 125ºC. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

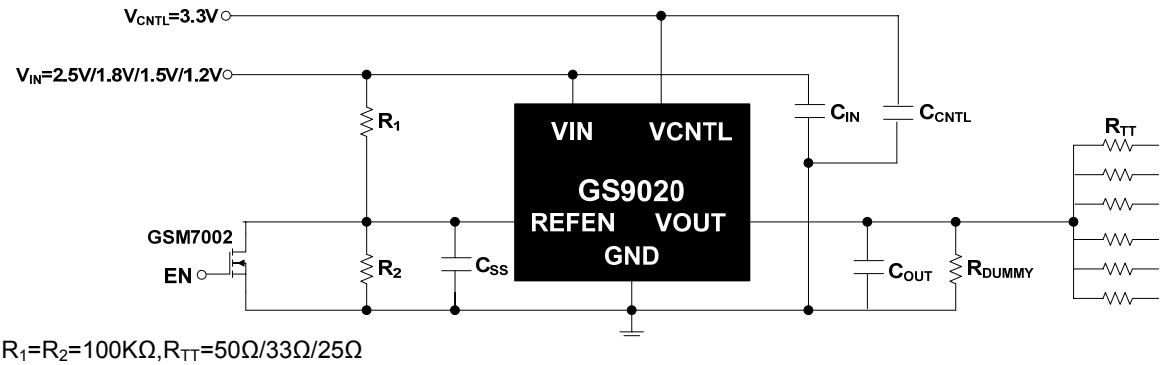
$$P_{D(MAX)} = ( T_{J(MAX)} - T_A ) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature of the (125ºC) and $T_A$ is the maximum ambient temperature. The junction to ambient thermal resistance ($\theta_{JA}$) for PSOP-8-EP (Exposed Pad) package at recommended minimum footprint is 40ºC/W on $1.5^2$ and Multi-layer PCB layout. The maximum power dissipation at $T_A$ = 25ºC can be calculated by following formula:

$P_{D(MAX)}$ = (125ºC - 25ºC) / 40℃/W = 2.5W

The thermal resistance $\theta_{JA}$ of PSOP-8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of PSOP-8L-EP package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

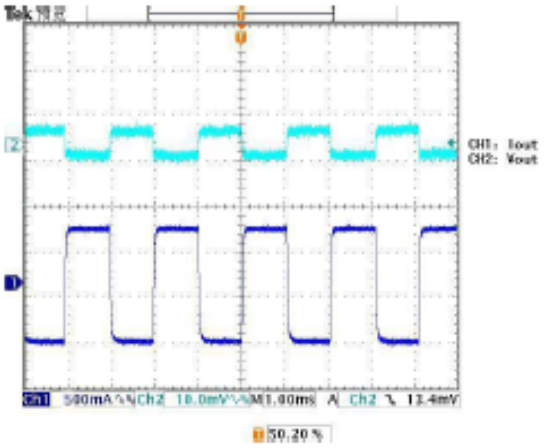
## Typical Application Circuit



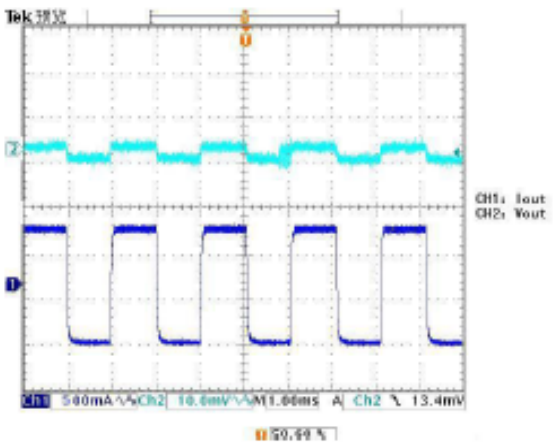

$R_1$=$R_2$=100KΩ,$R_{TT}$=50Ω/33Ω/25Ω
$C_{OUT, min}$=10μF(Ceramic)+1000μF under the worst case testing condition
$R_{DUMMY}$=1kΩ as for $V_{OUT}$ discharge when $V_{IN}$ is not present but $V_{CNTL}$ is present
$C_{SS}$=1μF,$C_{IN}$=470μF(ESR), $C_{CNTL}$=1μF

## Typical Operating Characteristics

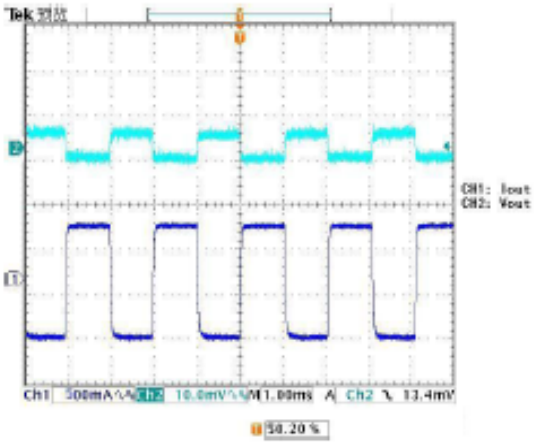
### Transient Test



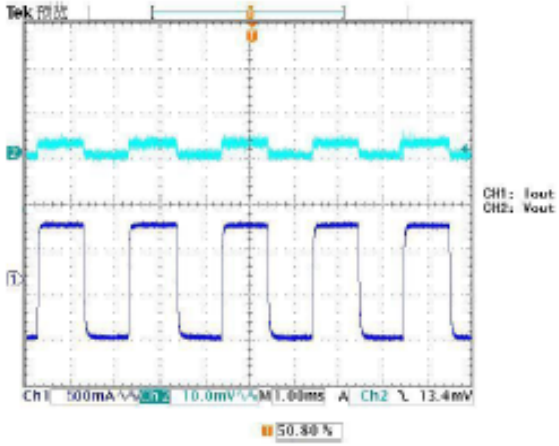

$V_{IN}$=2.5V, $V_{OUT}$=1.25V,$V_{CNTL}$=3.3V, $I_{OUT}$=1.5A



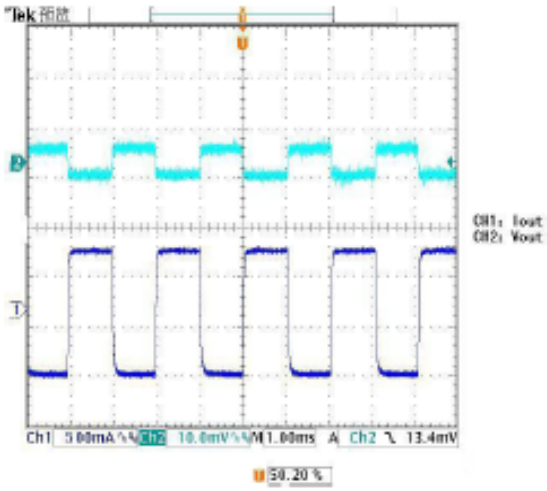

$V_{IN}$=2.5V, $V_{OUT}$=1.25V,$V_{CNTL}$=3.3V, $I_{OUT}$= -1.5A



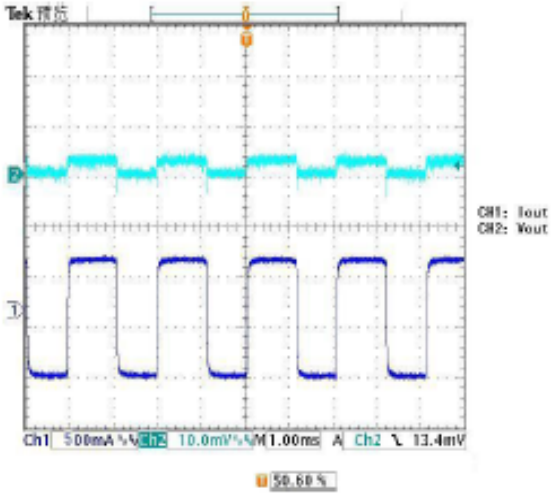

$V_{IN}$=1.8V, $V_{OUT}$=0.9V,$V_{CNTL}$=3.3V, $I_{OUT}$=1.5A




$V_{IN}$=1.8V, $V_{OUT}$=0.9V,$V_{CNTL}$=3.3V, $I_{OUT}$= -1.5A

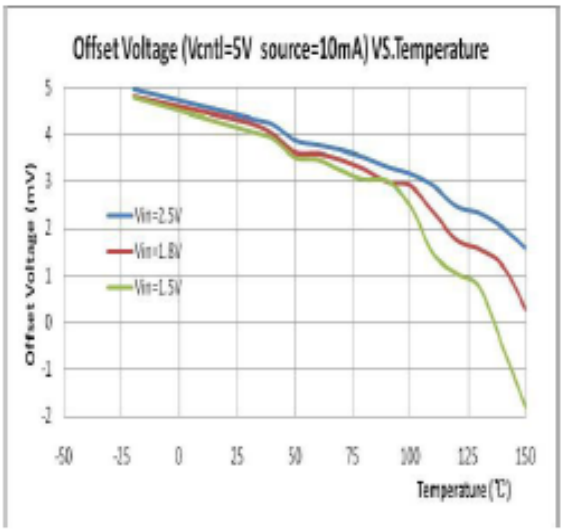


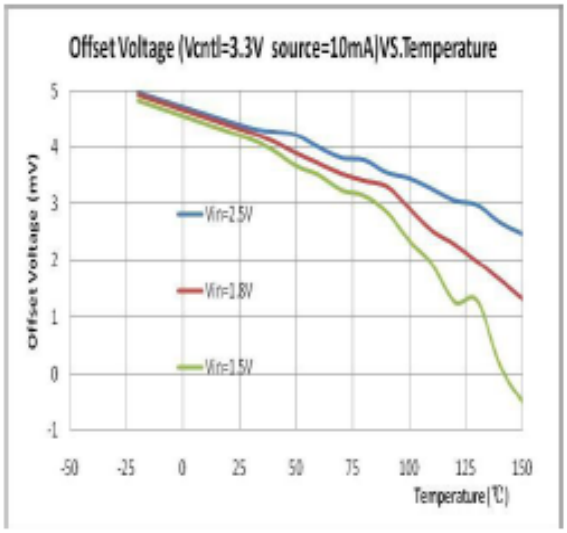

$V_{IN}$=1.5V, $V_{OUT}$=0.75V,$V_{CNTL}$=3.3V,$I_{OUT}$=1.5A

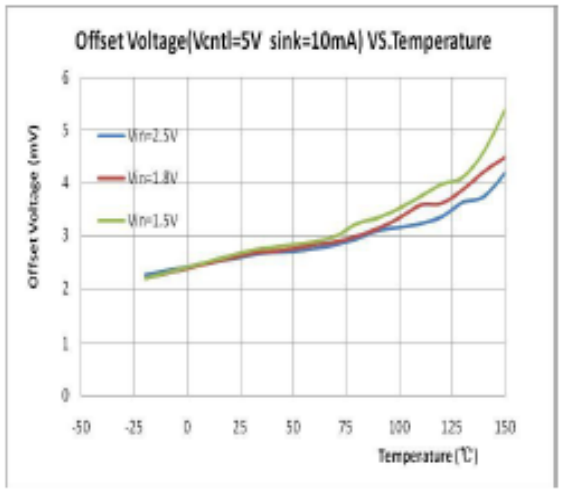


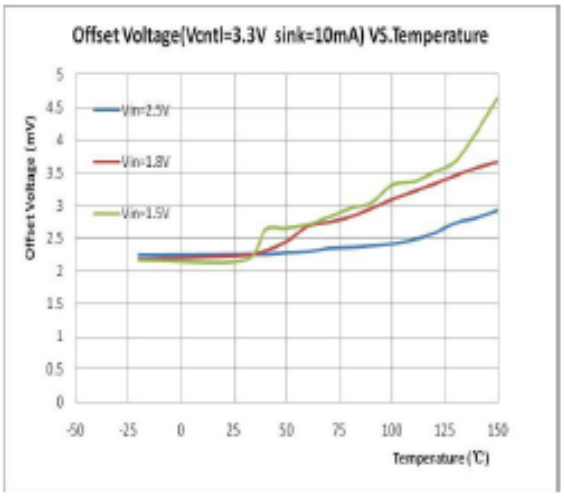

$V_{IN}$=1.5V, $V_{OUT}$=0.75V,$V_{CNTL}$=3.3V,$I_{OUT}$= -1.5A

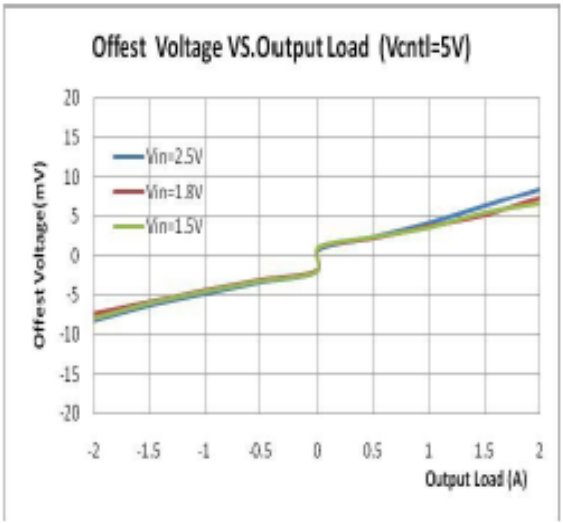
## Typical Operating Characteristics (continuous)

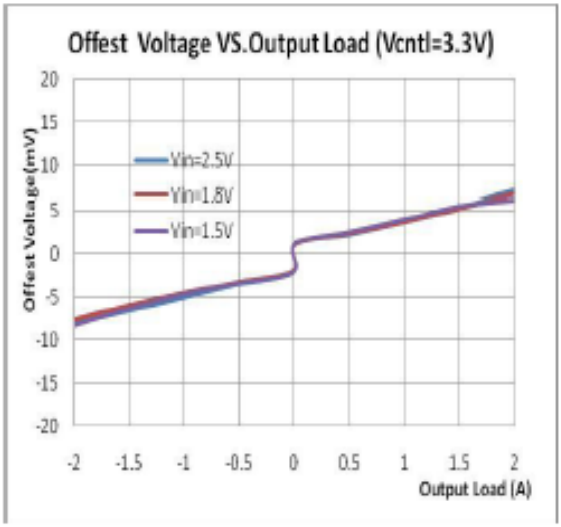


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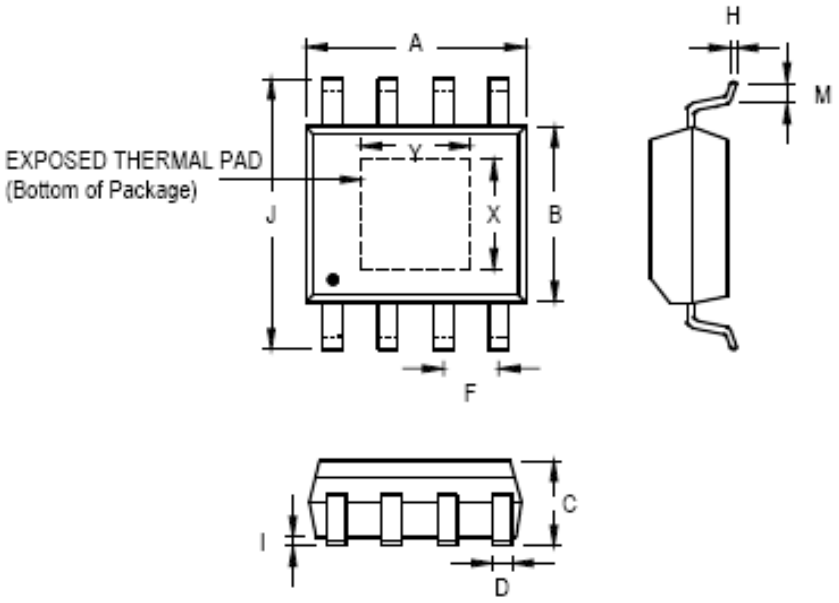
## Package Dimension

# PSOP-8 PLASTIC PACKAGE




| Dimensions | | | | |
|---|---|---|---|---|
| SYMBOL | Millimeters | | Inches | |
| | MIN | MAX | MIN | MAX |
| A | 4.801 | 5.004 | 0.189 | 0.197 |
| B | 3.810 | 3.988 | 0.150 | 0.157 |
| C | 1.346 | 1.753 | 0.053 | 0.069 |
| D | 0.330 | 0.508 | 0.013 | 0.020 |
| F | 1.194 | 1.346 | 0.047 | 0.053 |
| H | 0.191 | 0.254 | 0.008 | 0.010 |
| I | 0.000 | 0.152 | 0.000 | 0.006 |
| J | 5.791 | 6.198 | 0.228 | 0.244 |
| M | 0.406 | 1.270 | 0.016 | 0.050 |
| X | 2.057 | 2.515 | 0.081 | 0.099 |
| Y | 2.057 | 3.404 | 0.081 | 0.134 |

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