

GSC3842

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

Description

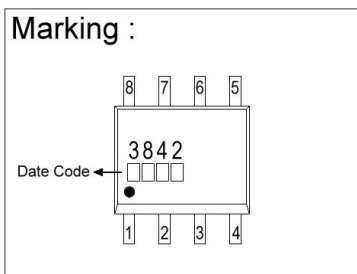
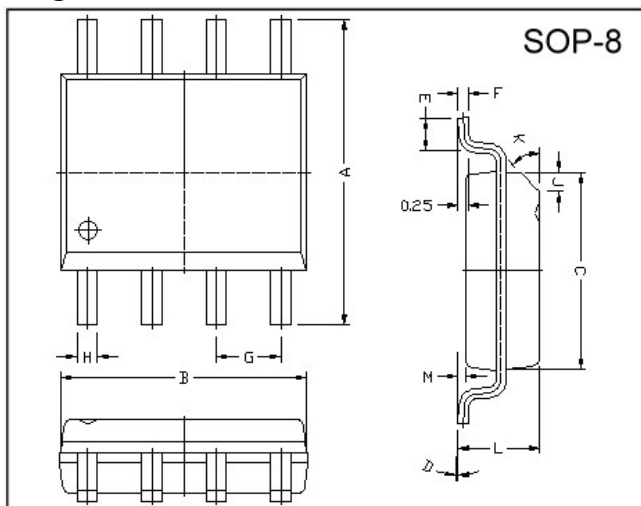
The GSC3842 is high performance fixed frequency current mode controllers. This is specifically designed for Off-Line and DC To DC converter applications offering the designer a cost-effective solution with minimal external components.

These integrated circuits feature a trimmed oscillator for precise duty cycle control. A temperature compensated reference, high gain Error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET. Also Included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and latch for single pulse metering.

Features

- *Trimmed Oscillator for Precise Frequency Control
- *Oscillator Frequency Guaranteed at 250kHz
- *Current Mode Operation to 500kHz
- *Automatic Feed Forward Compensation
- *latching PWM for Cycle-By-Cycle Current Limiting
- *Internally Trimmed Reference with Undervoltage Lockout
- *High Current Totem Pole Output
- *Undervoltage Lockout with Hysteresis
- *Low Startup and Operating Current

Package Dimensions



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

SOP-8L	Function	Description
	Pin1: Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
	Pin2: Voltage Feedback	This is the inverting input of the Error Amplifier. It's normally connected to the Switching power supply output through a resistor divider.
	Pin3: Current Sense	A voltage proportional to inductor current is connected to this input .The PWM uses this information to terminate the output switch conduction.
	Pin4: RT/CT	The oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground .Operation 500kHz is possible.
	Pin5: Ground	This pin is the combined control circuitry and power ground.
	Pin6: Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1 A are sourced and sunk by this pin.
	Pin7: Vcc	This pin is the positive supply of the control IC.
	Pin8: Vref	This is the reference output .It provides charging current for capacitor CT through resistor RT.

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Value	Unit
Total power Supply and Zener current	(IC _C +I _Z)	30	mA
Output current, source or sink(note1)	I _o	1.0	A
Output energy(capacitive load per cycle)	W	5.0	μJ
Current sense and voltage feedback inputs	V _{in}	-0.3 to 5.5	V
Error Amplifier Output Sink Current	I _o	10	mA

Power Dissipation at Thermal characteristics	PD P _{θJA}	702 178	mW °C/W
Storage Temperature Range	T _{stg}	-65 to 150	°C
Operating Junction Temperature	T _J	+150	°C
Operating ambient Temperature	T _A	0~+70	°C

Electrical Characteristics (0°C ≤ T_A ≤ 70°C, V_{CC}=15V [note 2], R_T=10k, C_T=3.3nF, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reference Section						
Output Voltage	VREF	T _J =25°C, I _o =1mA	4.90	5	5.1	V
Line Regulation	Regline	V _{CC} =12V to 25V	-	2.0	20	mV
Load Regulation	Regload	I _o =1mA to 20mA	-	3.0	25	mV
Temperature Stability	T _s	-	-	0.2	-	mV/°C
Total Output Variation	VREF	Line, Load, Temperature	4.82	-	5.18	V
Output Noise Voltage	V _n	F=10kHz to 10Hz, T _J =25°C	-	50	-	μV
Long Term Stability	S	T _A =125°C, 1000Hrs	-	5	-	mV
Output Short Circuit current	ISC	-	-30	-85	-180	mA
Oscillator Section						
Frequency		T _J =25°C	49	52	55	KHz
		T _A =0°C to 70°C	48	-	56	
		T _J =25°C (R _T =6.2k, C _T =1.0nF)	225	250	275	
Frequency Change with Voltage	Δfosc/ΔV	V _{CC} =12V to 25V	-	0.2	1.0	%
Frequency Change with Temperature	Δfosc/ΔT	T _A = 0°C to 70 °C	-	0.5	-	%
Oscillator Voltage Swing(Peak to Peak)	VOSC	-	-	1.6	-	V
Discharge Current	I _{dischg}	T _J =25°C	7.8	8.3	8.8	mA
		T _A = 0°C to 70°C	7.6	-	8.8	
Error Amplifier Section						
Voltage Feedback Input	VFB	V _o =2.5V	2.42	2.50	2.58	V
Input Bias Current	I _{IB}	VFB=5.0V	-	-0.1	-2.0	μA
Open Loop Voltage Gain	AVOL	V _o =2V to 4V	65	90	-	dB
Unity Gain Bandwidth	BW	T _J =25°C	0.7	1.0	-	MHz
Power Supply Rejection Ratio	PSRR	V _{CC} =12V to 25V	60	70	-	dB
Output Sink Current	I _{sink}	V _o =1.1V, VFB=2.7V	2.0	12	-	mA
Output Source Current	I _{source}	V _o =5.0V, VFB=2.3V	-0.5	-1.0	-	mA
Output Voltage Swing High State	V _{OH}	VFB=2.3V, R _L =15K to GND	5.0	6.2	-	V
Output Voltage Swing Low State	V _{OL}	VFB=2.7V, R _L =15K to Vref	-	0.8	1.1	V
Current Sense section						
Current Sense Input Voltage gain	A _v	(Note 3,4)	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold	V _{th}	(Note 3)	0.9	1.0	1.1	V
Power Supply Rejection Ratio	PSRR	V _{CC} = 12 to 25V (Note 3)	-	70	-	dB
Input Bias Current	I _{IB}	-	-	-2	-10	μA
Propagation Delay	T _{plh} (in/out)	Current Sense Input to Output	-	150	300	ns
Output Low Voltage	V _{OL}	I _{sink} =20mA	-	0.1	0.4	V
		I _{sink} =200mA	-	1.6	2.2	V
Output High Level	V _{OH}	I _{source} =20mA	13	13.5	-	V
		I _{source} =200mA	12	13.4	-	V
Output Voltage with UVLO Activated	V _{OL} (UVLO)	V _{CC} =6.0V, I _{sink} =1.0mA	-	0.1	1.1	V
Output Voltage Rise Time	t _r	T _J =25°C, C _L =1nF	-	50	150	ns
Output Voltage Fall Time	t _r	T _J =25°C, C _L =1nF	-	50	150	ns
Under-Voltage Lockout Section						
Startup Threshold	V _{th}	-	14.5	16	17.5	V
Min. Operating Voltage After Turn-on(V _{CC})	V _{CC} (min)	-	8.5	10	11.5	V

PWM Section						
Maximum Duty Cycle	DC(MAX)	-	94	96	-	%
Minimum Duty Cycle	DC(MIN)	-	-	-	0	%
Total Device						
Power Startup Supply Current	I _{CC+IC}	V _{CC} =14V	-	0.3	0.5	mA
Power Operating Supply Current	I _{CC+IC}	Note 2	-	12	17	mA
Power Supply Zener Voltage	V _Z	I _{CC} =25mA	30	36	-	V

Note 1: Maximum Package power dissipation limits must be observed.

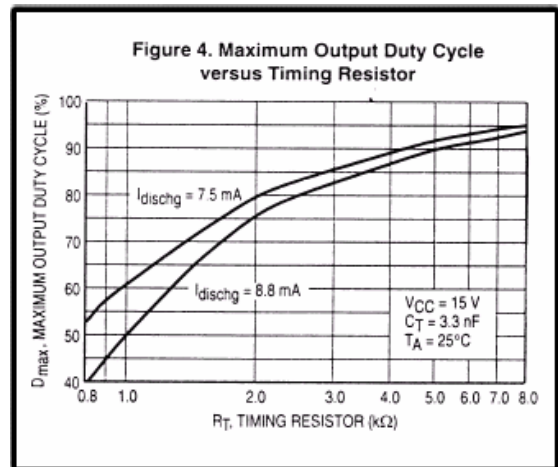
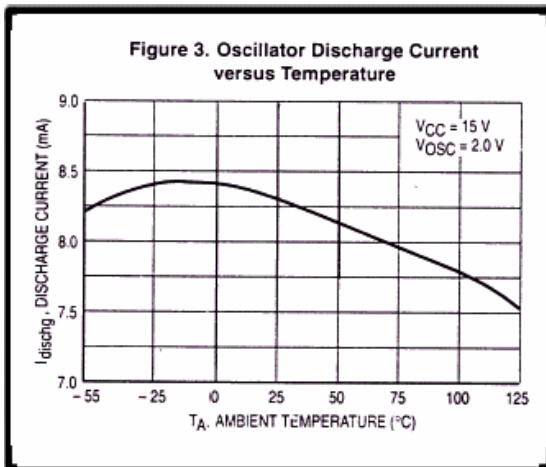
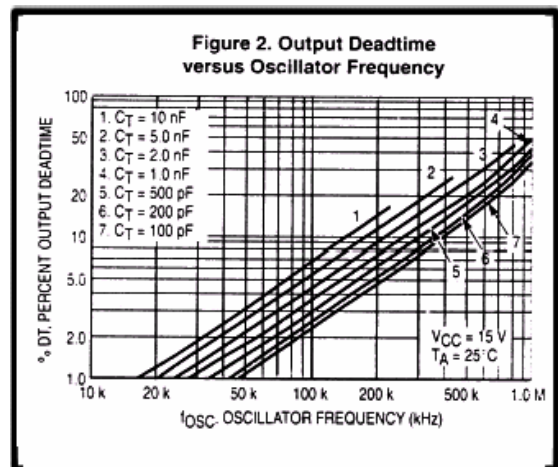
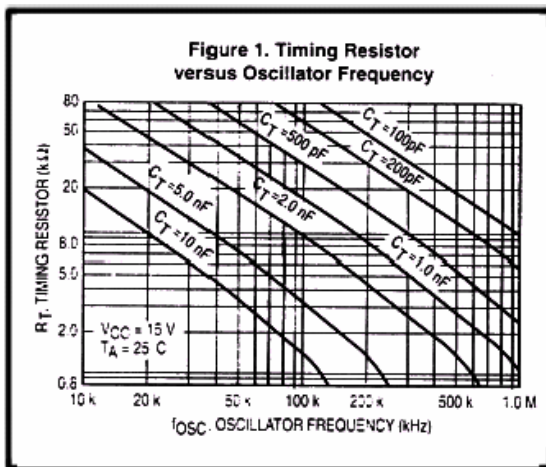
Note 2: Adjust V_{CC} above the Startup threshold before setting to 15V.

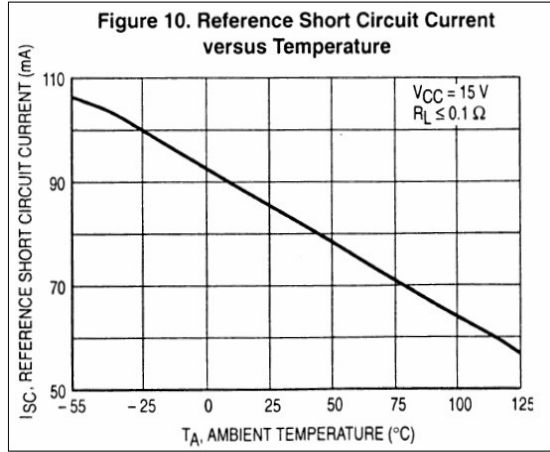
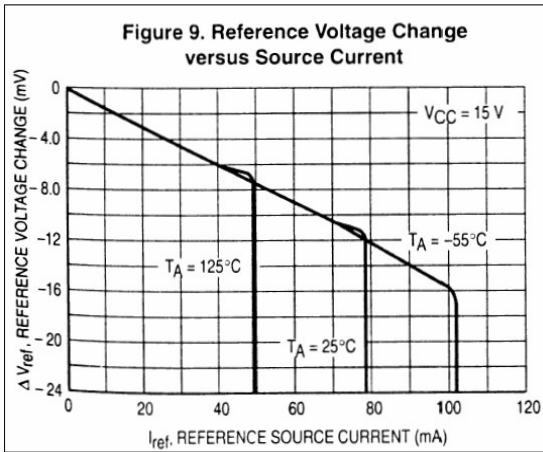
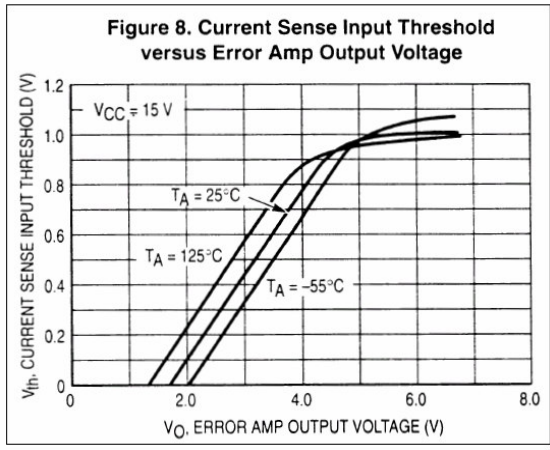
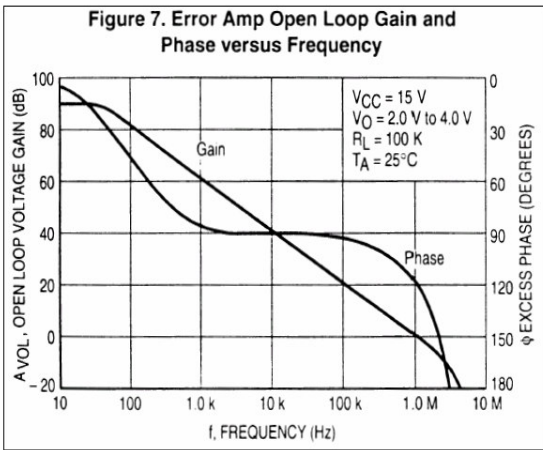
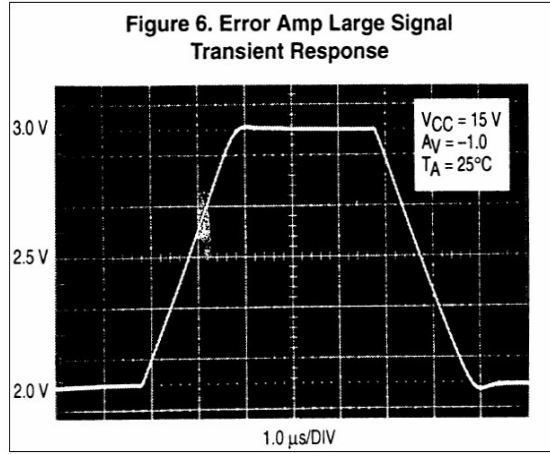
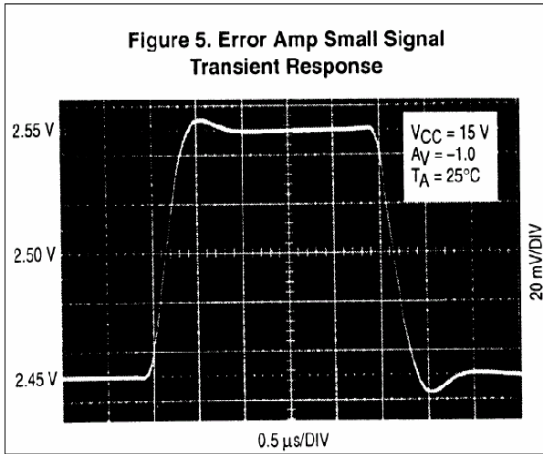
Note 3: This parameter is measured at the latch trip point with V_{FB}=0V.

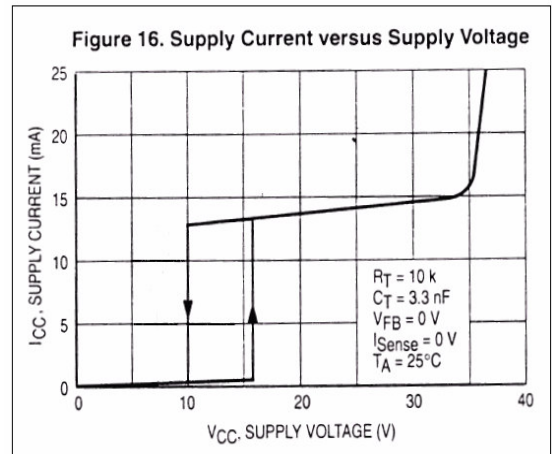
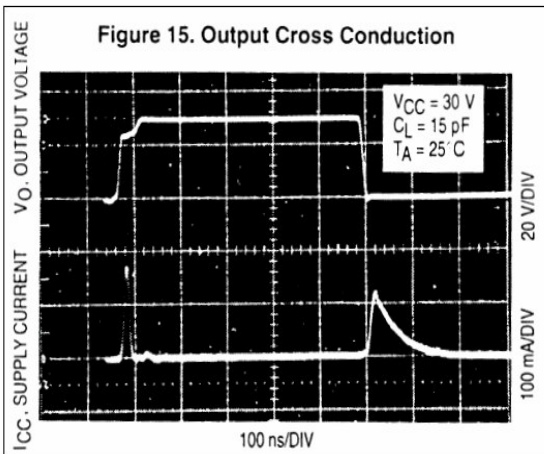
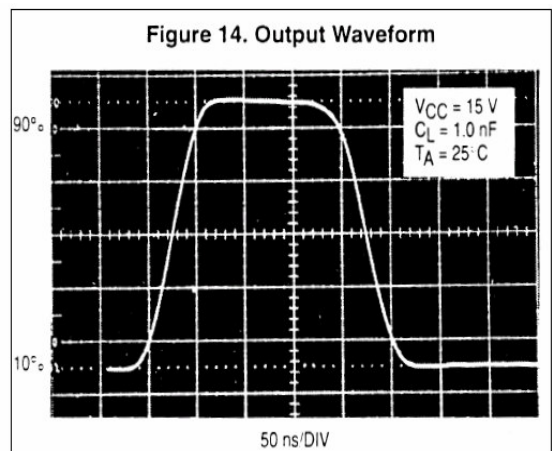
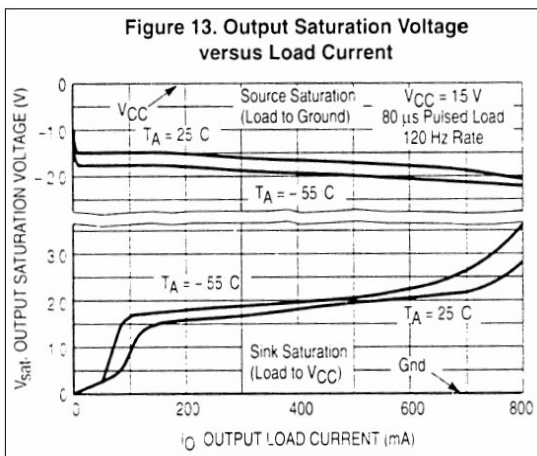
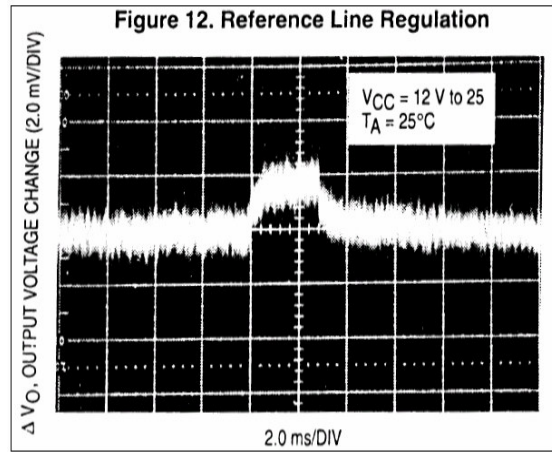
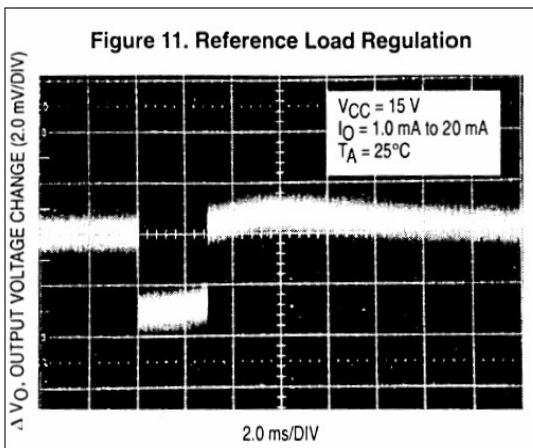
Note 4: Comparator gain is defined as::

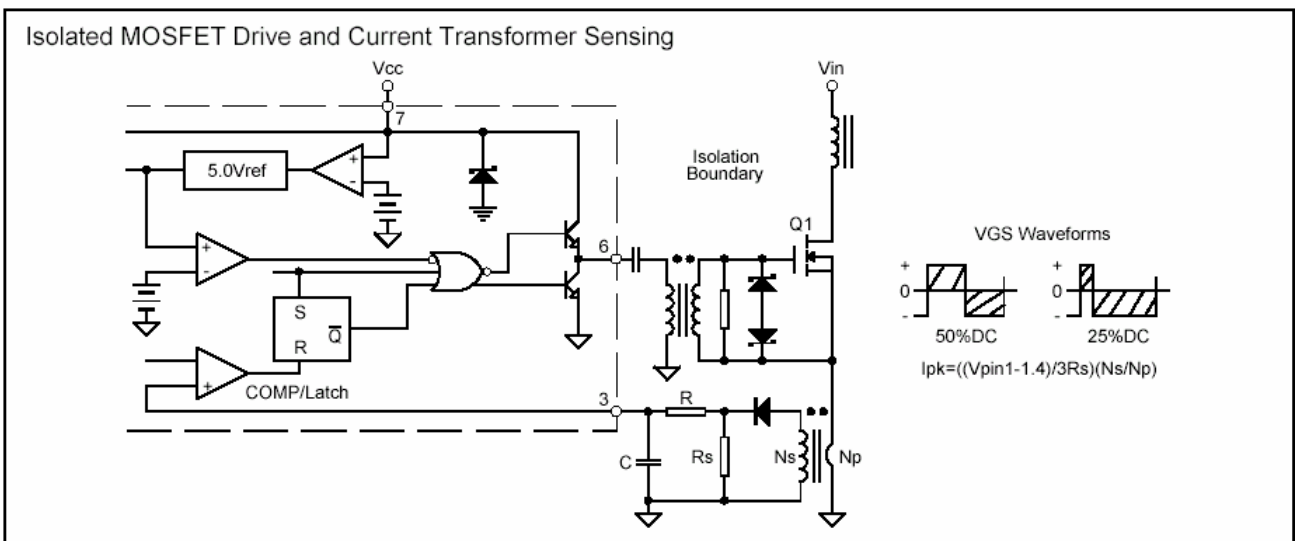
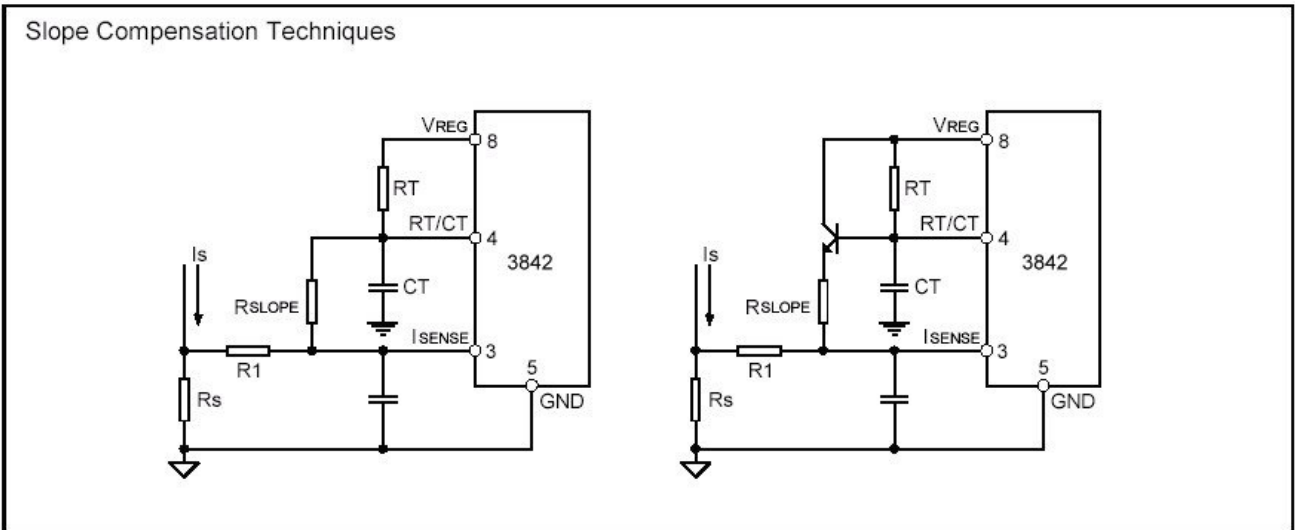
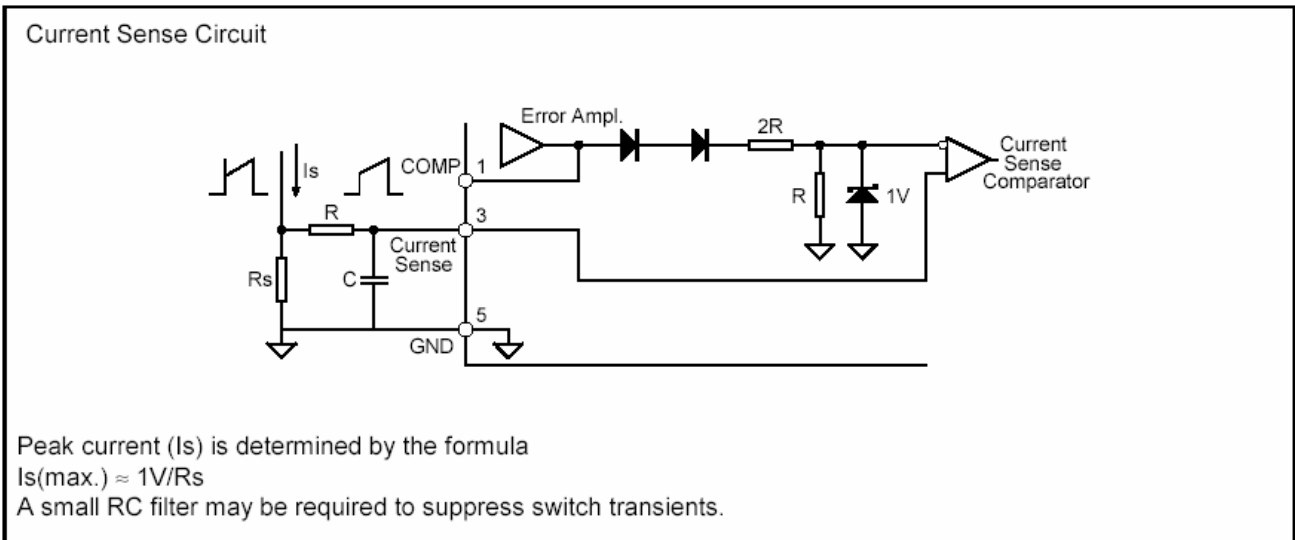
$$AV = \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$$

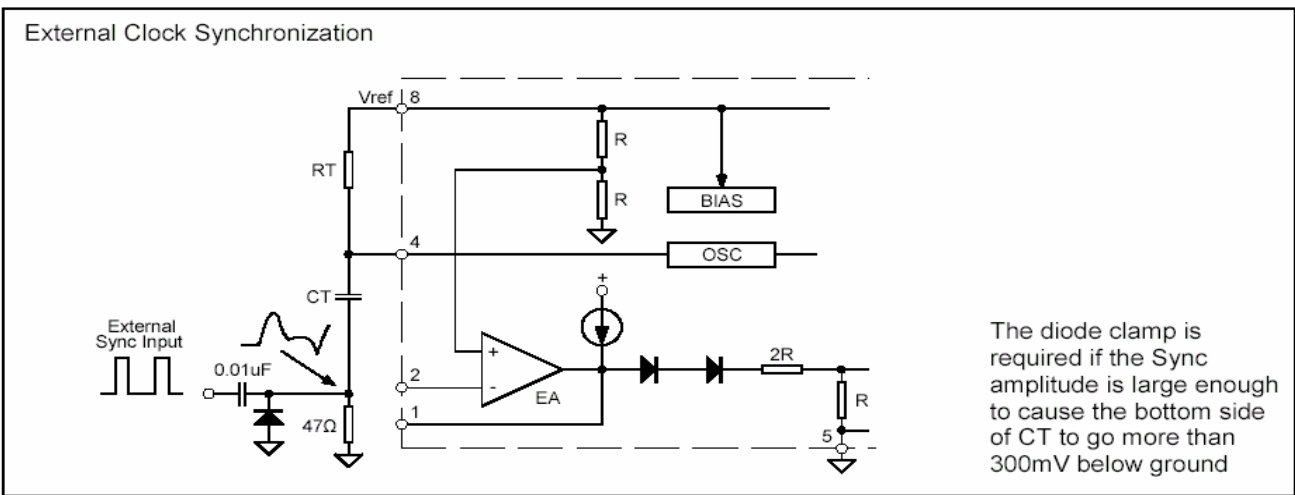
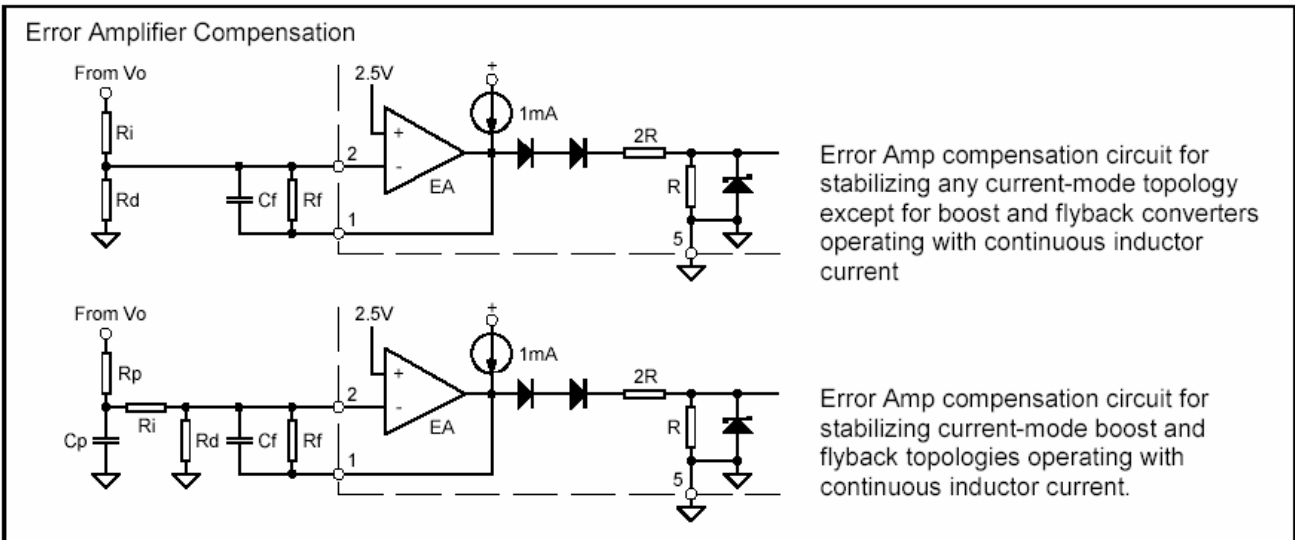
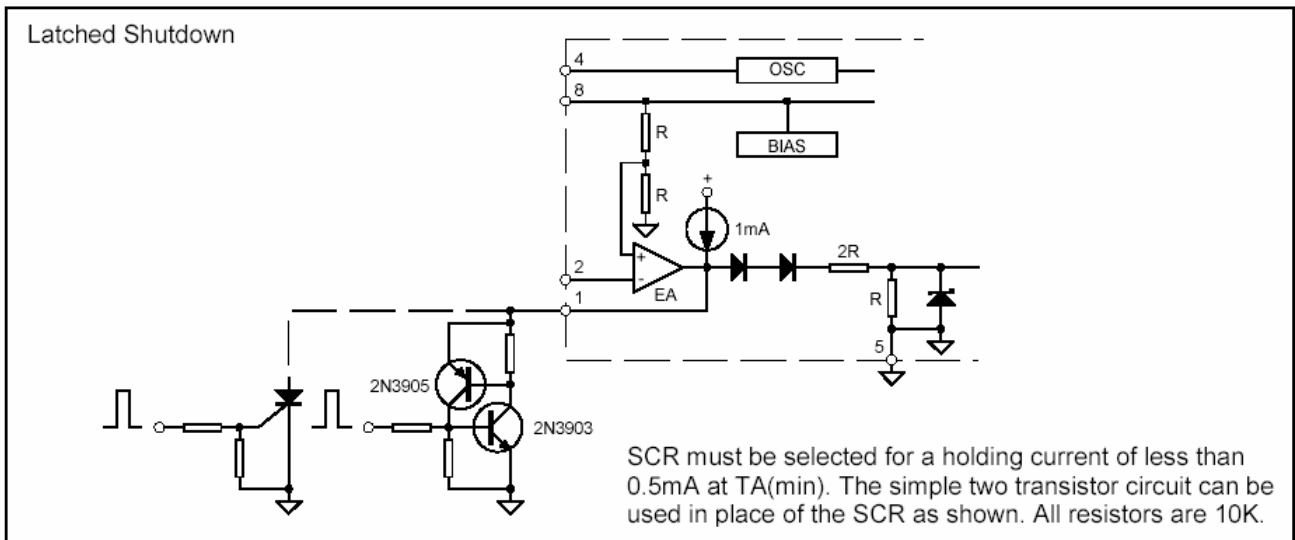
Characteristics Curve

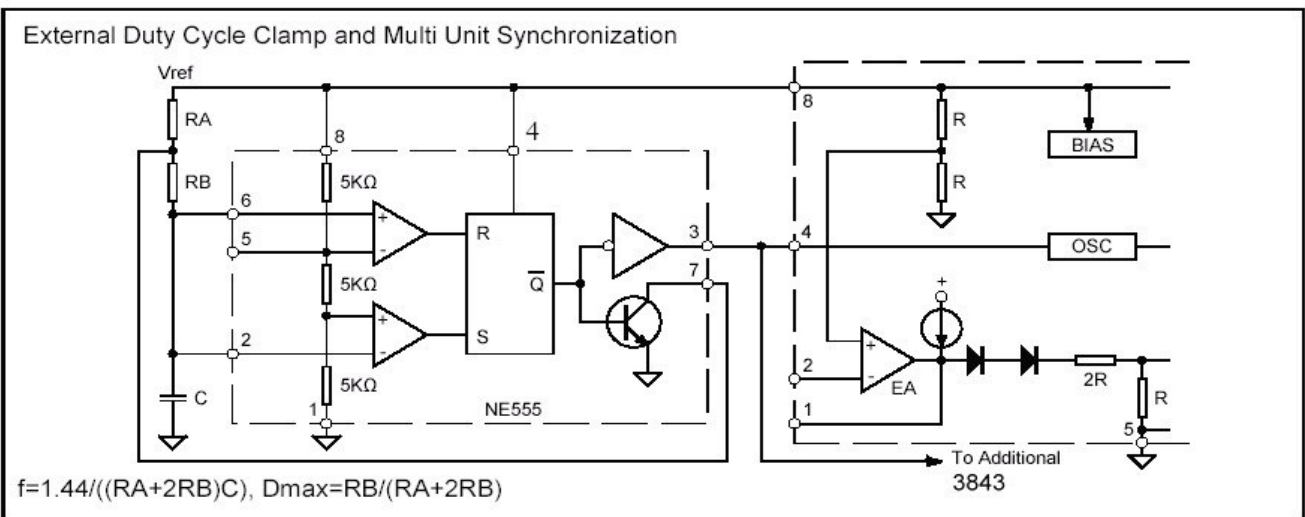
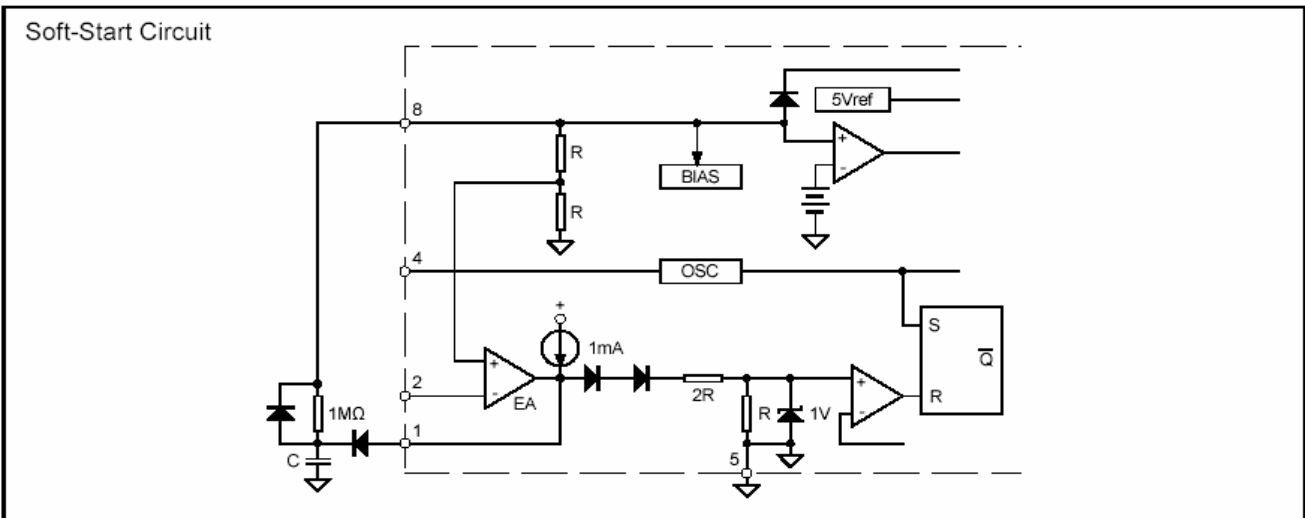
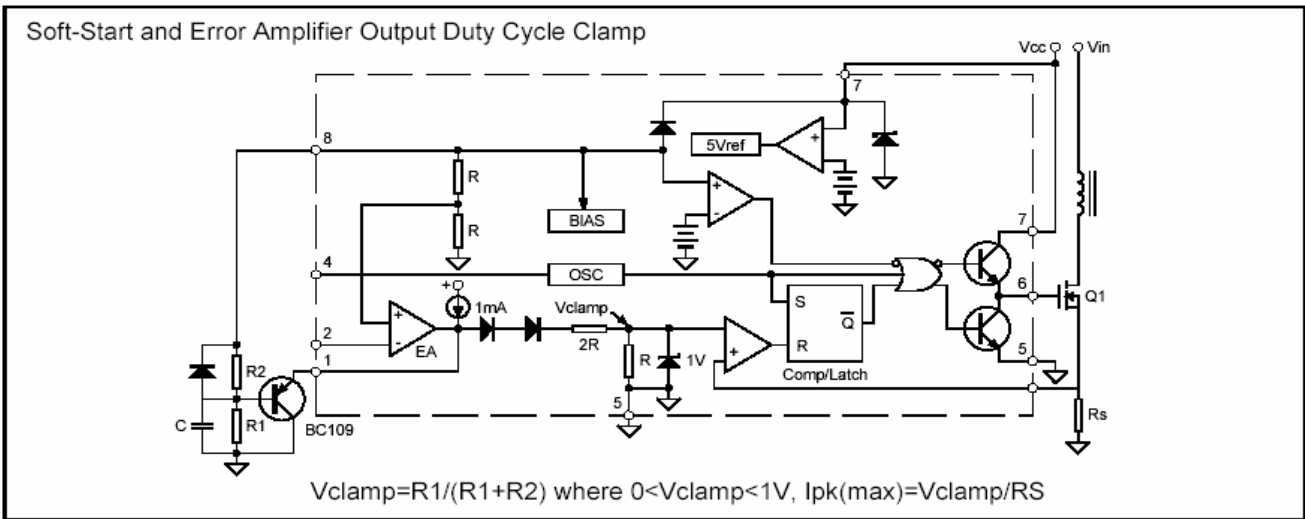












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Head Office And Factory:

- Taiwan:** No. 17-1 Tatung Rd. Fu Kou Hsin-Chu Industrial Park, Hsin-Chu, Taiwan, R. O. C.
- TEL : 886-3-597-7061 FAX : 886-3-597-9220, 597-0785
- China:** (201203) No.255, Jang-Jiang Tsai-Lueng RD. , Pu-Dung-Hsin District, Shang-Hai City, China
- TEL : 86-21-5895-7671 ~ 4 FAX : 86-21-38950165