

GSMD18N20

200V N-Channel MOSFETs

Product Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

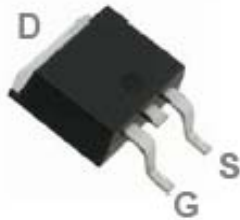
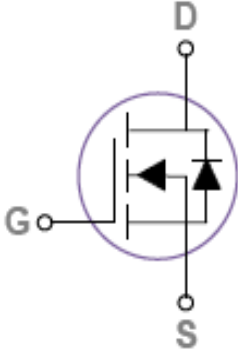
Features

- 200V, 18A, $R_{DS(ON)}=140m\Omega@V_{GS}=10V$
- Improved dv/dt capability
- Fast switching
- V_{GS} Guaranteed $\pm 25V$
- Green Device Available
- TO-252-2L package

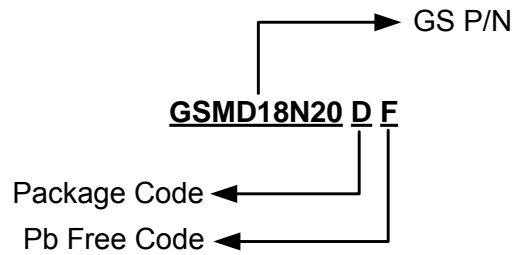
Applications

- LED Backlight & Lighting
- UPS
- High Voltage Switching
- Motor Drive Applications

Packages & Pin Assignments

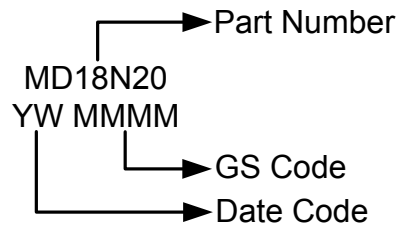
GSMD18N20DF (TO-252-2L)	
 <p>Top View</p>	
Description	
Gate	
Source	
Drain	

Ordering Information



Part Number	Package	Quantity Reel
GSMD18N20DF	TO-252-2L	2500 PCS

Marking Information



Absolute Maximum Ratings

$T_C=25^\circ\text{C}$ Unless otherwise noted

Symbol	Parameter	Typical	Unit
V_{DS}	Drain-Source Voltage	200	V
V_{GS}	Gate-Source Voltage	± 25	V
I_D	Continuous Drain Current	$T_C=25^\circ\text{C}$	18
		$T_C=100^\circ\text{C}$	11
I_{DM}	Pulsed Drain Current	72	A
EAS	Single Pulse Avalanche Energy	100	mJ
IAS	Single Pulse Avalanche Current	10	A
P_D	Power Dissipation ($T_C=25^\circ\text{C}$)	104	W
	Power Dissipation (Derate above 25°C)	0.83	W/ $^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to +150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance-Junction to Case	1.2	$^\circ\text{C}/\text{W}$

Note 1: Repetitive Rating : Pulsed width limited by maximum junction temperature.

Note 2: $V_{DD}=50\text{V}$, $V_{GS}=10\text{V}$, $L=2\text{mH}$, $I_{AS}=10\text{A}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

Electrical Characteristics

T_A=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	200			V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =1mA		0.08		V/°C
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient			-6		mV/°C
I _{GSS}	Gate Source Leakage Current	V _{DS} =0V, V _{GS} =±25V			±100	nA
I _{DSS}	Drain Source Leakage Current	V _{DS} =160V, V _{GS} =0V			1	μA
		V _{DS} =160V, V _{GS} =0V, T _J =125°C			30	
I _S	Continuous Source Current	V _G =V _D =0V, Force Current			18	A
I _{SM}	Pulsed Source Current				72	
R _{DS(on)}	Static Drain Source On-Resistance	V _{GS} =10V, I _D =9A		110	140	mΩ
V _{SD}	Diode Forward Voltage	V _{GS} =0V, I _S =1A			1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} =0V, I _S =1A, di/dt=100A/μs		105		ns
Q _{rr}	Reverse Recovery Charge			360		nC
Dynamic						
Q _g	Total Gate Charge	V _{DS} =100V, V _{GS} =10V, I _D =8A		40		nC
Q _{gs}	Gate-Source Charge			10		
Q _{gd}	Gate-Drain Charge			10		
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz		2000		pF
C _{oss}	Output Capacitance			145		
C _{rss}	Reverse Transfer Capacitance			60		
t _{d(on)}	Turn-On Delay Time	V _{DD} =30V, V _{GS} =10V, R _G =6Ω, I _D =1A		9		ns
t _r	Rise Time			6		
t _{d(off)}	Turn-Off Delay Time			48		
t _f	Fall Time			12		

Note 3: The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%.

Note 4: Essentially independent of operating temperature.

Typical Performance Characteristics

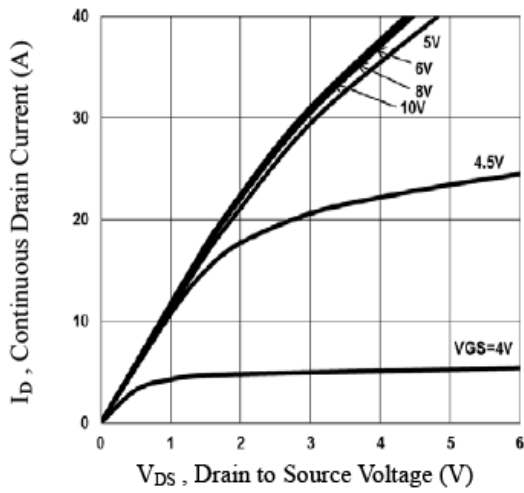


Fig.1 Output Characteristics

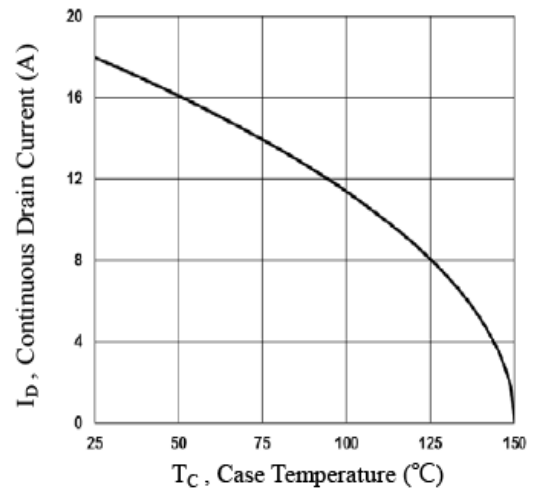


Fig.2 Continuous Drain Current vs. T_c

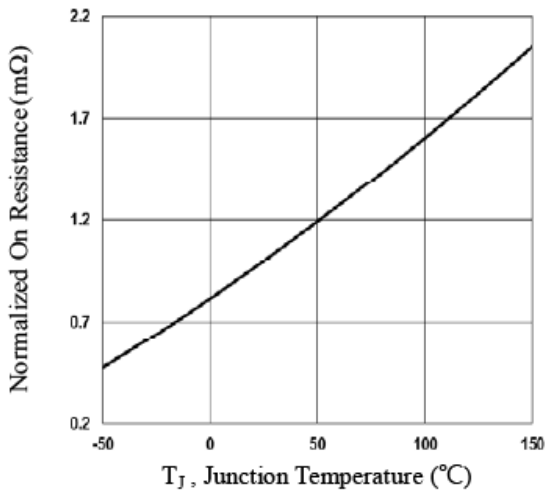


Fig.3 Normalized $R_{DS(on)}$ vs. T_j

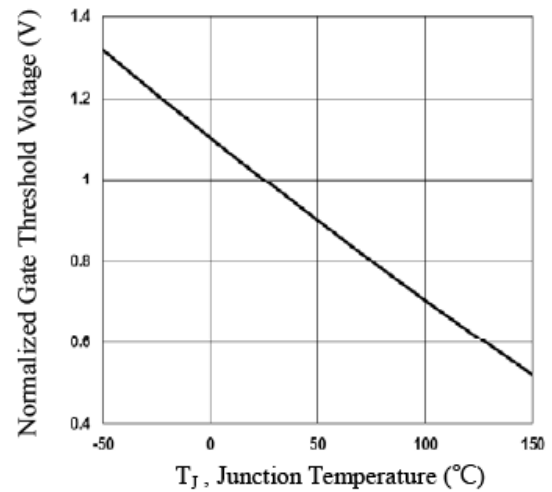


Fig.4 Normalized V_{th} vs. T_j

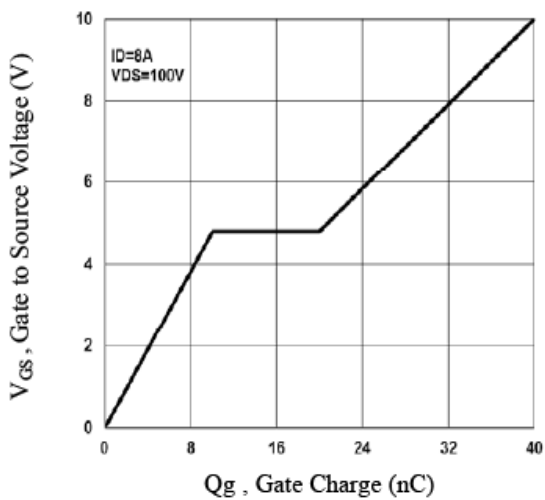


Fig.5 Gate Charge Waveform

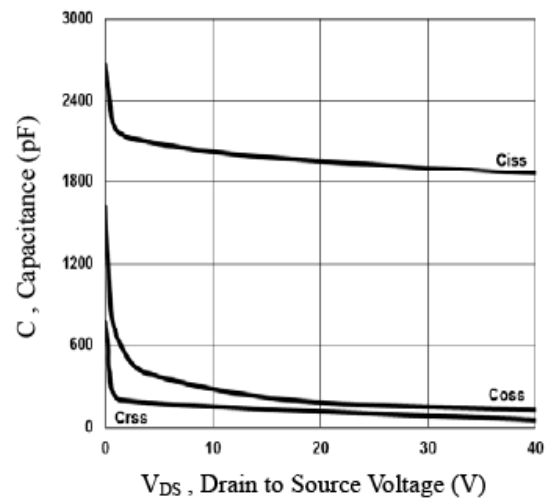


Fig.6 Capacitance Characteristics

Typical Performance Characteristics (Continue)

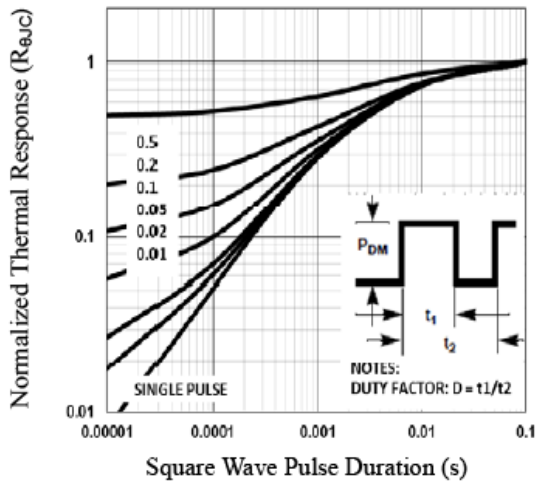


Fig.7 Normalized Transient Impedance

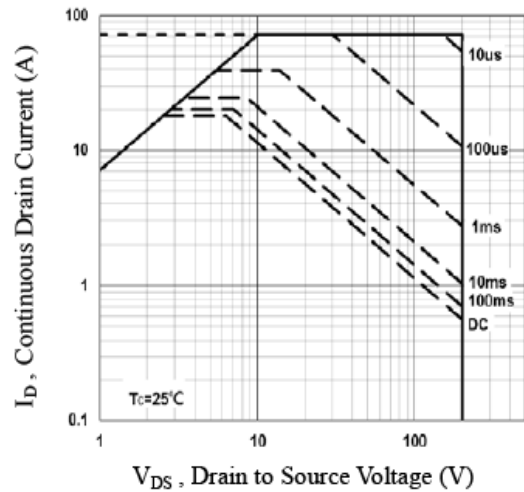
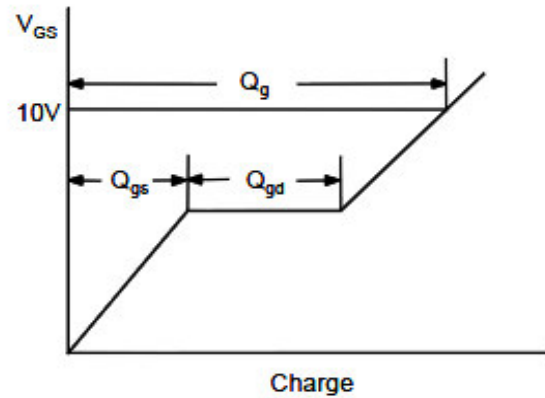
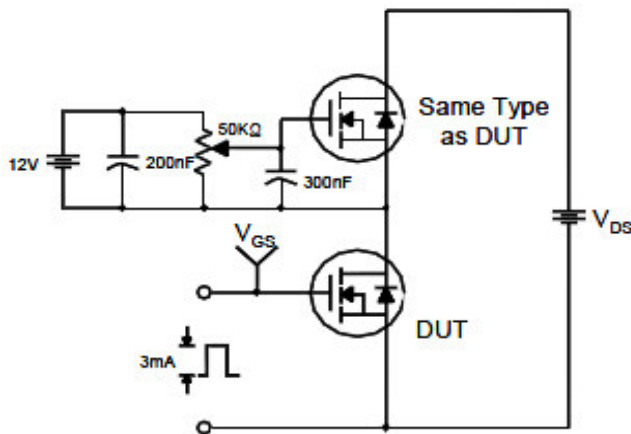
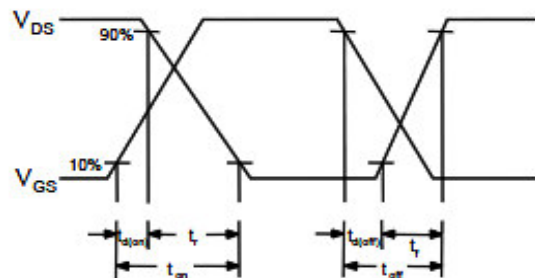
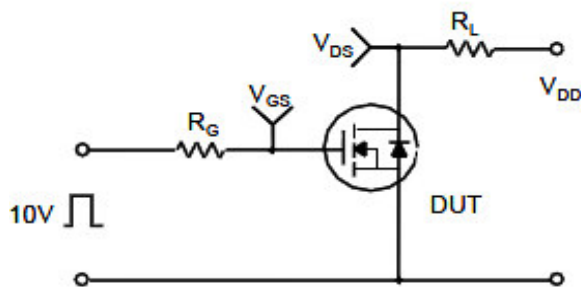


Fig.8 Maximum Safe Operation Area

Gate Charge Test Circuit & Waveform

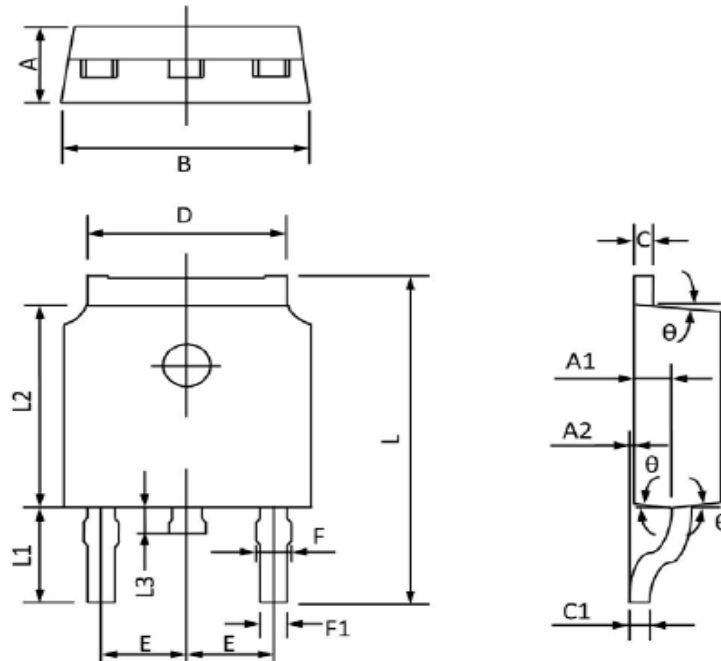


Resistive Switching Test Circuit & Waveforms



Package Dimension

TO-252-2L










Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.20	2.40	0.087	0.094
A1	0.91	1.11	0.036	0.044
A2	0.00	0.15	0.000	0.006
B	6.50	6.70	0.256	0.264
C	0.46	0.580	0.018	0.230
C1	0.46	0.580	0.018	0.030
D	5.10	5.46	0.201	0.215
E	2.186	2.386	0.086	0.094
F	0.74	0.94	0.029	0.037
F1	0.660	0.860	0.026	0.034
L	9.80	10.40	0.386	0.409
L1	2.9REF		0.114REF	
L2	6.00	6.20	0.236	0.244
L3	0.60	1.00	0.024	0.039
θ	3°	9°	3°	9°



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