Advanced

GT24CN512A

2-WIRE 512K Bits

Serial EEPROM

With NFC Forum Type2 Tag

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Table of Contents

1. Features

- Dual interface combined
  - Two-Wire Serial Interface, I^2C^{TM} Compatible same as standard EEPROM protocol
  - RF communication interface which conform to ISO/IEC14443A standard for NFC Forum Type2
- EEPROM organization: 128Kb (16,384 x 8)
- NFC Forum Type 2 Tag compliant IC
- RF field detection interrupt functionality
- Lead-free, RoHS, Halogen free, Green
- Industrial grade: -40°C~+85°C
- Packages: SOIC, TSSOP, UDFN
- High-reliability
  - Endurance: 1 million cycles
  - Data retention: 100 years
- The target application: connection handover, Bluetooth simple pairing, Wi-Fi Protected set-up, device authentication, gaming and others

1.1 EEPROM Features

- Two-Wire Serial Interface, I^2C^{TM} Compatible
  - Bi-directional data transfer protocol
- Wide-voltage Operation
  - V_{CC} = 1.7V to 5.5V
- Speed: 400 KHz (1.7V) and 1 MHz (2.5V~5.5V)
- Standby current (max.): 1 μA, 5.5V
- Operating current (max.): 0.5 mA, 5.5V
- Hardware Data Protection
  - Write Protect Pin
- Sequential & Random Read Features
- Page Size: 128 bytes
- Page write mode
  - Partial page writes allowed
  - Addition write lockable page (Identification Page)
- Self timed write cycle: 5 ms (max.)
- Noise immunity on inputs, besides Schmitt trigger

1.2 Tag Features

- Contactless transmission of data and supply energy
- Up to 100mm operation distance
- 13.56MHz operating frequency
- 106k bit/s date rate
- High data integrity: 16-bit CRC, parity, bit coding, bit counting
- True anti-collision
- 7 byte serial number (cascade level 2 according to ISO/IEC 14443-3)
- 168 bytes of total memory, divided in 42 pages (4 bytes each)
- 144 bytes of user Read/Write memory area, divided in 36 pages (4 bytes each)
- Field programmable read-only locking function per page 16 pages (64 bytes) of the memory
- Field programmable read-only locking function per block (2 pages)
- 32-bit user definable One-Time Programmable (OTP) area
- 16-bit counter
- RF field detection functionality for waking up MCU or trigger further actions.
- Anti-cloning support by unique 7-byte serial number for each device
- The UID is 7 bytes long and supports cascade level 2 according to ISO/IEC 14443-3.
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2. General Description

The GT24CN512A is an EEPROM combined with and NFC Forum Type2 product which is fully compatible to industrial standard I^2C/SMBus interface and compliant to ISO/IEC 14443A standard. The GT24CN512A contains a memory array of 512K-bits (65,536x8), which is organized in 128-byte per page.

The EEPROM can operate in a wide voltage range from 1.7V to 5.5V which fits most application. This product can provide a low-power 2-wire EEPROM solution. The device is offered in Lead-free, RoHS, halogen free or Green. The available package types are 8-pin SOIC, TSSOP and UDFN.

Under no circumstance, the device will be hung up. In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, the device does not respond to any instructions until the supply voltage (V_{CC}) has reached an acceptable stable level above the reset threshold voltage. Once V_{CC} passes the power on reset threshold, the device is reset and enters into the Standby mode. This would also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once V_{CC} drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is illegal to send a command unless the V_{CC} is within its operating level.

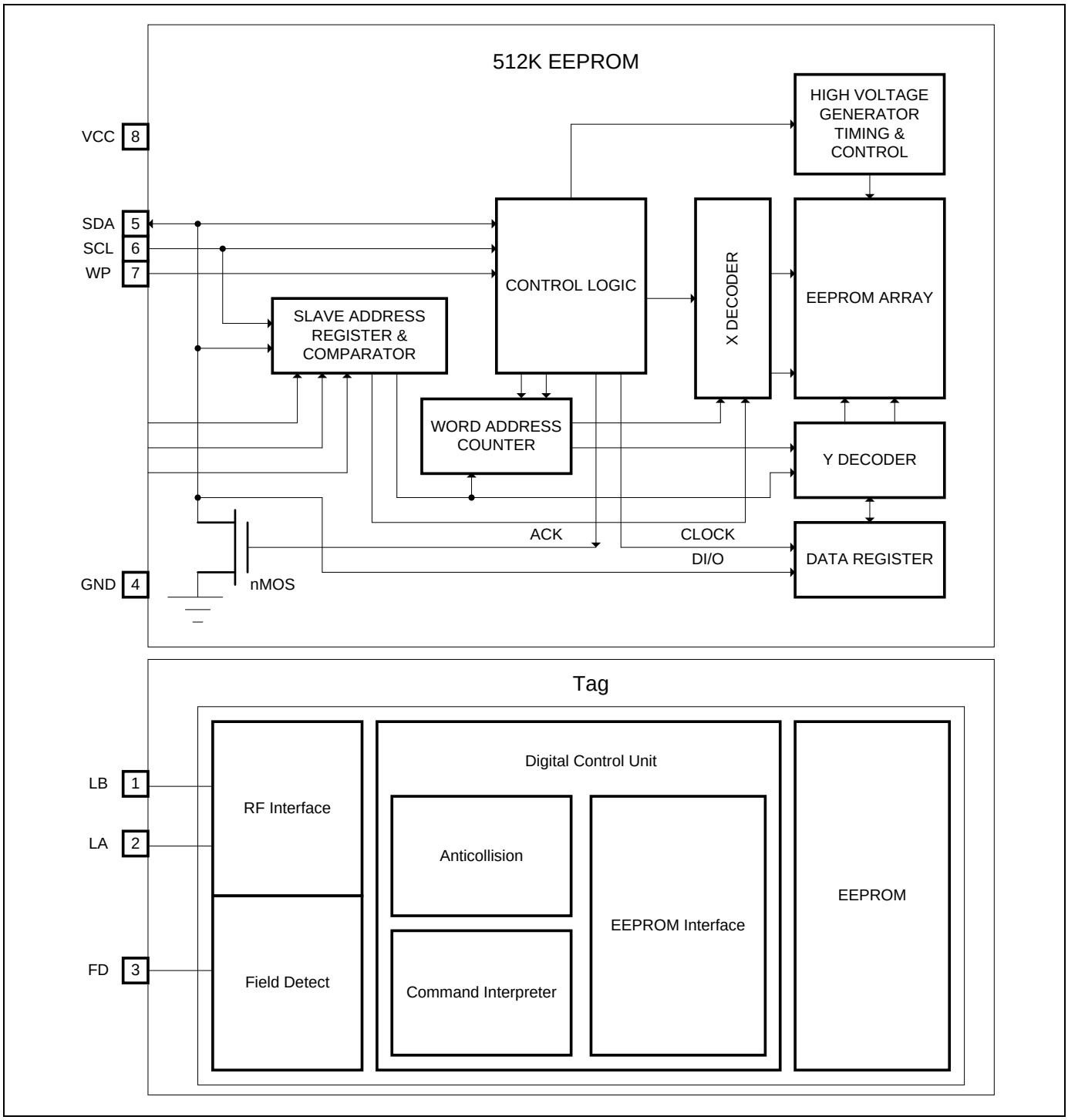
The GT24CN512A is compatible to the standard 2-wire bus protocol. The simple bus consists of Serial Clock (SCL) and Serial Data (SDA) signals. Utilizing such bus protocol, a Master device, such as a microcontroller, can usually control one or more Slave devices, alike this GT24CN512A. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The GT24CN512A also has a Write Protect function via WP pin to cease from overwriting the data stored inside the memory array. The GT24CN512A offers an additional page (Identification Page) of 64 bytes. The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

The GT24CN512A is NFC Forum Type 2 Tag compliant IC - to be used with NFC enabled devices according to NFC Forum technical specifications, according to NFC Forum recommendations or Proximity Coupling Devices (PCD), according to ISO/IEC 14443A. The communication layer (RF Interface) complies to parts 2 and 3 of the ISO/IEC 14443A standard.

The communication to Tag can be established only when the IC is connected to an antenna. When the Tag is positioned in the RF field, the high speed RF communication interface allows the transmission of the data with a baud rate of 106 kbit/s.

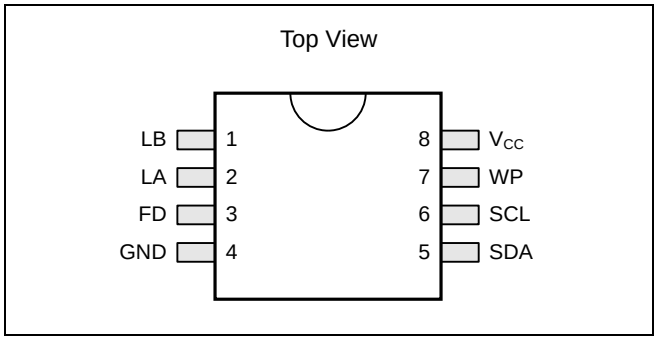
The combo product GT24CN512A is primarily designed for NFC Forum Type 2 Tag applications in electronics (i.e. connection handover, Bluetooth simple pairing, Wi-Fi Protected set-up, device authentication, gaming and others).

3. Functional Block Diagram

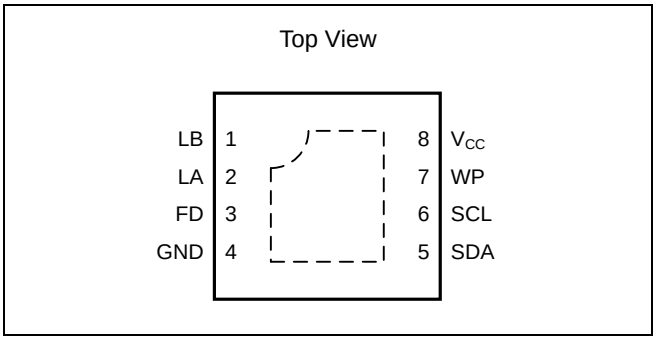


4. Pin Configuration

4.1 8-Pin SOIC and TSSOP



4.2 8-Lead UDFN



4.3 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	LB	I	Antenna connection LB
2	LA	I	Antenna connection LA
3	FD	O	RF Field Detect connection
4	GND	-	Ground
5	SDA	I/O	Serial Address, Data input and Data output
6	SCL	I	Serial Clock Input
7	WP	I	Write Protect Input
8	V_{CC}	-	Power Supply

4.4 Pin Descriptions

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

SDA

The SDA is a bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wired with other open drain or open collector outputs. However, the SDA pin requires a pull-up resistor connected to the power supply.

LB, LA

The A0, A1 and A2 are the device address inputs.

Typically, the A0, A1, and A2 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. When A0, A1, and A2 are left floating, the inputs are defaulted to zero.

FD

GT24CN512A features an additional RF field detection functionality. The corresponding output signal can be used as interrupt source to e.g. wake up an embedded microcontroller or trigger further actions.

WP

WP is the Write Protect pin. While the WP pin is connected to the power supply of GT24CN512A, the entire array becomes Write Protected (i.e. the device becomes Read only). When WP is tied to Ground or left floating, the normal write operations are allowed.

V_{CC}

Supply voltage

GND

Ground of supply voltage

5. Device Operation

The GT24CN512A serial interface supports communications using industrial standard 2-wire bus protocol, such as I^2C.

5.1 2-WIRE Bus

The two-wire bus is defined as Serial Data (SDA), and Serial Clock (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device that generates the SCL, controls the bus access, and generates the Start and Stop conditions. The GT24CN512A is the Slave device.

5.2 The Bus Protocol

Data transfer may be initiated only when the bus is not busy. During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated by a Stop condition.

5.3 Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

5.4 Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

5.5 Acknowledge

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

5.6 Reset

The GT24CN512A contains a reset function in case the 2-wire bus transmission on is accidentally interrupted (e.g. a power loss), or needs to be terminated mid-stream. The reset is initiated when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

5.7 Standby Mode

While in standby mode, the power consumption is minimal. The GT24CN512A enters into standby mode during one of the following conditions: a) After Power-up, while no Op-code is sent; b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related; or c) After the completion of any internal write operations.

5.8 Device Addressing

The Master begins a transmission on by sending a Start condition, then sends the address of the particular Slave devices to be communicated. The Slave device address is 8 bits format as shown in Figure. 5-5.

The four most significant bits of the Slave address are fixed (1010) for GT24CN512A.

The next three bits, A0, A1 and A2, of the Slave address are specifically related to EEPROM. Up to eight GT24CN512A units can be connected to the 2-wire bus.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, Read operation is selected. While it is set to 0, Write operation is selected.

After the Master transmits the Start condition and Slave address byte appropriately, the associated 2-wire Slave device, GT24CN512A, will respond with ACK on the SDA line. Then GT24CN512A will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data.

The GT24CN512A then prepares for a Read or Write operation by monitoring the bus.

5.9 Write Operation

5.9.1 Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the GT24CN512A. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The GT24CN512A acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

5.9.2 Page Write

The GT24CN512A is capable of 128-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 127 more bytes. After the receipt of each data word, the EEPROM responds immediately with an ACK on SDA line, and the seven lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 128 bytes prior to issuing the Stop condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 128 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the GT24CN512A in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

5.9.3 Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the GT24CN512A initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the GT24CN512A has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

5.9.4 Write Identification Page

The Identification Page (128 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier=1011b
- MSB address bits A15/A7 are don’t care except for address bit A10 which must be ‘0’. LSB address bits A6/A0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoACK).

5.9.5 Lock Identification Page

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The lock ID instruction is similar to Byte Write (into memory array) with the following specific condition:

- Device type identifier=1011b
- Address bit A10 must be ‘1’; all other address bits are don’t care
- The data byte must be equal to the binary value xxxx xx1x, where x is don’t care

5.10 Read Operation

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read and sequential read.

5.10.1 Current Address Read

The GT24CN512A contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the EEPROM receives the Slave Addressing Byte with a Read operation (R/W bit set to “1”), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the GT24CN512A discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 5-8. Current Address Read Diagram.)

5.10.2 Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the GT24CN512A acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The EEPROM then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 5-9. Random Address Read Diagram.)

5.10.3 Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the GT24CN512A sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the GT24CN512A. The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition. The data output is sequential, with the data from address n followed by the data from address n+1,n+2 ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of the array is reached, the address counter “rolls over” to address 0, and the device continues to output data. (Refer to Figure 5-10. Sequential Read Diagram).

5.10.4 Read Identification Page

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits A15/A7 are don’t care, the LSB address bits A6/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.:when reading the Identification Page from location 100d, the number of bytes should be less than or equal to 28, as the ID page boundary is 128 bytes).

5.10.5 Read the lock status

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification page is unlocked, otherwise a NoACK bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a start followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic.
- Stop: the device is then set back into Standby mode by the Stop condition.

5.11 Diagrams

Figure 5-1. Typical System Bus Configuration

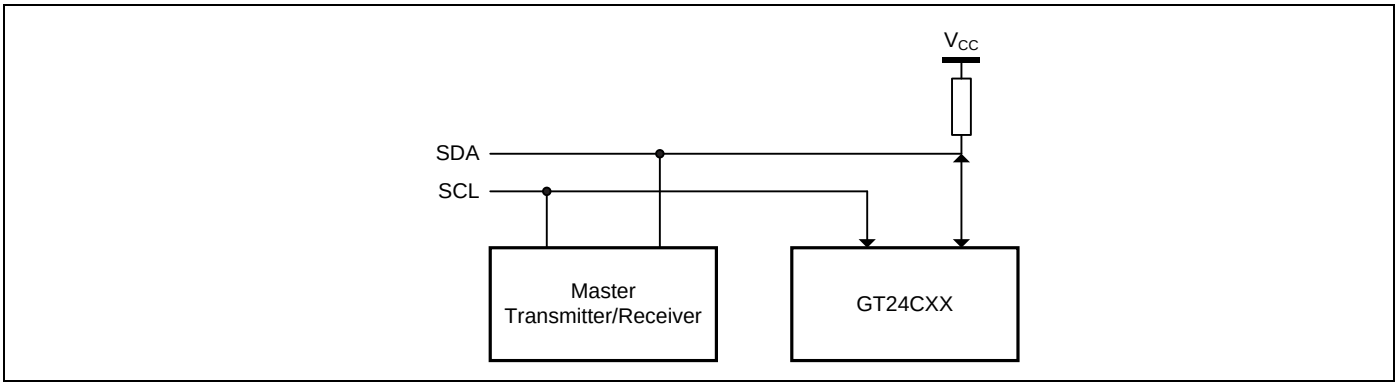


Figure 5-2. output Acknowledge

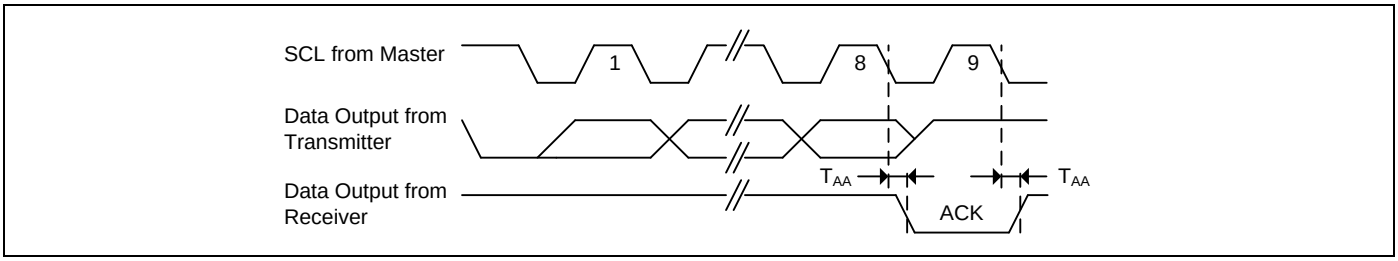


Figure 5-3. Start and Stop Conditions

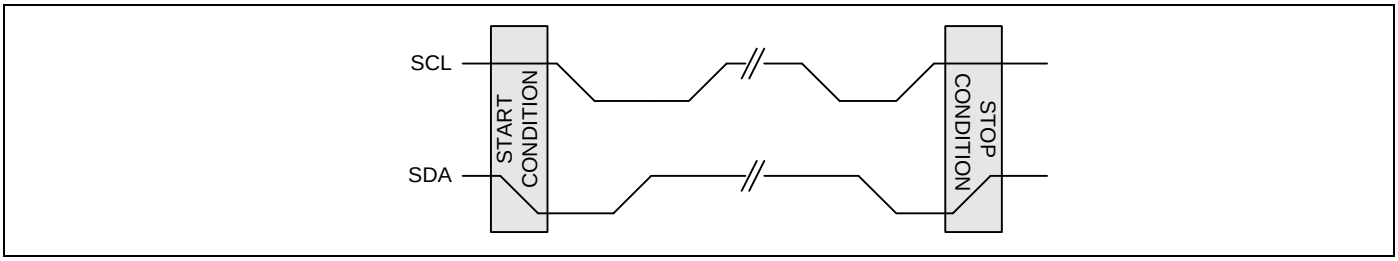


Figure 5-4. Data Validity Protocol

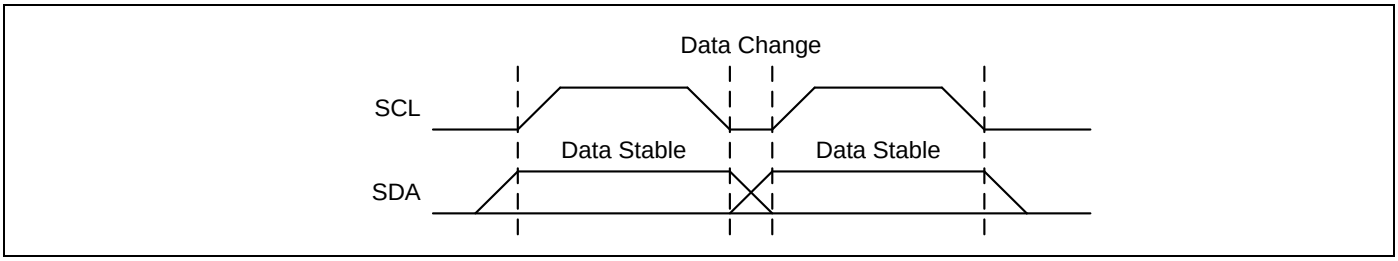


Figure 5-5. Slave Address

Bit	7	6	5	4	3	2	1	0
	1	0	1	0	A2	A1	A0	R/$\overline{W}$

Figure 5-6. Byte Write

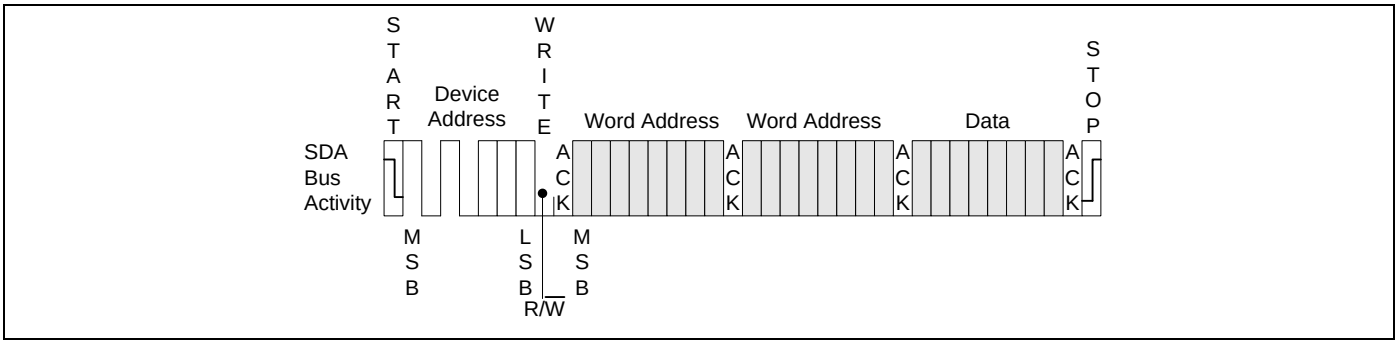


Figure 5-7. Page Write

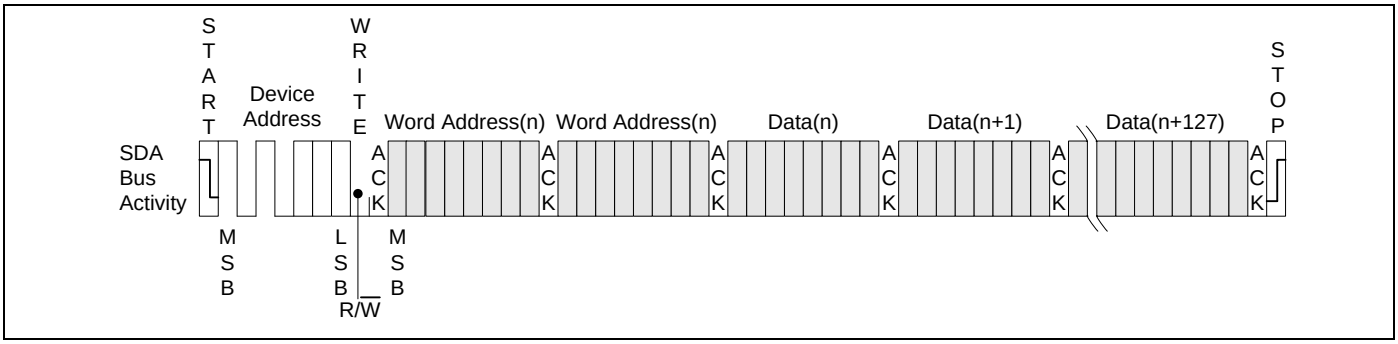


Figure 5-8. Current Address Read

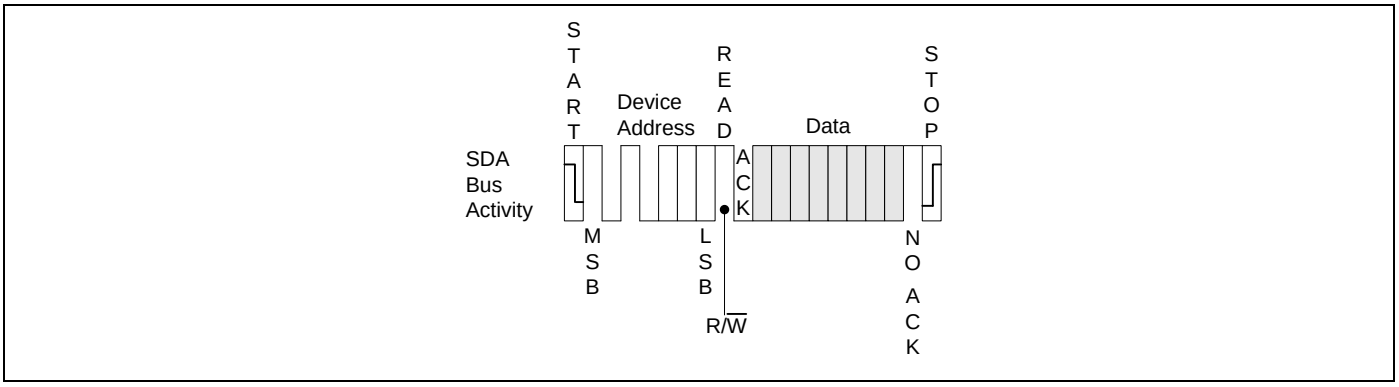


Figure 5-9. Random Address Read

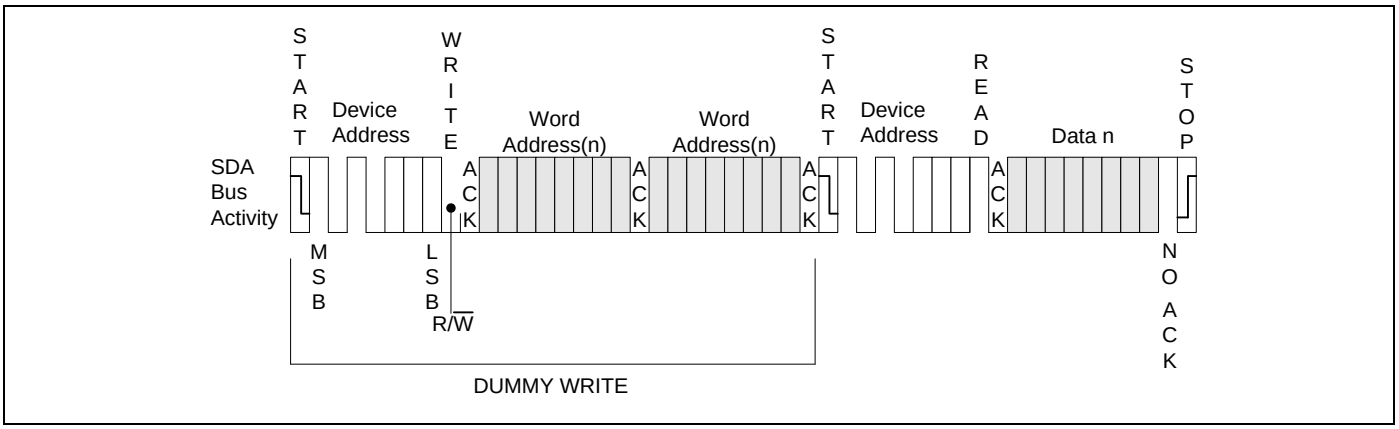
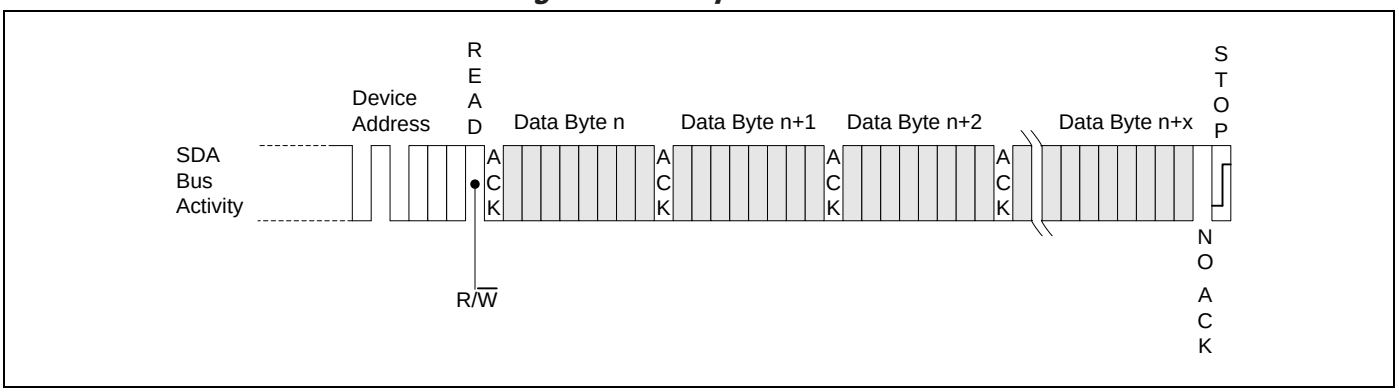


Figure 5-10. Sequential Read



5.12 Timing Diagrams

Figure 5-11. Bus Timing

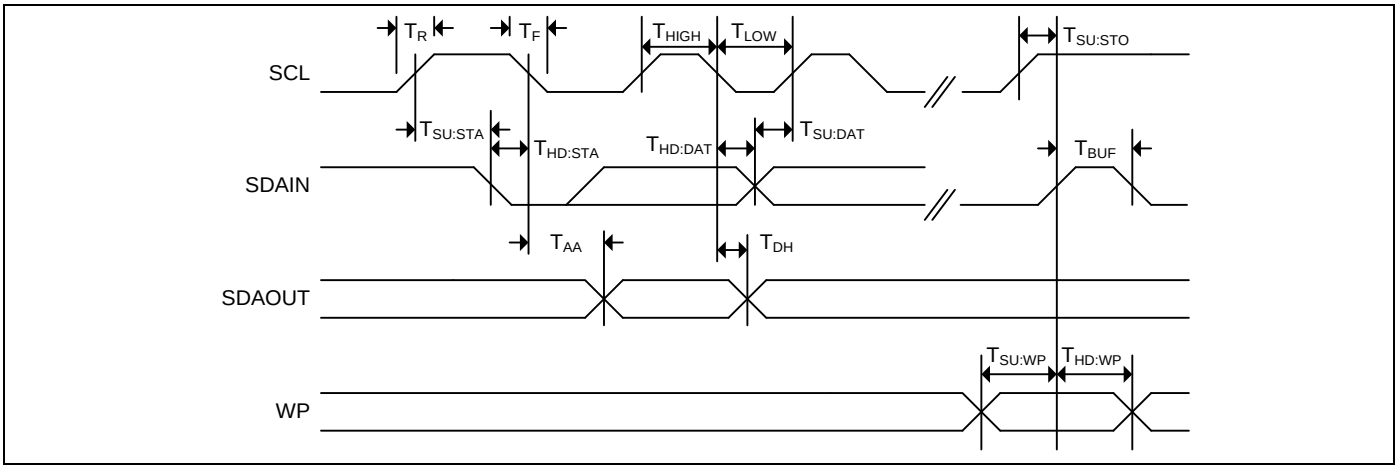
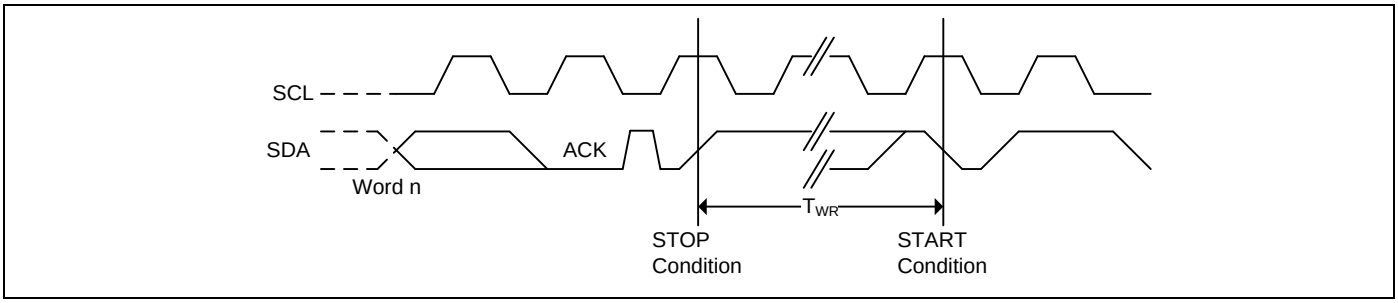


Figure 5-12. Write Cycle Timing



6. RF Communication Interface

The GT24CN512A consists of the 168 bytes of the total EEPROM memory organized in 42 pages each 4 bytes. 144 bytes (36 pages) are available for the user defined data. Along with the memory, GT24CN512A contains the RF-Interface and the Digital Control Unit. Energy and data are transferred via an antenna, which consists of a coil with a few turns directly connected to the LA and LB of the GT24CN512A. No further external components are needed.

6.1 Logical states and State Diagram

Commands are initiated by the NFC device and controlled by the GT24CN512A command interpreter. This processes the internal states and generates the appropriate response. Refer to Figure 6.15.

6.1.1 Idle state

After a Power-On Reset (POR), the GT24CN512A switches directly to the idle state. It only exits this state when a REQA or a WUPA command is received from the NFC device. Any other data received while in the idle state is interpreted as an error and the GT24CN512A remains Idle. After a correctly executed HALT command, the halt state changes to the wait state which can be exited with a WUPA command.

6.1.2 Ready1 state

In this state, the GT24CN512A supports the NFC device when resolving the first part of its UID (3 bytes) with the ANTICOLLISION or SELECT command from cascade level 1. This state is exited correctly after execution of either of the following commands:

- SELECT command from cascade level 1: the NFC device switches GT24CN512A into Ready2 state where the second part of the UID is resolved.
- READ command (from address 0): all anti-collision mechanisms are bypassed and GT24CN512A switches directly to the active state.

Note: If more than one GT24CN512A is in the NFC device field, a READ command from address 0 causes a collision due to the different serial numbers and all GT24CN512A devices are selected. Any other data received in the Ready 1 state is interpreted as an error and depending on its previous state the GT24CN512A returns to the wait, idle or halt state.

6.1.3 Ready2 state

In this state, the GT24CN512A supports the NFC device when resolving the second part of its UID (4 bytes) with the cascade level 2 ANTICOLLISION command. This state is usually exited using the cascade level 2 Select command. Alternatively, state Ready2 may be skipped using a READ command (from address 0) as described in state Ready1.

Note: If more than one GT24CN512A is in the NFC device field, a READ command from address 0 causes a collision due to the different serial numbers and all GT24CN512A devices are selected. The response of the GT24CN512A to the cascade level 2 SELECT command is the Select Acknowledge (SAK) byte. In accordance with ISO/IEC 14443 this byte indicates if the anti-collision cascade procedure has finished. The GT24CN512A is now uniquely selected and only this device will communicate with the NFC device even when other contactless devices are present in the NFC device field. Any other data received when the device is in this state is interpreted as an error and depending on its previous state the GT24CN512A returns to the wait, idle or halt state.

6.1.4 Active state

In the active state either a 16-byte READ or 4-byte WRITE command can be performed. The HALT command exits either the READ or WRITE commands in their active state. Any other data received when the device is in this state is interpreted as an error and depending on its previous state the GT24CN512A returns to the wait, idle or halt state.

6.1.5 Halt state

The halt and idle states constitute the second wait state implemented in the GT24CN512A. An already processed GT24CN512A can be set into the halt state using the HALT command. In the anti-collision phase, this state helps the NFC device to distinguish between processed tags and tags yet to be selected. The GT24CN512A can only exit this state on execution of the WUPA command. Any other data received when the device is in this state is interpreted as an error and the GT24CN512A state is unchanged. Refer to the document MIFARE collection of currently available application notes for correct implementation of an anti-collision procedure based on the idle and halt states

and the REQA and WUPA commands.

6.2 Data integrity

The following mechanisms are implemented in the contactless communication link between NFC device and GT24CN512A to ensure a reliable data transmission:

- 16 bits CRC per block
- Parity bit for each byte
- Bit count checking
- Bit coding to distinguish between "1", "0", and no information
- Channel monitoring (protocol sequence and bit stream analysis)

6.3 RF interface

The RF-interface is according to the standard for contactless smart cards ISO/IEC 14443A.

The RF-field from the NFC device is always present (with short modulation pulses when transmitting data), because it is used for the power supply of the tag. For both directions of data communication there is one start bit at the beginning of each frame. Each byte is transmitted with a parity bit (odd parity) at the end. The LS Bit of the byte with the lowest address of the selected block is transmitted first. The maximum frame length is 164 bits (16 data bytes + 2 CRC bytes = 16 * 9 + 2 * 9 + 1 start bit + 1 end bit).

6.4 Memory organization

The 168 bytes of the total EEPROM memory are organized in 42 pages each 4 bytes. 144 bytes (36 pages) are available for the user defined data. Each page contains 4 bytes (32 bits).

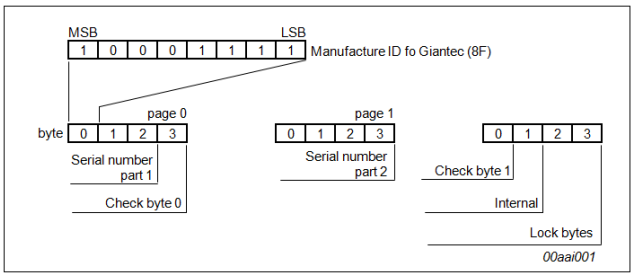
Table 6.1 Memory organization

Page Address		Byte Number			
Decim	Hex	0	1	2	3
0	00h	Serial Number			
1	01h	Serial Number			
2	02h	Serial Number	Internal	Lock byte0	Lock byte1
3	03h	Capability Containner(CC)			
4 to 39	04h to 27h	User Memory	User Memory		User Memory
40	28h	Lock byte2	Lock byte3		
41	29h	16-bit counter	16-bit counter		

6.4.1 UID/serial number

The unique 7 byte serial number (UID) and its two Block Check Character Bytes (BCC) are programmed into the first 9 bytes of the memory. It therefore covers page 00h, page 01h and the first byte of page 02h. The second byte of page 02h is reserved for internal data. Due to security and system requirements these bytes are write-protected after the programming during the IC production.

Figure 6.1 UID/ Serial Number



According to ISO/IEC 14443-3 BCC0 is defined as CT SN0 SN1 SN2.

Abbreviations CT stays for Cascade Tag byte (88h) and BCC1 is defined as SN3 SN4 SN5 SN6.

SN0 holds the Manufacturer ID for Giantec (8Fh) according to ISO/IEC 14443-3 and ISO/IEC 7816-6 AMD.1.

6.4.2 Lock bytes

Lock bytes enable the user to lock parts of the complete memory area for writing. A Read from user memory area cannot be restricted via lock bytes functionality. The lock bytes functionality is enabled with a WRITE command (see Section 6.8.7 “WRITE”) or COMPATIBILITY WRITE command (see Section 6.8.8 “COMPATIBILITY WRITE”), where 2 out of 4 bytes transmitted are used for setting the lock bytes. Two corresponding bytes - either bytes 2 and 3 for page 02h or bytes 0 and 1 for page 28h - and the actual content of the lock bytes are bit-wise “OR-ed”. The result of OR operation becomes the new content of the lock bytes. Two unused bytes do not have to be considered. Although included in the COMPATIBILITY WRITE or WRITE command, they are ignored when programming the memory.

Table 6.2 Lock byte

Name	Page		Function
	Number	Address	
Lock byte 0	2	02h	page and block locking
Lock byte 1	2	02h	page locking
Lock byte 2	40	28h	page and block locking
Lock byte 3	40	28h	functionality and block locking

Due to the built-in bitwise OR operation, this process is irreversible. If a bit is set to “1”, it cannot be changed back to “0” again. Therefore, before locking the lock bytes, the user must ensure that the corresponding user memory area and/or configuration bytes are correctly written. The configuration written in the lock bytes is active upon the next REQA or WUPA command.

The single bits of the 4 bytes available for locking incorporate 3 different functions:

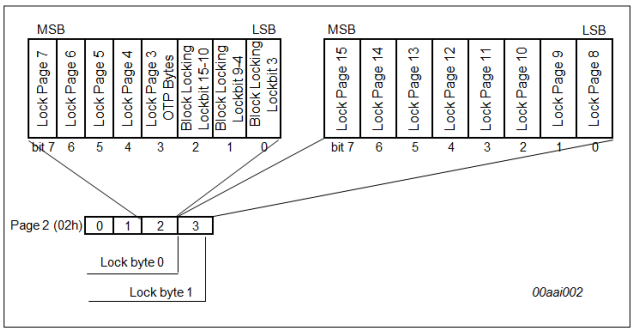
- •the read-only locking of the single pages or blocks of the user memory area
- the read-only locking of the single bytes of the configuration memory area
- the locking of the lock bits themselves

The mapping of single bits to memory area for the first 64 bytes (512 bits) is shown in Figure 6.2.

The bits of byte 2 and 3 of page 02h represent the field-programmable read-only locking mechanism. Each page from 03h (OTP bits) to 0Fh may be locked individually to prevent further write access by setting the corresponding locking bit Lx to 1. After locking the page is read-only memory.

The 3 least significant bits of lock byte 0 of page 2 are the block-locking bits. Bit 2 handles pages 0Fh to 0Ah, bit 1 pages 09h to 04h and bit 0 page 03h (OTP bits). Once the block locking bits are set, the locking configuration for the corresponding memory area is frozen.

Figure 6.2 Lock Byte 0 and 1

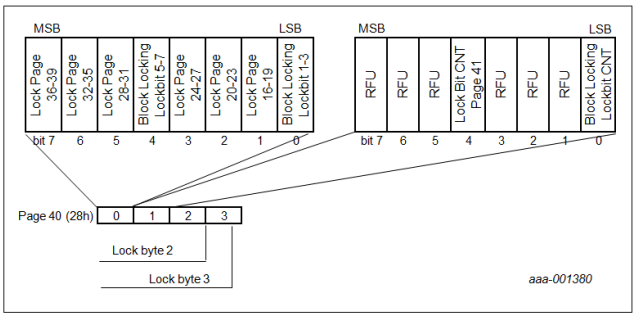


For locking of pages starting at page address 10h onwards, lock bytes located in page 28h are used. Those two lock bytes cover the memory area of 96 data bytes together with configuration area from page address 28h onwards. Therefore, the granularity is larger then for the first 64 bytes as shown in Figure 6.3 “Lock bytes 2 and 3”.

The functionality beyond page address 28h which can be locked read-only is:

- the counter
- the lock bytes themselves

Figure 6.3 Lock Byte 2 and 3

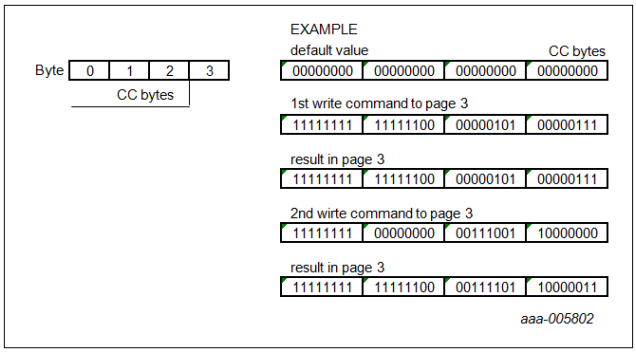


6.4.3 Capability Container (CC)

The Capability Container CC (page 3) is programmed during the IC production according to the NFC Forum Type 2 Tag specification. These bytes may be bit-wise modified by a WRITE command.

The bytes of the WRITE command and the current contents of the CC bytes are bit-wise “OR-ed” and the result becomes the new content of the CC bytes. This process is irreversible. If a bit is set to “1”, it cannot be changed back to “0” again.

Figure 6.4 CC Byte



Note: This memory area may be used as a 32 ticks one-time counter.

6.4.4 Data pages

GT24CN512A features 144 bytes of data memory. The address range from page 04h to 27h constitutes the read/write area. Initial state of each byte in the user area is

00h. A write access to data memory is achieved with WRITE (see Section 6.8.7 “WRITE”) or COMPATIBILITY WRITE (see 6.8.8 “COMPATIBILITY WRITE”) command. In both cases, 4 bytes of memory (one page) will be overwritten. Write access to data memory can be permanently restricted via lock bytes (see 6.4.2 “Lock bytes”).

NFC Forum Type 2 Tag compliance

GT24CN512A has been designed to be compliant with NFC Forum Type 2 Tag specification. With its 144 bytes of data memory, it can easily support use cases like connection handover, Bluetooth simple pairing, Wi-Fi Protected set-up, device authentication, gaming and others.

6.4.5 Initial memory configuration

The memory configuration of GT24CN512A in delivery state is shown in Table 6.3 “Initial memory organization”:

The memory configuration in pages 3 to 5 ensures that GT24CN512A is a NFC forum Type 2 Tag in INITIALIZED state according to the NFC Forum Technical Specification, NFC Forum Tag 2 Type Operation, and Technical Specification. It is recommended that any further modification of the memory pages 2 to 40 should be according to the NFC Forum Tag 2 Type Operation and Technical Specification. All lock bytes are set to zero meaning that no page or functionality is locked. Counter is set to zero. Refer to Table 6.3

Table 6.3 Initial Memory Organization

Page Address		Byte Number			
Dec.	Hex	0	1	2	3
0	00h	UID0	UID1	UID2	BCC0
1	01h	UID3	UID4	UID5	UID6
2	02h	BCC1	Internal	00h	00h
3	03h	E1h	10h	12h	00h
4	04h	01h	03h	A0h	10h
5	05h	44h	03h	00h	Feh
6 to 39	06h to	00h	00h	00h	00h
40	28h	00h	00h	RFU	RFU
41	29h	00h	00h	RFU	RFU

6.5 Counter

GT24CN512A features 16-bit one-way counter, located at first two bytes of page 29h. In its delivery state, counter value is set to 0000h. The first valid Write or Compatibility write to the address 29h can be performed with any value in the range between 0001h and FFFFh and corresponds to initial counter value. Every consequent valid WRITE command, which represents the increment, can contain values between 0001h and 000Fh. Upon such WRITE command and following mandatory RF reset, the value written to the address 29h is added to the counter content.

If - after initial write - a value higher than 000Fh is used as a parameter, GT24CN512A will answer with NAK. Once counter value reaches FFFFh and an increment is performed via valid command, GT24CN512A will answer with NAK. If the sum of counter value and increment is higher than FFFFh, GT24CN512A will answer with NAK and will not update the counter. Increment by zero (00h) is always possible, but does not have any impact to counter value.

6.6 Tag response

NFC Tag Type 2 compliant IC uses, apart from the responses defined in the following sections, two half-byte answers to acknowledge the command received in Active state (see Figure 6.15 “Communication principle state diagram - 4-byte; 16-byte”). NFC Tag Type 2 compliant IC distinguishes between positive (ACK) and negative (NAK) acknowledge. Valid values for ACK and NAK are shown in Table 6.4 “ACK and NAK values”. After every NAK, GT24CN512A will perform an internal reset.

Table 6.4 ACK and NAK values

Answer value	Answer explanation
Ah	positive acknowledge (ACK)
1h	parity or CRC error (NAK)
0h	any other error (NAK)

6.7 NFC Forum Device timings requirements

For all READ (Section 6.8.5) and WRITE (Section 6.8.7) timings for the NFC device see section 7.4.

6.8 Command set

The ATQA and SAK are identical as for MIFARE Ultralight (see MF0ICU1 Functional specification MIFARE Ultralight). For information on ISO 14443 card activation, see AN10834 MIFARE ISO/IEC 14443 PICC Selection. Summary of data

relevant for device identification is given in Section 6.9 “Summary of relevant data for device identification”. GT24CN512A comprises the command set as described in following chapters.

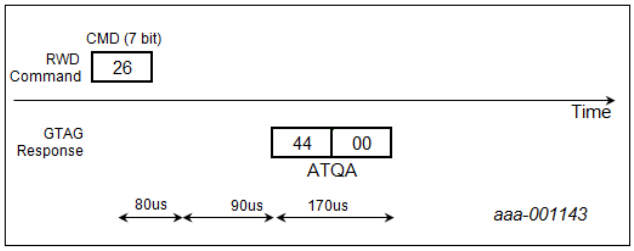
6.8.1 REQA

Table 6.5 READ

Code	Parameter	Data	Integrity Mechanism	Response
26h (7-bit)	-	-	Parity	0044h

Description: The GT24CN512A accepts the REQA command in Idle state only. The response is the 2-byte ATQA (0044h). REQA and ATQA are implemented fully according to ISO/IEC 14443-3.

Figure 6.5 REQA



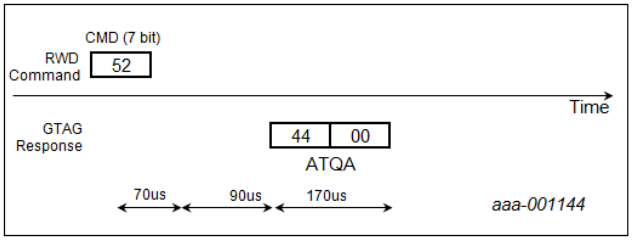
6.8.2 WUPA

Table 6.6 WUPA

Code	Parameter	Data	Integrity Mechanism	Response
52h (7-bit)	-	-	Parity	0044h

Description: GT24CN512A accepts the WUPA command in the Idle and Halt state only. The response is the 2-byte ATQA (0044h). WUPA is implemented fully according to ISO/IEC 14443-3.

Figure 6.6 WUPA



6.8.3 ANTICOLLISION and SELECT of cascade level 1

Table 6.7 ANTICOLLISION and SELECT of cascade level 1

Code	Parameter	Data	Integrity Mechanism	Response
Anticollision: 93h	20h	-	Parity, BCC	-
Anticollision: 93h	21h to 67h	Part of the UID	Parity, BCC	Part of the UID
Select: 93h	70h	First 3 bytes of UID	Parity, BCC, CRC	SAK ('04')

Description: The ANTICOLLISION and SELECT commands are based on the same command code. They differ only in the Parameter byte. This byte is per definition 70h in case of SELECT. GT24CN512A accepts these commands in the Ready1 state only. The response is part 1 of the UID. Even with incorrect CRC value, the SELECT command will be fully functional.

Figure 6.7 Anticollision of cascade level 1

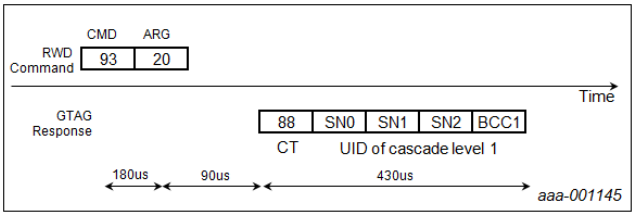
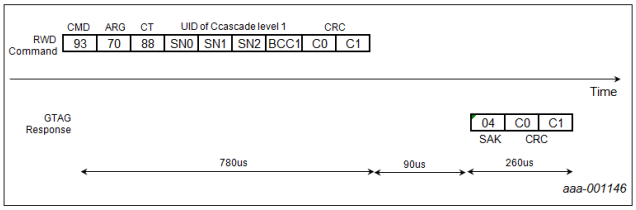


Figure 6.8 Select of cascade level 1



6.8.4 ANTICOLLISION and SELECT of cascade level 2

Table 6.8 ANTICOLLISION and SELECT of cascade level 2

Code	Parameter	Data	Integrity Mechanism	Response
Anticollision: 95h	20h	-	Parity, BCC	-
Anticollision: 95h	21h to 67h	Part of the UID	Parity, BCC	Part of the UID
Select: 95h	70h	Second 4 bytes of UID	Parity, BCC, CRC	SAK ('00')

Description: The ANTICOLLISION and SELECT commands are based on the same command code. They differ only in the parameter byte. This byte is per definition 70h in case of SELECT. GT24CN512A accepts these commands in the Ready2 state only. The response is part 2 of the UID. Even with incorrect CRC value, the SELECT command will be fully functional.

Figure 6.9 Anticollision of cascade level 2

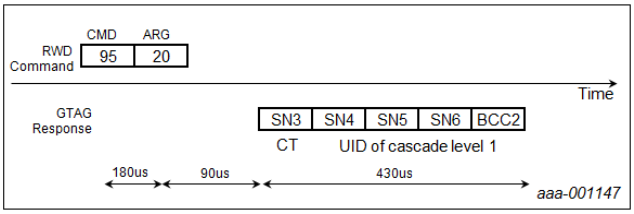
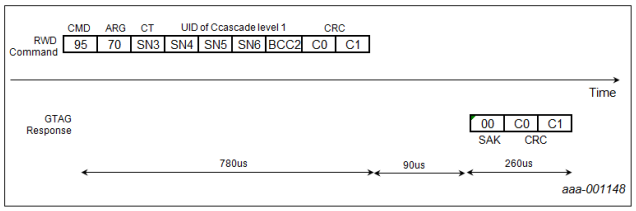


Figure 6.10 Select of cascade level 2



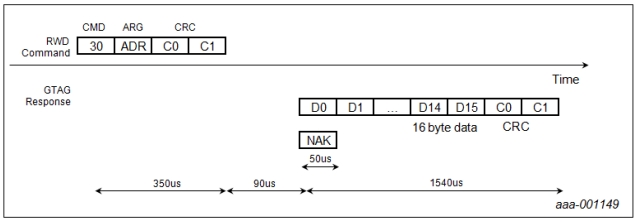
6.8.5 READ

Table 6.9 READ

Code	Parameter	Data	Integrity Mechanism	Response
30h	ADR: '00h' to '29h'	-	Parity, CRC	16 Byte Date

Description: The READ command needs the page address as a parameter. Only addresses 00h to 29h are decoded. For higher addresses, GT24CN512A returns a ACK. The GT24CN512A responds to the READ command by sending 16 bytes starting from the page address defined in the command (e.g. if ADR is '03h' pages 03h, 04h, 05h, 06h are returned. If ADR is '29h', the contents of pages 29h, 00h, 01h and 02h is returned).

Figure 6.11 READ



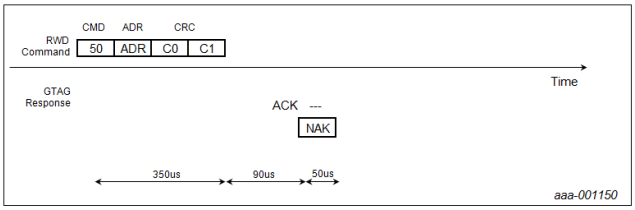
6.8.6 HALT

Table 6.10 HALT

Code	Parameter	Data	Integrity Mechanism	Response
50h	00h	-	Parity, CRC	Passive ACK, NAK

Description: The HALT command is used to set already processed GT24CN512A devices into a different waiting state (Halt instead of Idle), which allows a simple separation between devices whose UIDs are already known (as they have already passed the anticollision procedure) and devices that have not yet been identified by their UIDs. This mechanism is a very efficient way of finding all contactless devices in the field of a NFC device. Even with incorrect parity value, the HALT command will be fully functional.

Figure 6.12 HALT



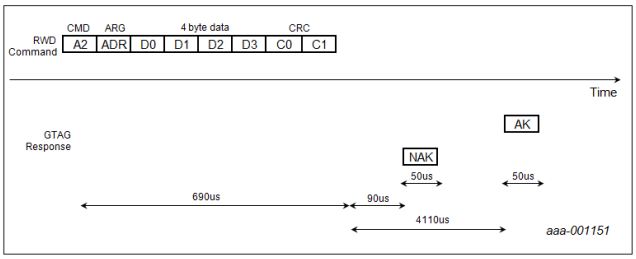
6.8.7 WRITE

Table 6.11 WRITE

Code	Parameter	Data	Integrity Mechanism	Response
A2h	ADR: '02h' to '29h'	4 Byte	Parity, CRC	ACK or NAK

Description: The WRITE command is used to program the lock bytes in page 02h, the CC bytes in page 03h or the data bytes in pages 04h to 05h. A WRITE command is performed page-wise, programming 4 bytes in a page.

Figure 6.13 WRITE



6.8.8 COMPATIBILITY WRITE

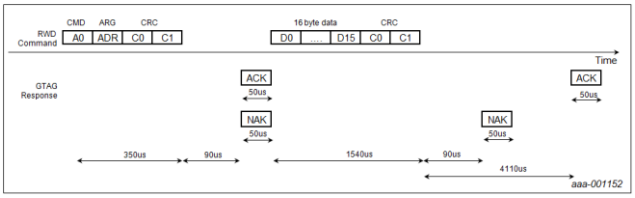
Table 6.12 COMPATIBILITY WRITE

Code	Parameter	Data	Integrity Mechanism	Response
A0h	ADR: '02h' to '29h'	16 Byte	Parity, CRC	ACK or NAK

Description: The COMPATIBILITY WRITE command was implemented to accommodate the established NFC device infrastructure. Even though 16 bytes are transferred to the GT24CN512A, only the least significant 4 bytes (bytes D0

to D3) will be written to the specified address. It is recommended to set the remaining bytes D4 to D15 to '0'.

Figure 6.14 COMPATIBILITY WRITE



Notes: The timings in Figure are typical timings. The NFC forum device must respect the following minimum timings and maximum timeouts.

Table 6.13 COMPATIBILITY WRITE timing

	T_{ACK} Min	T_{ACK} Max	T_{NAK} Min	T_{NAK} Max	$T_{TimeOut}$
COMPATIBILITY_WRITE 1st ACK/NAK	71us	$T_{TimeOut}$	71us	$T_{TimeOut}$	5ms
COMPATIBILITY_WRITE 2nd ACK/NAK	71us	$T_{TimeOut}$	71us	$T_{TimeOut}$	10ms

6.9 Summary of relevant data for device identification

Table 6.14 Summary of relevant data for device identification

Code	Type	Value	Binary Format	Remark
ATQA	2 Byte	0044h	0000 0000 000 0100 1st '1' indicateds cascade level 2 2nd '1' indicates family	OK
CT	1 Byte Cascade Tag	88h	1000 1000 ensures collision with cascade level 1 products	Hard Coded
SAK(casc. Level 1)	1 Byte	04h	0000 0100 '1' indicates additional cascade level	OK
SAK(casc. Level 2)	1 Byte	00h	0000 0000 indicates complete UID and GTAG functionality	OK
Manufacturer Byte	1 Byte	8fh	0000 0100 indicates manufacturer Giantec	Acc. To ISO/IEC 14443-3 and ISO/IEC 7816-6 AMD.1

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to + 6.5	V
V_P	Voltage on Any Pin	–0.5 to V_{CC} + 0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

7.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	–40°C to +85°C	1.7V to 5.5V

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

7.3 Capacitance

Symbol	Parameter[1, 2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input / Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
[2] Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

7.4 DC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, V_{CC} = 1.7V ~ 5.5V

Symbol	Parameter[1]	Vcc	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage			1.7		5.5	V
V_{IH}	Input High Voltage			0.7*V_{CC}		V_{CC}+1	V
V_{IL}	Input Low Voltage			-1		0.3* V_{CC}	V
I_{LI}	Input Leakage Current	5 V	V_{IN} = V_{CC} max	--		2	µA
I_{LO}	Output Leakage Current	5V		--		2	µA
V_{OL1}	Output Low Voltage	1.7V	I_{OL} = 0.15 mA	—		0.2	V
V_{OL2}	Output Low Voltage	3V	I_{OL} = 2.1 mA	—		0.4	V
I_{SB1}	Standby Current	1.7V	V_{IN} = V_{CC} or GND	—	0.2	1	µA
I_{SB2}	Standby Current	2.5V	V_{IN} = V_{CC} or GND	—	0.3	1	µA
I_{SB3}	Standby Current	5V	V_{IN} = V_{CC} or GND	—	0.5	1	µA
I_{CC1}	Read Current	1.7V	Read at 400 KHz	—		0.15	mA
		2.5V	Read at 1 MHz			0.2	mA
		5.5V	Read at 1 MHz			0.5	mA
I_{CC2}	Write Current	1.7V	Write at 400 KHz	—		0.5	mA
		2.5V	Write at 1 MHz			0.6	mA
		5.5V	Write at 1 MHz			1	mA

Note: The parameters are characterized but not 100% tested.

7.5 AC Electrical Characteristic

Industrial: T_A = –40°C to +85°C, Supply voltage = 1.7V to 5.5V

Symbol	Parameter [1] [2]	1.7V≤Vcc<2.5V		2.5V≤Vcc<4.5V		4.5V≤Vcc≤5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{SCL}	SCK Clock Frequency		400		1000		1000	KHz
T_{LOW}	Clock Low Period	1200	—	400	—	400	—	ns
T_{HIGH}	Clock High Period	600	—	400	—	400	—	ns
T_R	Rise Time (SCL and SDA)	—	300	—	300	—	300	ns
T_F	Fall Time (SCL and SDA)	—	300	—	100	—	100	ns
$T_{SU:STA}$	Start Condition Setup Time	600	—	200	—	200	—	ns
$T_{SU:STO}$	Stop Condition Setup Time	600	—	200	—	200	—	ns
$T_{HD:STA}$	Start Condition Hold Time	600	—	200	—	200	—	ns
$T_{SU:DAT}$	Data In Setup Time	100	—	40	—	40	—	ns
$T_{HD:DAT}$	Data In Hold Time	0	—	0	—	0	—	ns
T_{AA}	Clock to Output Access time (SCL Low to SDA Data Out Valid)	100	900	50	400	50	400	ns
T_{DH}	Data Out Hold Time (SCL Low to SDA Data Out Change)	100	—	50	—	50	—	ns
T_{WR}	Write Cycle Time	—	5	—	5	—	5	ms
T_{BUF}	Bus Free Time Before New Transmission	1000	—	400	—	400	—	ns
$T_{SU:WP}$	WP pin Setup Time	600	—	400	—	400		ns
$T_{HD:WP}$	WP pin Hold Time	1200	—	1200	—	1200	—	ns
T	Noise Suppression Time	—	100	—	50	—	50	ns

Notes: [1] The parameters are characterized but not 100% tested.

[2] AC measurement conditions:

R_L (connects to V_{CC}): 1.3 kΩ (2.5V, 5.0V), 10 kΩ (1.7V)

C_L = 100 pF

Input pulse voltages: 0.3*V_{CC} to 0.7*V_{CC}

Input rise and fall times: ≤ 50 ns

Timing reference voltages: half V_{CC} level

8. Ordering Information

Industrial Grade: -40°C to +85°C, Lead-free

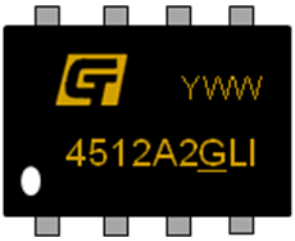
Voltage Range	Part Number*	Package (8-pin)*
1.7V to 5.5V	GT24CN512A-2GLI-TR	150-mil SOIC
	GT24CN512A-2ZLI-TR	3 x 4.4 mm TSSOP
	GT24CN512A-2UDLI-TR	2 x 3 x 0.55 mm UDFN
	GT24CN512A-2CLI-TR	CSP

*

1. Contact Giantec Sales Representatives for availability and other package information.
2. The product is packed in tape and reel “-TR” (4K per reel), except UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

98. Top Markings

9.1 SOIC Package



G: Giantec Logo

4512A2GLI: GT24CN512A-2GLI-TR

YWW: Date Code, Y=year, WW=week

9.2 TSSOP Package

GT: Giantec Logo

4512A2ZLI: GT24CN512A-2ZLI-TR

YWW: Date Code, Y=year, WW=week

9.3 UDFN Package

GT: Giantec Logo

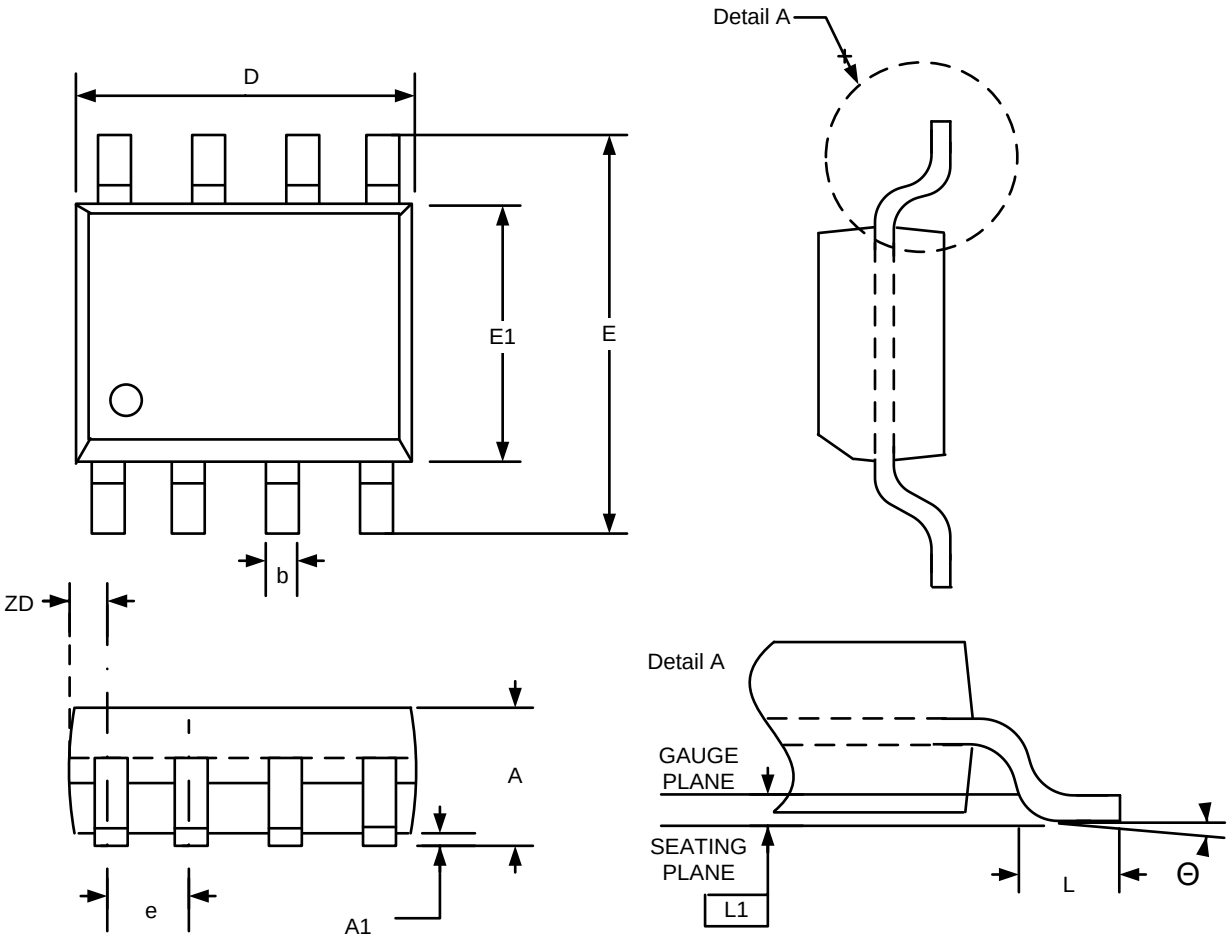
49A: GT24CN512A-2UDLI-TR

YWW: Date Code, Y=year, WW=week

10. Package Information

10.1 SOIC

8L 150mil SOIC Package Outline

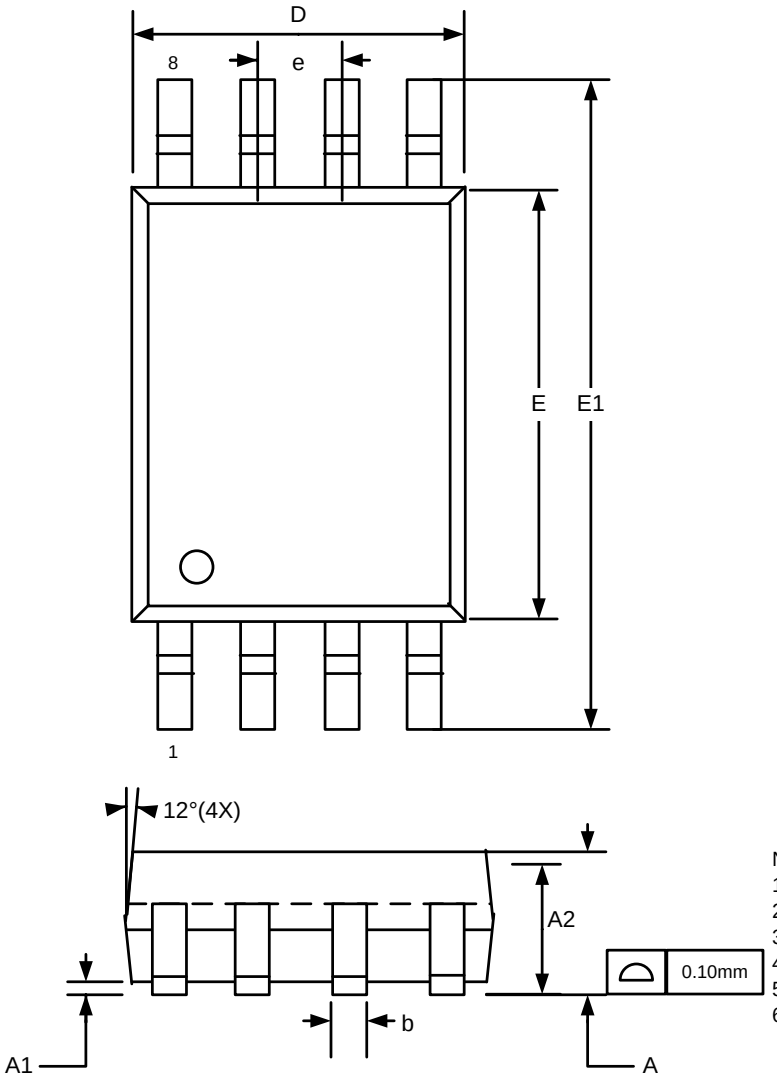


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

10.2 TSSOP

8L 3x4.4mm TSSOP Package Outline

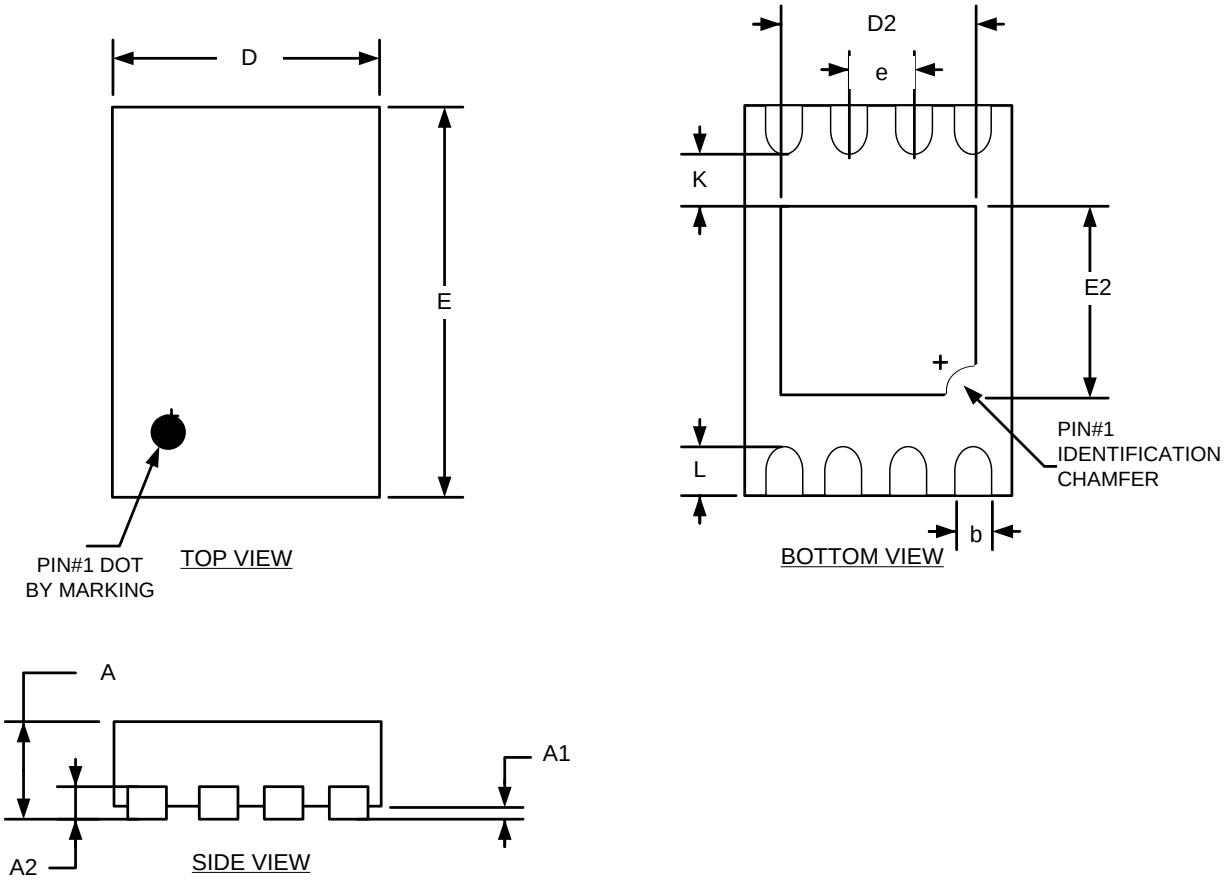


Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.4 BSC			0.252 BSC		
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

10.3 UDFN

8L 2x3mm UDFN Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

11. Revision History

Revision	Date	Descriptions
C0	Feb. 2014	Initial version