1.8 Volt Intel® Wireless Flash Memory (W18)

28F320W18, 28F640W18, 28F128W18

Preliminary Datasheet

Product Features

- **Performance**
  - 70 ns Asynchronous reads for 32 and 64 Mbit, 90 ns for 128 Mbit
  - 14 ns Clock to Data Output (t_{CHQV})
  - 20 ns Page Mode Read Speed
  - 4-Word, 8-Word, and Continuous-Word Burst Modes
  - Burst and Page Modes in Parameter and Main Partitions
  - Programmable WAIT Configuration
  - Enhanced Factory Programming Mode@ 3.50 µs/Word (Typ)
  - Glueless 12 V interface for Fast Factory Programming @ 8 µs/Word (Typ)
  - 1.8 V Low-Power Programming @ 12 µs/Word (Typ)
  - Program or Erase during Reads
- **Architecture**
  - Multiple 4-Mbit Partitions
  - Dual-Operation: Read-While-Write or Read-While-Erase
  - Eight, 4-Kword Parameter Code and Data Blocks
  - 32-Kword Main Code and Data Blocks
  - Top and Bottom Parameter Configurations
- **Power Operation**
  - 1.7 V to 1.95 V Read and Write Operations
  - 1.7 V to 2.24 V V_{CCQ} for I/O Isolation
  - Standby Current: 5 µA (Typ)
  - Read Current: 7 mA (Typ)
- **Software**
  - 5 µs (Typ) Program Suspend
  - 5 µs (Typ) Erase Suspend
  - Intel® Flash Data Integrator (FDI) Software Optimized
  - Intel Basic Command Set Compatible
  - Common Flash Interface (CFI)
- **Quality and Reliability**
  - Extended Temperature: –40 °C to +85 °C
  - Minimum 100,000 Erase Cycles per Block
  - ETOX™ VII Flash Technology (0.18 µm)
- **Security**
  - 128-bit Protection Register: 64 Unique Device Identifier Bits; 64 User-Programmable OTP Bits
  - Absolute Write Protection ⇒V_{PP} = GND
  - Erase/Program Lockout during Power Transitions
  - Individual Dynamic Zero-Latency Block Locking
  - Individual Block Lock-Down
- **Density and Packaging**
  - 32 Mbit and 128 Mbit in a VF BGA Package
  - 64 Mbit in a µBGA*Package
  - 56 Active Ball Matrix, 0.75 mm Ball-Pitch µBGA* and VF BGA Packages
  - 16-bit wide Data Bus

The 1.8 Volt Intel® Wireless Flash memory with flexible multi-partition dual-operation provides high-performance asynchronous and synchronous burst reads. It is an ideal memory for low-voltage burst CPUs. Combining high read performance with flash memory's intrinsic non-volatility, 1.8 Volt Intel Wireless Flash memory eliminates the traditional system-performance paradigm of shadowing redundant code memory from slow nonvolatile storage to faster execution memory. It reduces the total memory requirement that increases reliability and reduces overall system power consumption and cost.

The 1.8 Volt Intel Wireless Flash memory's flexible multi-partition architecture allows programming or erasing to occur in one partition while reading from another partition. This allows for higher data write throughput compared to single partition architectures. The dual-operation architecture also allows two processors to interleave code operations while program and erase operations take place in the background. The designer can also choose the size of the code and data partitions via the flexible multi-partition architecture.

The 1.8 Volt Intel Wireless Flash memory is manufactured on Intel's 0.18 µm ETOX™ VII process technology. It is available in µBGA and VF BGA packages which are ideal for board-constrained applications.

Notice: This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

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Revision History

Date of Revision	Version	Description
09/13/00	290701-001	Original Version
01/29/01	290701-002	Deleted 16-Mbit density Revised *ADV#,* Section 2.2 Revised *Protection Registers*, Section 4.16 Revised *Program Protection Register*, Section 4.18 Revised Example in *First Access Latency Count*, Section 5.0.2 Revised Figure 5, *Data Output with LC Setting at Code 3* Added *WAIT Signal Function*, Section 5.0.3 Revised *WAIT Signal Polarity*, Section 5.0.4 Revised *Data Output Configuration*, Section 5.0.5 Added Figure 7, *Data Output Configuration with WAIT Signal Delay* Revised *WAIT Delay Configuration*, Section 5.0.6 Changed V_{CCQ} Spec from 1.7 V – 1.95 V to 1.7 V – 2.24 V in Section 8.2, *Extended Temperature Operation* Changed I_{CCS} Spec from 15 µA to 18 µA in Section 8.4, *DC Characteristics* Changed I_{CCR} Spec from 10 mA (CLK = 40 MHz, burst length = 4) and 13 mA (CLK = 52 MHz, burst length = 4) to 13 mA, and 16 mA respectively in Section 8.4, *DC Characteristics* Changed I_{CCWS} Spec from 15 µA to 18 µA in Section 8.4, *DC Characteristics* Changed I_{CCES} Spec from 15 µA to 18 µA in Section 8.4, *DC Characteristics* Changed t_{CHQX} Spec from 5ns to 3ns in Section 8.6, *AC Read Characteristics* Added Figure 25, WAIT Signal in Synchronous Non-Read Array Operation Waveform Added Figure 26, *WAIT Signal in Asynchronous Page Mode Read Operation Waveform* Added Figure 27, *WAIT Signal in Asynchronous Single Word Read Operation Waveform* Revised Appendix E, *Ordering Information*
06/12/01	290701-003	Revised entire Section 4.10, *Enhanced Factory Program Command (EFP)* and Figure 6, *Enhanced Factory Program Flowchart* Revised Section 4.13, *Protection Register* Revised Section 4.15, *Program Protection Register* Revised Section 7.3, *Capacitance,* to include 128-Mbit specs Revised Section 7.4, *DC Characteristics,* to include 128-Mbit specs Revised Section 7.6, *AC Read Characteristics,* to include 128-Mbit device specifications Added t_{VHGL} Spec in Section 7.6, *AC Read Characteristics* Revised Section 7.7, *AC Write Characteristics*, to include 128-Mbit device specifications Minor text edits

1.0 Introduction

This datasheet contains information about the 1.8 Volt Intel® Wireless Flash memory family. Section 1.0 provides a flash memory overview. Section 2.0 through Section 6.0 describe the memory functionality. Section 7.0 describes the electrical specifications for extended temperature product offerings.

1.1 Document Conventions

Many terms and phrases are used throughout this document as a short-hand version of full, and more accurate verbiage:

- The term “1.8 V” refers to the full VCC voltage range of 1.7 V – 1.95 V (except where noted) and “V_{PP} = 12 V” refers to 12 V ±5%.
- When referring to registers, the term **set** means the bit is a ‘1’, and **clear** means the bit is a ‘0’.
- Even though this product supports multiple package types, the terms **pin** and **signal** are often used interchangeably to refer to the external signal connections on the package. (e.g., *balls* in the case of µBGA*).
- A **word** is 2 bytes, or 16 bits.
- For voltage and ground signals, the signal name is denoted in all CAPS as seen in Section 2.2, “Signal Descriptions” on page 4, whereas the *voltage* applied to the signal uses subscripted notation. For example VPP refers to a signal, while V_{PP} is a voltage level.

Throughout this document, references are made to top, bottom, parameter, and main partitions. To clarify these references, the following conventions have been adopted:

- A **block** is a group of bits (or words) that erase simultaneously with one block erase instruction.
- A **main block** contains 32 Kwords.
- A **parameter block** contains 4 Kwords.
- The **Block Base Address** (BBA) is the first address of a block.
- A **partition** is a group of blocks that share erase and program circuitry and a common status register. If one block is erasing or one word is programming, only the status register, rather than array data, is available when any address within the same partition is read.
- The **Partition Base Address** (PBA) is the first address of a partition. For example, on a 32-Mbit top-parameter device, partition number 5 has a PBA of 140000h.
- The **top partition** is located at the highest physical device address. This partition may be a main partition or a parameter partition.
- The **bottom partition** is located at the lowest physical device address. This partition may be a main partition or a parameter partition.
- A **main partition** contains only main blocks.
- A **parameter partition** contains a mixture of main and parameter blocks.
- A **top parameter device** (**TPD**) has the parameter partition at the top of the memory map with the parameter blocks at the top of that partition. This was formerly referred to as top-boot device.

- A **bottom parameter device** (**BPD**) has the parameter partition at the bottom of the memory map with the parameter blocks at the bottom of that partition. This was formerly referred to as bottom-boot block flash device.

Additionally, many acronyms which describe product features or usage are used throughout the document. They are defined here:

- **EFP**: Enhanced Factory Programming
- **RWW**: Read-While-Write
- **RWE**: Read-While-Erase
- **CFI**: Common Flash Interface
- **CUI**: Command User Interface
- **WSM**: Write State Machine
- **OTP**: One-Time Programmable
- **PBA**: Partition Base Address
- **BBA**: Block Base Address
- **APS**: Automatic Power Savings
- **FDI**: Flash Data Integrator
- **SRD**: Status Register Data

1.2 Product Overview

The 1.8 Volt Intel® Wireless Flash memory provides RWW/RWE capability with high-performance synchronous and asynchronous reads on package-compatible densities with a 16-bit data bus. Individually-erasable memory blocks are optimally sized for code and data storage. Eight 4-Kword parameter blocks are located in the parameter partition at either the top or bottom of the memory map. The rest of the memory array is grouped into 32-Kword main blocks.

The memory architecture for the 1.8 V Intel Wireless Flash memory consists of multiple 4-Mbit partitions, the exact number depending on device density. By dividing the memory array into partitions, program or erase operations can take place simultaneously during read operations. Burst reads can traverse partition boundaries, but user application code is responsible for ensuring that they don’t extend into a partition that is actively programming or erasing. Although each partition has burst-read, write, and erase capabilities, simultaneous operation is limited to write or erase in one partition while other partitions are in a read mode.

Augmented erase suspend functionality further enhances the RWW capabilities of this device. An erase can be suspended to perform a program or read operation within any block, except that which is erase-suspended. A program operation nested within a suspended erase can subsequently be suspended to read yet another memory location.

After device power-up or reset, the 1.8 Volt Intel Wireless Flash memory defaults to asynchronous read configuration. Writing to the device’s configuration register enables synchronous burst-mode read operation. In synchronous mode, the CLK input increments an internal burst address generator. CLK also synchronizes the flash memory with the host CPU and outputs data on every, or on every other, CLK cycle after initial latency. A programmable WAIT output signal provides easy CPU-to-flash memory synchronization.

In addition to its enhanced architecture and interface, the 1.8 Volt Intel Wireless Flash memory incorporates technology that enables fast factory programming and low-power designs. The EFP option renders the fastest available program performance, which can increase a factory's manufacturing throughput.

The device supports read operations at 1.8 V V_{CC} and erase and program operations at 1.8 V or 12 V V_{PP}. With the 1.8 V V_{PP} option, VCC and VPP can be tied together for a simple, ultra-low-power design. In addition to voltage flexibility, the dedicated VPP input provides complete data protection when $V_{PP} \leq V_{PPLK}$.

A 128-bit protection register enhances the user's ability to implement new security techniques and data protection schemes. Unique flash device identification and fraud-, cloning-, or content-protection schemes are possible via a combination of Intel-programmed and user-OTP data cells. Zero-latency locking/unlocking on any memory block provides instant and complete protection for critical system code and data. An additional block lock-down capability provides hardware protection where software commands alone cannot change the block's protection status.

The device's CUI is the system processor's link to internal flash memory operation. A valid command sequence written to the CUI initiates device WSM operation that automatically executes the algorithms, timings, and verifications necessary to manage flash memory program and erase. An internal status register provides ready/busy indication results of the operation (success, fail, etc.).

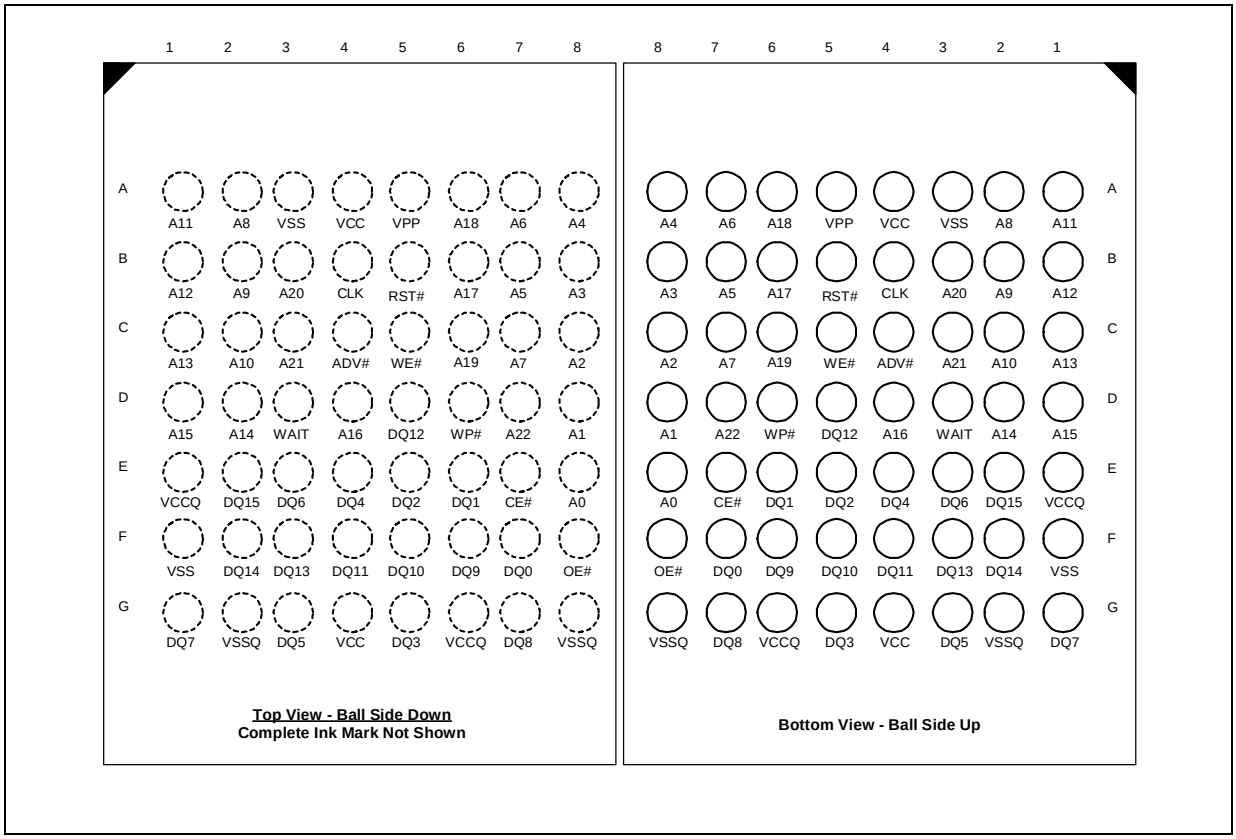
Three power-savings features, APS, standby, and RST#, can significantly reduce power consumption. The device automatically enters APS mode following read cycle completion. Standby mode begins when the system deselects the flash memory by deasserting CE#. Driving RST# low produces power savings similar to standby mode. It also resets the part to read array mode (important for system-level reset), clears internal status registers, and provides an additional level of flash write protection.

2.0 Product Description

2.1 Package and Ballouts

The 1.8 Volt Intel® Wireless Flash memory is available in 56 active ball matrix µBGA* and VF BGA Chip Scale Packages with 0.75 mm ball pitch that is ideal for board-constrained applications. Figure 1, "56 Active Ball Matrix µBGA* and VF BGA Packages" on page 4 shows device ballout.

Figure 1. 56 Active Ball Matrix µBGA* and VF BGA Packages



NOTES:
1. On lower density devices, upper address balls can be treated as NC. (Example: For 32-Mbit density, A[21] and A[22] will be NC).
2. See Appendix C, "Mechanical Specifications" on page 76 for package mechanical specifications.

2.2 Signal Descriptions

Table 1, "Signal Descriptions" on page 5 describes ball usage.

Table 1. Signal Descriptions

Symbol	Type	Name and Function
A[22:0]	I	**ADDRESS INPUTS:** for memory addresses. 32 Mbit: A[20:0]; 64 Mbit: A[21:0]; 128 Mbit: A[22:0]
DQ[15:0]	I/O	**DATA INPUT/OUTPUTS:** Inputs data and commands during write cycles, outputs data during memory, status register, protection register, and configuration code reads. Data pins float when the chip or outputs are deselected. Data is internally latched during writes.
ADV#	I	**ADDRESS VALID:** ADV# indicates valid address presence on address inputs. During synchronous read operations, all addresses are latched on ADV#'s rising edge or CLK's rising (or falling) edge, whichever occurs first.
CE#	I	**CHIP ENABLE:** CE#-low activates internal control logic, I/O buffers, decoders, and sense amps. CE#-high deselects the device, places it in standby state, and places data and WAIT outputs at High-Z.
CLK	I	**CLOCK:** CLK synchronizes the device to the system bus frequency in synchronous-read configuration and increments an internal burst address generator. During synchronous read operations, addresses are latched on ADV#'s rising edge or CLK's rising (or falling) edge, whichever occurs first.
OE#	I	**OUTPUT ENABLE:** Active low OE# enables the device's output data buffers during a read cycle. With OE# at V_{IH}, device data outputs are placed in High-Z state.
RST#	I	**RESET:** When low, RST# resets internal automation and inhibits write operations. This provides data protection during power transitions. RST#-high enables normal operation. Exit from reset places the device in asynchronous read array mode.
WAIT	O	**WAIT:** Indicates data valid in synchronous read modes. Configuration Register bit 10 (CR.10, WT) determines its polarity when set to '1'. With CE# at V_{IL}, WAIT's active output is V_{OL} or V_{OH}. WAIT is High-Z if CE# is V_{IH}. WAIT is not gated by OE#.
WE#	I	**WRITE ENABLE:** WE# controls writes to the CUI and array. Addresses and data are latched on the WE# pulse's rising edge.
WP#	I	**WRITE PROTECT:** Disables/enables the lock-down function. When WP# is a logic low, the lock-down mechanism is enabled and blocks marked lock-down cannot be unlocked through software. See Section 4.12, "Block Locking Commands" on page 27 for details on block locking.
VPP	Pwr/I	**ERASE AND PROGRAM POWER:** A valid V_{PP} voltage on this pin allows erase or programming. Memory contents cannot be altered when $V_{PP} \le V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{CC}$ for in-system program and erase operations. To accommodate resistor or diode drops from the system supply, V_{PP}'s V_{IH} level can be as low as V_{PP1} min. V_{PP} must remain above V_{PP1} min to perform in-system flash modification. VPP may be 0 V during read operations. V_{PP2} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. VPP can be connected to 12 V for a cumulative total not to exceed 80 hours maximum. Extended use of this pin at 12 V may reduce block cycling capability.
VCC	Pwr	**DEVICE POWER SUPPLY:** Writes are inhibited at $V_{CC} \le V_{LKO}$. Device operations at invalid V_{CC} voltages should not be attempted.
VCCQ	Pwr	**OUTPUT POWER SUPPLY:** Enables all outputs to be driven at V_{CCQ}. This input may be tied directly to VCC.
VSS	Pwr	**GROUND:** Pins for all internal device circuitry must be connected to system ground.
VSSQ	Pwr	**OUTPUT GROUND**: Provides ground to all outputs which are driven by VCCQ. This signal may be tied directly to VSS.
DU		**DON'T USE:** Do not use this pin. This pin should not be connected to any power supplies, signals or other pins and must be floated.
NC		**NO CONNECT:** No internal connection; can be driven or floated.

2.3 Memory Partitioning

The 1.8 Volt Intel® Wireless Flash memory is divided into 4-Mbit physical partitions which allows simultaneous RWW or RWE operations and allows users to segment code and data areas on 4-Mbit boundaries. The device's asymmetrically-blocked architecture enables system code and data integration within a single flash device. Each block can be erased independently in block erase mode. Simultaneous program and erase is not allowed. Only one partition at a time can be actively programming or erasing. See Table 2, "Bottom Parameter Memory Map" on page 7 and Table 3, "Top Parameter Memory Map" on page 8.

The 32-Mbit device has eight partitions, the 64-Mbit device has 16 partitions, and the 128-Mbit device has 32 partitions. Each device density contains one parameter partition and several main partitions: the 4-Mbit parameter partition contains eight 4-Kword parameter blocks and seven 32-Kword main blocks; and each 4-Mbit main partition contains eight 32-Kword blocks each.

The bulk of the array is divided into main blocks that can store code or data, and parameter blocks allow storage of frequently updated small parameters that would normally be stored in EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated.

Table 2. Bottom Parameter Memory Map

		Size (KW)	Blk #	32 Mbit	Blk #	64 Mbit	Blk #	128 Mbit
Main Partitions	Sixteen Partitions	32					262	7F8000-7FFFFF
		⋮					⋮	⋮
		32					135	400000-407FFF
	Eight Partitions	32			134	3F8000-3FFFFF	134	3F8000-3FFFFF
		⋮			⋮	⋮	⋮	⋮
		32			71	200000-207FFF	71	200000-207FFF
	Four Partitions	32	70	1F8000-1FFFFF	70	1F8000-1FFFFF	70	1F8000-1FFFFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		32	39	100000-107FFF	39	100000-107FFF	39	100000-107FFF
	One Partition	32	38	0F8000-0FFFFF	38	0F8000-0FFFFF	38	0F8000-0FFFFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		32	31	0C0000-0C7FFF	31	0C0000-0C7FFF	31	0C0000-0C7FFF
	One Partition	32	30	0B8000-0BFFFF	30	0B8000-0BFFFF	30	0B8000-0BFFFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		32	23	080000-087FFF	23	080000-087FFF	23	080000-087FFF
	One Partition	32	22	078000-07FFFF	22	078000-07FFFF	22	078000-07FFFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		32	15	040000-047FFF	15	040000-047FFF	15	040000-047FFF
Parameter Partition	One Partition	32	14	038000-03FFFF	14	038000-03FFFF	14	038000-03FFFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		32	8	008000-00FFFF	8	008000-00FFFF	8	008000-00FFFF
		4	7	007000-007FFF	7	007000-007FFF	7	007000-007FFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		4	0	000000-000FFF	0	000000-000FFF	0	000000-000FFF

Table 3. Top Parameter Memory Map

		Size (KW)	Blk #	32 Mbit	Blk #	64 Mbit	Blk #	128 Mbit
Parameter Partition	One Partition	4	70	1FF000-1FFFFF	134	3FF000-3FFFFF	262	7FF000-7FFFFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		4	63	1F8000-1F8FFF	127	3F8000-3F8FFF	255	7F8000-7F8FFF
		32	62	1F0000-1F7FFF	126	3F0000-3F7FFF	254	7F0000-7F7FFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		32	56	1C0000-1C7FFF	120	3C0000-3C7FFF	248	7C0000-7C7FFF
Main Partitions	One Partition	32	55	1B8000-1BFFFF	119	3B8000-3BFFFF	247	7B8000-7BFFFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		32	48	18000-187FFF	112	380000-387FFF	240	780000-787FFF
	One Partition	32	47	178000-17FFFF	111	378000-37FFFF	239	778000-77FFFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		32	40	140000-147FFF	104	340000-347FFF	232	740000-747FFF
	One Partition	32	39	138000-13FFFF	103	338000-33FFFF	231	738000-73FFFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		32	32	100000-107FFF	96	300000-307FFF	224	700000-707FFF
	Four Partitions	32	31	0F8000-0FFFFF	95	2F8000-2FFFFF	223	6F8000-6FFFFF
		⋮	⋮	⋮	⋮	⋮	⋮	⋮
		32	0	000000-007FFF	64	200000-207FFF	192	600000-607FFF
	Eight Partitions	32			63	1F8000-1FFFFF	191	5F8000-5FFFFF
		⋮			⋮	⋮	⋮	⋮
		32			0	000000-007FFF	128	400000-407FFF
	Sixteen Partitions	32					127	3F8000-3FFFFF
		⋮					⋮	⋮
		32					0	000000-007FFF

3.0 Principles of Operation

The 1.8 Volt Intel® Wireless Flash memory family includes an on-chip WSM to manage block erase and program algorithms. Its CUI allows minimal processor overhead with RAM-like interface timings.

3.1 Bus Operations

Table 4. Bus Operations

Mode	Note	RST#	CE#	OE#	WE#	ADV#	WAIT	DQ[15:0]
Read (Array, Status, Configuration, Identifier, or Query)	1,2	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Valid only in Synchronous Mode	D_{OUT}
Output Disable	3	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High-Z	High-Z
Standby	3	V_{IH}	V_{IH}	X	X	X	High-Z	High-Z
Reset	3,4	V_{IL}	X	X	X	X	High-Z	High-Z
Write	5	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	High-Z	D_{IN}

NOTES:
1. Manufacturer and device codes are accessed in read identifier mode (A[MAX:1]=0).
2. Query accesses use only DQ[7:0]. All other accesses use DQ[15:0].
3. X must be V_{IL} or V_{IH} for control pins and addresses.
4. RST# must be at $V_{SS} \pm 0.2$ V to meet the maximum specified power-down current.
5. Refer to the *Table 6, "Bus Cycle Definitions" on page 13* for valid D_{IN} during a write operation.

3.1.1 Read

The 1.8 Volt Intel Wireless Flash memory has several read configurations:

- Asynchronous page mode read.
- Synchronous burst mode read.
  - — outputs four, eight, or continuous words, from main blocks and parameter blocks.

The device's partitions have several available read modes:

- **Read array mode:** read accesses return flash array data from the addressed locations.
- **Read identifier mode:** reads return manufacturer and device identifier data, block lock status, and protection register data. The identification plane occupies the 4-Mbit partition address locations corresponding to the command's address; the flash array is not accessible in read identifier mode.
- **Read query mode:** reads return device CFI data. The query plane occupies the 4-Mbit partition address locations corresponding to the command's address; the flash array is not accessible in read query mode.
- **Read status register mode:** reads return status register data from the addressed partition. That partition's array data is not accessible. A system processor can check the status register to determine an addressed partition's state or monitor program and erase progress.

All partitions support synchronous burst mode that internally sequences addresses with respect to the input CLK to select and supply data to the outputs.

Identifier codes, query data, and status register read operations execute as single-synchronous or asynchronous read cycles. WAIT is inactive during these reads.

Access to the modes listed above is independent of V_{PP}. An appropriate CUI command places the device in a read mode. At initial power-up or after reset, the device defaults to asynchronous read array mode.

Asserting CE# enables device read operations. The device internally decodes upper address inputs to determine which partition is accessed. ADV#-active opens the internal address latches. Asserting OE# activates the outputs and gates selected data onto the I/O bus. In asynchronous mode, the address is latched when ADV# is deasserted (when the device is configured to use ADV#). In synchronous mode, the address is latched by either the rising edge of ADV# or the rising (or falling) CLK edge while ADV# remains asserted, whichever occurs first. WE# and RST# must be at deasserted during read operations.

3.1.2 Standby

CE# inactive deselects the device and places it in standby mode, substantially reducing device power consumption. In standby mode, outputs are placed in a high-impedance state independent of OE#. If deselected during a program or erase algorithm, the device will consume active power until the program or erase operation completes.

3.1.3 Write

A write occurs when CE# and WE# are asserted and OE# is deasserted. Flash control commands are written to the CUI using standard microprocessor write timings. The address and data are latched on the rising edge of WE#. Write operations are asynchronous; CLK is ignored.

The CUI does not occupy an addressable memory location within any partition. The system processor must access it at the correct address range depending on the kind of command executed. Programming or erasing may occur in only one partition at a time. Other partitions must be in one of the read modes or erase suspend mode.

Table 5, “Command Codes and Descriptions” on page 12 shows the available commands. Appendix A, “Write State Machine States” on page 65 provides information on moving between different operating modes using CUI commands.

3.1.4 Reset

The device enters a reset mode when RST# is driven low. In reset mode, internal circuitry is turned off and outputs are placed in a high-impedance state.

After returning from reset, a time t_{PHQV} is required until outputs are valid, and a delay (t_{PHWV}) is required before a write sequence can be initiated. After this wake-up interval, normal operation is restored. The device defaults to read array mode, the status register is set to 80h, and the configuration register defaults to asynchronous page-mode reads.

If RST# is asserted during an erase or program operation, the operation will be aborted and the memory contents at the aborted block or address are invalid. See Figure 29, “Reset Operations Waveforms” on page 64 for detailed information regarding reset timings.

Like any automated device, it is important to assert RST# during system reset. When the system comes out of reset, the processor expects to read from the flash memory array. Automated flash memories provide status information when read during program or erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. 1.8 Volt Intel® Flash memories allow proper CPU initialization following a system reset through the use of the RST# input. In this application, RST# is controlled by the same CPU reset signal, RESET#.

4.0 Command Definitions

The device's on-chip WSM manages erase and program algorithms. The local CPU controls the device's in-system read, program, and erase operations. Bus cycles to or from the flash memory conform to standard microprocessor bus cycles. RST#, CE#, OE#, WE#, and ADV# control signals dictate data flow into and out of the device. WAIT informs the CPU of valid data during burst reads. Table 4, "Bus Operations" on page 9 summarizes bus operations.

Device operations are selected by writing specific commands into the device's CUI. Table 5, "Command Codes and Descriptions" on page 12 lists all possible command codes and descriptions, Table 6, "Bus Cycle Definitions" on page 13 lists command definitions. Since commands are partition-specific, it is important to issue write commands within the target address range.

Multi-cycle command writes to a flash memory partition must be issued sequentially without intervening command writes. For example, an Erase Setup command to partition X must be immediately followed by the Erase Confirm command in order to be executed properly. The address given during the Erase Confirm command determines the location of the erase. If the Erase Confirm command is given to partition X, then the command will be executed and a block in partition X will be erased. Alternatively, if the Erase Confirm command is given to partition Y, the command will still be executed and a block in partition Y will be erased. Any other command given to *any* partition prior to the Erase Confirm command will result in a command sequence error, which is posted in the status register. After the erase is successfully started in partition X or Y, read cycles may occur in any other partition Z (e.g., code or data reads).

4.1 Read-While-Write and Read-While-Erase

The 1.8 Volt Intel® Wireless Flash memory supports flexible multi-partition dual-operation architecture. By dividing the flash memory into many separate partitions, the device is capable of reading from one partition while programing or erasing in another partition; hence the terms, RWW and RWE. Both of these features greatly enhance data storage performance.

The product does not support simultaneous program and erase operations. Attempting to perform operations such as these will result in a command sequence error. Only one partition may be programming or erasing while another partition is reading. However, one partition may be in erase suspend mode while a second partition is performing a program operation, and yet another partition may be executing a Read Array command.

Table 5. Command Codes and Descriptions

Mode	Code	Device Command	Description
Read	FFh	Read Array	Places selected partition in read array mode.
	70h	Read Status Register	Places selected partition in status register read mode. The partition enters this mode after a Program or Erase command is issued to it.
	90h	Read Identifier	Puts the selected partition in read identifier mode. Device reads from partition addresses output manufacturer/device codes, configuration register data, block lock status, or protection register data on DQ[15:0].
	98h	Read Query	Puts the addressed partition in read query mode. Device reads from the partition addresses output CFI information on DQ[7:0].
	50h	Clear Status Register	The WSM can set the status register's block lock (SR.1), V_{PP} (SR.3), program (SR.4), and erase (SR.5) status bits, but it cannot clear them. SR.1,3,4,5 can only be cleared by a device reset or through the Clear Status Register command.

Table 5. Command Codes and Descriptions

Mode	Code	Device Command	Description
Program	40h	Word Program Setup	This preferred program command's first cycle prepares the CUI for a program operation. The second cycle latches address and data and executes the WSM Program algorithm at this location. Status register updates occur when CE# or OE# is toggled. A Read Array command is required to read array data after programming.
	10h	Alternate Setup	Equivalent to a Program Setup command (40h).
	30h	EFP Setup	This program command activates EFP mode. The first write cycle sets up the command. If the second cycle is an EFP Confirm command (D0h), subsequent writes provide program data. All other commands are ignored once EFP mode begins.
	D0h	EFP Confirm	If the first command was EFP Setup (30h), the CUI latches the address and data and prepares the device for EFP mode.
Erase	20h	Erase Setup	Prepares the CUI for Block Erase. The device erases the block addressed by the Erase Confirm command. If the next command is not Erase Confirm, the CUI: (a) sets status register bits SR.4 and SR.5, (b) places the partition in the read status register mode, and (c) waits for another command.
	D0h	Erase Confirm	If the first command was Erase Setup (20h), the CUI latches address and data and erases the block indicated by the erase confirm cycle address. During program or erase, the partition responds only to Read Status Register, Program Suspend, and Erase Suspend commands. CE# or OE# toggle updates status register data.
Suspend	B0h	Program Suspend or Erase Suspend	This command issued at any device address suspends the currently executing program or erase operation. The status register, invoked by a Read Status Register command, indicates successful operation suspension by setting status bits SR.2 (program suspend) or SR.6 (erase suspend) and SR.7. The WSM remains in the suspend mode regardless of control signal states, except RST# = V_{IL}.
	D0h	Suspend Resume	This command issued at any device address resumes suspended program or erase operation.
Block Locking	60h	Lock Setup	Prepares the CUI lock configuration. If the next command is not Block-Lock, Unlock, or Lock-Down, the CUI sets SR.4 and SR.5 to indicate command sequence error.
	01h	Lock Block	If the previous command was Lock Setup (60h), the CUI locks the addressed block.
	D0h	Unlock Block	If the previous command was Lock Setup (60h) command, the CUI latches the address and unlocks the addressed block. If previously locked-down, the operation has no effect.
	2Fh	Lock-Down	If the previous command was Lock Setup (60h) command, the CUI latches the address and locks-down the addressed block.
Protection	C0h	Protection Program Setup	Prepares the CUI for a protection register program operation. The second cycle latches address and data and starts the WSM's protection register program or lock algorithm. Toggling CE# or OE# updates the flash status register data. To read array data after programming, issue a Read Array command.
Configuration	60h	Configuration Setup	Prepares the CUI for device configuration. If Set Configuration Register is not the next command, the CUI sets SR.4 and SR.5 to indicate command sequence error.
	03h	Set Configuration Register	If the previous command was Configuration Setup (60h), the CUI latches the address and writes A[15:0] data into the configuration register. Following a Set Configuration Register command, subsequent read operations access array data.

NOTE: Do not use unassigned commands. Intel reserves the right to redefine these codes for future functions.

Table 6. Bus Cycle Definitions

Mode	Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
			Oper	Addr(1)	Data(2,3)	Oper	Addr(1)	Data(2,3)
Read	Read Array/Reset	1	Write	PnA	FFh			
	Read Identifier	≥ 2	Write	PnA	90h	Read	PBA+IA	IC
	Read Query	≥ 2	Write	PnA	98h	Read	PBA+QA	QD
	Read Status Register	2	Write	PnA	70h	Read	BA	SRD
	Clear Status Register	1	Write	XX	50h			
Program Erase	Block Erase	2	Write	BA	20h	Write	BA	D0h
	Word Program	2	Write	WA	40h/10h	Write	WA	WD
	EFP	≥2	Write	WA	30h	Write	WA	D0h
	Program/Erase Suspend	1	Write	XX	B0h			
	Program/Erase Resume	1	Write	XX	D0h			
Lock	Lock Block	2	Write	BA	60h	Write	BA	01h
	Unlock Block	2	Write	BA	60h	Write	BA	D0h
	Lock-Down Block	2	Write	BA	60h	Write	BA	2Fh
Protec-tion	Protection Program	2	Write	PA	C0h	Write	PA	PD
	Lock Protection Program	2	Write	LPA	C0h	Write	LPA	FFFDh
Config-uration	Set Configuration Register	2	Write	CD	60h	Write	CD	03h

NOTES:

1. First cycle command addresses should be the same as the operation's target address. Examples: the first-cycle address for the Read Identifier command should be the same as the Identification code address (IA); the first cycle address for the Word Program command should be the same as the word address (WA) to be programmed; the first cycle address for the Erase/Program Suspend command should be the same as the address within the block to be suspended; etc.
   XX = Any valid address within the device.
   IA = Identification code address.
   BA = Block Address. Any address within a specific block.
   LPA = Lock Protection Address is obtained from the CFI (via the Read Query command). The 1.8 Volt Intel Wireless Flash memory family's LPA is at 0080h.
   PA = User programmable 4-word protection address in the device identification plane.
   PnA = Any address within a specific partition.
   PBA = Partition Base Address. The very first address of a particular partition.
   QA = Query code address.
   WA = Word address of memory location to be written.
2. SRD = Data read from the status register.
   WD = Data to be written at location WA.
   IC = Identifier code data.
   PD = User programmable 4-word protection data.
   QD = Query code data on DQ[7:0].
   CD = Configuration register code data presented on device addresses A[15:0]. A[MAX:16] address bits can select any partition. See Table 12, "Configuration Register Definitions" on page 34 for configuration register bits descriptions.
3. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

4.2 Read Array Command

The Read Array command places (or resets) the partition in read array mode. Upon initial device power-up or after reset (RST# transitions from V_{IL} to V_{IH}), all partitions default to read array mode and to asynchronous page mode read configuration. A Read Array command written to a partition that is performing an erase or program operation will present invalid data until the operation completes; it will then display array data when read. If an Erase- or Program-Suspend command suspends the WSM, a subsequent Read Array command will place the addressed partition in read array mode. The Read Array command functions independently of V_{PP}.

4.3 Read Identifier Command

The read identifier mode outputs the manufacturer/device identifier, block lock status, protection register codes, and configuration register. The identifier plane occupies the 4-Mbit partition address range supplied by the Read Identifier command (90h) address. Reads from addresses in Table 7 retrieve ID information. Issuing a Read Identifier command to a partition that is programming or erasing places that partition's outputs in read ID mode while the partition continues to program or erase in the background.

Table 7. Device Identification Codes

Item	Address(1)		Data	Description
	Base	Offset		
Manufacturer ID	Partition	00h	0089h	
Device ID	Partition	01h	8862h	32-Mbit TPD
			8863h	32-Mbit BPD
			8864h	64-Mbit TPD
			8865h	64-Mbit BPD
			8866h	128-Mbit TPD
			8867h	128-Mbit BPD
Block Lock Status(2)	Block	02h	DQ[0] = 0	Block is unlocked
			DQ[0] = 1	Block is locked
Block Lock-Down Status(2)	Block	02h	DQ[1] = 0	Block is not locked-down
			DQ[1] = 1	Block is locked down
Configuration Register	Partition	05h	Register Data	
Protection Register Lock Status	Partition	80h	Lock Data	
Protection Register	Partition	81h - 88h	Register Data	Multiple reads required to read the entire 128-bit Protection Register.

NOTES:
1. The address is constructed from a base address plus an offset. For example, to read the Block Lock Status for block number 38 in a BPD, set the address to the BBA (0F8000h) plus the *offset* (02h), i.e. 0F8002h. Then examine bit 0 of the data to determine if the block is locked.
2. See Section 4.12.4, "Block Lock Status" on page 29 for valid lock status.

4.4 Read Query Command

The query plane comes to the foreground and occupies a 4-Mbit address range at the partition supplied by the Read Query command address. The mode outputs CFI data when partition addresses are read. Appendix B, “Common Flash Interface” on page 68 shows query mode information and addresses. Issuing a Read Query command to a partition that is programming or erasing places that partition’s outputs in read query mode while the partition continues to program or erase in the background.

4.5 Read Status Register Command

The device’s status register displays program and erase operation status. A partition’s status can be read after writing the Read Status Register command to the partition’s address range. The status register can also be read following a Program, Erase, or Lock Block command sequence. Subsequent single reads from that partition will return its status until another valid command is written.

The read status mode supports single synchronous and single asynchronous reads only; it doesn’t support page mode or burst reads. The first OE# or CE# falling edge latches and updates status register data. The operation doesn’t affect other partitions’ modes. DQ[7:0] outputs status register data while DQ[15:8] outputs 00h. See Table 8, “Status Register Definitions” on page 16.

The status register occupies the 4-Mbit partition to which the Read Status, Program, or Erase command was issued. Status register bit SR.7 is the DWS (Device WSM Status) bit and provides program and erase status of the device. The PWS (Partition Write/Erase Status) bit tells whether the addressed partition or some other partition is actively programming or erasing. Status register bits SR.6-1 present information about the WSM’s program, erase, suspend, V_{PP}, and block-lock status. Table 9, “Status Register DWS and PWS Description” on page 16 presents descriptions of DWS (SR.7) and PWS (SR.0) combinations.

Table 8. Status Register Definitions

DWS	ESS	ES	PS	VPPS	PSS	DPS	PWS
7	6	5	4	3	2	1	0

Bit	Name	State	Description
7	**DWS** Device WSM Status	0 = Device WSM is Busy 1 = Device WSM is Ready	SR.7 indicates erase or program completion in the device. SR.1–6 are invalid while SR.7 = 0. See Table 9 for valid SR.7 and SR.0 combinations.
6	**ESS** Erase Suspend Status	0 = Erase in progress/completed 1 = Erase suspended	After issuing an Erase Suspend command, the WSM halts and sets SR.7 and SR.6. SR.6 remains set until the device receives an Erase Resume command.
5	**ES** Erase Status	0 = Erase successful 1 = Erase error	SR.5 is set if an attempted erase failed. A Command Sequence Error is indicated when SR.4, SR.5 and SR.7 are set.
4	**PS** Program Status	0 = Program successful 1 = Program error	SR.4 is set if the WSM failed to program a word.
3	**VPPS** VPP Status	0 = V_{PP} OK 1 = V_{PP} low detect, operation aborted	The WSM indicates the V_{PP} level after program or erase completes. SR.3 does not provide continuous V_{PP} feedback and isn't guaranteed when $V_{PP} \neq V_{PP1/2}$.
2	**PSS** Program Suspend Status	0 = Program in progress/completed 1 = Program suspended	After receiving a Program Suspend command, the WSM halts execution and sets SR.7 & SR.2. They remain set until a Resume command is received.
1	**DPS** Device Protect Status	0 = Unlocked 1 = Aborted erase/program attempt on locked block	If an erase or program operation is attempted to a locked block (if WP# = V_{IL}), the WSM sets SR.1 and aborts the operation.
0	**PWS** Partition Write Status	0 = Depending on SR.7's state, the addressed partition is busy or no other partition is busy. 1 = Another partition is busy	Addressed partition or another partition is erasing or programming. In EFP mode, SR.0 indicates that a data-stream word has finished programming or verifying depending on the particular EFP phase. See Table 9 for valid SR.7 and SR.0 combinations.

Table 9. Status Register DWS and PWS Description

DWS (SR.7)	PWS (SR.0)	Description
0	0	The addressed partition is performing a program/erase operation. EFP: device is finished programming or verifying data or is ready for data.
0	1	A partition other than the one currently addressed is performing a program/erase operation. EFP: the device is either programming or verifying data.
1	0	No program/erase operation is in progress in any partition. Erase and Program suspend bits (SR.6 and SR.2) indicate whether other partitions are suspended. EFP: the device has exited EFP mode.
1	1	Won't occur in standard program or erase modes. EFP: this combination will not occur.

4.6 Clear Status Register Command

The Clear Status Register command clears the status register and leaves all partition output states unchanged. The command functions independently of the applied V_{PP} voltage. The WSM can set all status register bits and clear bits 0, 2, 6, and 7. Because bits 1, 3, 4 and 5 indicate various error conditions, they can only be cleared by the Clear Status Register command. By allowing system software to reset these bits, several operations (such as cumulatively programming several addresses or erasing multiple blocks in sequence), may be performed before reading the status register to determine error occurrence. The status register should be cleared before beginning another command or sequence. Device reset (RST# = V_{IL}) also clears the status register.

4.7 Word Program Command

Writing a Word Program command to the device initiates internally timed sequences that program the requested word.

Programming can occur in only one partition at a time. Other partitions must be in one of the read modes or in erase suspend mode. Note that only one partition at a time can be in erase suspend mode.

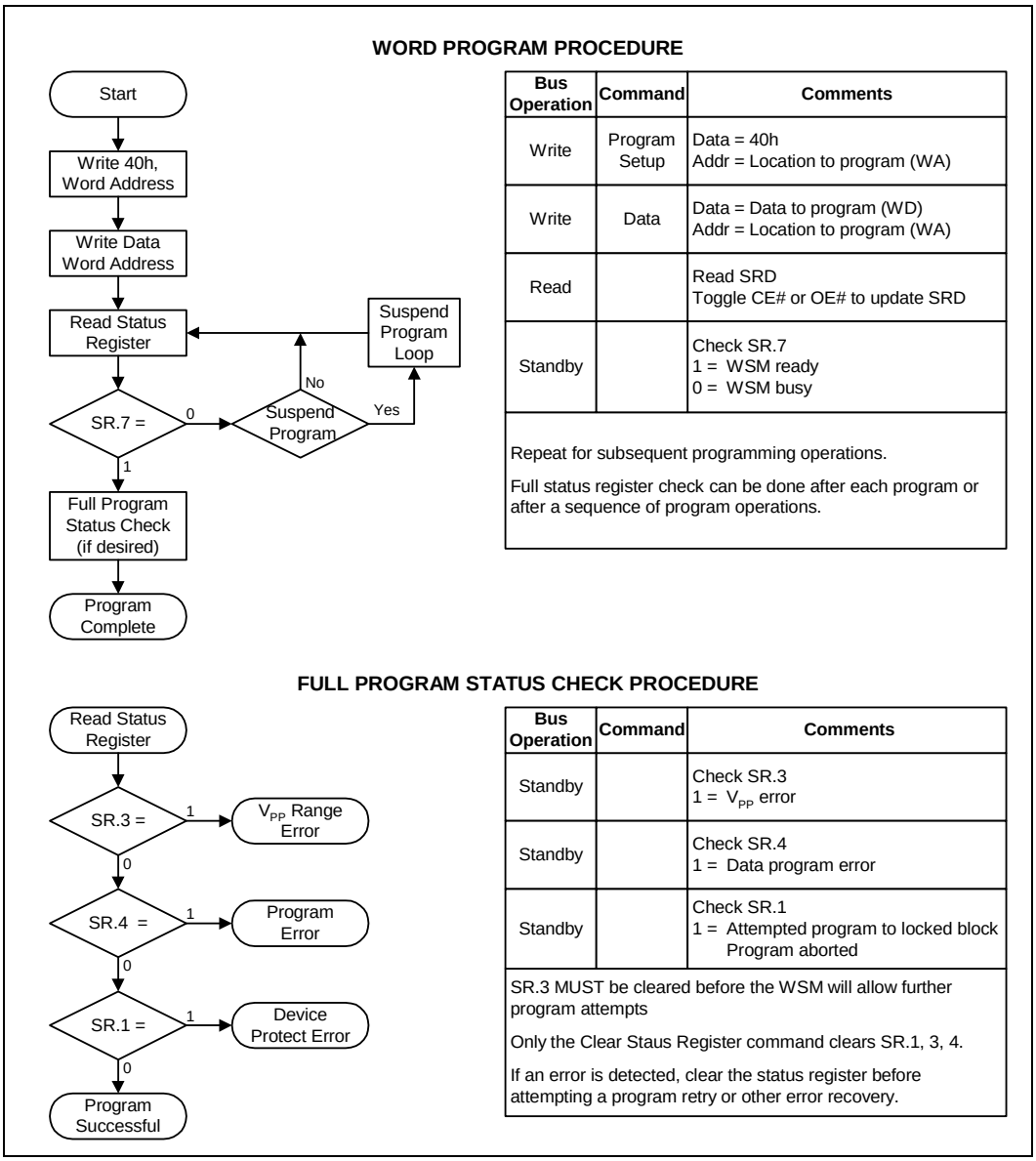
The WSM executes a sequence of internally timed events to program desired bits at the addressed location and verify that the bits are sufficiently programmed. Programming the memory changes specifically addressed bits to ‘0.’ ‘1’ bits do not change the memory cell contents.

The status register can be examined for program progress and errors by reading any address within the partition that’s programming. Issuing a Read Status Register command to other partitions brings the status register to the foreground in those partitions, allowing program progress to be monitored or detected at other device addresses. Status register bit SR.7 indicates device program status while the program sequence executes. CE# or OE# toggle (during polling) updates the status register. Valid commands that can be issued to the programming partition during programming are Read Status Register, Program Suspend, Read Identifier, Read Query, and Read Array (which returns unknown data).

When programming completes, SR.4=1 indicates program failure. If SR.3 is set, the WSM couldn’t execute the Word Program command because V_{PP} was outside acceptable limits. If SR.1 is set, the program operation targeted a locked block and was aborted.

After examining the status register, it should be cleared by the Clear Status Register command before issuing a new command. The partition remains in status register mode until another command is written to that partition. Any command can follow once program completes.

Figure 2. Word Program Flowchart



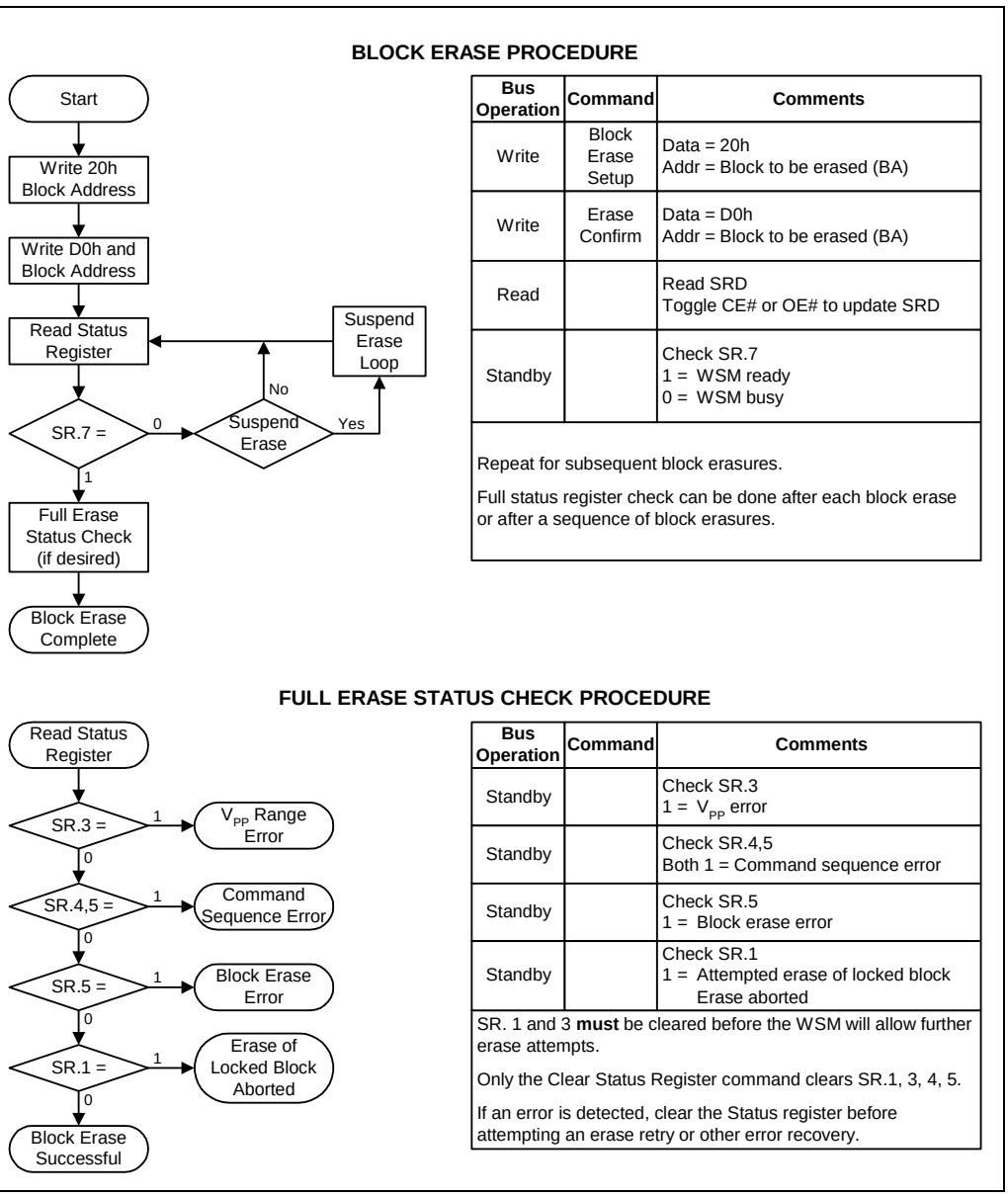
4.8 Block Erase Command

The two-cycle block erase command sequence, consisting of Erase Setup (20h) and Erase Confirm (D0h), initiates one block erase at the addressed block. Only one partition can be in an erase mode at a time; other partitions must be in a read mode. The Erase Confirm command internally latches the address of the block to be erased. Erase forces all bits within the block to '1'. SR.7 is cleared while the erase executes.

After writing the Erase Confirm command, the selected partition is placed in read status register mode and reads performed to that partition will return current status data. The CPU can detect block erase completion by analyzing SR.7 of that partition. SR.5=1 indicates an erase failure, SR.3=1 indicates an invalid V_{PP} supply voltage, and SR.1=1 indicates an erase operation was attempted on a locked block.

If an error bit was flagged, the status register can be cleared by issuing the Clear Status Register command before attempting the next operation. The partition will remain in read status register mode until another command is written to its CUI. Any CUI instruction can follow once erasing completes. The CUI can be set to read array mode to prevent inadvertent status register reads.

Figure 3. Block Erase Flowchart



4.9 Program Suspend, Program Resume Erase Suspend, Erase Resume Commands

The Program Suspend and Erase Suspend commands halt an in-progress program or erase operation. The command can be issued at any device address. The partition corresponding to the command's address remains in its previous state. The Suspend command allows data to be accessed from memory locations other than the one being programmed or the block being erased.

A program operation can be suspended to perform reads only. An erase operation can be suspended to perform either a program or a read operation within any block, except the block that is erase suspended. A Program command nested within a suspended erase can subsequently be suspended to read yet another location. Once a program/erase process starts, the Suspend command requests that the WSM suspend the program/erase sequence at predetermined points in the algorithm. The partition that is actually suspended continues to output status register data after the Suspend command is written. An operation is suspended when status bits SR.7 and SR.6 and/or SR.2 display '1'. t_{WHRH1}/t_{EHRH1} specifies suspend latency.

To read data from blocks within the partition (other than an erase-suspended block), a Read Array command can be written. During Erase Suspend, a Program command can be issued to a block other than the erase-suspended block. Block erase cannot resume until program operations initiated during erase suspend complete. Read Array, Read Status Register, Read Identifier (ID), Read Query, and Program Resume are valid commands during Program or Erase Suspend. Additionally, Clear Status Register, Program, Program Suspend, Erase Resume, Lock Block, Unlock Block, and Lock-Down Block are valid commands during erase suspend.

To read data from a block in a partition that is not programming/erasing, the operation does not need to be suspended. If the other partition is already in read array, ID, or Query mode, issuing a valid address will return corresponding data. If the other partition is not in a read mode, one of the read commands must be issued to the partition before data can be read.

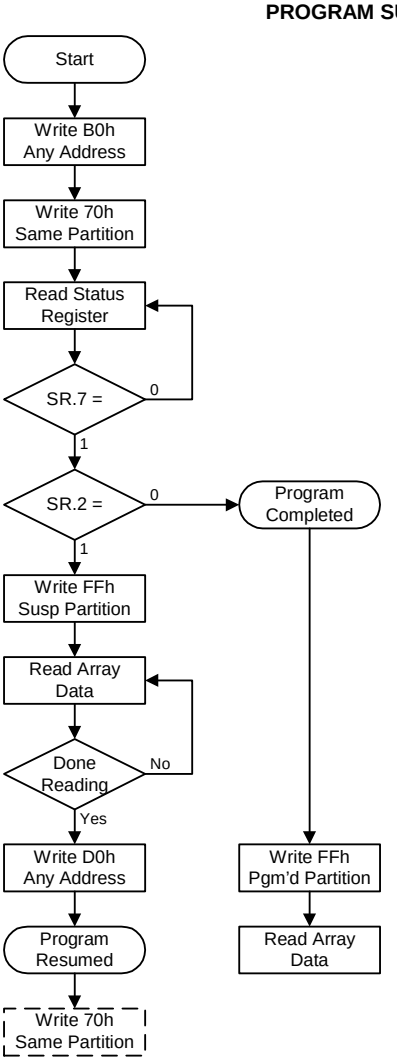
During a suspend, CE# = V_{IH} places the device in standby state, which reduces active current. V_{PP} must remain at its program level and WP# must remain unchanged while in suspend mode.

A Resume command instructs the WSM to continue programming or erasing and clears status register bits SR.2 (or SR.6) and SR.7. The Resume command can be written to any partition. When read at the partition that is programming or erasing, the device outputs data corresponding to the partition's last mode. If status register error bits are set, the status register can be cleared before issuing the next instruction. RST# must remain at V_{IH}. See Figure 4, "Program Suspend/Resume Flowchart" on page 21 and Figure 5, "Erase Suspend/Resume Flowchart" on page 22.

If a suspended partition was placed in read array, read status register, read identifier (ID), or read query mode during the suspend, the device remains in that mode and outputs data corresponding to that mode after the program or erase operation is resumed. After resuming a suspend operation, issue the read command appropriate to the read operation. To read status after resuming a suspended operation, issue a Read Status Register command (70h) to return the suspended partition to status mode.

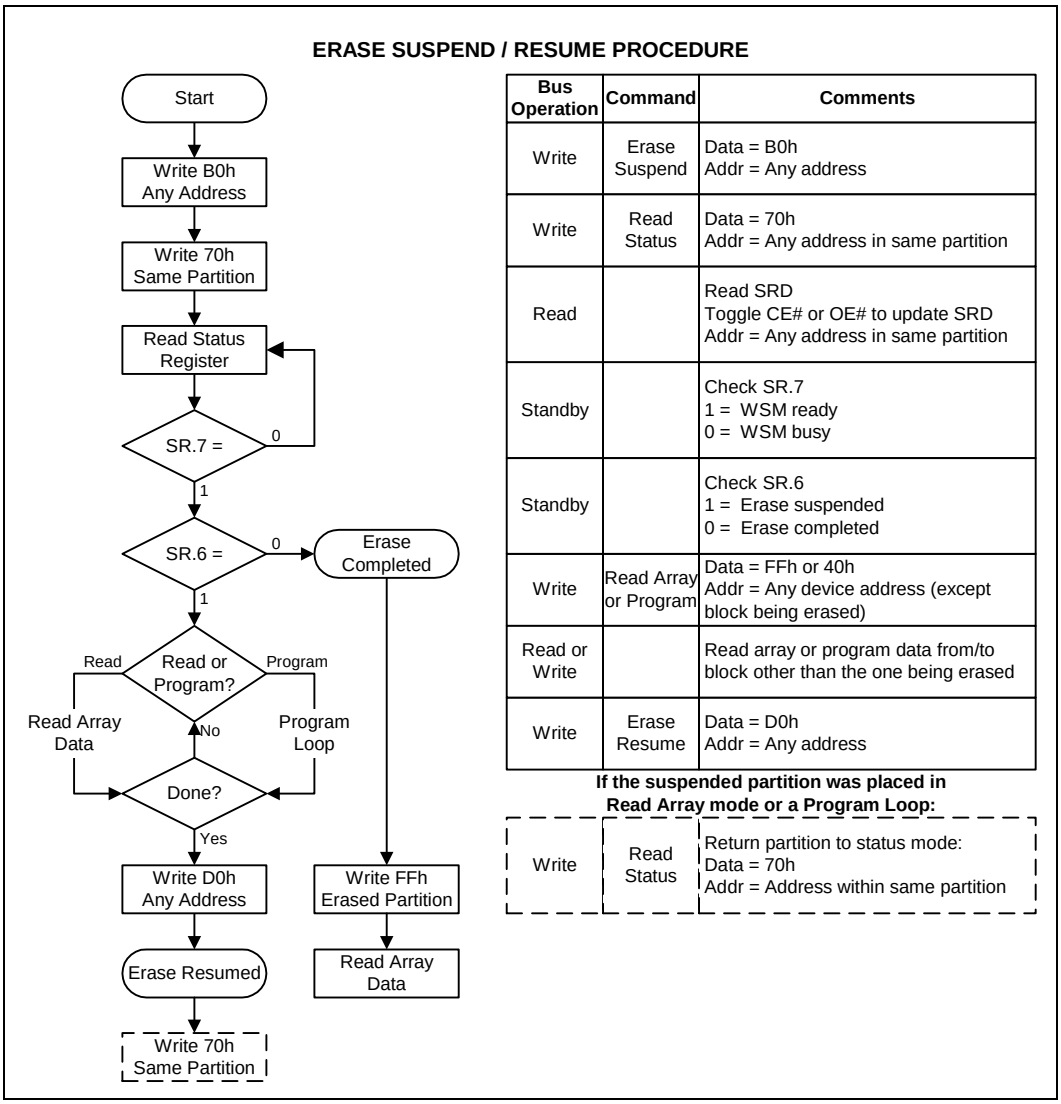
A minimum t_{WHWH} time should elapse between an Erase command and a subsequent Erase Suspend command to ensure that the device achieves sufficient cumulative erase time. Occasional Erase-to-Suspend interrupts do not cause problems, but Erase-to-Suspend commands issued too frequently may produce undetermined results.

Figure 4. Program Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0h Addr = Any address within programming partition
Write	Read Status	Data = 70h Addr = Any address in same partition
Read		Read SRD Toggle CE# or OE# to update SRD Addr = Any address in same partition
Standby		Check SR.7 1 = WSM ready 0 = WSM busy
Standby		Check SR.2 1 = Program suspended 0 = Program completed
Write	Read Array	Data = FFh Addr = Any device address (except word being programmed)
Read		Read array data from block other than the one being programmed
Write	Program Resume	Data = D0h Addr = any device address
If the suspended partition was placed in Read Array mode:		
Write	Read Status	Return partition to status mode: Data = 70h Addr = address within same partition

Figure 5. Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0h Addr = Any address
Write	Read Status	Data = 70h Addr = Any address in same partition
Read		Read SRD Toggle CE# or OE# to update SRD Addr = Any address in same partition
Standby		Check SR.7 1 = WSM ready 0 = WSM busy
Standby		Check SR.6 1 = Erase suspended 0 = Erase completed
Write	Read Array or Program	Data = FFh or 40h Addr = Any device address (except block being erased)
Read or Write		Read array or program data from/to block other than the one being erased
Write	Erase Resume	Data = D0h Addr = Any address

If the suspended partition was placed in Read Array mode or a Program Loop:

Write	Read Status	Return partition to status mode: Data = 70h Addr = Address within same partition

4.10 Enhanced Factory Program Command (EFP)

EFP substantially improves device programming performance via a number of enhancements to the conventional 12-volt word program algorithm. EFP's more efficient WSM algorithm eliminates the traditional overhead delays of conventional word program mode in both the host programming system and the flash device. Changes to the conventional word programming flowchart and internal WSM routine were developed because of today's beat-rate-sensitive manufacturing environments; a balance between programming speed and cycling performance was struck.

After a single command sequence, host programmer bus cycles write data words followed by status checks to determine when the next data word is ready to be accepted. This modification essentially cuts write bus cycles in half. Following each internal program pulse, the WSM increments the device's address to the next physical location. Now, programming equipment can sequentially stream program data throughout an entire block without having to setup and present each new address. In combination, these enhancements reduce much of the host programmer overhead, enabling more of a data streaming approach to device programming.

Additionally, EFP speeds up programming by performing internal code verification. With this, PROM programmers can rely on the device to verify that it's been programmed properly. From the device side, EFP streamlines internal overhead by eliminating the delays previously associated to switch voltages between programming and verify levels at each memory-word location.

EFP consists of four phases: setup, program, verify and exit. Refer to Figure 6, "Enhanced Factory Program Flowchart" on page 26 for a detailed graphical representation on how to implement EFP.

4.10.1 EFP Requirements and Considerations

EFP requirements:

- Ambient temperature: T_A = 25 °C ±5 °C
- V_{CC} within specified operating range
- V_{PP} within specified V_{PP2} range
- Target block unlocked

EFP considerations:

- Block cycling below 10 erase cycles (1)
- RWW not supported(2)
- EFP programs one block at a time
- EFP cannot be suspended

1. Recommended for optimum performance. Some degradation in performance may occur if this limit is exceeded, but the internal algorithm will continue to work properly.
2. Code or data cannot be read from another partition during EFP.

See Figure 6, "Enhanced Factory Program Flowchart" on page 26 for a detailed flowchart on how to implement an EFP operation.

4.10.2 Setup Phase

After receiving the EFP Setup (30h) and EFP Confirm (D0h) command sequence, SR.7 transitions from a '1' to a '0' indicating that the WSM is busy with EFP algorithm startup. A delay before checking SR.7 is required to allow the WSM time to perform all of its setups and checks (V_{PP} level and block lock status). If an error is detected, status register bits SR.4, SR.3 and/or SR.1 are set and EFP operation terminates.

NOTE: After the EFP Setup and Confirm command sequence, reads from the device automatically output status register data. Do not issue the Read Status Register command; it will be interpreted as data to program at WA0.

4.10.3 Program Phase

After setup completion, the host programming system must check SR.0 to determine "data-stream ready" status (SR.0=0). Each subsequent write after this is a program-data write to the flash array. Each cell within the memory word to be programmed to '0' will receive one WSM pulse; additional pulses, if required, occur in the verify phase. SR.0=1 indicates that the WSM is busy applying the program pulse.

The host programmer must poll the device's status register for the "program done" state after each data-stream write. SR.0=0 indicates that the appropriate cell(s) within the accessed memory location have received their single WSM program pulse, and that the device is now ready for the next word. Although the host may check full status for errors at any time, it is only necessary on a block basis, after EFP exit.

Addresses must remain within the target block. Supplying an address outside the target block immediately terminates the program phase; the WSM then enters the EFP verify phase.

The address can either hold constant or it can increment. The device compares the incoming address to that stored from the setup phase (WA_0); if they match, the WSM programs the new data word at the next sequential memory location. If they differ, the WSM jumps to the new address location.

The program phase concludes when the host programming system writes to a different block address, data supplied must be FFFFh. Upon program phase completion, the device enters the EFP verify phase.

4.10.4 Verify Phase

A high percentage of the flash bits program on the first WSM pulse. However, for those cells that do not completely program on their first attempt, EFP internal verification identifies them and applies additional pulses as required.

The verify phase is identical in flow to that of the program phase, except that instead of programming incoming data, the WSM compares the verify-stream data to that which was previously programmed into the block. If the data compares correctly, the host programmer proceeds to the next word. If not, the host waits while the WSM applies an additional pulse(s).

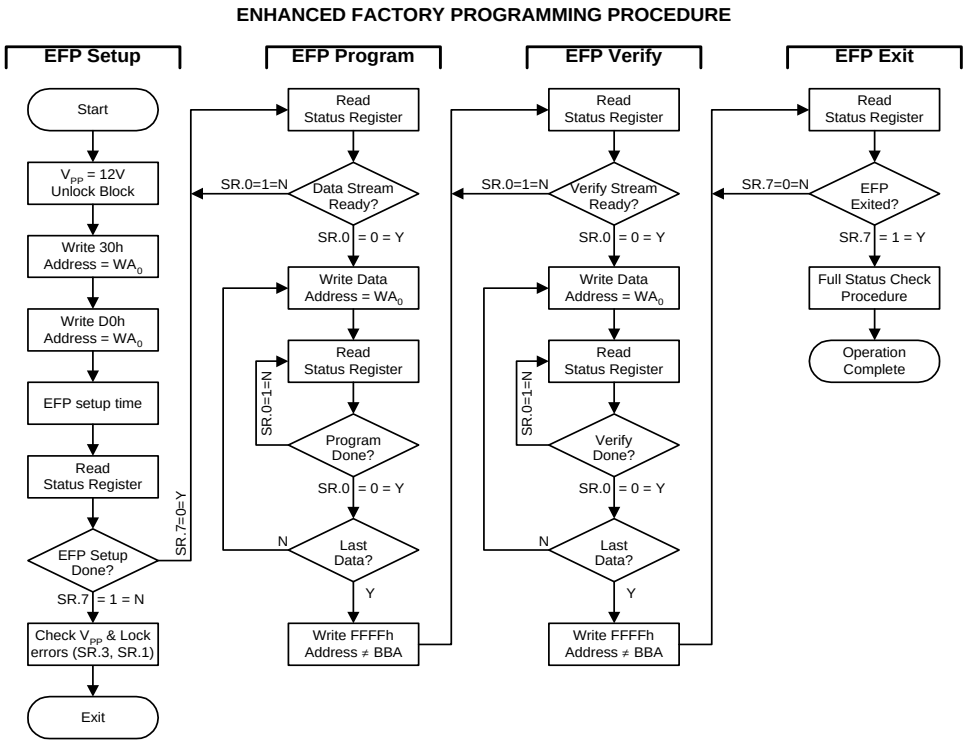
The host programmer must reset its initial verify-word address to the same starting location supplied during the program phase. It then reissues each data word in the same order it did during the program phase. Like programming, the host may write each subsequent data word to WA_0 or it may increment up through the block addresses.

The verification phase concludes when the interfacing programmer writes to a different block address; data supplied must be FFFFh. Upon verify phase completion, the device enters the EFP exit phase.

4.10.5 Exit Phase

SR.7=1 indicates that the device has returned to normal operating conditions. A full status check should be performed at this time to ensure the entire block programmed successfully. After EFP exit, any valid CUI command can be issued.

Figure 6. Enhanced Factory Program Flowchart



EFP Setup

Bus State		Comments
Write	Unlock Block	V_{PP} = 12V Unlock block
Write	EFP Setup	Data = 30h Address = WA_0
Write	EFP Confirm	Data = D0h Address = WA_0
Standby		EFP setup time
Read		Status Register
Standby	EFP Setup Done?	Check SR.7 0 = EFP ready 1 = EFP not ready
Standby	Error Condition Check	If SR.7 = 1: Check SR.3, SR.1 SR.3 = 1 = V_{PP} error SR.1 = 1 = locked block

EFP Program

Bus State		Comments
Read		Status Register
Standby	Data Stream Ready?	Check SR.0 0 = Ready for data 1 = Not ready for data
Write (note 1)		Data = Data to program Address = WA_0
Read		Status Register
Standby	Program Done?	Check SR.0 0 = Program done 1 = Program not done
Standby	Last Data?	Device automatically increments address.
Write	Exit Program Phase	Data = FFFFh Address not within same BBA

EFP Verify

Bus State		Comments
Read		Status Register
Standby	Verify Stream Ready?	Check SR.0 0 = Ready for verify 1 = Not ready for verify
Write (note 2)		Data = Word to verify Address = WA_0
Read		Status Register
Standby (note 3)	Verify Done?	Check SR.0 0 = Verify done 1 = Verify not done
Standby	Last Data?	Device automatically increments address.
Write	Exit Verify Phase	Data = FFFFh Address not within same BBA

EFP Exit

Read		Status Register
Standby	EFP Exited?	Check SR.7 0 = Exit not finished 1 = Exit completed

Repeat for subsequent operations.

After EFP exit, a Full Status Check can determine if any program error occurred.

See the Full Status Check procedure in the Word Program flowchart.

1. WA_0 = first Word Address to be programmed within the target block. The BBA (Block Base Address) must remain constant throughout the program phase data stream; WA can be held constant at the first address location, or it can be written to sequence up through the addresses within the block. Writing to a BBA not equal to that of the block currently being written to terminates the EFP program phase, and instructs the device to enter the EFP verify phase.
2. For proper verification to occur , the verify data stream must be presented to the device in the same sequence as that of the program phase data stream. Writing to a BBA not equal to WA terminates the EFP verify phase, and instructs the device to exit EFP .
3. Bits that did not fully program with the single WSM pulse of the EFP program phase receive additional program-pulse attempts during the EFP verify phase. The device will report any program failure by setting SR.4=1; this check can be performed during the full status check after EFP has been exited for that block, and will indicate any error within the entire data stream.

4.11 Security Modes

The 1.8 Volt Intel® Wireless Flash memory offers both hardware and software security features to protect the flash data. The software security feature is used by executing the Lock Block command. The hardware security feature is used by executing the Lock-Down Block command *and* by asserting the WP# signal.

Refer to Figure 7, “Block Locking State Diagram” on page 28 for a state diagram of the flash security features. Also see Figure 8, “Locking Operations Flowchart” on page 30.

4.12 Block Locking Commands

Individual instant block locking protects code and data by allowing any block to be locked or unlocked with no latency. This locking scheme offers two levels of protection. The first allows software-only control of block locking (useful for frequently changed data blocks), while the second requires hardware interaction before locking can be changed (protects infrequently changed code blocks).

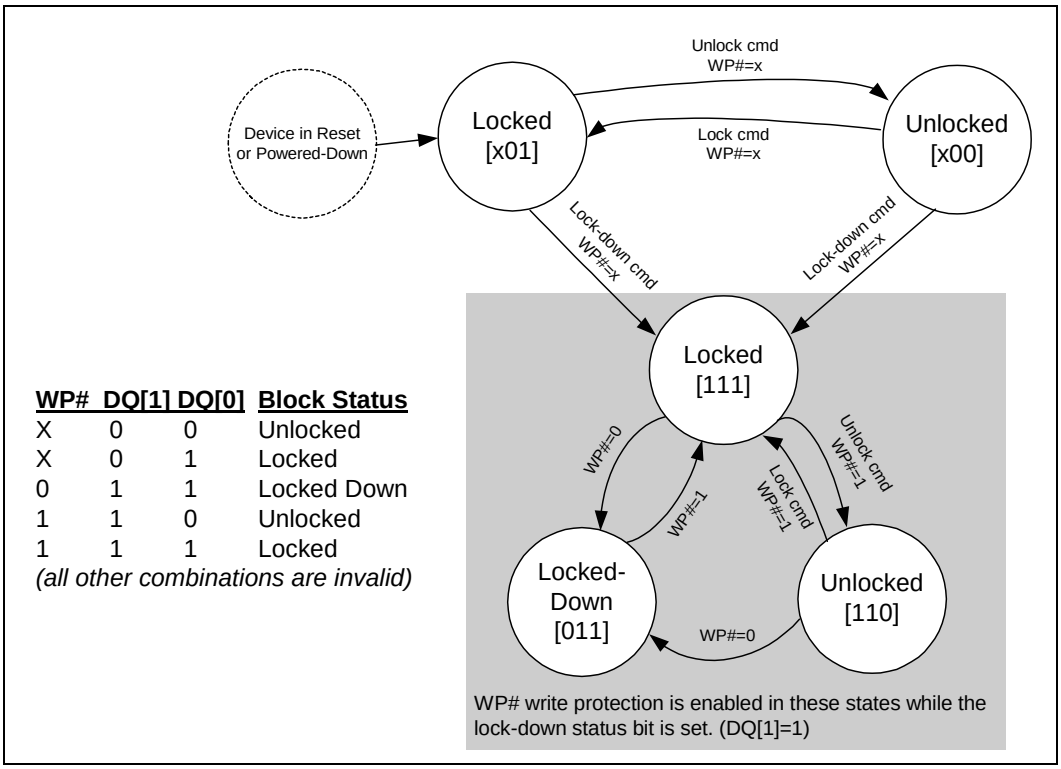
The following sections discuss the locking system operation. The term “state [XYZ]” specifies locking states; e.g., “state [001],” where X = WP# value, Y = Block Lock status register bit DQ_1, and Z = Block Lock status register bit DQ_0. Figure 7, “Block Locking State Diagram defines possible locking states.

The following summarizes the locking functionality.

- All blocks power-up in a locked state. Unlock commands can unlock these blocks.
- The Lock-Down command locks a block and prevents it from being unlocked when WP# = V_{IL}.
  - WP# = V_{IH} overrides lock-down so commands can unlock or lock blocks.
  - When WP# returns to V_{IL}, previously locked-down blocks return to lock-down.
  - The Lock-Down state is cleared only when the device is reset or powered-down.

Each block’s locking status can be set to locked, unlocked, and lock-down, as described in the following sections. Figure 7, “Block Locking State Diagram” on page 28 shows the state table for the locking functions. See also Figure 8, “Locking Operations Flowchart” on page 30.

Figure 7. Block Locking State Diagram



WP#	DQ[1]	DQ[0]	Block Status
X	0	0	Unlocked
X	0	1	Locked
0	1	1	Locked Down
1	1	0	Unlocked
1	1	1	Locked

(all other combinations are invalid)

NOTES:
1. The notation [X,Y,Z] denotes the locking state of a block, The current locking state of a block is defined by the state of WP# and the two bits of the block-lock status DQ[1:0].

4.12.1 Lock Block

All blocks default to locked (states [001] or [101]) after initial power-up or reset. Locked blocks are fully protected from alteration. Attempted program or erase operations to a locked block will return an error in SR.1. Unlocked blocks can be locked by using the Lock Block command sequence. Similarly, a locked block's status can be changed to unlocked or lock-down using the appropriate software commands.

4.12.2 Unlock Block

Unlocked blocks (states [000], [100], [110]) can be programmed or erased. All unlocked blocks return to the locked state when the device is reset or powered-down. An unlocked block's status can be changed to the locked or locked-down state using the appropriate software commands. A locked block can be unlocked by writing the Unlock Block command sequence if the block is not locked-down.

4.12.3 Lock-Down Block

Locked-down blocks (state [011]) offer the user an addition level of write protection beyond that of a regular locked block. A block that is locked-down cannot have it's state changed by software if WP# is asserted. A locked or unlocked block can be locked-down by writing the Lock-Down Block

command sequence. If a block was set to locked-down, then later changed to unlocked, asserting WP# will force that block back to the locked-down. When WP# is deasserted, locked-down blocks are changed to the locked state and can then be unlocked by Unlock Block command. Locked-down blocks revert to the locked state at device reset or power-down.

4.12.4 Block Lock Status

Every block's lock status can be read in read identifier mode. To enter this mode, write 90h to the device. Subsequent reads at Block Address + 02h will output that block's lock status. For example, to read the block lock status of block 10, the address sent to the device should be 50002h (for a top-parameter device). The lowest two data bits, DQ[1] and DQ[0], represent the lock status. DQ[0] indicates the block lock status. It is set by the Lock Block command and cleared by the Block Unlock command. It is also set when entering lock-down state. DQ[1] indicates lock-down status and is set by the Lock-Down command. The lock-down status bit cannot be cleared by software, only by device reset or power-down. See Table 10.

Table 10. Write Protection Truth Table

VPP	WP#	RST#	Write Protection
X	X	V_{IL}	Device inaccessible
V_{IL}	X	V_{IH}	Word program and block erase prohibited
X	V_{IL}	V_{IH}	All lock-down blocks locked
X	V_{IH}	V_{IH}	All lock-down blocks can be unlocked

4.12.5 Locking Operations During Erase Suspend

Block lock configurations can be performed during an erase suspend operation by using the standard locking command sequences to unlock, lock, or lock-down a block. This feature is useful when another block requires immediate updating.

To change block locking during an erase operation, first write the Erase Suspend command. After checking SR.6 to determine the erase operation has suspended, write the desired lock command sequence to a block; the lock status will be changed. After completing lock, unlock, read, or program operations, resume the erase operation with the Erase Resume command (D0h).

If a block is locked or locked-down during a suspended erase of the same block, the locking status bits will change immediately. But, when resumed, the erase operation will complete.

Locking operations cannot occur during program suspend. Appendix A, "Write State Machine States" on page 65 shows valid commands during erase suspend.

4.12.6 Status Register Error Checking

Using nested locking or program command sequences during erase suspend can introduce ambiguity into status register results.

Since locking changes require two-cycle command sequences, e.g., 60h followed by 01h to lock a block, following the Configuration Setup command (60h) with an invalid command produces a command sequence error (SR.4=1 and SR.5=1). If a Lock Block command error occurs during erase suspend, the device sets SR.4 and SR.5 to '1' even after the erase is resumed. When erase is

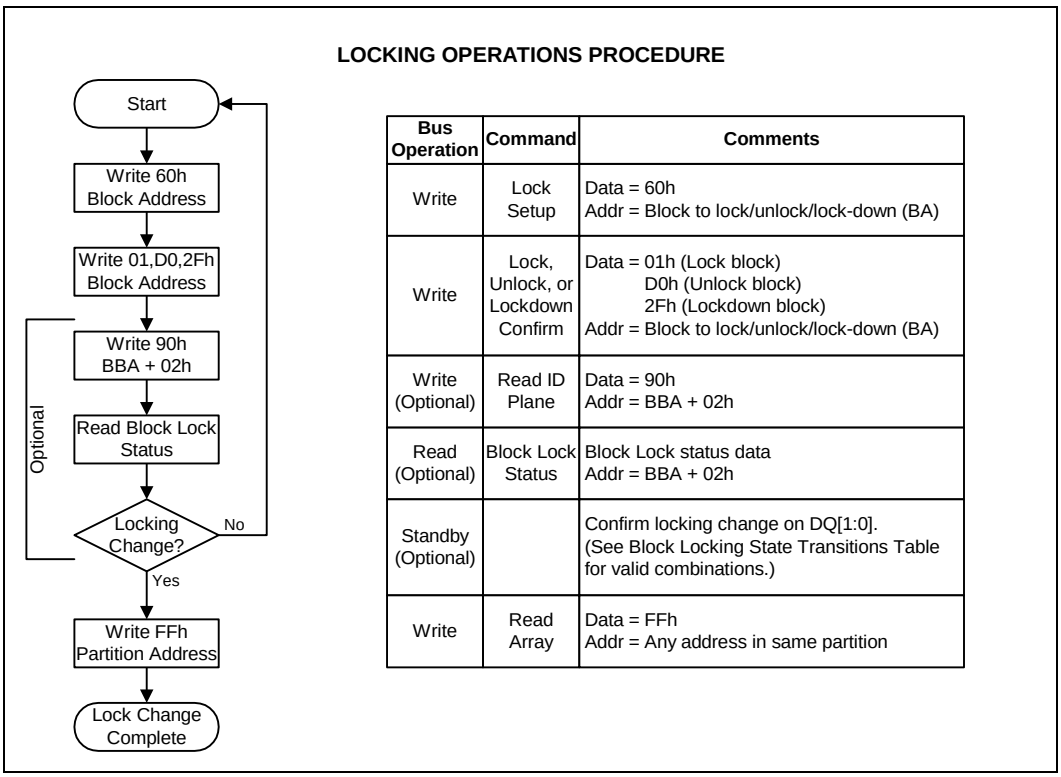
complete, possible errors during the erase cannot be detected via the status register because of the previous locking command error. A similar situation occurs if a program operation error is nested within an erase suspend.

4.12.7 WP# Lock-Down Control

WP# allows block lock-down to be overridden. Table 10, “Write Protection Truth Table” on page 29 defines the write protection methods.

WP# controls the lock-down function. WP# = V_{IL} protects locked-down blocks [011] from program, erase, and lock status changes. When WP# = V_{IH}, the block’s lock-down state reverts to locked [111]. A software command can then individually unlock a block [110] for erase or program operations. These blocks can then be re-locked [111] while WP# remains high. When WP# returns low, previously locked-down blocks are forced back to the lock-down state [011] regardless of changes made while WP# was high. Device reset or power-down resets all blocks to the locked state [101] or [001].

Figure 8. Locking Operations Flowchart



Bus Operation	Command	Comments
Write	Lock Setup	Data = 60h Addr = Block to lock/unlock/lock-down (BA)
Write	Lock, Unlock, or Lockdown Confirm	Data = 01h (Lock block) D0h (Unlock block) 2Fh (Lockdown block) Addr = Block to lock/unlock/lock-down (BA)
Write (Optional)	Read ID Plane	Data = 90h Addr = BBA + 02h
Read (Optional)	Block Lock Status	Block Lock status data Addr = BBA + 02h
Standby (Optional)		Confirm locking change on DQ[1:0]. (See Block Locking State Transitions Table for valid combinations.)
Write	Read Array	Data = FFh Addr = Any address in same partition

4.13 Protection Register

The 1.8 Volt Intel® Wireless Flash Memory includes a 128-bit protection register. This protection register is used to increase system security and/or for identification purposes. The protection register value can match the flash component to the system’s CPU or ASIC to prevent device substitution.

The lower 64 bits within the protection register are programmed by Intel with a unique number in each flash device. The upper 64 OTP bits within the protection register are left for the customer to program. Once programmed, the customer segment can be locked to prevent further programming. Note that the individual bits of the user segment of the protection register are OTP, not the register in total. The user may program each OTP bit individually, one at a time, if desired. Once the protection register is locked, however, the entire user segment is locked and no more user bits may be programmed.

The protection register shares some of the same internal flash resources as the parameter partition. Therefore, RWW is only allowed between the protection register and main partitions. Table 11 describes the operations allowed in the protection register, parameter partition, and main partition during RWW and RWE.

Table 11. Simultaneous Operations Allowed with the Protection Register

Protection Register	Parameter Partition Array Data	Main Partitions	Description
Read	See Description	Write/Erase	While programming or erasing in a main partition, the protection register may be read from any other partition. Reading the parameter partition data is not allowed if the protection register is being read from addresses within the parameter partition.
See Description	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the protection registers from parameter partition addresses is not allowed.
Read	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the protection registers in a partition that is *different* from the one being programed/erased, and also *different* from the parameter partition, is allowed.
Write	No Access Allowed	Read	While programming the protection register, reads are only allowed in the other main partitions. Access to the parameter partition is not allowed. This is because programming of the protection register can only occur in the parameter partition, so it will exist in status mode.
No Access Allowed	Write/Erase	Read	While programming or erasing the parameter partition, reads of the protection registers are not allowed in *any* partition. Reads in other main partitions are supported.

4.14 Read Protection Register

Writing the Read Identifier command allows the protection register data to be read 16 bits at a time from addresses shown in Table 7, “Device Identification Codes” on page 14. The protection register is read via the Read Identifier command and can be read in any partition.Writing the Read Array command returns the device to read array mode.

4.15 Program Protection Register

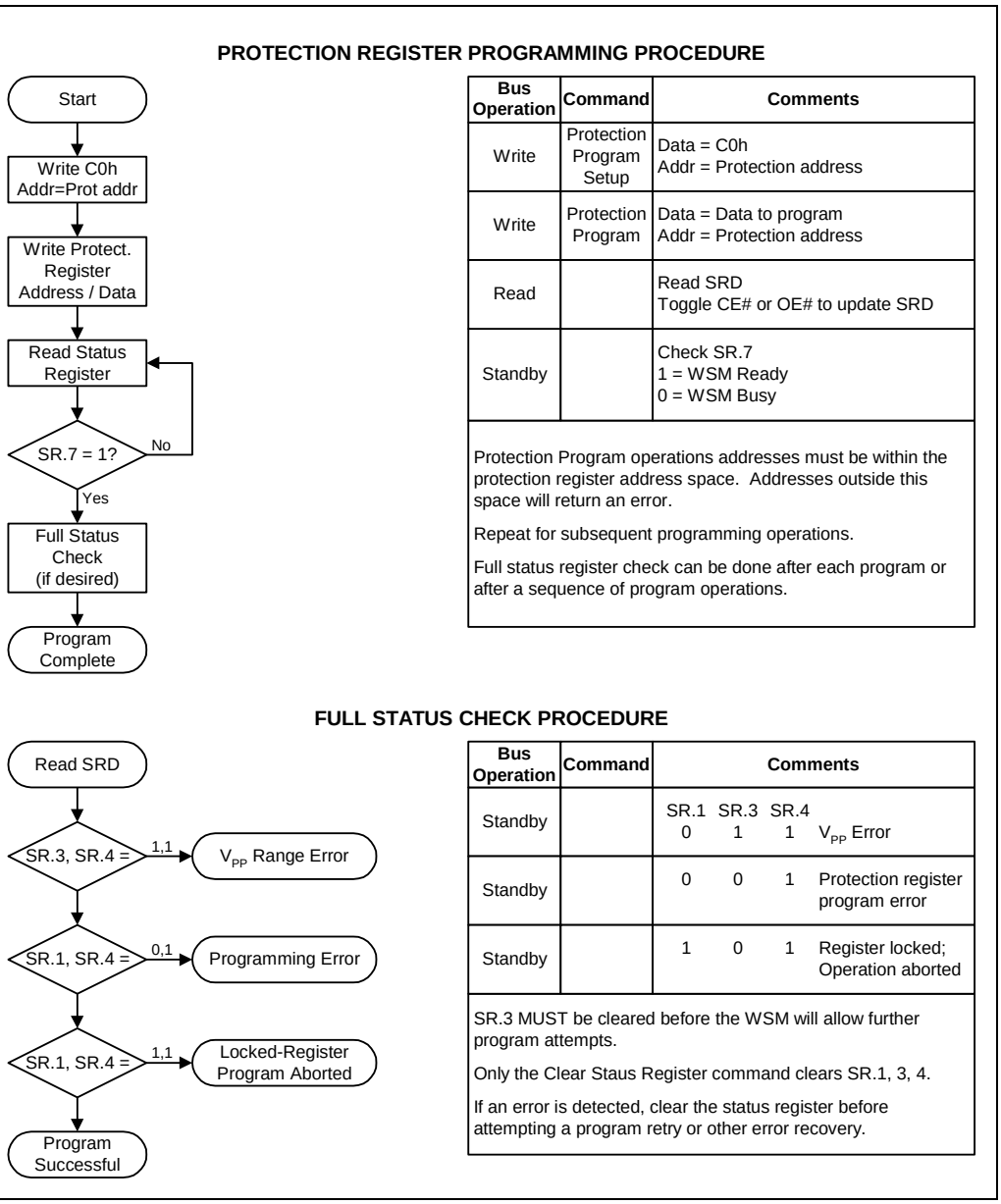
The Protection Program command should be issued only at the bottom partition followed by the data to be programed at the specified location. It programs the upper 64 bits of the protection register 16 bits at a time. Table 7, “Device Identification Codes” on page 14 shows allowable addresses. See also Figure 9, “Protection Register Programming Flowchart” on page 32. Issuing a Protection Program command outside the register’s address space results in a status register error (SR.4=1).

4.15.1 Lock Protection Register

PR-LK.0 is programmed to ‘0’ by Intel to protect the unique device number. PR-LK.1 can be programmed by the user to lock the user portion (upper 64 bits) of the protection register (see Figure 10, “Protection Register Locking). This bit is set using the Protection Program command to program “FFFDh” into PR-LK.

After PR-LK register bits are programmed (locked), the protection register’s stored values can’t be changed. Protection Program commands written to a locked section result in a status register error (SR.4=1, SR.5=1).

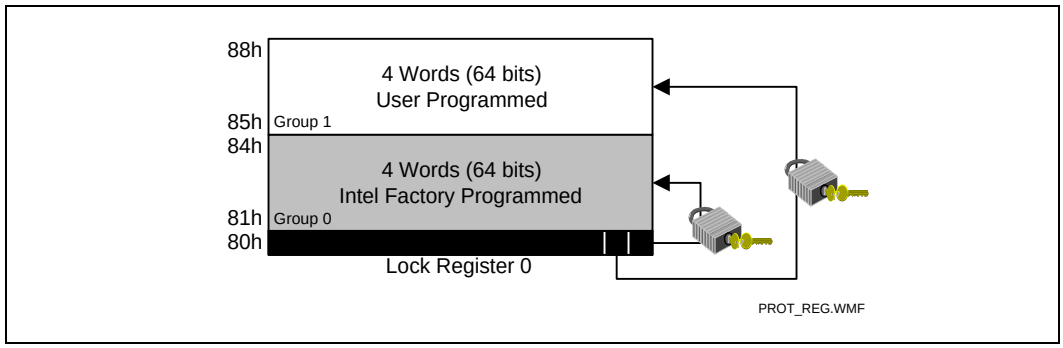
Figure 9. Protection Register Programming Flowchart



Bus Operation	Command	Comments
Write	Protection Program Setup	Data = C0h Addr = Protection address
Write	Protection Program	Data = Data to program Addr = Protection address
Read		Read SRD Toggle CE# or OE# to update SRD
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Protection Program operations addresses must be within the protection register address space. Addresses outside this space will return an error. Repeat for subsequent programming operations. Full status register check can be done after each program or after a sequence of program operations.		

Bus Operation	Command	Comments
Standby		SR.1 SR.3 SR.4 0 1 1 V_{PP} Error
Standby		0 0 1 Protection register program error
Standby		1 0 1 Register locked; Operation aborted
SR.3 MUST be cleared before the WSM will allow further program attempts. Only the Clear Staus Register command clears SR.1, 3, 4. If an error is detected, clear the status register before attempting a program retry or other error recovery.		

Figure 10. Protection Register Locking



4.16 Set Configuration Register

The Set Configuration Register command sets the burst order, frequency configuration, burst length, and other parameters.

A two-bus cycle command sequence initiates this operation. The configuration register data is placed on the lower 16 bits of the address bus (A[15:0]) during both bus cycles. The Set Configuration Register command is written along with the configuration data (on the address bus). This is followed by a second write that confirms the operation and again presents the configuration register data on the address bus. The configuration register data is latched on the rising edge of ADV#, CE#, or WE# (whichever occurs first). This command functions independently of the applied V_{PP} voltage. After executing this command, the device returns to read array mode. The configuration register's contents can be examined by writing the Read Identifier command and then reading location 05h.

Table 12. Configuration Register Definitions

Read Mode	Res'd	First Access Latency Count			WAIT Polarity	Data Output Config	WAIT Config	Burst Seq	Clock Config	Res'd	Res'd	Burst Wrap	Burst Length		
RM	R	LC2	LC1	LC0	WT	DOC	WC	BS	CC	R	R	BW	BL2	BL1	BL0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Bit	Name	Description	Notes[1]
15	**RM** Read Mode	0 = Synchronous Burst Reads Enabled 1 = Asynchronous Reads Enabled (Default)	2
14	**R**	Reserved	
13-11	**LC2-0** First Access Latency Count	000 = Code 0 (Reserved) 001 = Code 1 (Reserved) 010 = Code 2 011 = Code 3 100 = Code 4 101 = Code 5 110 = Code 6 (Reserved) 111 = Code 7 (Reserved) (Default)	
10	**WT** WAIT Signal Polarity	0 = WAIT signal is active low 1 = WAIT signal is active high (Default)	3
9	**DOC** Data Output Configuration	0 = Hold Data for One Clock 1 = Hold Data for Two Clock (Default)	
8	**WC** WAIT Configuration	0 = WAIT Asserted During Delay 1 = WAIT Asserted One Data Cycle before Delay (Default)	
7	**BS** Burst Sequence	0 = Intel Burst Order 1 = Linear Burst Order (Default)	
6	**CC** Clock Configuration	0 = Burst Starts and Data Output on Falling Clock Edge 1 = Burst Starts and Data Output on Rising Clock Edge (Default)	
5	**R**	Reserved	
4	**R**	Reserved	
3	**BW** Burst Wrap	0 = Wrap bursts within burst length set by CR.2–0 1 = Don't wrap accesses within burst length set by CR.2–0.(Default)	
2-0	**BL2-0** Burst Length	001 = 4-Word Burst 010 = 8-Word Burst 011 = Reserved 111 = Continuous Burst (Default)	4

NOTES:
1. Undocumented combinations of bits are reserved by Intel for future implementations.
2. Synchronous and page read mode configurations affect reads from main blocks and parameter blocks. Status register and configuration reads support single read cycles. CR.15=1 disables configuration set by CR.14-1.
3. Data is not ready when WAIT is active.
4. Set the synchronous burst length. In asynchronous page mode, the burst length equals four words.

4.16.1 Read Mode (CR.15)

All partitions support two high-performance read configurations: synchronous burst mode and asynchronous page mode (default). CR.15 sets the read configuration to one of these modes.

Status register, query, and identifier modes support only asynchronous and single-synchronous read operations.

4.16.2 First Access Latency Count (CR.13-11)

The First Access Latency Count (CR.13-11) configuration tells the device how many clocks must elapse from ADV#-inactive (V_{IH}) before the first data word should be driven onto its data pins. The input clock frequency determines this value. See Table 12, “Configuration Register Definitions” on page 34 for latency values. Figure 13, “First Access Latency Configuration” on page 37 shows data output latency from ADV#-active for different latencies.

Use these equations to calculate First Access Latency Count:

(1) {1/ Frequency} = CLK Period

(2) n (CLK Period) ≥ t_{AVQV} (ns) + $t_{ADD\text{-}DELAY}$ (ns) + t_{DATA} (ns)

(3) n-2 = First Access Latency Count (LC) *

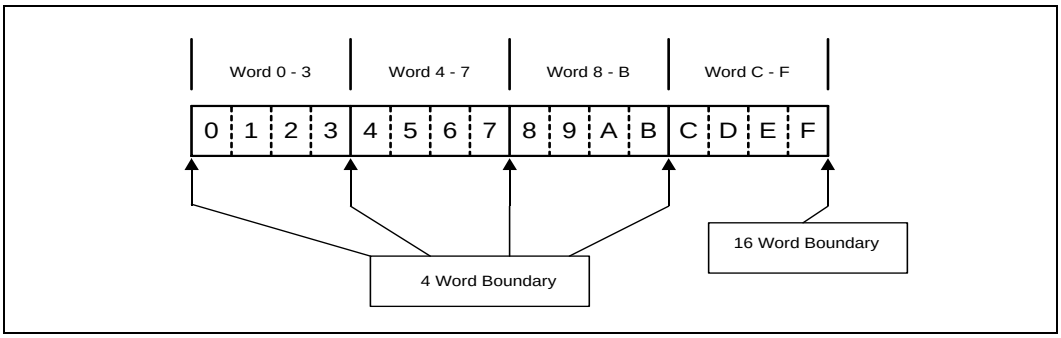
n: # of Clock periods (rounded up to the next integer)

*Must use LC = n - 1 when the starting address is **not** aligned to a four-word boundary and CR.3=1 (No Wrap).

Table 13. First Latency Count (LC)

LC Setting	Mode	Wrap	Aligned To 4-word Boundary	Wait Asserted on 16-Word Boundary Crossing
n-1	4 or 8	disabled	no	yes, occurs on the every occurrence
n-2	4 or 8	disabled	yes	no
n-2	4 or 8	enabled	no	no
n-2	4 or 8	enabled	yes	no
n-1	continuous	X	X	yes, occurs once

Figure 11. Word Boundary



NOTE:
1. The 16-word boundary is the end of the device sense word-line.

Parameters defined by CPU:

$t_{ADD-DELAY}$ = Clock to CE#, ADV#, or Address Valid whichever occurs last.
t_{DATA} = Data set up to Clock.

Parameters defined by flash:

t_{AVQV} = Address to Output Delay.

Example:

CPU Clock Speed = 52 MHz
$t_{ADD-DELAY}$ = 6 ns (typical speed from CPU) (max)
t_{DATA} = 4 ns (typical speed from CPU) (min)
t_{AVQV} = 70 ns (from AC Characteristic - Read Only Operations Table)
From Eq. (1): 1/52 (MHz) = 19.2 ns
From Eq. (2) n(19.2 ns) ≥ 70 ns + 6 ns + 4 ns
n(19.2 ns) ≥ 80 ns
n ≥ 80/19.2 = 4.17 = 5 (Integer)
From Eq. (3) n - 2 = 5 - 2 = 3
First Access Latency Count Setting to the CR is Code 3.
(Figure 12, “Data Output with LC Setting at Code 3” on page 37 displays example data)

The formula t_{AVQV} (ns) + $t_{ADD-DELAY}$ (ns) + t_{DATA} (ns) is also known as initial access time.

Figure 12 shows the data output available and valid after four clocks from ADV# going low in the first clock period with the LC setting at 3.

Figure 12. Data Output with LC Setting at Code 3

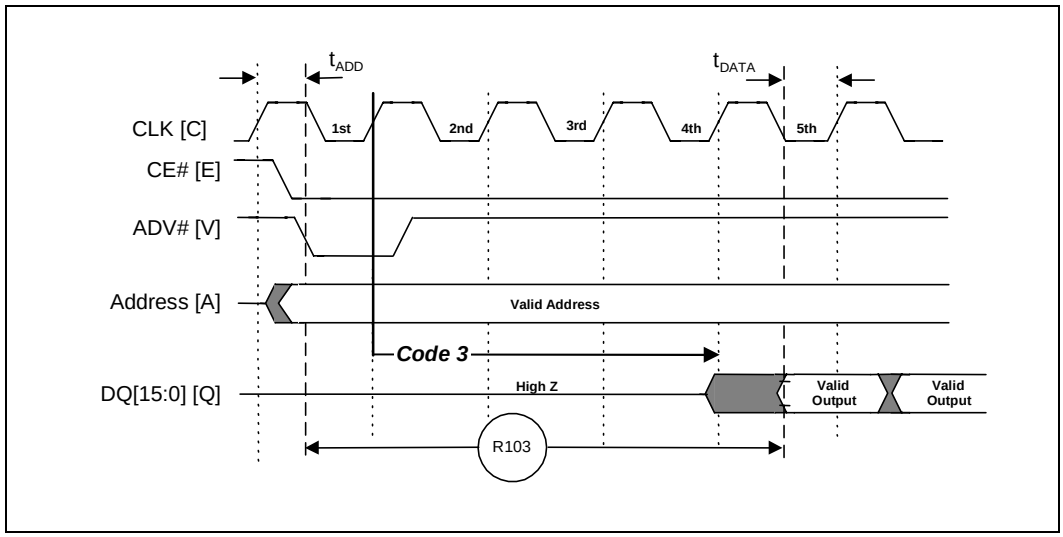
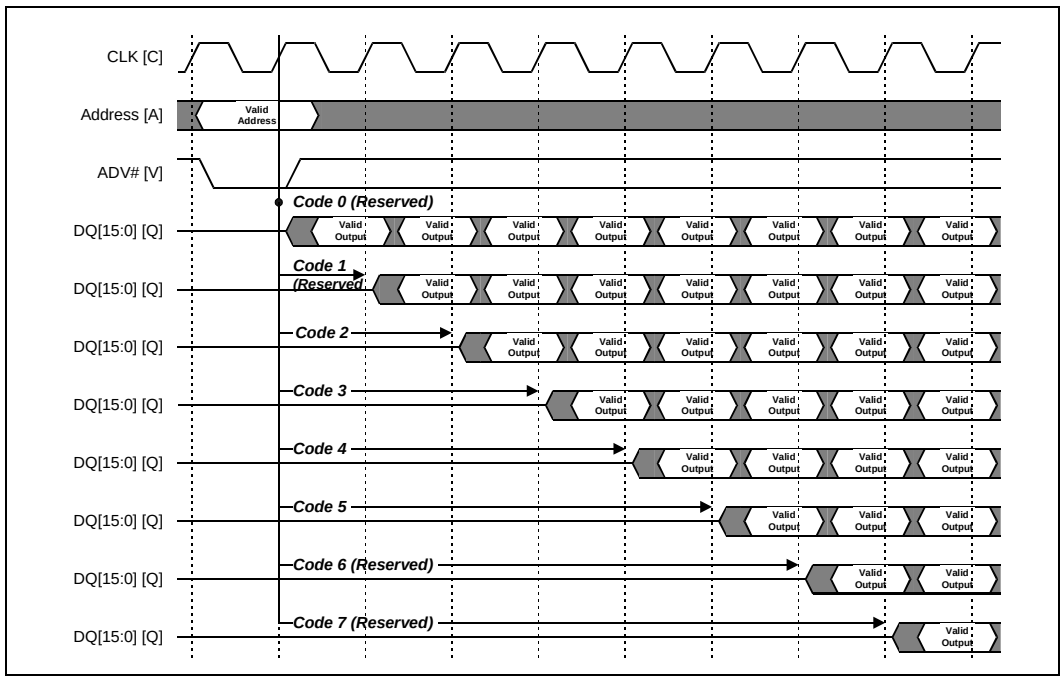


Figure 13. First Access Latency Configuration



4.16.3 WAIT Signal Polarity (CR.10)

The WAIT signal polarity is set by CR.10 (WT).

If the WT bit is cleared (CR.10=0), then WAIT is configured to be active low. This means that a ‘0’ on the WAIT signal indicates that data is not ready and the data bus contains invalid data. Conversely, if CR.10 is set (CR.10=1), then WAIT is active high. In either case, if WAIT is deasserted, then data is ready and valid.

WAIT is High-Z until the device is active (CE# = V_{IL}). In synchronous read array mode, when the device is active (CE# = V_{IL}) and data is valid, CR.10 determines if WAIT goes to V_{OH} or V_{OL}. The WAIT signal is only “deasserted” once data is valid on the bus. Invalid data drives the WAIT signal to the asserted state. WAIT is asserted during asynchronous page mode reads.

4.16.4 WAIT Signal Function

The WAIT signal indicates data valid when the device is operating in synchronous burst mode (CR.15=0), and when addressing a partition that is currently in read array mode. The WAIT signal is only “deasserted” when data is valid on the bus.

When the device is operating in synchronous non-read array mode, such as read status, read ID, or read query, WAIT is set to an “asserted” state as determined by CR.10. Figure 25, “WAIT Signal in Synchronous Non-Read Array Operation Waveform” on page 58 displays WAIT Signal in Synchronous Non-Read Array Operation Waveform.

When the device is operating in asynchronous page mode or asynchronous single word read mode, WAIT is set to an “asserted” state as determined by CR.10. See Figure 26, “WAIT Signal in Asynchronous Page-Mode Read Operation Waveform” on page 59 and Figure 27, “WAIT Signal in Asynchronous Single-Word Read Operation Waveform” on page 60.

From a system perspective, the WAIT signal will be in the asserted state (based on CR.10) when the device is operating in synchronous non-read array mode (such as Read ID, Read Query, or Read Status), or if the device is operating in asynchronous mode (CR.15=1). In these cases, the system software should ignore (mask) the WAIT signal, as it does not convey any useful information about the validity of what is appearing on the data bus.

Systems may tie several components’ WAIT signals together.

4.16.5 Data Output Configuration (CR.9)

The Data Output Configuration bit (CR.9) determines whether a data word remains valid on the data bus for one or two clock cycles. The processor’s minimum data set-up time and the flash memory’s clock-to-data output delay determine whether one or two clocks are needed.

If the Data Output Configuration is set at one-clock data hold, this corresponds to a one-clock data cycle; if the Data Output Configuration is set at two-clock data hold, this corresponds to a two-clock data cycle. This configuration bit’s setting depends on the system and CPU characteristics. Refer to Figure 14, “Data Output Configuration with WAIT Signal Delay” on page 39 for clarification.

A method for determining what this configuration should be set at is shown below.

To set the device at one clock data hold for subsequent reads, the following condition must be satisfied:

$$t_{CHQV}\ (ns) + t_{DATA}\ (ns) \leq \text{One CLK Period (ns)}$$

As an example, a clock frequency of 52 MHz will be used. The clock period is 19.2 ns. This data is applied to the formula above for the subsequent reads assuming the data output hold time is one clock:

$$14\ ns + 4\ ns \leq 19.2\ ns$$

This equation is satisfied and data output will be available and valid at every clock period. If t_{DATA} is long, hold for two cycles.

Now assume the clock frequency is 66 MHz. This corresponds to a 15 ns period. The initial access time is calculated to be 80 ns (Latency Count = Code 4). This condition satisfies t_{AVQV} (ns) + $t_{ADD-DELAY}$ (ns) + t_{DATA} (ns) = 70 ns + 6 ns + 4 ns = 80 ns, as shown above in the First Access Latency Count equations. However, the data hold time of one clock violates the one-clock data hold condition:

$$t_{CHQV} \text{ (ns)} + t_{DATA} \text{ (ns)} \leq \text{One CLK Period}$$

14 ns + 4 ns = 18 ns is not less than one clock period of 15 ns. To satisfy the formula above, the data output hold time must be set at 2 clocks to correctly allow for data output setup time. This formula is also satisfied if the CPU has t_{DATA} (ns) ≤ 1 ns, which yields:

$$14 \text{ ns} + 1 \text{ ns} \leq 15 \text{ ns}$$

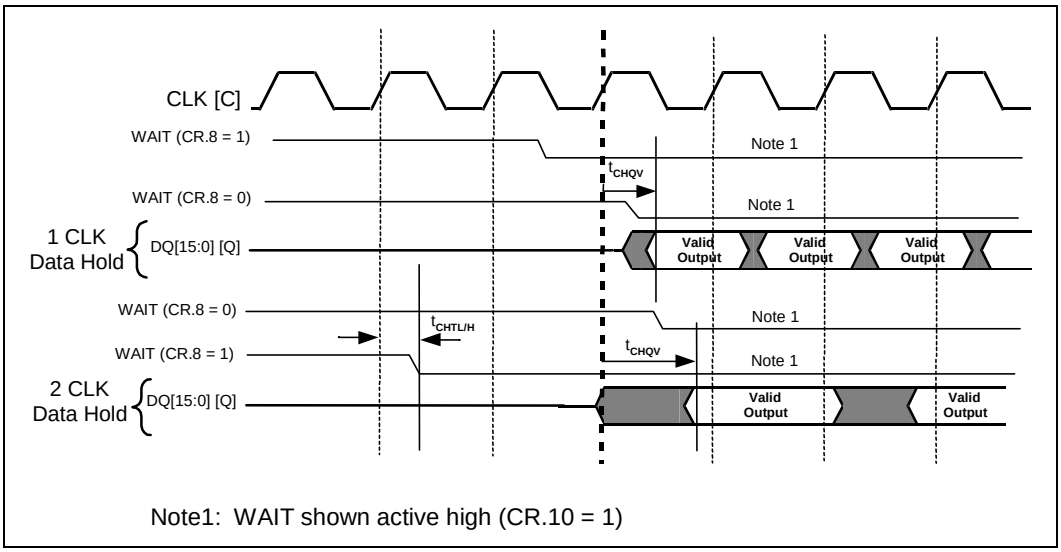
In page-mode reads, the initial access time can be determined by the formula:

$$t_{ADD-DELAY} \text{ (ns)} + t_{DATA} \text{ (ns)} + t_{AVQV} \text{ (ns)}$$

and subsequent reads in page mode are defined by:

$$t_{APA} \text{ (ns)} + t_{DATA} \text{ (ns)} \qquad \text{(minimum time)}$$

Figure 14. Data Output Configuration with WAIT Signal Delay



4.16.6 WAIT Delay Configuration (CR.8)

The WAIT configuration bit (CR.8) controls WAIT signal delay behavior for all synchronous read array modes. Its setting depends on the system and CPU characteristics. The WAIT can be asserted either during or one data cycle before a valid output.

In synchronous linear read array (no-wrap mode CR.3=1) of 4-, 8-, or continuous-word burst mode, an output delay may occur when a burst sequence crosses its first device-row boundary (16-word boundary). If the burst start address is four-word boundary aligned, the delay will not occur. If the start address is misaligned to a four-word boundary, the delay occurs once per burst-mode read sequence. The WAIT signal informs the system of this delay.

4.16.7 Burst Sequence Configuration (CR.7)

The burst sequence specifies the synchronous burst mode data order (Table 14, “Sequence and Burst Length” on page 41). Set this bit for linear or Intel burst order. Continuous burst mode supports only linear burst order.

When operating in a linear burst mode, either 4-word or 8-word burst length with the burst wrap bit (CR.3) set, or in continuous burst mode, the device may incur an output delay when the burst sequence crosses the first 16-word boundary. (See Figure 11, “Word Boundary” on page 36 for word boundary description.) This is dependent on the starting address. If the starting address is aligned to a four-word boundary, the delay will not occur. If the starting address is the end of a four-word boundary, the output delay will be one clock cycle less than the First Access Latency Count; this is the worst-case delay. The delay will take place only once and will not happen if the burst sequence does not cross a 16-word boundary. The WAIT pin informs the system of this delay. See Figure 22, “Single Synchronous Read Operation Waveform” on page 55 through Figure 24, “WAIT Functionality for EOWL (End of Word Line) Condition Waveform” on page 57 for timing diagrams of WAIT functionality.

Table 14. Sequence and Burst Length

Start Addr. (Dec)	Wrap CR.3= 0	No Wrap CR.3= 1	Burst Addressing Sequence (Dec)				
			4-Word Burst Length CR.2–0 = 001		8-Word Burst Length CR.2–0 = 010		Continuous Burst CR.2–0 = 111
			Linear	Intel	Linear	Intel	Linear
0	0		0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-...
1	0		1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7-...
2	0		2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8-...
3	0		3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9-...
4	0				4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3-	4-5-6-7-8-9-10...
5	0				5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7-8-9-10-11...
6	0				6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8-9-10-11-12-...
7	0				7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13...
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
14	0						14-15-16-17-18-19-20-...
15	0						15-16-17-18-19-20-21-...
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0		1	0-1-2-3	NA	0-1-2-3-4-5-6-7	NA	0-1-2-3-4-5-6-...
1		1	1-2-3-4	NA	1-2-3-4-5-6-7-8	NA	1-2-3-4-5-6-7-...
2		1	2-3-4-5	NA	2-3-4-5-6-7-8-9	NA	2-3-4-5-6-7-8-...
3		1	3-4-5-6	NA	3-4-5-6-7-8-9-10	NA	3-4-5-6-7-8-9-...
4		1			4-5-6-7-8-9-10-11	NA	4-5-6-7-8-9-10...
5		1			5-6-7-8-9-10-11-12	NA	5-6-7-8-9-10-11...
6		1			6-7-8-9-10-11-12-13	NA	6-7-8-9-10-11-12-...
7		1			7-8-9-10-11-12-13-14	NA	7-8-9-10-11-12-13...
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
14		1					14-15-16-17-18-19-20-...
15		1					15-16-17-18-19-20-21-...

4.16.8 Clock Configuration (CR.6)

Clock-edge facilitates easy memory interface to a wide range of burst CPUs. Clock configuration sets the device to start a burst cycle, output data, and assert WAIT on the clock's rising or falling edge.

4.16.9 Burst Wrap (CR.5)

The burst wrap bit determines whether 4-word or 8-word burst accesses wrap within the burst-length boundary or whether they cross word-length boundaries to perform linear accesses. No-wrap mode (CR.3=1) enables WAIT to hold off the system processor, as it does in the continuous burst mode, until valid data is available. In the no-wrap mode (CR.3=0), the device operates similar to continuous linear burst mode but consumes less power during 4 or 8-word bursts.

For example, if CR.3=0 (wrap mode) and CR.2–0 = 1h (4-word burst), possible linear burst sequences are 0-1-2-3, 1-2-3-0, 2-3-0-1, 3-0-1-2.

If CR.3=1 (no-wrap mode) and CR.2–0 = 1h (4-word burst length), then possible linear burst sequences are 0-1-2-3, 1-2-3-4, 2-3-4-5, and 3-4-5-6. CR.3=1 not only enables limited non-aligned sequential bursts, but also reduces power by minimizing the number of internal read operations.

Setting CR.2-0 bits for continuous linear burst mode (7h) also achieves the above 4-word burst sequences. However, significantly more power may be consumed. The 1-2-3-4 sequence, for example, will consume power during the initial access, again during the internal pipeline lookup as the processor reads word 2, and possibly again, depending on system timing, near the end of the sequence as the device pipelines the next 4-word sequence. CR.3=1 while in 4-word burst mode (no wrap mode) reduces this excess power consumption.

4.16.10 Burst Length (CR.2-0)

The burst length is the number of words the device outputs in a synchronous read access. 4-, 8-, and continuous burst lengths are supported. In 4- or 8-word burst configuration, the burst wrap bit (CR.3) determines if burst accesses wrap within word-length boundaries or whether they cross word-length boundaries to perform a linear access. Once an address is given, the device will output data until it reaches the end of its burstable address space. Continuous burst access are linear only and do not wrap within word-length boundaries. (see Table 14, “Sequence and Burst Length” on page 41).

5.0 Program and Erase Voltages

The 1.8 Volt Intel® Wireless Flash memory provides in-system program and erase at V_{PP1}. For factory programming, it also includes a low-cost, backward-compatible 12 V programming feature. The EFP feature can also be used to greatly improve factory program performance.

5.1 Factory Program Mode

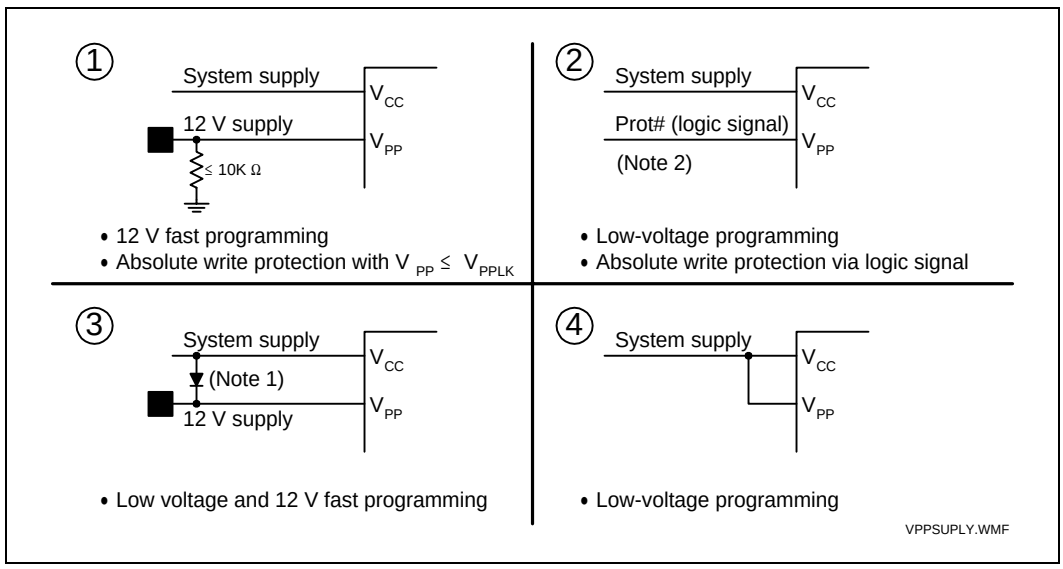
The standard factory programming mode uses the same commands and algorithm as the Word Program mode (40h/10h). When V_{PP} is at V_{PP1}, program and erase currents are drawn through VCC. Note that if VPP is driven by a logic signal, V_{PP1} must remain above the V_{PP1}Min value to perform in-system flash modifications. When VPP is connected to a 12 V power supply, the device draws program and erase current directly from VPP. This eliminates the need for an external switching transistor to control the V_{PP} voltage. Figure 15, “Example VPP Power Supply Configuration shows examples of flash power supply usage in various configurations.

The 12 V V_{PP} mode enhances programming performance during the short time period typically found in manufacturing processes; however, it is not intended for extended use. 12 V may be applied to V_{PP} during program and erase operations as specified in Section 7.2, “Extended Temperature Operation” on page 47. VPP may be connected to 12 V for a total of t_{PPH} hours maximum. Stressing the device beyond these limits may cause permanent damage.

5.2 Programming Voltage Protection (V_{PP})

In addition to the flexible block locking, holding the V_{PP} programming voltage low can provide absolute hardware write protection of all flash-device blocks. If V_{PP} is below V_{PPLK}, program or erase operations will result in an error displayed in SR.3.

Figure 15. Example VPP Power Supply Configuration



NOTE:
1. If the V_{CC} supply can sink adequate current, an appropriately valued resistor can be used.

6.0 Power Consumption

1.8 Volt Intel® Flash memory devices have a layered approach to power savings that can significantly reduce overall system power consumption. The APS feature reduces power consumption when the device is selected but idle. If CE# is de-asserted, the memory enters its standby mode, where current consumption is even lower. Asserting RST# provides current savings similar to standby mode. The combination of these features can minimize memory power consumption, and therefore, overall system power consumption.

6.1 Active Power

With CE# at V_{IL} and RST# at V_{IH}, the device is in the active mode. Refer to the Section 7.4, "DC Characteristics" on page 48, for I_{CC} values.

6.2 Automatic Power Savings

APS mode provides low-power operation during read mode. After data is read from the memory array and the address lines are quiescent, APS circuitry places the device in a mode where typical current is comparable to I_{CCS}. The flash stays in this static state with outputs valid, OE# low, until a new location is read.

6.3 Standby Power

With CE# at V_{IH} and the device in read mode, the flash memory is in standby mode, which disables most device circuitry and substantially reduces power consumption. Outputs are placed in a high-impedance state independent of the OE# signal state. If CE# transitions to V_{IH} during erase or program operations, the device will continue to perform the operation and consume corresponding active power until the operation is complete.

6.4 Power-Up/Down Operation

The device is protected against accidental block erasure or programming during power transitions. It does not matter whether V_{PP} or V_{CC} powers-up first. Power supply sequencing is not required.

6.4.1 System Reset and RST#

The use of RST# during system reset is important with automated program/erase devices since the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization will not occur because the flash memory may be providing status information instead of array data. Intel recommends connecting RST# to the system CPU RESET# signal to allow proper CPU/flash initialization at system reset.

System designers must guard against spurious writes when VCC voltages are above V_{LKO}. Since both WE# and CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until RST# is brought to V_{IH}, regardless of its control input states. By

holding the device in reset (RST# connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

6.4.2 VCC, VPP, and RST# Transitions

The CUI latches commands issued by system software and is not altered by VPP or CE# transitions or WSM actions. Read array mode is its power-up default state after exit from reset mode or after VCC transitions above V_{LKO} (Lockout voltage).

After completing program or block erase operations (even after VPP transitions below V_{PPLK}), the Read Array command must reset the CUI to read array mode if flash memory array access is desired.

6.4.3 Power Supply Decoupling

When the device is accessed, many internal conditions change. Circuits are enabled to charge pumps and switch voltages. This internal activity produces transient noise. To minimize the effect of this transient noise, device decoupling capacitors are required. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between each power (VCC, VCCQ, VPP), and ground (VSS, VSSQ) signal. High-frequency, inherently low-inductance capacitors should be as close as possible to package signals.

7.0 Electrical Specifications

7.1 Absolute Maximum Ratings

Parameter	Note	Maximum Rating
Temperature under Bias		–40 °C to +85 °C
Storage Temperature		–65 °C to +125 °C
Voltage On Any Pin (except VCC, VCCQ, VPP)	1	–0.5 V to +2.45 V
VPP Voltage	1,2,3	–0.2 V to +14 V
VCC and VCCQ Voltage	1	–0.2 V to +2.45 V
Output Short Circuit Current	4	100 mA

NOTES:
1. All specified voltages are with respect to VSS. Minimum DC voltage is –0.5 V on input/output pins and –0.2 V on VCC and VPP pins. During transitions, this level may undershoot to –2.0 V for periods <20 ns which, during transitions, may overshoot to V_{CC} +2.0 V for periods < 20 ns.
2. Maximum DC voltage on VPP may overshoot to +14.0 V for periods < 20 ns.
3. V_{PP} program voltage is normally V_{PP1}. V_{PP} can be 12V ± 0.6 V for 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase.
4. Output shorted for no more than one second. No more than one output shorted at a time.

Notice: This datasheet contains preliminary information on new products in production. Specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

7.2 Extended Temperature Operation

Symbol	Parameter[1]		Note	Min	Nom	Max	Unit
T_A	Operating Temperature			–40	25	85	°C
V_{CC}	V_{CC} Supply Voltage		3	1.7	1.80	1.95	V
V_{CCQ}	I/O Supply Voltage		3	1.7	1.80	2.24	V
V_{PP1}	V_{PP} Voltage Supply (Logic Level)		2	0.90	1.80	1.95	V
V_{PP2}	Factory Programming V_{PP}		2	11.4	12.0	12.6	V
t_{PPH}	Maximum V_{PP} Hours	V_{PP} = 12 V	2			80	Hours
Block Erase Cycles	Main and Parameter blocks	$V_{PP} \le V_{CC}$	2	100,000			Cycles
	Main Blocks	V_{PP} = 12 V	2			1000	Cycles
	Parameter Blocks	V_{PP} = 12 V	2			2500	Cycles

NOTES:
1. See DC Characteristics tables for voltage-range specific specifications.
2. VPP is normally V_{PP1}. VPP can be connected to 11.4 V–12.6 V for 1000 cycles on main blocks for extended temperatures and 2500 cycles at extended temperature on parameter blocks.
3. Contact your Intel field representative for enhanced V_{CC}/V_{CCQ} operations down to 1.65 V.

7.3 Capacitance

T_A = +25 °C, f = 1 MHz

Sym	Parameter[1]	32/64 Mbit		128 Mbit		Unit	Condition
		Typ	Max	Typ	Max		
C_{IN}	Input Capacitance	6	8	8	9	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	8	12	pF	V_{OUT} = 0.0 V
C_{CE}	CE# Input Capacitance	10	12	10	12	pF	V_{IN} = 0.0 V

NOTE: Sampled, not 100% tested.

7.4 DC Characteristics

Sym	Parameter [1]		Note	32/64 Mbit		128 Mbit		Unit	Test Condition	
				Typ	Max	Typ	Max			
I_{LI}	Input Load Current				±1		±1	µA	$V_{CC} = V_{CC}Max$ $V_{CCQ} = V_{CCQ}Max$ $V_{IN} = V_{CCQ}$ or GND	
I_{LO}	Output Leakage Current	DQ[15:0]			±1		±1	µA	$V_{CC} = V_{CC}Max$ $V_{CCQ} = V_{CCQ}Max$ $V_{IN} = V_{CCQ}$ or GND	
I_{CCS}	V_{CC} Standby Current			5	18	5	25	µA	$V_{CC} = V_{CC}Max$ $V_{CCQ} = V_{CCQ}Max$ CE# = V_{CC} RST# = V_{CC} or GND	
I_{CCR}	Average V_{CC} Read Current	Synchronous CLK = 40 MHz	2, 3	6	13	6	13	mA	Burst length = 4	$V_{CC} = V_{CC}Max$ CE# = V_{IL} OE# = V_{IH} Inputs = V_{IH} or V_{IL}
				8	14	8	14	mA	Burst length = 8	
				11	20	11	20	mA	Burst length = Continuous	
		Synchronous CLK = 52 MHz	2, 3	7	16	7	16	mA	Burst length = 4	
				10	18	10	18	mA	Burst length = 8	
				13	25	13	25	mA	Burst length = Continuous	
I_{CCW}	V_{CC} Program Current		4, 5	18	40	18	40	mA	$V_{PP} = V_{PP1,}$ Program in Progress	
				8	15	8	15	mA	$V_{PP} = V_{PP2,}$ Program in Progress	
I_{CCE}	V_{CC} Block Erase Current		4, 6	18	40	18	40	mA	$V_{PP} = V_{PP1,}$ Block Erase in Progress	
				8	15	8	15	mA	$V_{PP} = V_{PP2,}$ Block Erase in Progress	
I_{CCWS}	V_{CC} Program Suspend Current		4, 7	5	18	5	25	µA	CE# = $V_{CC,}$ Program Suspended	
I_{CCES}	V_{CC} Erase Suspend Current		4, 7	5	18	5	25	µA	CE# = $V_{CC,}$ Erase Suspended	
I_{PPS} ($I_{PPWS,}$ I_{PPES})	V_{PP} Standby Current V_{PP} Program Suspend Current V_{PP} Erase Suspend Current		4	0.2	5	0.2	5	µA	$V_{PP} \leq V_{CC}$	
I_{PPR}	V_{PP} Read Current			2	15	2	15	µA	$V_{PP} \leq V_{CC}$	
I_{PPW}	V_{PP} Program Current		4	0.05	0.10	0.05	0.10	mA	$V_{PP} = V_{PP1,}$ Program in Progress	
				8	22	8	22		$V_{PP} = V_{PP2,}$ Program in Progress	
I_{PPE}	V_{PP} Erase Current		4	0.05	0.10	0.05	0.10	mA	$V_{PP} = V_{PP1,}$ Erase in Progress	
				8	22	8	22		$V_{PP} = V_{PP2,}$ Erase in Progress	

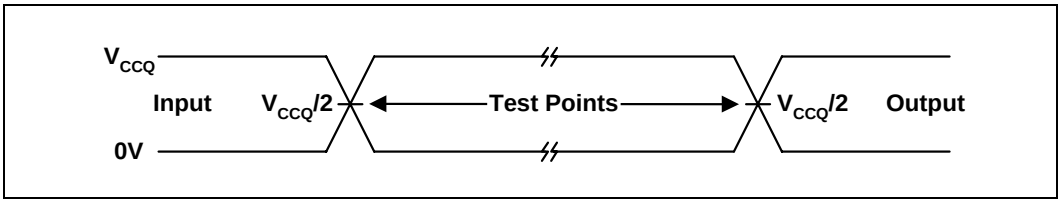
DC Characteristics, continued

Sym	Parameter	Note	Min	Typ	Max	Unit	Test Condition
V_{IL}	Input Low Voltage	8	0		0.4	V	
V_{IH}	Input High Voltage	8	V_{CCQ} – 0.4		V_{CCQ}	V	
V_{OL}	Output Low Voltage				0.1	V	$V_{CC} = V_{CC}Min$ $V_{CCQ} = V_{CCQ}Min$ I_{OL} = 100 µA
V_{OH}	Output High Voltage		V_{CCQ} – 0.1			V	$V_{CC} = V_{CC}Min$ $V_{CCQ} = V_{CCQ}Min$ I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lock-Out Voltage	9			0.4	V	
V_{LKO}	V_{CC} Lock Voltage		1.0			V	

NOTES:
1. All currents are RMS unless noted. Typical values at typical V_{CC}, T_A = +25 °C.
2. APS reduces I_{CCR} to approximately standby levels in static operation.
3. CR.3 determines whether 4- or 8-word burst accesses wrap within the burst-length boundary or whether they cross word-length boundaries to perform linear accesses. In the no-wrap mode (CR.3=1), the device operates similar to continuous linear burst mode but consumes less power.
4. Sampled, not 100% tested.
5. V_{CC} read + program current is the summation of V_{CC} read and V_{CC} program currents.
6. V_{CC} read + erase current is the summation of V_{CC} read and V_{CC} block erase currents.
7. I_{CCES} is specified with device deselected. If device is read while in erase suspend, current draw is sum of I_{CCES} and I_{CCR}.
8. V_{IL} can undershoot to –0.4 V and V_{IH} can overshoot to V_{CCQ}+0.4 V for durations of 20 ns or less.
9. Erase and program operations are inhibited when $V_{PP} \leq V_{PPLK}$ and not guaranteed outside valid V_{PP1} and V_{PP2} ranges.

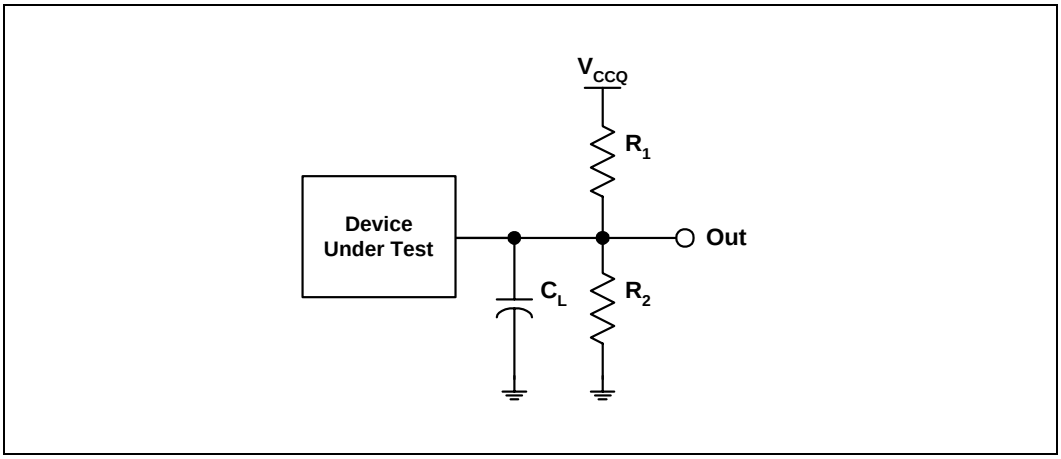
7.5 AC I/O Test Conditions

Figure 16. AC Input/Output Reference Waveform



NOTE: AC test inputs are driven at V_{CCQ} for a Logic '1' and 0.0 V for a Logic '0'. Input timing begins, and output timing ends, at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5 ns. Worst case speed conditions are when $V_{CC} = V_{CC}$Min.

Figure 17. Transient Equivalent Testing Load Circuit



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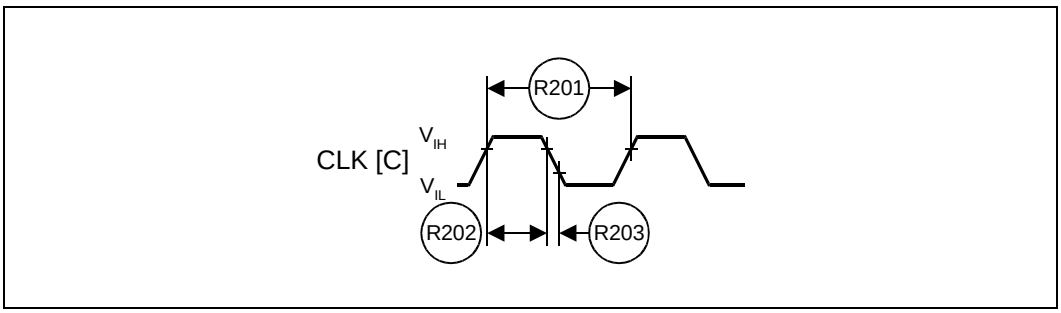
NOTE: See table for component values.

Test configuration component value for worst case speed conditions

Test Configuration	C_L (pF)	R_1 (Ω)	R_2 (Ω)
V_{CCQ}Min Standard Test	30	16.7K	16.7K

NOTE: C_L includes jig capacitance.

Figure 18. Clock Input AC Waveform



7.6 AC Read Characteristics

#	Sym	Parameter [1,2]	Notes	32/64 Mbit				128 Mbit		Unit
				–70		–85		-90		
				Min	Max	Min	Max	Min	Max	
Asynchronous Specifications										
R1	t_{AVAV}	Read Cycle Time		70		85		90		ns
R2	t_{AVQV}	Address to Output Delay			70		85		90	ns
R3	t_{ELQV}	CE# Low to Output Delay			70		85		90	ns
R4	t_{GLQV}	OE# Low to Output Delay	4		30		30		30	ns
R5	t_{PHQV}	RST# High to Output Delay			150		150		150	ns
R6	t_{ELQX}	CE# Low to Output in Low-Z	5	0		0		0		ns
R7	t_{GLQX}	OE# Low to Output in Low-Z	4,5	0		0		0		ns
R8	t_{EHQZ}	CE# High to Output in High-Z	5		20		25		25	ns
R9	t_{GHQZ}	OE# High to Output in High-Z	4,5		20		25		25	ns
R10	t_{OH}	CE# (OE#) High to Output in Low-Z	4,5	0		0		0		ns
Latching Specifications										
R101	t_{AVVH}	Address Setup to ADV# High		10		10		10		ns
R102	t_{ELVH}	CE# Low to ADV# High		10		10		10		ns
R103	t_{VLQV}	ADV# Low to Output Delay			70		85		90	ns
R104	t_{VLVH}	ADV# Pulse Width Low		10		10		10		ns
R105	t_{VHVL}	ADV# Pulse Width High		10		10		10		ns
R106	t_{VHAX}	Address Hold from ADV# High	3	9		9		9		ns
R108	t_{APA}	Page Address Access Time			20		25		30	ns
Clock Specifications										
R200	f_{CLK}	CLK Frequency			52		40		40	MHz
R201	t_{CLK}	CLK Period		19		25		25		ns
R202	$t_{CH/L}$	CLK High or Low Time		5		5		5		ns
R203	t_{CHCL}	CLK Fall or Rise Time			3		3		3	ns

#	Sym	Parameter (1,2)	Notes	32/64 Mbit				128 Mbit		Unit
				–70		–85		-90		
				Min	Max	Min	Max	Min	Max	
Synchronous Specifications										
R301	t_{AVCH}	Address Valid Setup to CLK		9		9		9		ns
R302	t_{VLCH}	ADV# Low Setup to CLK		10		10		10		ns
R303	t_{ELCH}	CE# Low Setup to CLK		9		9		9		ns
R304	t_{CHQV}	CLK to Output Valid			14		18		18	ns
R305	t_{CHQX}	Output Hold from CLK		3.5		3.5		3.5		ns
R306	t_{CHAX}	Address Hold from CLK	3	10		10		10		ns
R307	t_{CHTV}	CLK to WAIT Valid			14		18		18	ns
R308	t_{ELTV}	CE# Low to WAIT Valid	6		14		18		18	ns
R309	t_{EHTZ}	CE# High to WAIT High-Z	5,6		20		25		25	ns
R310	t_{EHEL}	CE# Pulse Width High	6	15		20		20		ns

NOTES:
1. See Figure 16, “AC Input/Output Reference Waveform” on page 50 for timing measurements and maximum allowable input slew rate.
2. AC specifications assume the data bus voltage is less than or equal to V_{CCQ} when a read operation is initiated.
3. Address hold in synchronous burst-mode is defined as t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.
4. OE# may be delayed by up to t_{ELQV}– t_{GLQV} after the falling edge of CE# without impact to t_{ELQV}.
5. Sampled, not 100% tested.
6. Applies only to subsequent synchronous reads.

Figure 19. Asynchronous Read Operation Waveform

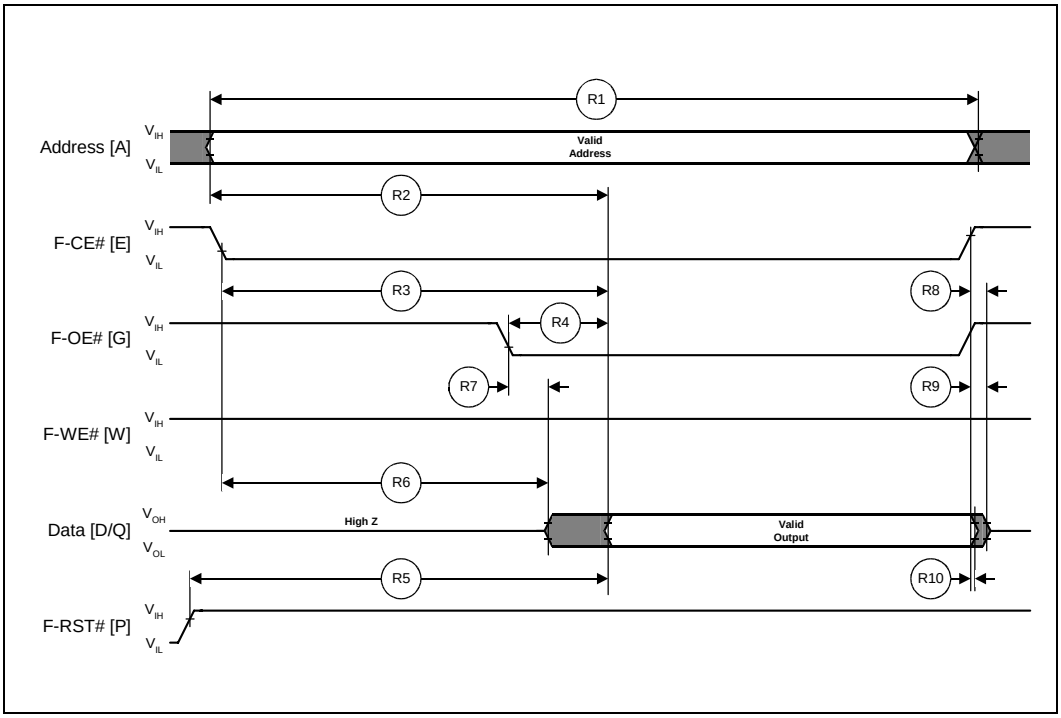


Figure 20. Latched Asynchronous Read Operation Waveform

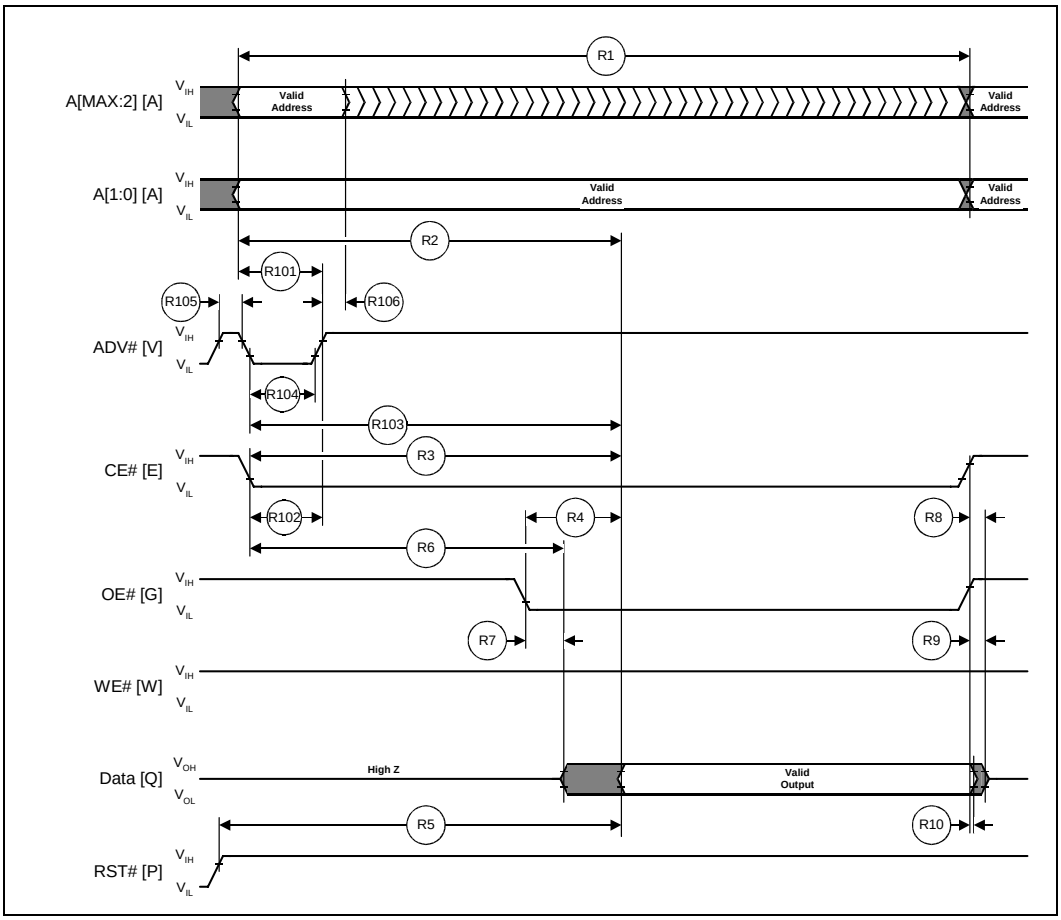


Figure 21. Page-Mode Read Operation Waveform

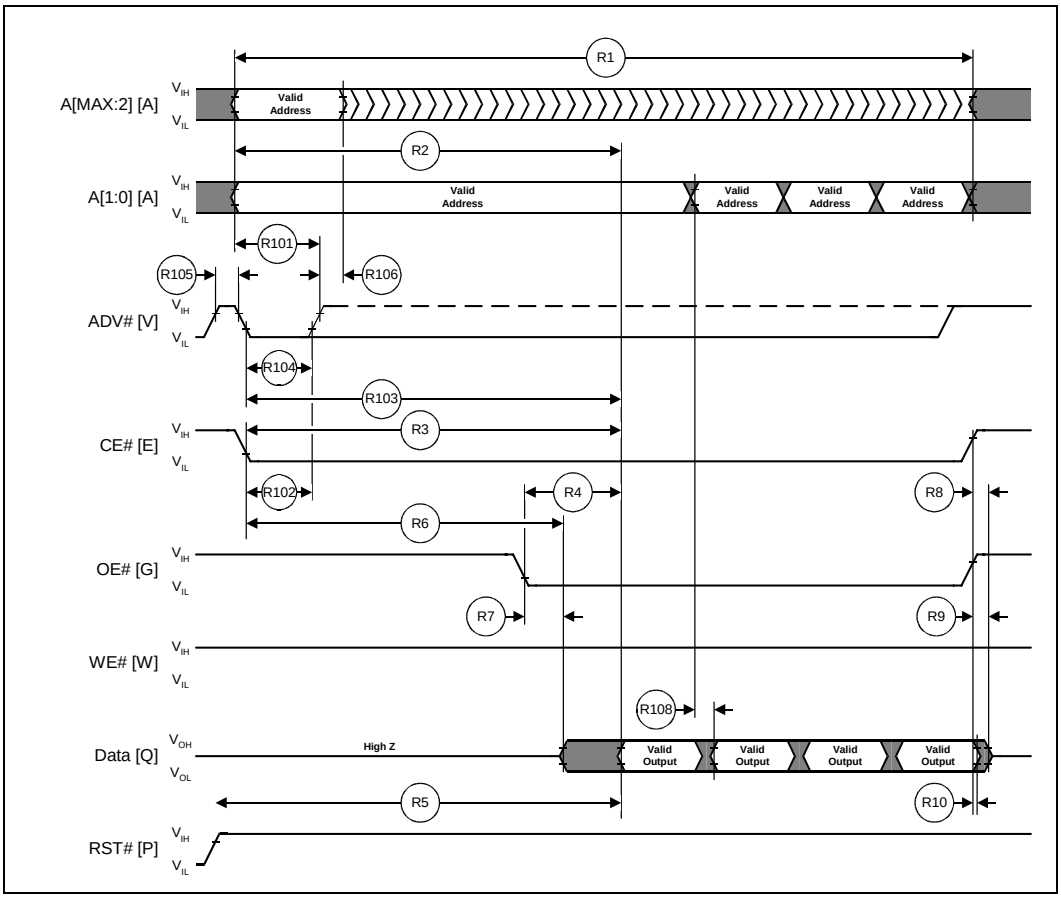
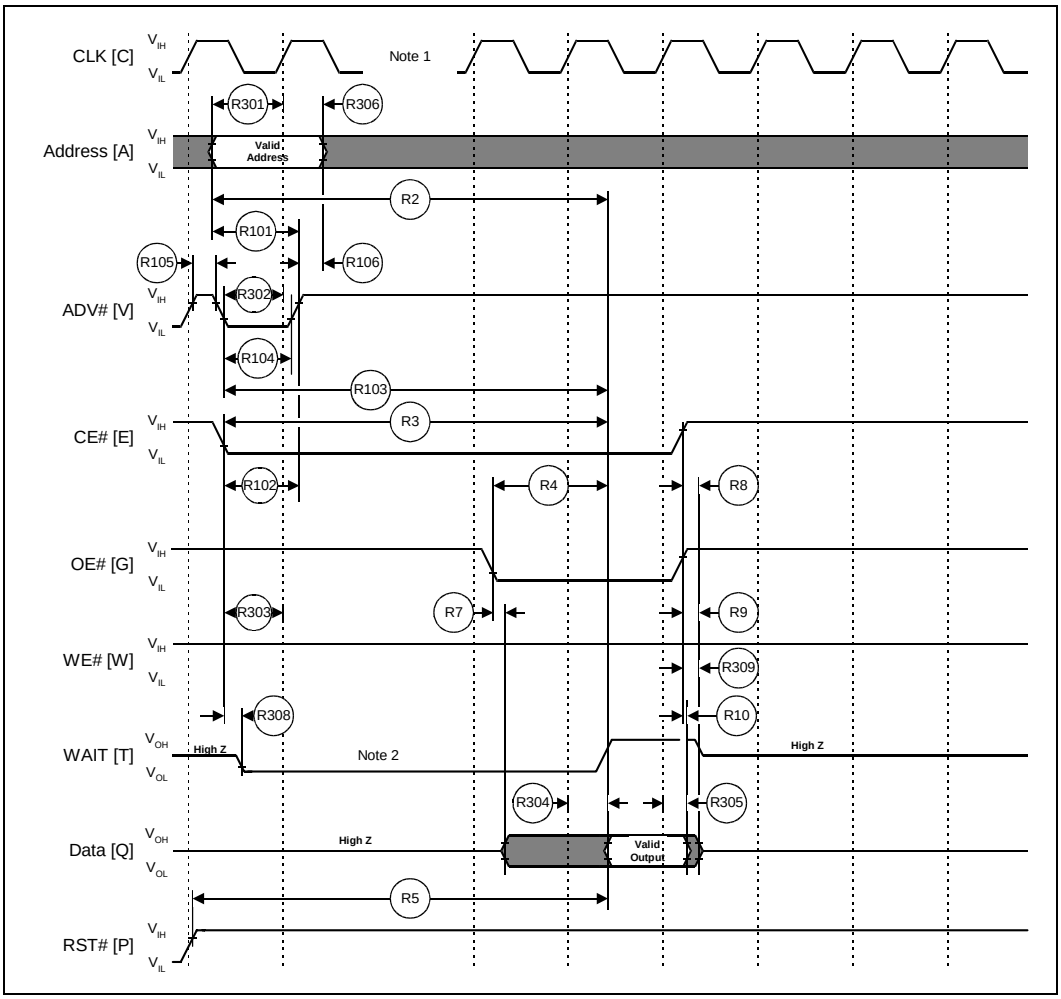


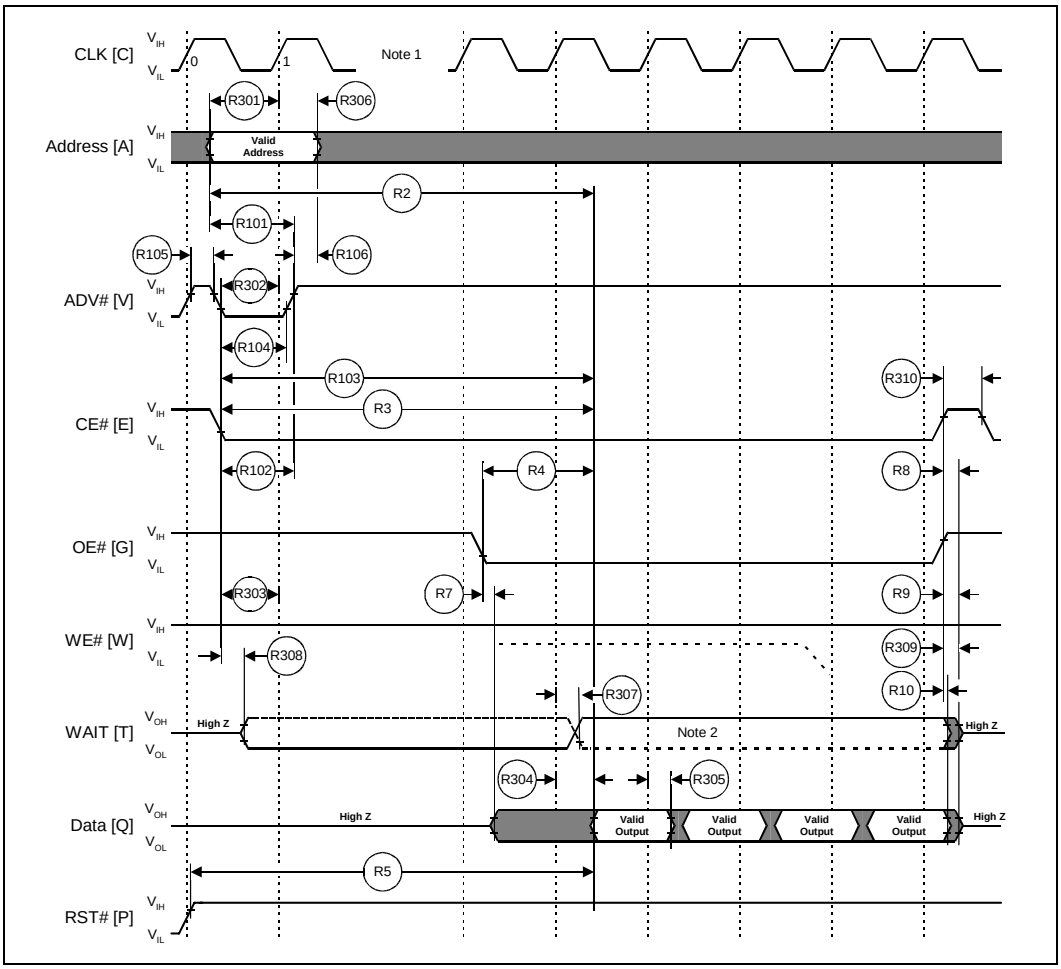
Figure 22. Single Synchronous Read Operation Waveform



NOTES:

1. Section 4.16.2, “First Access Latency Count (CR.13-11)” on page 35 describes how to insert clock cycles during the initial access.
2. WAIT (shown active low) can be configured to assert either during or one data cycle before valid data.

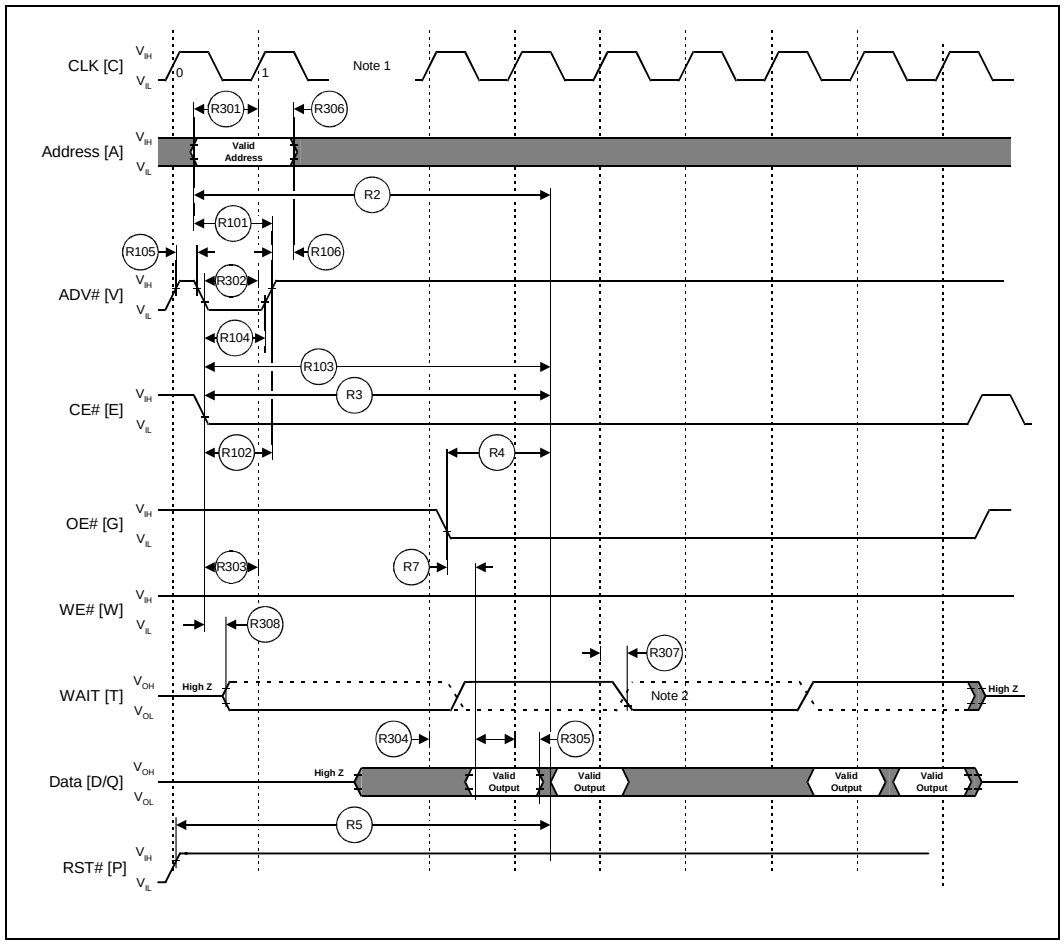
Figure 23. Synchronous Four-Word Burst Read Operation Waveform



NOTES:

1. Section 4.16.2, “First Access Latency Count (CR.13-11)” on page 35 describes how to insert clock cycles during the initial access.
2. WAIT (shown active low) can be configured to assert either during or one data cycle before valid data.

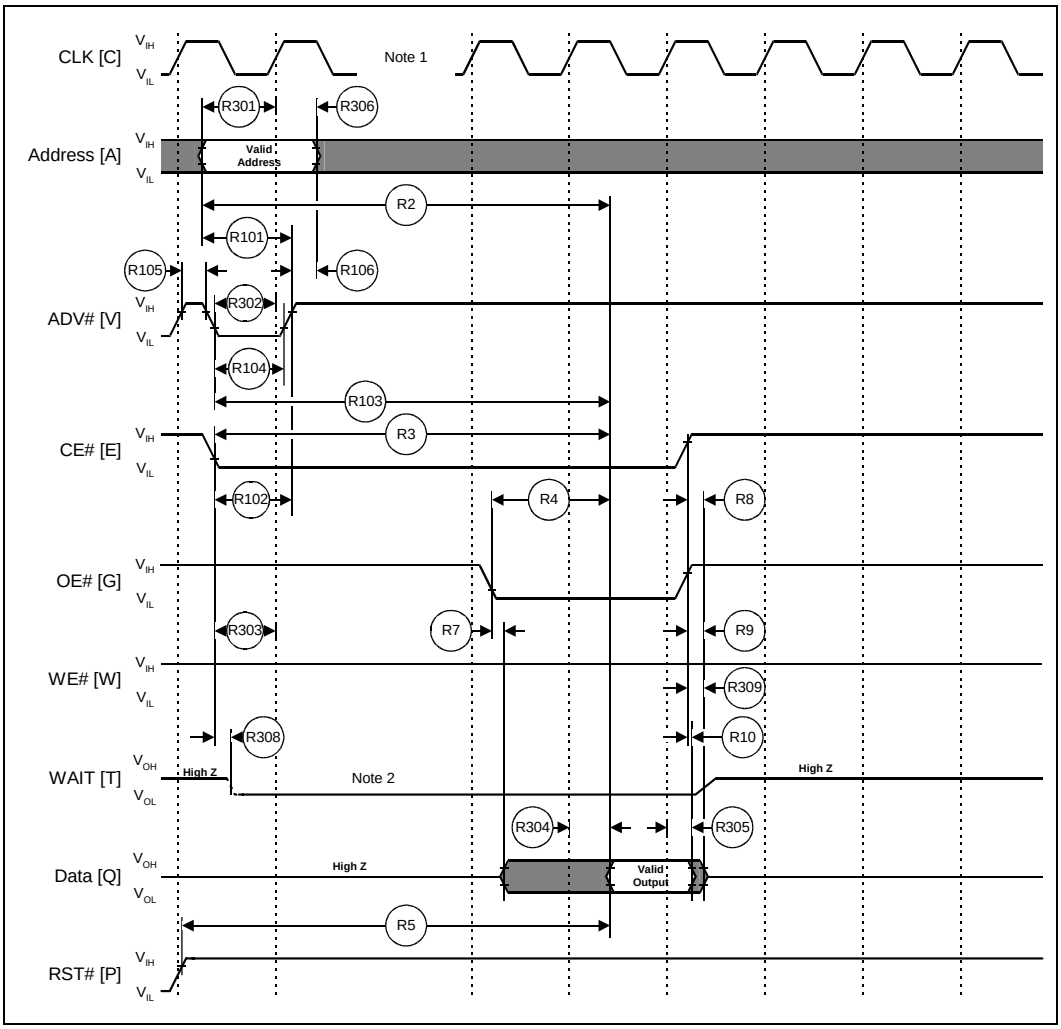
Figure 24. WAIT Functionality for EOWL (End of Word Line) Condition Waveform



NOTES:

1. Section 4.16.2, “First Access Latency Count (CR.13-11)” on page 35 describes how to insert clock cycles during the initial access.
2. WAIT (shown active low) can be configured to assert either during or one data cycle before valid data.

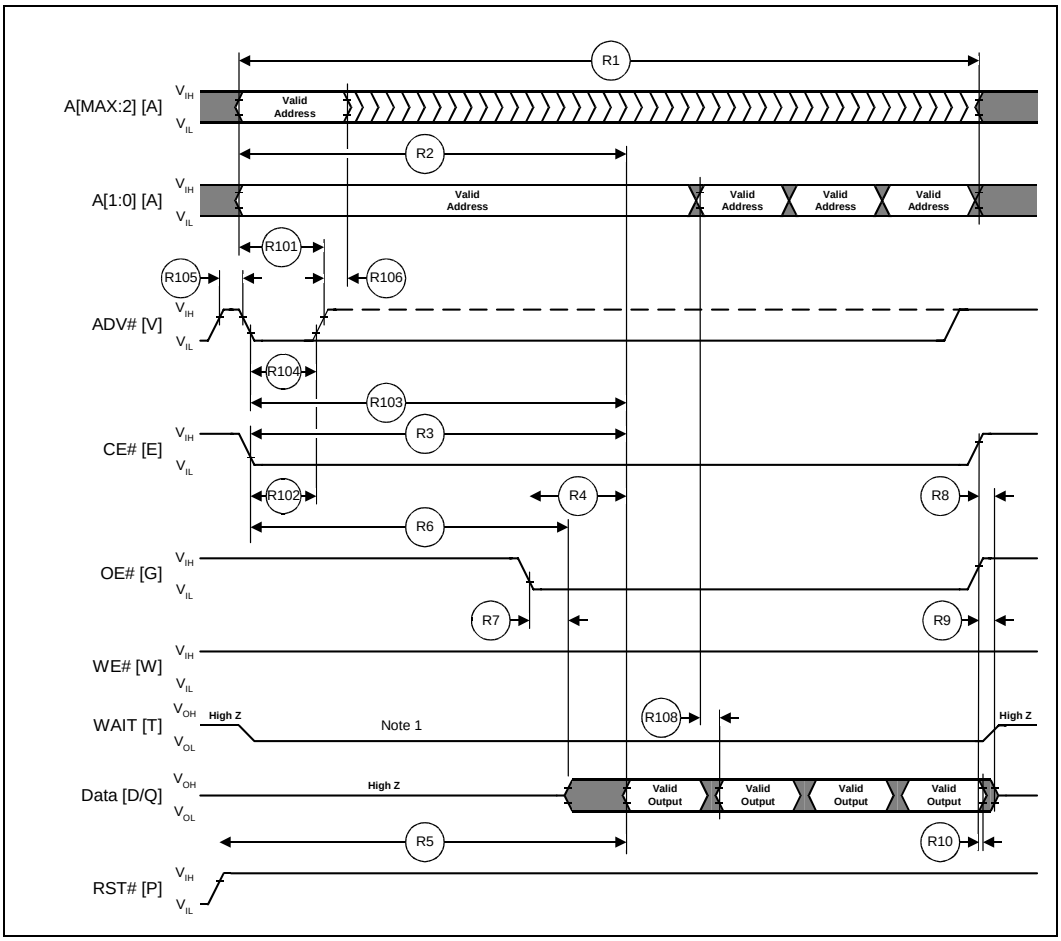
Figure 25. WAIT Signal in Synchronous Non-Read Array Operation Waveform



NOTES:

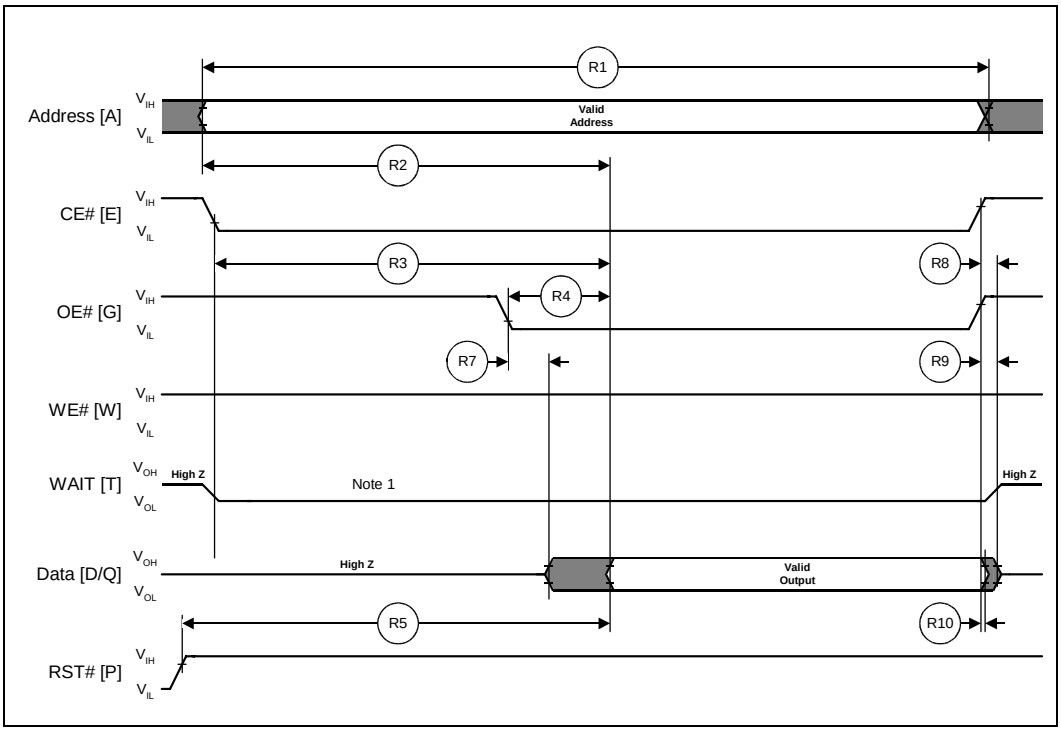
1. Section 4.16.2, “First Access Latency Count (CR.13-11)” on page 35 describes how to insert clock cycles during the initial access.
2. WAIT shown active low.

Figure 26. WAIT Signal in Asynchronous Page-Mode Read Operation Waveform



NOTES:
1. WAIT shown active low.

Figure 27. WAIT Signal in Asynchronous Single-Word Read Operation Waveform



NOTES:
1. WAIT shown active low.

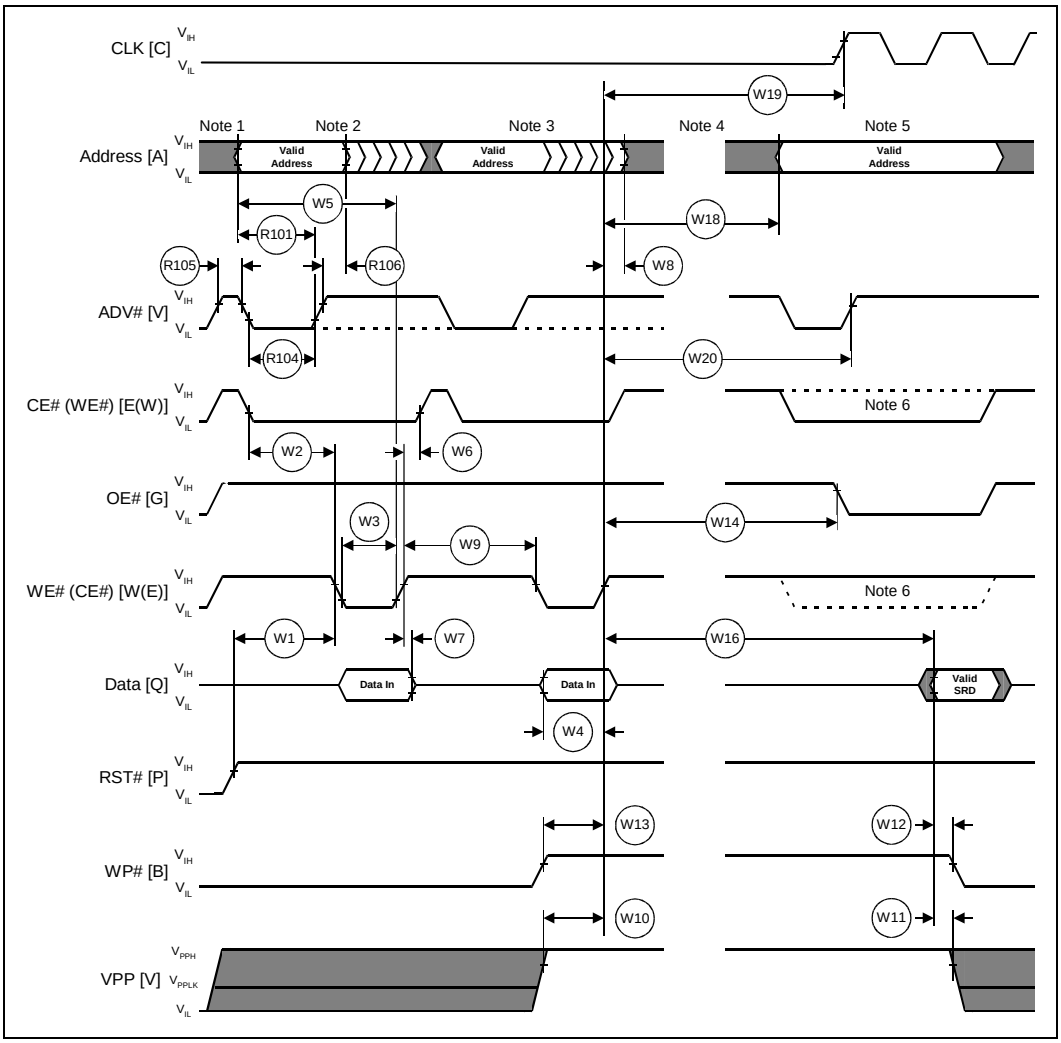
7.7 AC Write Characteristics

#	Sym	Parameter [1,2]	Notes	32 Mbit / 64 Mbit				128 Mbit		Unit
				–70		–85		-90		
				Min	Max	Min	Max	Min	Max	
W1	t_{PHWL} (t_{PHEL})	RST# High Recovery to WE# (CE#) Low	3	150		150		150		ns
W2	t_{ELWL} (t_{WLEL})	CE# (WE#) Setup to WE# (CE#) Low		0		0		0		ns
W3	t_{WLWH} (t_{ELEH})	WE# (CE#) Write Pulse Width Low	4	45		60		60		ns
W4	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE#) High		45		60		60		ns
W5	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE#) High		45		60		60		ns
W6	t_{WHEH} (t_{EHWH})	CE# (WE#) Hold from WE# (CE#) High		0		0		0		ns
W7	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE#) High		0		0		0		ns
W8	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE#) High		0		0		0		ns
W9	t_{WHWL} (t_{EHEL})	WE# (CE#) Pulse Width High	5, 6, 7	25		25		25		ns
W10	t_{VPWH} (t_{VPEH})	VPP Setup to WE# (CE#) High	3	200		200		200		ns
W11	t_{QVVL}	VPP Hold from Valid SRD	3, 8	0		0		0		ns
W12	t_{QVBL}	WP# Hold from Valid SRD	3, 8	0		0		0		ns
W13	t_{BHWH} (t_{BHEH})	WP# Setup to WE# (CE#) High	3	200		200		200		ns
W14	t_{WHGL} (t_{EHGL})	Write Recovery before Read		0		0		0		ns
W16	t_{WHQV}	WE# High to Valid Data	6	t_{AVQV} + 40		t_{AVQV} + 50		t_{AVQV} + 50		ns
W18	t_{WHAV}	WE# High to Address Valid	9	0		0		0		ns
W19	t_{WHCV}	WE# High to CLK Valid	10	25		25		25		ns
W20	t_{WHVH}	WE# High to ADV# High	10	25		25		25		ns

NOTES:

1. Write timing characteristics during erase suspend are the same as during write-only operations.
2. A write operation can be terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WLWH} or t_{ELEH}) is defined from CE# or WE# low (whichever occurs last) to CE# or WE# high (whichever occurs first). Hence, $t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Write pulse width high (t_{WHWL} or t_{EHEL}) is defined from CE# or WE# high (whichever is first) to CE# or WE# low (whichever is last). Hence, $t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
6. t_{WHQV} is t_{AVQV} + 50 ns. System designers should take this into account and may insert a software No-Op instruction to delay the first read after issuing a command.
7. For command other than resume commands.
8. V_{PP} should be held at V_{PP1} or V_{PP2} until block erase or program success is determined.
9. Applicable during asynchronous reads following a write.
10. During synchronous reads, either t_{WHCV} or t_{WHVH} must be met, whichever occurs first.

Figure 28. Write Operations Waveform



NOTES:

1. V_{CC} power-up and standby.
2. Write Program or Erase Setup command.
3. Write valid address and data (for program) or Erase Confirm command.
4. Automated program/erase delay.
5. Read status register data (SRD) to determine program/erase operation completion.
6. OE# and CE# must be asserted and WE# deasserted for read operations.

7.8 Erase and Program Times

Operation	Symbol	Parameter	Description	Notes	V_{PP1}		V_{PP2}		Unit
					Typ	Max	Typ	Max	
Erasing and Suspending									
Erase Time	W500	$t_{ERS/PB}$	4-KW Parameter Block	1,2	0.3	2.5	0.25	2.5	s
	W501	$t_{ERS/MB}$	32-KW Main Block	1,2	0.7	4	0.4	4	s
Suspend Latency	W600	$t_{SUSP/P}$	Program Suspend	1	5	10	5	10	µs
	W601	$t_{SUSP/E}$	Erase Suspend	1	5	20	5	20	µs
Conventional Word Programming									
Program Time	W200	$t_{PROG/W}$	Single Word	1	12	150	8	130	µs
	W201	$t_{PROG/PB}$	4-KW Parameter Block	1,2	0.05	.23	0.03	0.07	s
	W202	$t_{PROG/MB}$	32-KW Main Block	1,2	0.4	1.8	0.24	0.6	s
Enhanced Factory Programming									
Program	W400	$t_{EFP/W}$	Single Word				3.5	16	µs
	W401	$t_{EFP/PB}$	4-KW Parameter Block	1,2			15		ms
	W402	$t_{EFP/MB}$	32-KW Main Block	1,2			120		ms
Operation Latency	W403	$t_{EFP/SETUP}$	EFP Setup					5	µs
	W404	$t_{EFP/TRAN}$	Program to Verify Transition				2.7	5.6	µs
	W405	$t_{EFP/VERIFY}$	Verify				1.7	130	µs

Unless noted otherwise, all above parameters are measured at T_A = +25 °C and nominal voltages, and they are sampled, not 100% tested.

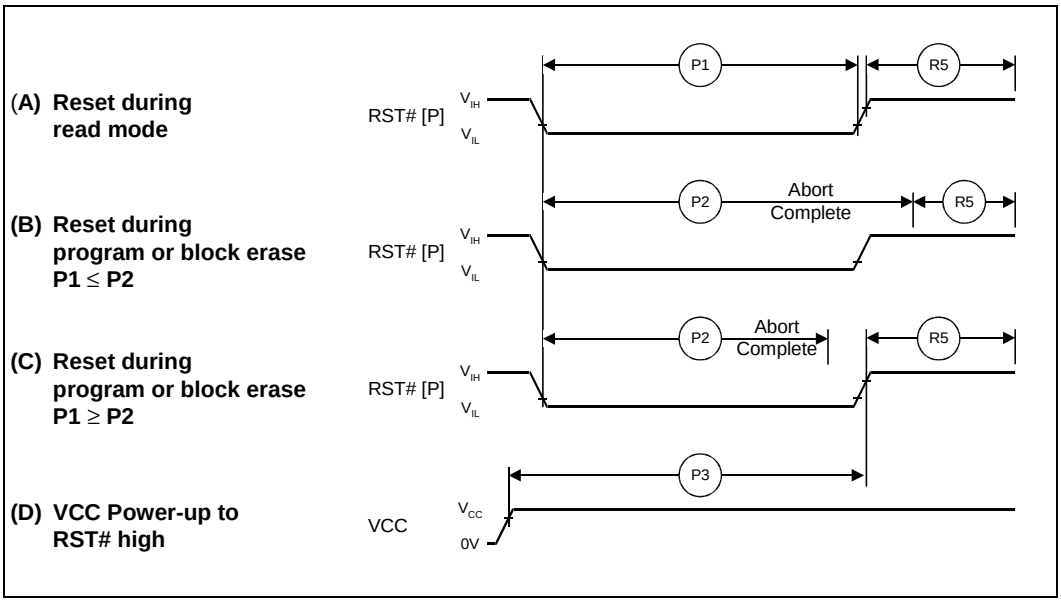
NOTES:
1. Excludes external system-level overhead.
2. Exact results may vary based on system overhead.

7.9 Reset Specifications

#	Symbol	Parameter[1]	Notes	Min	Max	Unit
P1	t_{PLPH}	RST# Low Pulse Width	2, 3, 4	100		ns
P2	t_{PLRH}	RST# Low to device reset during Block Erase	3, 4, 5		20	µs
		RST# Low to device reset during Program	3, 4, 5		10	µs
P3	t_{VCCPH}	VCC Power Valid to RST# High	1,3,4,5,6	60		µs

NOTES:
1. These specifications are valid for all product versions (packages and speeds).
2. The device may reset if $t_{PLPH} < t_{PLPH}$Min, but this is not guaranteed.
3. Not applicable if RST# is tied to VCC.
4. Sampled, but not 100% tested.
5. If RST# is tied to VCC, the device is not ready until t_{VCCPH} after time when $V_{CC} \geq V_{CC}$Min.
6. If RST# is tied to any supply/signal with V_{CCQ} voltage levels, the RST# input voltage must not exceed V_{CC} until $V_{CC} \geq V_{CC}$Min.

Figure 29. Reset Operations Waveforms



Appendix A Write State Machine States

This table shows the command state transitions based on incoming commands. Only one partition can be actively programming or erasing at a time. Each partition stays in its last output state (Array, ID/CFI or Status) until a new command changes it. The next WSM state does not depend on the partition's output state.

Table A1. Write State Machine - Next State Table

Current State		Next State After Command Input								
		Read Array[3] (FFh)	Program Setup[4,5] (10h/ 40h)	Erase Setup[4,5] (20h)	EFP Setup[4] (30h)	Block Erase Confirm, Pgm/Erase Resume, ULB Confirm[9] (D0h)	Program/ Erase Suspend (B0h)	Read Status Register (70h)	Clear Status Register[6] (50h)	Read Identifier/ Query (90h, 98h)
Ready		Ready	Program Setup	Erase Setup	EFP Setup	Ready				
Lock/CR Setup		Ready (Lock Error)				Ready	Ready (Lock Error)			
OTP	Setup	OTP Busy								
	Busy	OTP Busy								
Program	Setup	Program Busy								
	Busy	Program Busy					Program Suspend	Program Busy		
	Suspend	Program Suspend				Program Busy	Program Suspend			
Erase	Setup	Ready (Error)				Erase Busy	Ready (Error)			
	Busy	Erase Busy					Erase Suspend	Erase Busy		
	Suspend	Erase Suspend	Program in Erase Suspend Setup	Erase Suspend		Erase Busy	Erase Suspend			
Program in Erase Suspend	Setup	Program in Erase Suspend Busy								
	Busy	Program in Erase Suspend Busy					Program in Erase Suspend	Program in Erase Suspend Busy		
	Suspend	Program in Erase Suspend				Program in Erase Suspend Busy	Program in Erase Suspend			
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock Error)				Erase Suspend	Erase Suspend (Lock Error)			
EFP	Setup	Ready (Error)				EFP Busy	Ready (Error)			
	Busy	EFP Busy[7]								
	Verify	Verify Busy[7]								

	State Output After Command Input					
Program Erase Erase Setup OTP Setup Program in Erase Suspend EFP Setup, EFP Busy Verify Busy	Status					
Lock/CR Setup Lock/CR Setup in Erase Suspend	Status					
OTP Busy	Array[3]	Status	Output doesn't change	Status	Output doesn't change	Status
Ready Program Busy Program Suspend Erase Busy Erase Suspend Program in Erase Suspend Pgm Suspend in Erase Suspend	Array	Status	Output doesn't change	Status	Output doesn't change	ID/Query

Table A1. Write State Machine -- Next State Table (continued)

Current State		Next State After Command Input							
		Lock, Unlock, Lock-Dwn, CR Setup[5] (60h)	OTP Setup[5] (C0h)	Lock Block Confirm[9] (01h)	Lock-Dwn Block Confirm[9] (2Fh)	Write CR Confirm[9] (03h)	EFP Exit (BlkAdr≠WAO) (XXXXh)	Illegal Cmds or EFP Data[2] (other codes)	WSM Operation Completes
Ready		Lock/CR Setup	OTP Setup	Ready					N/A
Lock/CR Setup		Ready (Lock Error)		Ready			Ready (Lock Error)		N/A
OTP	**Setup**	OTP Busy							N/A
	Busy	OTP Busy							Ready
Program	**Setup**	Program Busy							N/A
	Busy	Program Busy							Ready
	Suspend	Program Suspend							N/A
Erase	**Setup**	Ready (Error)							N/A
	Busy	Erase Busy							Ready
	Suspend	Lock/CR Setup in Erase Suspend	Erase Suspend						N/A
Program in Erase Suspend	**Setup**	Program in Erase Suspend Busy							N/A
	Busy	Program in Erase Suspend Busy							Erase Suspend
	Suspend	Program in Erase Suspend Busy							N/A
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock Error)	Erase Suspend				Erase Suspend (Lock Error)		N/A
EFP	**Setup**	Ready (Error)							N/A
	Busy	EFP Busy[7]					EFP Verify	EFP Busy[7]	N/A
	Verify	Verify Busy[7]					Ready	EFP Verify[7]	Ready

State Output After Command Input

Program Erase **Erase Setup** **OTP Setup** **Program in Erase Suspend** **EFP Setup** **EFP Busy** **Verify Busy**	Status				Output doesn't change
Lock/CR Setup **Lock/CR Setup in Erase Suspend**	Status		Array	Status	Output doesn't change
OTP Busy	Status[7]	Output doesn't change		Array / Status	Output doesn't change
Ready **Program Busy** **Program Suspend** **Erase Busy** **Erase Suspend** **Program in Erase Suspend** **Pgm Suspend in Erase Suspend**	Status	Output doesn't change		Array / Status	Output doesn't change

NOTES:

1. The output state shows the type of data that appears at the outputs if the partition address is the same as the command address. A partition can be placed in Read Array, Read Status or Read ID/CFI, depending on the command issued. Each partition stays in its last output state (Array, ID/CFI or Status) until a new command changes it. The next WSM state does not depend on the partition's output state. For example, if partition #1's output state is Read Array and partition #4's output state is Read Status, every read from partition #4 (without issuing a new command) outputs the status register.
2. Illegal commands are those not defined in the command set.
3. All partitions default to Read Array mode at power-up. A Read Array command issued to a busy partition results in undermined data when a partition address is read.
4. Both cycles of 2-cycle commands should be issued to the same partition address. If they are issued to different partitions, the second write determines the active partition. Both partitions will output status information when read.
5. If the WSM is active, both cycles of a 2-cycle command are ignored. This differs from previous Intel devices.
6. The Clear Status command clears status register error bits except when the WSM is running (Pgm Busy, Erase Busy, Pgm Busy In Erase Suspend, OTP Busy, EFP modes) or suspended (Erase Suspend, Pgm Suspend, Pgm Suspend In Erase Suspend).
7. EFP writes are allowed only when status register bit SR.0=0. EFP is busy if Block Address = address at EFP Confirm command. Any other commands are treated as data.
8. The "current state" is that of the WSM, not the partition.
9. Confirm commands (Lock Block, Unlock Block, Lock-down Block, Configuration Register) perform the operation and then move to the Ready State.

Appendix B Common Flash Interface

This appendix defines the data structure or “database” returned by the Common Flash Interface (CFI) Query command. System software should parse this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. Once this information has been obtained, the software will know which command sets to use to enable flash writes, block erases, and otherwise control the flash component. The Query is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface, or CFI.

B.1 Query Structure Output

The Query database allows system software to obtain information for controlling the flash device. This section describes the device’s CFI-compliant interface that allows access to Query data.

Query data are presented on the lowest-order data outputs (DQ[7:0]) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the Query table device starting address is a 10h, which is a word address for x16 devices.

For a word-wide (x16) device, the first two Query-structure bytes, ASCII “Q” and “R,” appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00h data on upper bytes. The device outputs ASCII “Q” in the low byte (DQ[7:0]) and 00h in the high byte (DQ[15:8]).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the “h” suffix has been dropped. In addition, since the upper byte of word-wide devices is “00h,” the leading “00” has been dropped from the table notation and only the lower byte value is shown. Any x16 device outputs can be assumed to have 00h on the upper byte in this mode.

B.2 Query Structure Overview

The Read Query command causes the flash component to display the CFI Query structure or “database.” The structure subsections and address locations are summarized below.

Table B1. Query Structure

Offset	Subsection	Description[1]
00h		Manufacturer Code
01h		Device Code
BBA + 02h[2]	Block Status Register	Block-specific information
04h to 0Fh	Reserved	Reserved for vendor-specific information
10h	CFI Query identification string	Command set ID and vendor data offset
1Bh	System interface information	Device timing and voltage information
27h	Device geometry definition	Flash device layout
P[3]	Primary Intel-specific Extended Query Table	Addition vendor-defined information specific to the Primary Vendor Algorithm

NOTES:
1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of device bus width and mode.
2. BBA = Block Base Address beginning location (i.e., 08000h is block 1's beginning location when the block size is 32K-word).
3. Offset 15h defines "P" which points to the Primary Intel-specific Extended Query Table.

B.3 CFI Query Identification String

The Identification String provides verification that the component supports the CFI specification. It also indicates the specification version and supported vendor-specified command set(s).

Table B2. CFI Identification

Address Offset	Description	Data	Value
CFI Identification			
10h	Query unique ASCII string “QRY”	51h	‘Q’
11h		52h	‘R’
12h		59h	‘Y’
13h	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	03h	
14h		00h	
15h	Extended Query Table primary algorithm address. (Denotes the starting offset address for the vendor-specific query table.)	39h	
16h		00h	
17h	Alternate vendor command set and control interface ID code. 0000h means no second vendor-specified algorithm exists	00h	
18h		00h	
19h	Secondary algorithm Extended Query Table address. 0000h means none exists.	00h	
1Ah		00h	
System Interface Information			
1Bh	Vcc logic supply minimum program/erase voltage DQ[7:4] = Volts (BCD) DQ[3:0] = 100mV (BCD)	17h	1.7 V
1Ch	Vcc logic supply maximum program/erase voltage DQ[7:4] = Volts (BCD) DQ[3:0] = 100mV (BCD)	19h	1.9 V
1Dh	Vcc programming supply minimum program/erase voltage DQ[7:4] = Volts (BCD) DQ[3:0] = 100mV (BCD)	B4h	11.4 V
1Eh	Vcc programming supply minimum program/erase voltage DQ[7:4] = Volts (HEX) DQ[3:0] = 100mV (BCD)	C6h	12.6 V
1Fh	*n* such that typical single-word program time-out = 2^n µs	04h	16 µs
20h	*n* such that typical buffer write time-out = 2^n µs	00h	
21h	*n* such that typical block erase time-out = 2^n ms	0Ah	1 s
22h	*n* such that typical full-chip erase time-out = 2^n ms	00h	
23h	*n* such that max single-word program time-out = 2^n µs	04h	256 µs
24h	*n* such that max buffer write time-out = 2^n µs	00h	
25h	*n* such that max block erase time-out = 2^n ms	03h	8 s
26h	*n* such that max full-chip erase time-out = 2^n ms	00h	

Table B2. CFI Identification (Continued)

Address Offset	Description	Data	Value
Device Geometry Definition			
27h	Flash density: 2^n bytes	16h 17h 18h	32Mbit 64Mbit 128Mbit
28h	Data bus width (low byte): 00h=x8, 01h=x16, 02h=x32, 03h=x64	01h	x16
29h	Data bus width (high byte): not used	00h	0
2Ah	Write buffer size: 2^n bytes	00h	0
2Bh		00h	0
2Ch	Number of erase block regions (x) within device: 1. x = 0 means no erase blocking; the device erases in bulk 2. x specifies the number of device regions with one or more contiguous same-size erase blocks. 3. Symmetrically blocked partition	02h	2
2Dh	Erase Block Region 1 Information Bits 0–15 = y, y+1 = number of identical-size erase blocks Bits 16–31 = z, region erase block(s) size are z x 256 bytes BPD: 00200007h TPD: 32Mb = 0100 003Eh, 64Mb = 0100 007Eh, 128Mb = 0100 00FEh	See Description	
2Eh			
2Fh			
30h			
31h	Erase Block Region 2 Information Bits 0–15 = y, y+1 = number of identical-size erase blocks Bits 16–31 = z, region erase block(s) size are z x 256 bytes BPD: 32Mb = 0100 003Eh, 64Mb = 0100 007Eh, 128Mb = 0100 00FEh TPD: 0020 0007h	See Description	
32h			
33h			
34h			
35h	Reserved for future erase block region information		
36h			
37h			
38h			
Primary Vendor-Specific Extended Query			
39h(1)	Primary Extended Query Table, Unique ASCII string: “PRI”	50h	‘P’
3Ah		52h	‘R’
3Bh		49h	‘I’
3Ch	Major version number, ASCII	31h	‘1’
3Dh	Minor version number, ASCII	33h	‘3’

Table B2. CFI Identification (Continued)

Address Offset	Description	Data	Value
3Eh	Optional feature and command support: Bit Feature 0 - Full chip erase 1 - Erase suspend 2 - Program Suspend 3 - Legacy lock/unlock 4 - Queued erase 5 - Instant individual block locking 6 - Protection bits 7 - Pagemode read 8 - Synchronous read 9 - Simultaneous operations bits 10-31 are Reserved.	66h	bit 0=no bit 1=yes bit 2=yes bit 3=no bit 4=no bit 5=yes bit 6=yes bit 7=no bit 8=yes bit 9=yes
3Fh		03h	
40h		00h	
41h		00h	
42h	Supported functions after Program/Erase Suspend (besides Read Array, Read Status, and Read Query): Bit Feature 0 - Program after Erase Suspend	01h	bit 0=yes
43h	Block Status Register Mask (*bits 2-16 are reserved)* Bit Feature 0 - Block Lock status active 1 - Block Lock-down status active	03h	bit 0=yes bit 1=yes
44h		00h	
45h	Highest V_{CC} Supported: Bits 0-3 : 100mV (BCD) Bits 4-7 : Volts (BCD)	18h	1.8 V
46h	Highest V_{PP} Supported: Bits 0-3 : 100mV (BCD) Bits 4-7 : Volts (HEX)	C0h	12.0 V
Protection Register Information			
47h	Number of protection register fields in JEDEC ID space. '00h' indicates that 256 fields are available	01h	1
48h	Protection Field 1: Protection Description Bits 0-7 : Lower byte of protection register address Bits 8-15 : Upper byte of protection register address Bits 16-23 : 2^n bytes in factory pre-programmed region Bits 24-31 : 2^n bytes in user-programmable region	80h	0080h
49h		00h	
5Ah		03h	8 bytes
5Bh		03h	8 bytes
Burst Read Information			
5Ch	Page Mode Read Buffer Size BIts 0-7 : 2^n bytes in read page-mode buffer *(00h indicates no page buffer exists for reads)*	00h	None
5Dh	Number of Synchronous Read configurations fields that follow. 00h indicates no burst capability	03h	3 fields

Table B2. CFI Identification (Continued)

Address Offset	Description	Data	Value
5Eh	Synchronous Read Field 1 Bits 0-1 : 2^{n+1} words per synchronous read Bits 2-7 : Reserved	01h	4-words
5Fh	Synchronous Read Field 2 Bits 0-1 : 2^{n+1} words per synchronous read Bits 2-7 : Reserved	02h	8-words
60h	Synchronous Read Field 3 Bits 0-1 : 2^{n+1} words per synchronous read Bits 2-7 : Reserved	07h	Continuous

Table B3. Partition and Erase Block Region Information

Feature Description	Bottom-Parameter				Top-Parameter			
	Adrs	32 Mbit	62 Mbit	128 Mbit	Adrs	32 Mbit	64 Mbit	128 Mbit
Number of device hardware partition regions n = number of partition regions containing one or more contiguous erase block regions	51h	02			51h	02		
Partition Region 1 Information								
Number of identical partitions within partition region 1	52h	01			52h	07	0F	1F
	53h	00			53h	00		
Number of program or erase operations allowed in partition region 1: Bits 0-3 : Number of simultaneous program operations Bits 4-7 : Number of simultaneous erase operations	54h	11			54h	11		
Number of program or erase operations allowed in other partitions while a partition in this region is **Programming** Bits 0-3 : Number of simultaneous program operations Bits 4-7 : Number of simultaneous erase operations	55h	00			55h	00		
Number of program or erase operations allowed in other partitions while a partition in this region is **Erasing** Bits 0-3 : Number of simultaneous program operations Bits 4-7 : Number of simultaneous erase operations	56h	00			56h	00		
Types of erase block regions in partition region 1 n = number of erase block regions w/ contiguous same-size erase locks. Symmetrically blocked partitions have one blocking region.	57h	02			57h	01		
Partition Region 1 Erase Block Type 1 Information Bits 0-15 : n+1 = number of identical-sized erase blocks Bits 16-31 : n×256 = number of bytes in erase block region	58h	07			58h	07		
	59h	00			59h	00		
	5Ah	20			5Ah	00		
	5Bh	00			5Bh	01		
Partition Region 1 (Erase Block Type 1) Minimum block erase cycles × 1000	5Ch	64			5Ch	64		
	5Dh	00			5Dh	00		
Partition Region 1 (Erase Block Type 1): BIts per cell, internal ECC Bits 0-3 : bits per cell in erase region Bit 4 : reserved for “internal ECC used” BIts 5-7 : reserved	5Eh	01			5Eh	01		

Table B3. Partition and Erase Block Region Information (Continued)

Feature Description	Bottom-Parameter				Top-Parameter			
	Adrs	32 Mbit	62 Mbit	128 Mbit	Adrs	32 Mbit	64 Mbit	128 Mbit
Partition Region 1 (Erase Block Type 1): Page mode and synchronous mode capabilities (defined in table 10) Bit 0 : Page-mode host reads permitted Bit 1 : Synchronous host reads permitted Bit 2 : Synchronous host writes permitted Bits 3-7 : reserved	5Fh	02			5Fh	02		
Partition Region 1 Erase Block Type 2 Information Bits 0-15 : n+1 = number of identical-sized erase blocks Bits 16-31 : n×256 = number of bytes in erase block region	60h	06						
	61h	00						
	62h	00						
	63h	01						
Partition Region 1 (Erase Block Type 2) Minimum block erase cycles × 1000	64h	64						
	65h	00						
Partition Regions 1 (Erase Block Type 2): BIts per cell, internal ECC Bits 0-3 : bits per cell in erase region Bit 4 : reserved for “internal ECC used” BIts 5-7 : reserved	66h	01						
Partition Region 1 (Erase Block Type 2): Page mode and synchronous mode capabilities (defined in table 10) Bit 0 : Page-mode host reads permitted Bit 1 : Synchronous host reads permitted Bit 2 : Synchronous host writes permitted Bits 3-7 : reserved	67h	02						
Partition Region 2 Information								
Number of identical partitions within partition region 2	68h	07	0F	1F	60h	01		
	69h	00			61h	00		
Number of program or erase operations allowed in partition region 2: Bits 0-3 : Number of simultaneous program operations Bits 4-7 : Number of simultaneous erase operations	6Ah	01			62h	11		
Number of program or erase operations allowed in other partitions while a partition in this region is **Programming** Bits 0-3 : Number of simultaneous program operations Bits 4-7 : Number of simultaneous erase operations	6Bh	00			63h	00		
Number of program or erase operations allowed in other partitions while a partition in this region is **Erasing** Bits 0-3 : Number of simultaneous program operations Bits 4-7 : Number of simultaneous erase operations	6Ch	00			64h	00		
Types of erase block regions in partition region 2 n = number of erase block regions w/ contiguous same-size erase locks. Symmetrically blocked partitions have one blocking region.	6Dh	01			65h	02		
Partition Region 2 Erase Block Type 1 Information Bits 0-15 : n+1 = number of identical-sized erase blocks Bits 16-31 : n×256 = number of bytes in erase block region	6Eh	07			66h	06		
	6Fh	00			67h	00		
	70h	00			68h	00		
	71h	01			69h	00		
Partition Region 2 (Erase Block Type 1) Minimum block erase cycles × 1000	72h	64			6Ah	01		
	73h	00			6Bh	64		
Partition Region 2 (Erase Block Type 1): BIts per cell, internal ECC Bits 0-3 : bits per cell in erase region Bit 4 : reserved for “internal ECC used” BIts 5-7 : reserved	74h	01			6Ch	01		

Table B3. Partition and Erase Block Region Information (Continued)

Feature Description	Bottom-Parameter				Top-Parameter			
	Adrs	32 Mbit	62 Mbit	128 Mbit	Adrs	32 Mbit	64 Mbit	128 Mbit
Partition Region 2 (Erase Block Type 1): Page mode and synchronous mode capabilities (defined in table 10) Bit 0 : Page-mode host reads permitted Bit 1 : Synchronous host reads permitted Bit 2 : Synchronous host writes permitted Bits 3-7 : reserved	75h	02			6Dh	02		
Partition Region 2 Erase Block Type 2 Information Bits 0-15 : n+1 = number of identical-sized erase blocks Bits 16-31 : n×256 = number of bytes in erase block region					6Eh	07		
					6Fh	00		
					70h	02		
					71h	00		
Partition Region 2 (Erase Block Type 2) Minimum block erase cycles × 1000					72h	64		
					73h	00		
Partition Region 2 (Erase Block Type 2): BIts per cell, internal ECC Bits 0-3 : bits per cell in erase region Bit 4 : reserved for “internal ECC used” BIts 5-7 : reserved					74h	01		
Partition Region 2 (Erase Block Type 2): Page mode and synchronous mode capabilities (defined in table 10) Bit 0 : Page-mode host reads permitted Bit 1 : Synchronous host reads permitted Bit 2 : Synchronous host writes permitted Bits 3-7 : reserved					75h	02		
Feature Space definitions : Reserved	76h				76h			
Reserved	77h				77h			

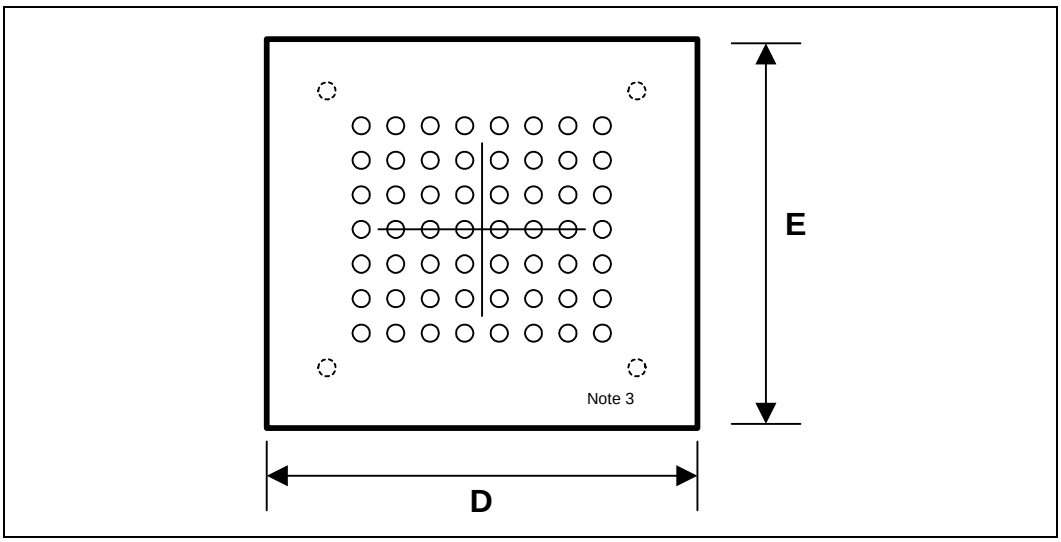
NOTES:

1. The variable P is a pointer which is defined at CFI offset 15h.
2. For a 16Mb the 1.8 Volt Intel® Wireless Flash memory z1 = 0100h = 256 ⇒ 256^2 = 64K, y1 = 17h = 23d ⇒ y1+1 = 24 ⇒
   24 * 64K = 1½MB ⇒ Partition 2’s offset is 0018 0000h bytes (000C 0000h words).
3. TPD - Top parameter device; BPD - Bottom parameter device.
4. Partition Region: Symmetrical partitions form a partition region. (there are two partition regions, A. contains all the partitions that are made up of main blocks only. B. contains the partition that is made up of the parameter and the main blocks.

Appendix C Mechanical Specifications

C.4 The 1.8 Volt Intel® Wireless Flash memory 56 Active Ball Matrix (7x8) 0.75 mm Ball Pitch Package Specifications

7 x 8 Ball Matrix



Mechanical Specifications

Pkg Type	Density	D (Width)(1) (± 0.1 mm)	E (Length)(2) (± 0.1 mm)	Height (max)
VF BGA	32 Mbit	7.7 mm	9.0 mm	1.0 mm
µBGA* CSP	64 Mbit	7.7 mm	9.0 mm	1.0 mm
VF BGA	128 Mbit	12.5 mm	12.0 mm	1.0 mm

NOTES:
1. 8 Ball direction of the matrix runs parallel to this dimension
2. 7 Ball direction of the matrix runs parallel to this dimension
3. 4 outrigger support balls on 128-Mbit density only

Appendix D Ordering Information

Component Ordering Information