Advanced

GT34C02

2Kb SPD EEPROM

Table of Content

1 FEATURES

- Supply voltage: 1.7V to 3.6V
- 2-wire serial interface I^2C compatible
- Speed up to 400 kHz
- Organization:
  - 256 X 8-bit
- Low operating current
  - Standby Current less than 1 μA (1.7V)
  - Standby Current less than 2 μA (3.6V)
  - Active Current less than 2 mA (3.6V)
- Byte and Page (up to 16 bytes) Write Operations
  - Partial Page-writes permitted
- Random and Sequential Read modes
- Self-Time Write Cycle (5ms, max)
- Data Protection Features
  - Write Protect Pin
  - Permanent Software Protection
  - Reversible Software Protection
- Filtered Inputs for Noise Suppression
- More than 1 million Erase/Write Endurance Cycles
- More than 40 years Data Retention
- Packages: SOIC/SOP, TSSOP and UDFN
- Operating Temperature range: -40°C to +85°C

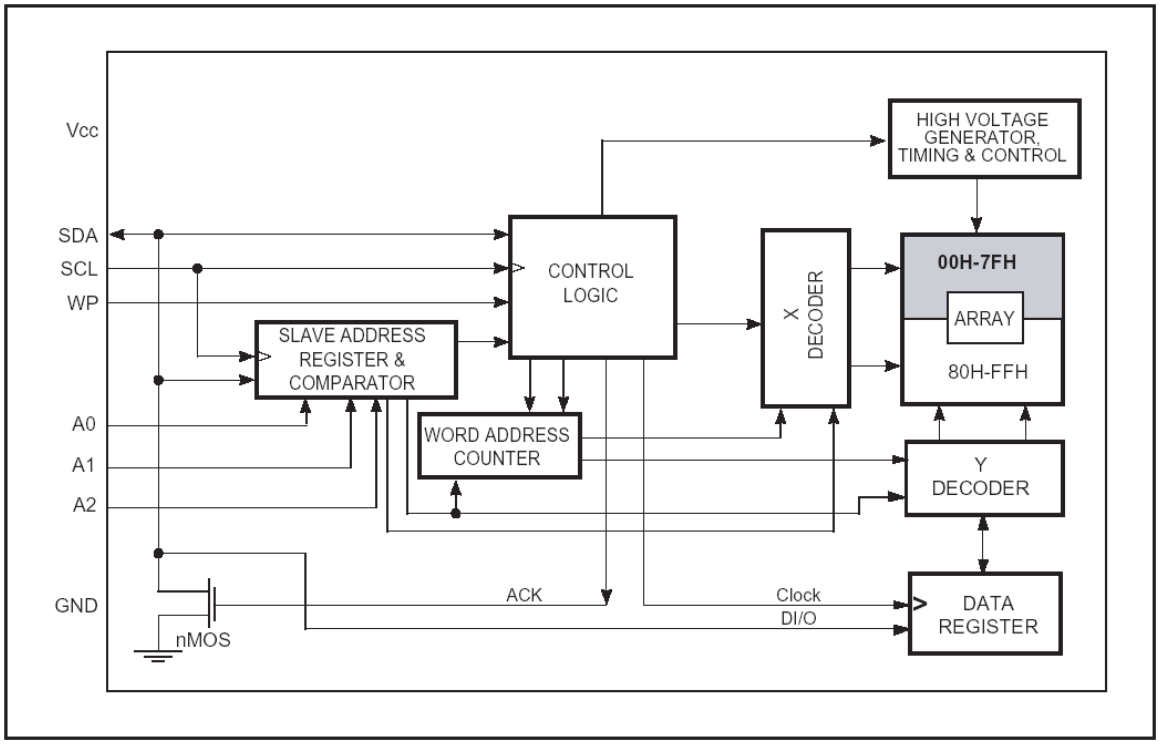
2 DESCRIPTION

The GT34C02 is a 2K-bit Serial Presence Detect (SPD) EEPROM, which is fully compatible to industrial standard I^2C™ interface. The GT34C02 contains a memory array of 2K bits (256x8), which is organized in 16-byte per page.

The GT34C02 product operates from 1.7V to 3.6V to satisfy the voltage requirements of DDR2, DDR1, and many other specifications. The device is offered in Lead-free, RoHS, halogen free or Green package. The available package types are 8-pin SOIC/SOP, TSSOP and UDFN.

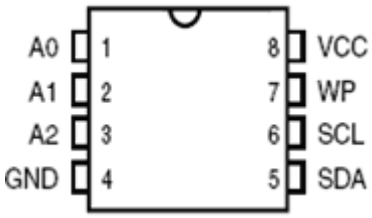
The GT34C02 have two data protection features. One of the features is to permanently lock the data in its first half (lower) 128 bytes (address 00h to 7Fh). This feature is specifically designed for use in DRAM DIMM with SPD. All information concerning the DRAM module configuration (e.g. access speed, size, and organization) can be kept write-protected in the first half of the memory. The second half (upper) 128 bytes of the memory (address 80h to FFh) can also be write-protected using two different software write protection mechanisms. By sending a specified sequence to the device, the first 128 bytes memory can be write-protected either permanently or reversible. The operating ambient temperature ranging is from -40°C to +85°C.

3 BLOCK DIAGRAM

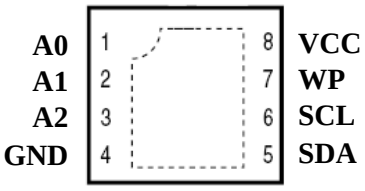


4 PIN CONFIGURATION

8-Pin SOIC/SOP and TSSOP



8-Lead UDFN



Pin #	Symbol	Description
1	A0	Device address selection pin
2	A1	Device address selection pin
3	A2	Device address selection pin
4	GND	Ground
5	SDA	Serial Data (Open drain)
6	SCL	Serial clock
7	WP	Write Protect Pin
8	V_{CC}	Supply voltage

5 PIN DESCRIPTIONS

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

SDA

The SDA is a bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wired with other open drain or open collector outputs. However, the SDA pin requires a pull-up resistor connected to the power supply.

A0, A1, A2

The A0, A1 and A2 are the device address inputs.

Typically, the A0, A1, and A2 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. When A0, A1, and A2 are left floating, the inputs are defaulted to zero.

WP

WP is the Write Protect pin. While the WP pin is connected to the power supply of GT34C02, the entire array becomes Write Protected (i.e. the device becomes Read only). When WP is tied to Ground or left floating, the normal write operations are allowed. If the device has already received a write-protection command, the memory in the range of 00h-7Fh is read-on regardless of the setting of the WP pin.

Vcc

Supply voltage

GND

Ground of supply voltage

6 DEVICE OPERATION

The GT34C02 serial interface supports communications using industrial standard 2-wire bus protocol, such as I2C™.

2-Wire bus

The GT34C02 utilizes the industrial standard 2-wire bus supporting either I^2C™ protocol to communicate with a master controller. The master generates the SCL signal and the GT34C02 being a slave device utilizes the SCL signal to receive or send data via the SDA line. Data transfer is serial, bi-directional, and is one bit at a time with the Most Significant Bit (MSB) transferred first, and a complete I^2C bus data is 1-byte. Since SDA is open-drain, pull-up resistor is required.

The Bus Protocol

- Data transfer may be initiated only when the bus is not busy
- During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated with a Stop condition.

Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

Acknowledge (ACK)

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

Standby Mode

While in standby mode, the power consumption is minimal. The GT34C02 enters into standby mode during one of the following conditions: a) After Power-up, while no Op-code is sent; b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related; or c) After the completion of any internal write operations.

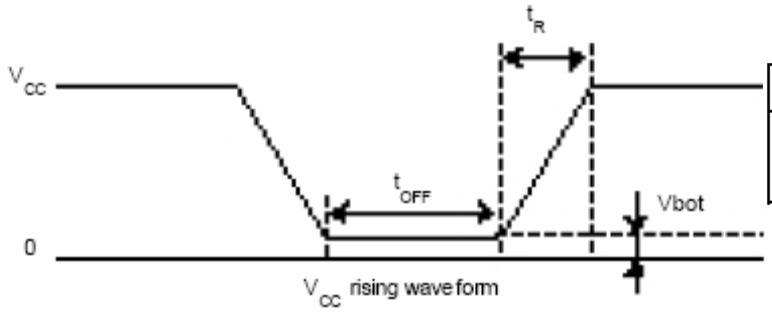
Reset

The GT34C02 contains a reset function in case the 2-wire bus transmission on is accidentally interrupted (e.g. a power loss), or needs to be terminated mid-stream. The reset is initiated when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

Power-On Reset

In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, the device does not respond to any instructions until the supply voltage (VCC) has reached an acceptable stable level above the reset threshold voltage. Once VCC passes the power on reset threshold, the device is reset and enters into the Standby mode. This would also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once VCC drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is not recommended to send a command until the Vcc reaches its operating level.

Nevertheless, the following conditions on power supply are recommended.



Tr	Toff	Vbot
Below 5ms	Above 10ms	Below 0.1V

7 DEVICE ADDRESSING

The Master begins a transmission on by sending a Start condition, and then sends the address of the particular Slave devices to be communicated. The Slave device address is 8 bits format as shown in Fig. 5.

The four most significant bits of the Slave address are fixed (1010) for normal read/write operation, and 0110 for permanent write-protection operation.

The next three bits, A0, A1 and A2, of the Slave address are specifically related to EEPROM. Up to eight GT34C02 units can be connected to the 2-wire bus.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, Read operation is selected. While it is set to 0, Write operation is selected.

Memory Area Function	Slave Address							
	Device Type Identifier				Select Address Signals			R/W#
	D3	D2	D1	D0	A2	A1	A0	
Read/Write EEPROM memory	1	0	1	0	A2	A1	A0	R/W#
Set Write Protection (SWP)	0	1	1	0	0	0	1	0
Clear Write Protection (CWP)					0	1	1	0
Permanently Set Write Protection (PSWP)					A2	A1	A0	0
Read SWP					0	0	1	1
Read CWP					0	1	1	1
Read PSWP					A2	A1	A0	1

Note: D3 (MSB), R/W# (LSB)

After the Master transmits the Start condition and Slave address byte appropriately, the associated 2-wire Slave device, GT34C02, will respond with ACK on the SDA line. Then GT34C02 will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data.

The GT34C02 then prepares for a Read or Write operation by monitoring the bus.

WRITE OPERATION

Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/$\overline{W}$ set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the GT34C02. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The GT34C02 acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The GT34C02 is capable of 16-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 15

more bytes. After the receipt of each data word, the EEPROM responds immediately with an ACK on SDA line, and the four lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 16 bytes prior to issuing the Stop condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 16 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the GT34C02 in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the GT34C02 initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the GT34C02 has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

READ OPERATION

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read and sequential read.

Current Address Read

The GT34C02 contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the EEPROM receives the Slave Addressing Byte with a Read operation (R/W bit set to “1”), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the GT34C02 discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the GT34C02 acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The EEPROM then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 9. Random Address Read Diagram.)

Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the GT34C02 sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the GT34C02. The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition. The data output is sequential, with the data from address n followed by the data from address n+1,n+2 ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of the array is reached, the address counter "rolls over" to address 0, and the device continues to output data. (Refer to Figure 10. Sequential Read Diagram).

WRITE PROTECTION

Hardware Write Protection

The GT34C02 has two forms of software write protection and one form of hardware write protection. The hardware write protection is enabled when the WP input is held High. In this case, the entire array of the GT34C02 is read-only regardless of the status of the software protection. The hardware protection is disabled when the WP input is held Low or is floating. In this case, the upper half of the array (80h-FFh) can be modified by a valid Write command, and the lower half of the array (00h-7Fh) can be modified only if software write protection has not been enabled.

Reversible Software Write Protection

There is a non-volatile flag for each of the two forms of software write protection. When the bit value for either flag or both flags is 1, it is not possible to modify the contents of the lower 128 bytes of the array (00h-7Fh). If the bit value for both flags is 0, it is possible to modify this half of the array with a valid Write command, assuming WP is held Low or is floating. The device is shipped with both flags cleared. One of those flags is the Reversible Software Write Protection (RSWP) flag, and can be changed with the Set RSWP and Clear RSWP commands. The flag can also be verified without being changed with a Read SWP command. In order to set, clear or read the RSWP, The GT34C02 input pins must be as follows: A0 must be held to an extra high voltage of VHV (see DC Characteristics), while A2 and A1 must be set High, Low, or left floating, depending on the desired command (seed Figure 5). Once these input conditions are met, a command can be issued to the device.

The reversible software commands are initiated similarly to a normal byte write operation; however, the slave device address begins with the bit values 0110. The next three bits are A2=0, A1=0 or 1, and A0=1, so that they logically match the values on the input pins. If the last bit of the slave device address($R/\overline{W}$) is 0, the RSWP flag can be Cleared or Set. If $R/\overline{W}$ is 1, the flag can be verified with the Read SWP command. Following this bit, the device responds with either ACK or NoACK, depending on the exact command and the flag status (see Table1: Reversible Instructions). To complete the Set RSWP or Clear RSWP command, the Master must transmit a dummy address byte, a dummy data byte, and a Stop signal. To actually

modify the RSWP flag, WP should be held Low or be floating during entire command sequence. Before resuming any other command, the internal write cycle time should be observed. To complete the Read SWP Status or Read CSP Status command, the Master can transmit a Stop signal after the ACK/NoACK. The WP input is not evaluated for the Read SWP Status or Read CWP Status commands.

Permanent Software Write Protection

The GT34C02 contains a permanent software write protection (PSWP) feature. If the non-volatile PSWP flag has a bit value of 1, the array region of 00h-7Fh is protected from modification. If the PSWP flag has a bit value of 0, the write protection for the lower half of the array is determined solely by the statuses of RSWP and the WP input. After the PSWP flag is set to 1 via the Permanent Write Protect command, the protected area becomes irreversibly read-only despite power removal and re-application on the device. Once enabled, the permanent protection is independent of the status of the WP pin.

The Permanent Software Write Protect command is initiated similarly to a normal byte write operation; however, the slave device address begins with the bit values of 0110 (see figure 5). The following three bits are A2-A0, so that they logically match the values on the input pins. The last bit of the slave address ($R/\overline{W}$) is 0. The GT34C02 responds with either ACK or NoACK, depending on the flag status (see Table1: Permanent Instructions). Assuming an ACK is received, Master then must complete the sequence by transmitting a dummy address byte, dummy data byte, and a Stop signal (see Figure 11). The WP pin should be held Low or left floating during the entire command. Before resuming any other command, the internal write cycle should be observed.

The status of the PSWP can be safely determined without any changes by transmitting the same slave address as above, but with the last bit ($R/\overline{W}$) set to 1(see Figure 12). If the PSWP has been set, the GT34C02 will not acknowledge any slave address starting with bits 0110 (see Figure 5). To complete the command, the Master can transmit a Stop signal after the ACK/NoACK.

Table 1

Normal Instructions

Command	PSWP (Permanent)	RSWP (Reversible)	WP[1]	ACK command	Address	ACK Address	Data Byte	Data Byte ACK	Write Cycle
Read	X	X	X	ACK	00h-FFh	ACK	Data Byte	ACK	No
Write	0	0	0	ACK	00h-FFh	ACK	Data Byte	ACK	Yes
Write	X	X	1	ACK	00h-FFh	ACK	Data Byte	ACK	No
Write	1	X	X	ACK	00h-7Fh	ACK	Data Byte	ACK	No
Write	X	1	X	ACK	00h-7Fh	ACK	Data Byte	ACK	No
Write	X	X	0	ACK	80h-FFh	ACK	Data Byte	ACK	Yes

Permanent Instructions

Command	PSWP (Permanent)	RSWP (Reversible)	WP[1]	ACK command	Address	ACK Address	Data Byte	Data Byte ACK	Write Cycle
Read PSWP Status[4]	0	X	X	ACK	Dummy Address	ACK	Dummy Byte	ACK	No
Read PSWP Status	1	X	X	NoACK	-	-	-	-	No
Set PSWP	0	X	0	ACK	Dummy Address	ACK	Dummy Byte	ACK	Yes
Set PSWP	1	X	0	NoACK	-	-	-	-	No
Set PSWP	0	X	1	ACK	Dummy Address	ACK	Dummy Byte	ACK	No
Set PSWP	1	X	1	NoACK	-	-	-	-	No

Reversible Instructions

Command	PSWP (Permanent)	RSWP (Reversible)	WP[1]	ACK command	Address	ACK Address	Data Byte	Data Byte ACK	Write Cycle
Read SWP Status[4]	X	0	X	ACK	Dummy Address	ACK	Dummy Byte	ACK	No
Read SWP Status	X	1	X	NoACK	-	-	-	-	No
Read CWP status[3,4]	0	X	X	ACK	Dummy Address	ACK	Dummy Byte	ACK	No
Read CWP status[3]	1	X	X	NoACK	-	-	-	-	No
Set RSWP	X	0	0	ACK	Dummy Address	ACK	Dummy Byte	ACK	Yes
Set RSWP	X	1	0	NoACK	-	-	-	-	No
Set RSWP	X	0	1	ACK	Dummy Address	ACK	Dummy Byte	ACK	No
Set RSWP	X	1	1	NoACK	-	-	-	-	No
Clear RSWP	0	X	0	ACK	Dummy Address	ACK	Dummy Byte	ACK	Yes
Clear RSWP	1	X	0	NoACK	-	-	-	-	No
Clear RSWP	0	X	1	ACK	Dummy Address	ACK	Dummy Byte	ACK	No
Clear RSWP	1	X	1	NoACK	-	-	-	-	No

Notes:

1. WP = 1 if input level is High. WP=0 if input level is GND or floating
2. X = Don't Care
3. Read CWP Status yields the same result as Read PSWP Status
4. Read out Don't Care Dummy Address and Dummy Data is optional

Fig. 1: Typical System Bus Configuration

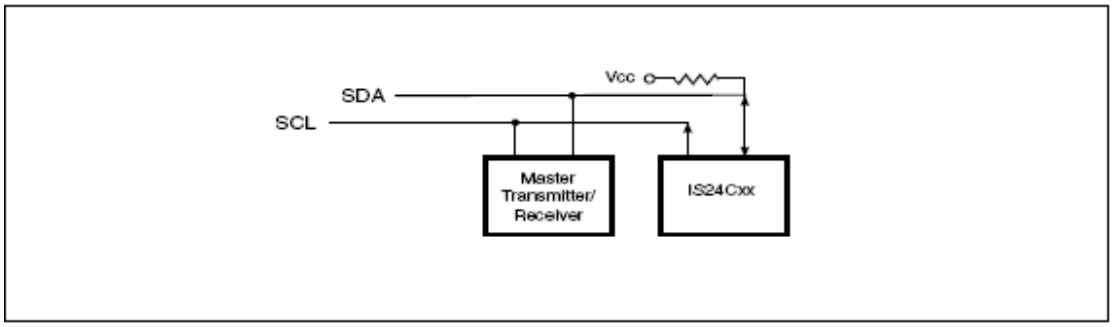


Fig. 2: output Acknowledge

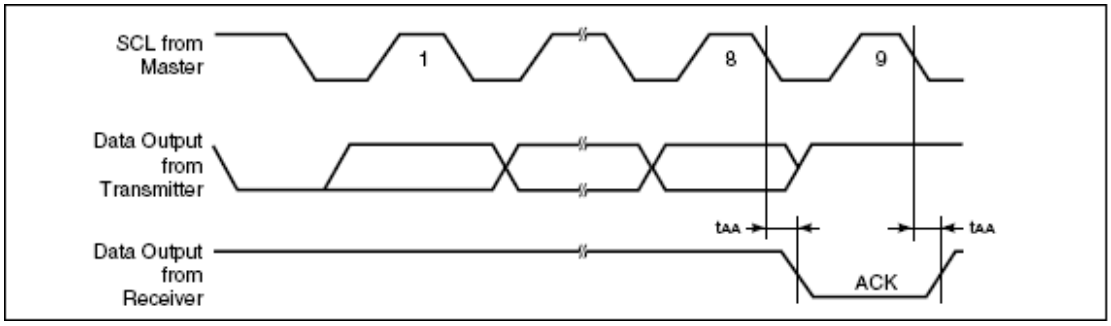


Fig. 3: Start and Stop Conditions

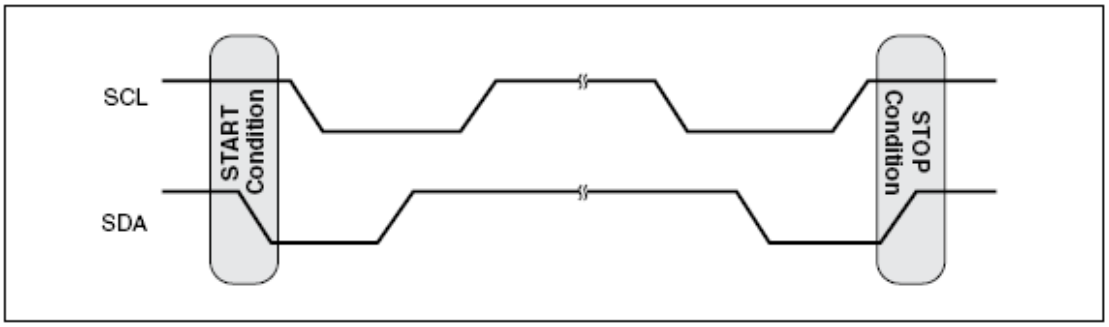


Fig. 4: Data Validity Protocol

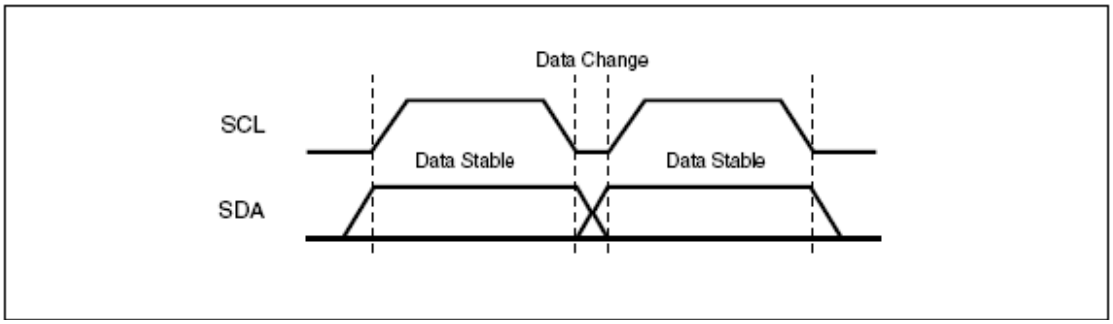


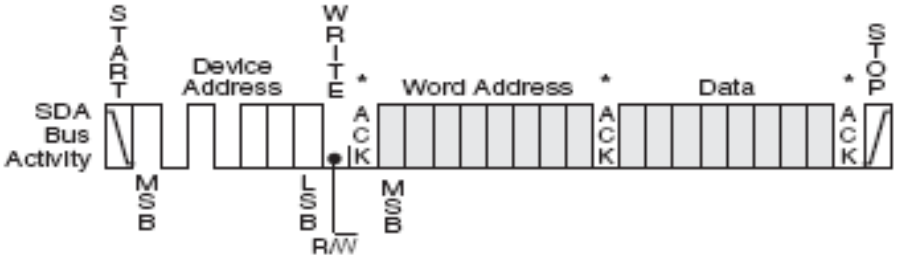
Fig. 5: Command Configuration

Pin Connection[1] **Slave Device Address**

A2	A1	A0	BIT	7	6	5	4	3	2	1	0	
A2	A1	A0		1	0	1	0	A2	A1	A0	R/$\overline{W}$	Normal Instruction[2]
A2	A1	A0		0	1	1	0	A2	A1	A0	R/$\overline{W}$	Permanent Write Protection Instruction[2]
GND	GND	VHV		0	1	1	0	0	0	1	0	Set Write Protection (SWP)
GND	VCC	VHV		0	1	1	0	0	1	1	0	Clear Write Protection (CWP)
GND	GND	VHV		0	1	1	0	0	0	1	1	Read SWP
GND	VCC	VHV		0	1	1	0	0	1	1	1	Read CWP

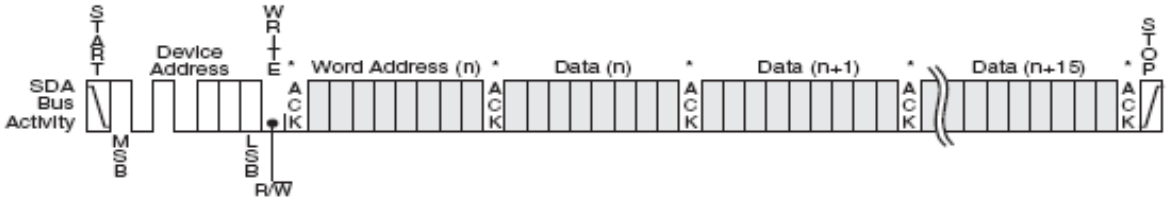
Note:
1. A2-A0 input pin connections must be GND (or floating), Vcc, or VHV.
2. Bits 1, 2, and 3 of the device address will be compared with the values on the external pins.

Fig. 6: Byte Write



* Acknowledges provided by the slave regardless of hardware or software Write Protection.

Fig. 7: Page Write



* Acknowledges provided by the slave regardless of hardware or software Write Protection.

Fig. 8: Current Address Read

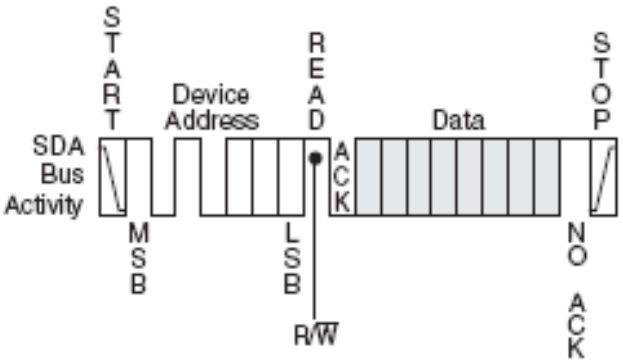


Fig. 9: Random Address Read

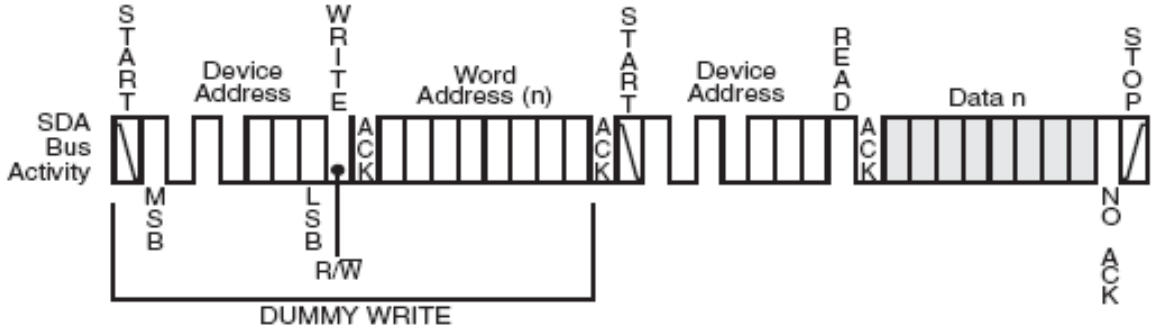


Fig. 10: Sequential Read

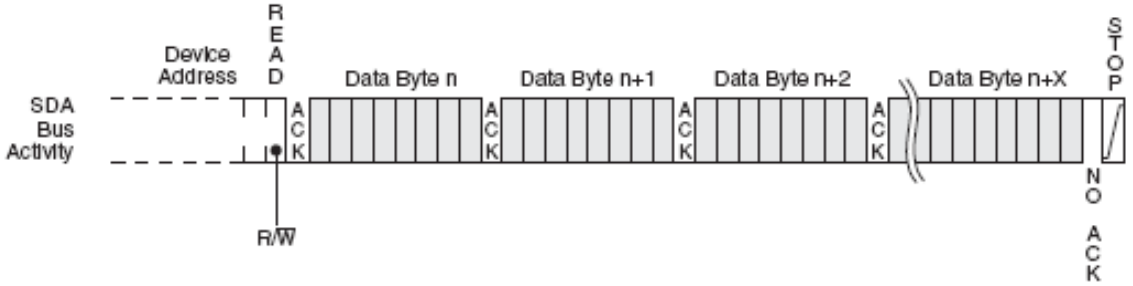
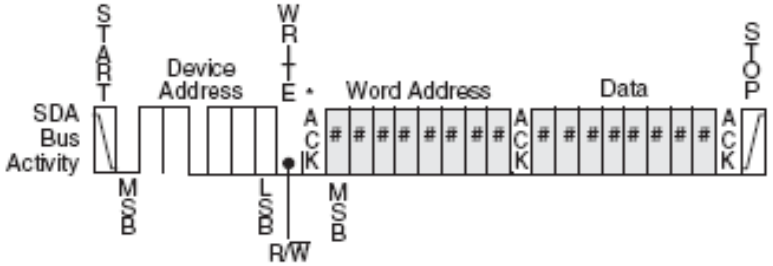


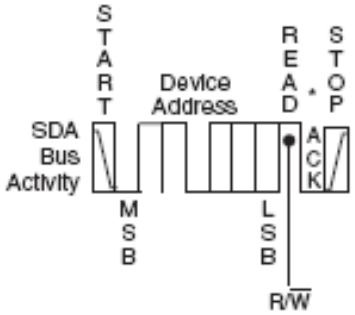
Fig. 11: Set Permanent Write Protection



* The slave does not provide an acknowledgement if the permanent write protection is already enabled.

Don't care bits are required.

Fig. 12: Read Permanent Write Protection



* The slave does not provide an acknowledgement if the permanent write protection is already enabled.

8 Maximum Absolute Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to + 4.2	V
V_P	Voltage on Any Pin	–0.5 to Vcc + 0.5	V
V_A	Voltage on A0 Pin	–0.5 to +10	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:
Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	–40°C to +85°C	1.7V to 3.6V

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

CAPACITANCE (1, 2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
$C_{I/O}$	Input /Output Capacitance	$V_{I/O}$ = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

9 DC Characteristics

Industrial: T_A = –40°C to +85°C, Vcc = 1.7V ~ 3.6V

Symbol	Parameter [1]	Vcc	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage			1.7	3.6	V
V_{IH}	Input High Voltage (SDA, SCL, WP)			0.7*V_{CC}	V_{CC}+0.5	V
V_{IL}	Input Low Voltage (SDA, SCL, WP)			-1	0.3* V_{CC}	V
V_{HV}	A0 High Voltage		$V_{HV} - V_{CC} \geq 4.8V$	7	10	V
I_{LI}	Input Leakage Current (SDA, SCL, WP, A0, A1 & A2)	3.6V	V_{IN} = 0V ~ V_{CC}, standby mode	--	3	µA
I_{LO}	Output Leakage Current	3.6V	V_{OUT} = 0V~V_{CC}, SDA in Hi-Z	--	3	µA
V_{OL1}	Output Low Voltage	1.7V	I_{OL} = 0.15 mA	—	0.2	V
V_{OL2}	Output Low Voltage	3.6V	I_{OL} = 2.1 mA	—	0.4	V
I_{SB1}	Standby Current	1.7V	V_{IN} = Vcc or GND	—	1	µA
		3.6V	V_{IN} = Vcc or GND	—	2	µA
I_{CC1}	Read Current	1.7V	Read at 100 KHz	—	1	mA
		3.6V	Read at 400 KHz	—	3	mA
I_{CC2}	Write Current	1.7V	Write at 100 KHz	—	1	mA
		3.6V	Write at 400 KHz	—	3	mA

Notes: [1] The parameters are characterized but not 100% tested.

10 AC Characteristics

T_A = –40°C to +85°C, Supply voltage = 1.7V to 3.6V

Symbol	Parameter [1] [2]	1.7V ≤ Vcc < 3.6V		2.2V ≤ Vcc < 3.6V		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCK Clock Frequency		100		400	KHz
T_{LOW}	Clock Low Period	4700	—	1200	—	ns
T_{HIGH}	Clock High Period	4000	—	600	—	ns
T_R	Rise Time (SCL and SDA)	—	1000	—	300	ns
T_F	Fall Time (SCL and SDA)	—	300	—	300	ns
$T_{SU:STA}$	Start Condition Setup Time	4000	—	600	—	ns
$T_{SU:STO}$	Stop Condition Setup Time	4000	—	600	—	ns
$T_{HD:STA}$	Start Condition Hold Time	4000	—	600	—	ns
$T_{HD:STO}$	Stop Condition Hold Time	4000	—	600	—	ns
$T_{SU:DAT}$	Data In Setup Time	100	—	100	—	ns
$T_{HD:DAT}$	Data In Hold Time	0	—	0	—	ns
T_{AA}	Clock to Output Access time (SCL Low to SDA Data Out Valid)	100	3500	50	900	ns
T_{DH}	Data Out Hold Time (SCL Low to SDA Data Out Change)	100	—	50	—	ns
T_{WR}	Write Cycle Time	—	5	—	5	ms
T_{BUF}	Bus Free Time Before New Transmission	4700	—	1200	—	ns
$T_{SU:WP}$	WP pin Setup Time	4000	—	600	—	ns
$T_{HD:WP}$	WP pin Hold Time	4700	—	1200	—	ns
T	Noise Suppression Time	—	100	—	50	ns

Notes: [1] The parameters are characterized but not 100% tested.

[2] AC measurement conditions:

R_L (connects to Vcc): 1.3 kΩ (2.2V, 3.6V), 10 kΩ (1.7V)

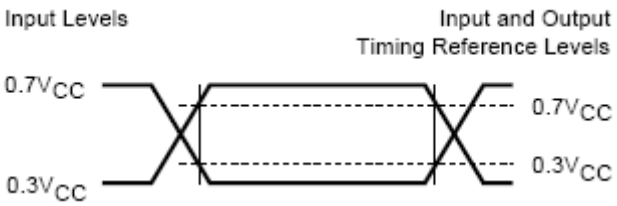
C_L = 100 pF

Input pulse voltages: 0.3*Vcc to 0.7*Vcc

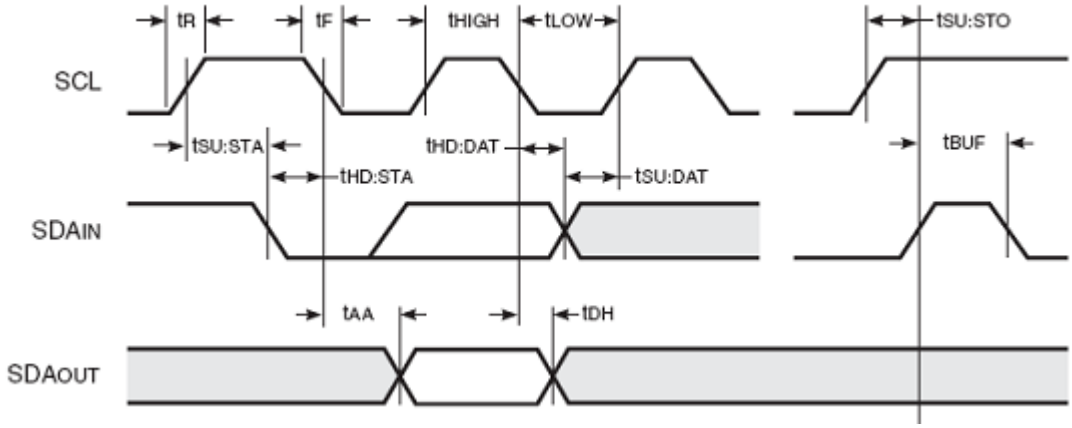
Input rise and fall times: ≤ 50 ns

Timing reference voltages: half Vcc level

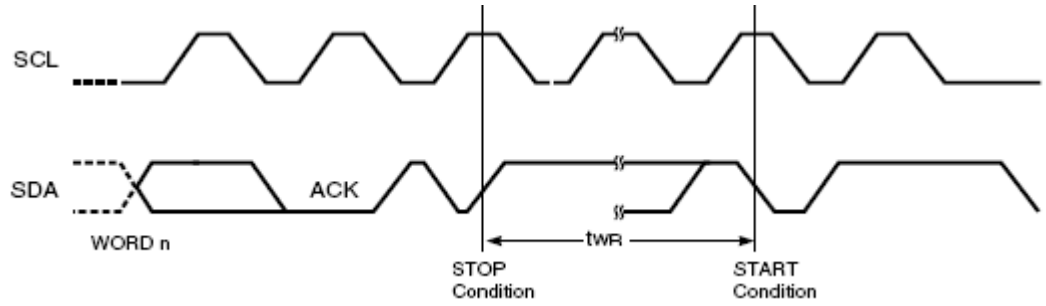
AC measurement I/O waveform



AC timing consideration:



Write cycle Timing:



11 Ordering Information

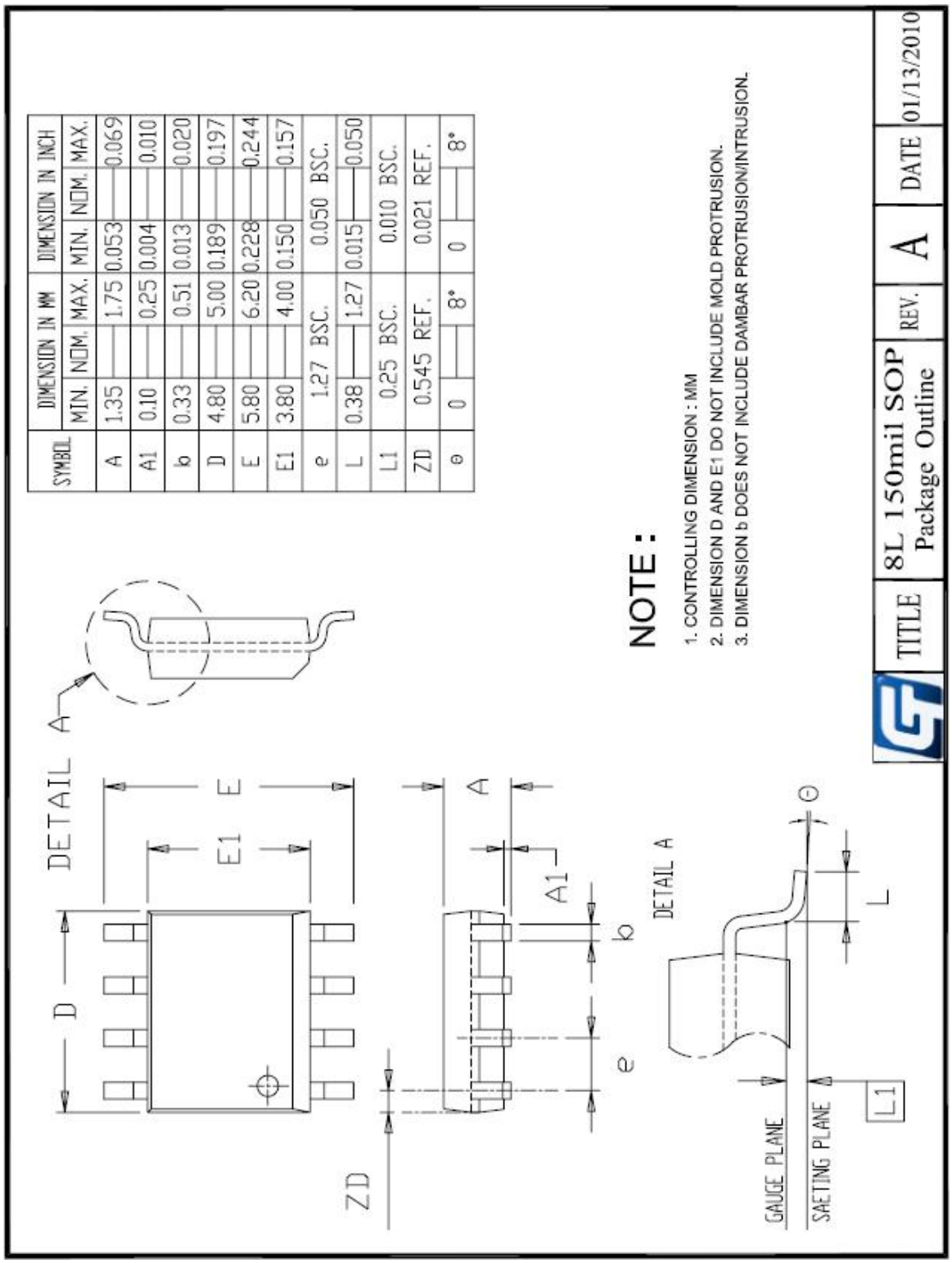
Voltage Range	Part Number	Package (8 Pins)
1.7V to 3.6V	GT34C02-2UDLI-TR	Ultra-thin DFN 2 x 3 x 0.6 (max.) mm
	GT34C02-2GLI-TR	150-mil SOIC/SOP (JEDEC)
	GT34C02-2ZLI-TR	3 x 4.4 mm TSSOP

Note:

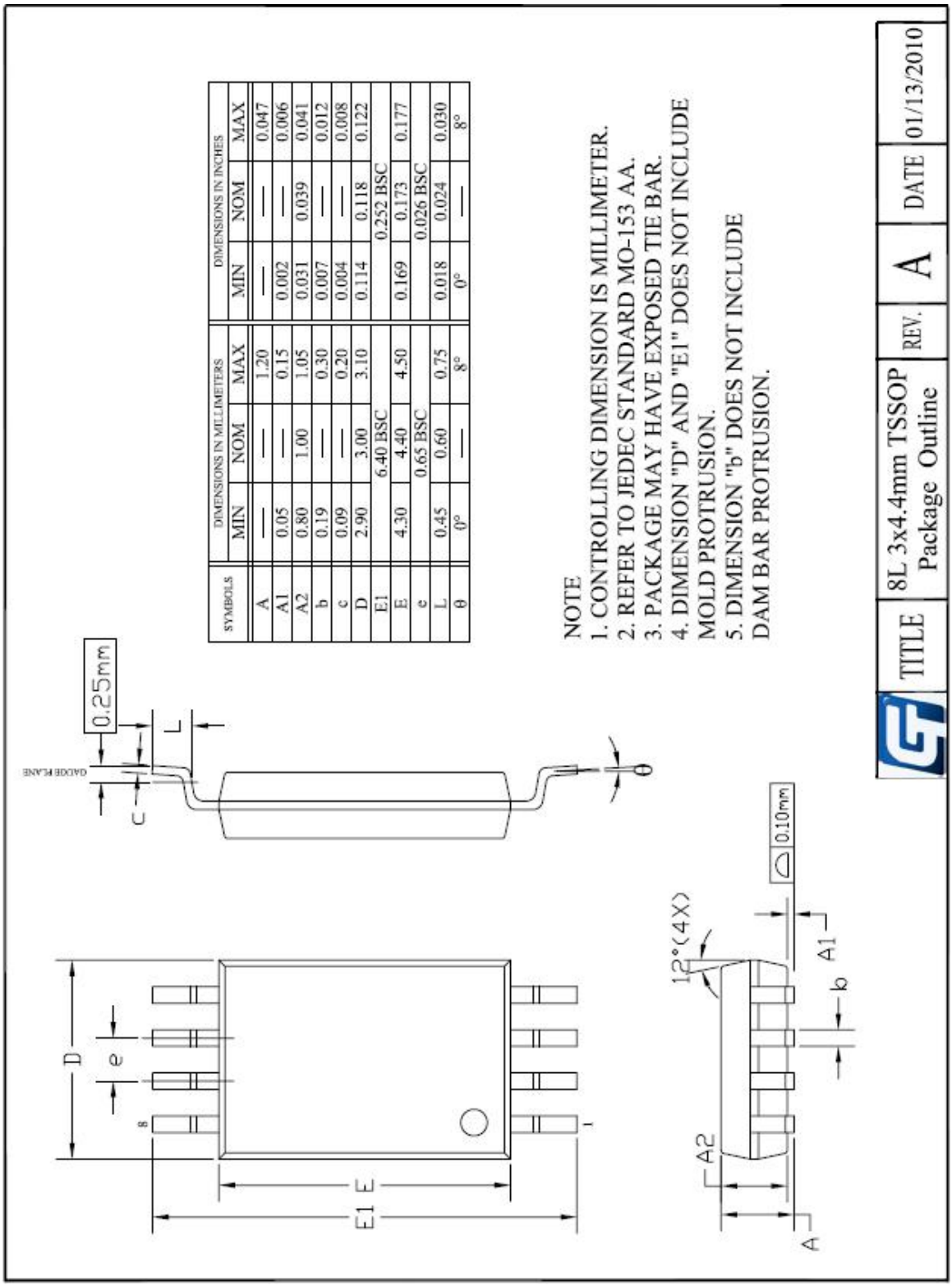
1. Contact Giantec Sales Representatives for availability and other information.
2. The listed part numbers are packed in tape and reel "-TR" (4K per reel). UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free, or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

12 Package

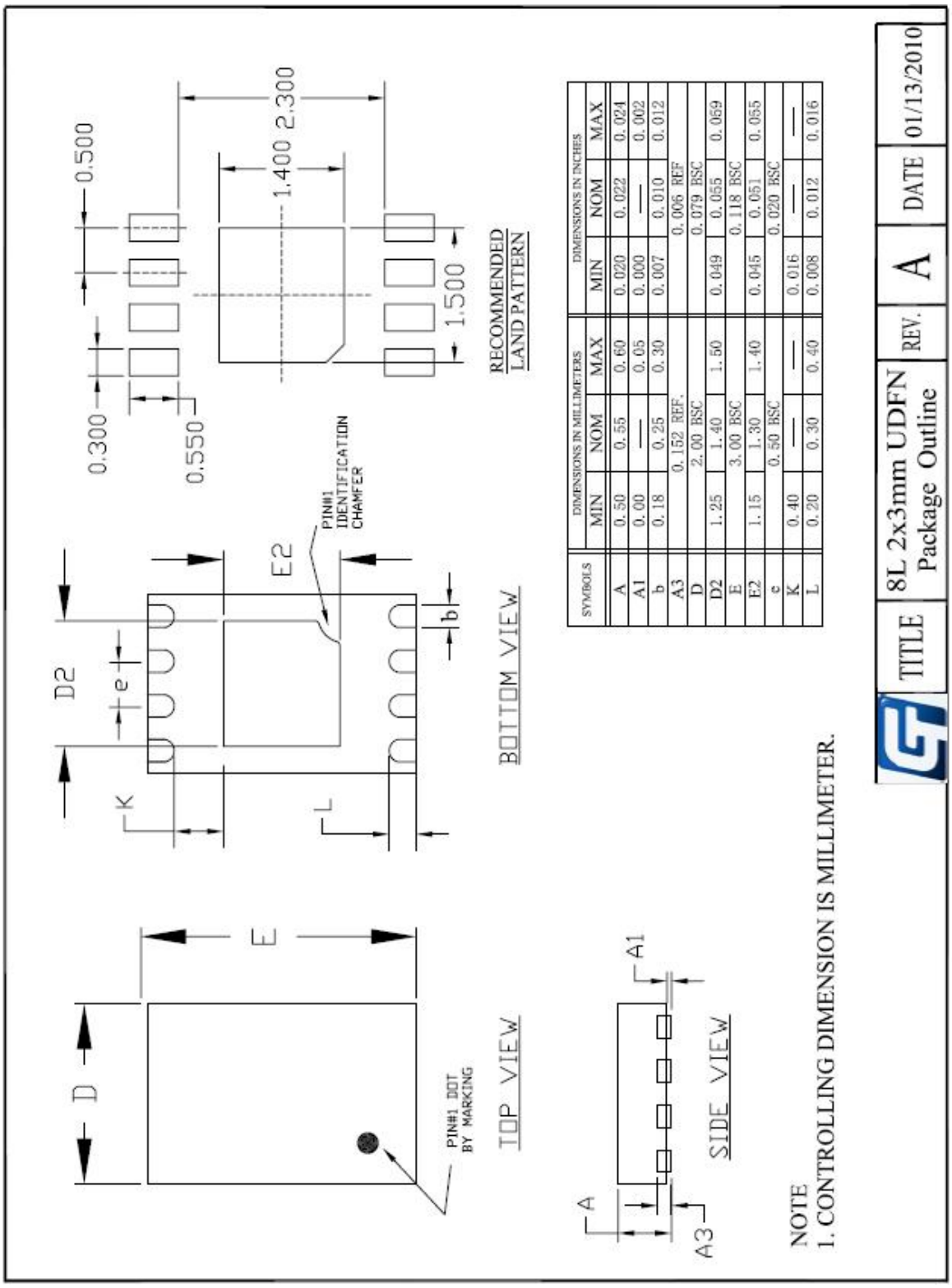
SOIC/SOP (JEDEC)



TSSOP


TITLE
8L 3x4.4mm TSSOP Package Outline
REV.
A
DATE
01/13/2010
NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
2. REFER TO JEDEC STANDARD MO-153 AA.
3. PACKAGE MAY HAVE EXPOSED TIE BAR.
4. DIMENSION "D" AND "E1" DOES NOT INCLUDE MOLD PROTRUSION.
5. DIMENSION "b" DOES NOT INCLUDE DAM BAR PROTRUSION.
SYMBOLS
DIMENSIONS IN MILLIMETERS
DIMENSIONS IN INCHES
MIN NOM MAX
A — — 1.20 — — 0.047
A1 0.05 — 0.15 0.002 — 0.006
A2 0.80 1.00 1.05 0.031 0.039 0.041
b 0.19 — 0.30 0.007 — 0.012
c 0.09 — 0.20 0.004 — 0.008
D 2.90 3.00 3.10 0.114 0.118 0.122
E1 6.40 BSC 0.252 BSC
E 4.30 4.40 4.50 0.169 0.173 0.177
e 0.65 BSC 0.026 BSC
L 0.45 0.60 0.75 0.018 0.024 0.030
θ 0° — 8° 0° — 8°
0.25mm
GAUGE PLANE
c
L
θ
D
e
8
1
E1
E
12°(4X)
0.10mm
A1
b
A2
A

Ultra-thin DFN (UDFN)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	—	0.05	0.000	—	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A3		0.152 REF.			0.006 REF	
D		2.00 BSC			0.079 BSC	
D2	1.25	1.40	1.50	0.049	0.055	0.069
E		3.00 BSC			0.118 BSC	
E2	1.15	1.30	1.40	0.045	0.051	0.055
e		0.50 BSC			0.020 BSC	
K	0.40	—	—	0.016	—	—
L	0.20	0.30	0.40	0.008	0.012	0.016

13 REVISION HISTORY

Revision	Date	Descriptions
a0	April 2010	Initial draft