Advanced

GT34C04

4K Bits

SPD EEPROM

Table of Contents

1. Features

- Supply voltage: 1.7V to 3.6V
- JEDEC JC42.4 (EE1004-v) Serial Presence Detect (SPD) compliant
- 2-wire serial interface I^2C/SMBus compatible
  - Bus Timeout Supported
- Speed up to 1 MHz in I^2C bus (Fast Mode) and 100KHz in SMBus 2.0
- Low operating current
  - Standby Current less than 1 μA (1.7V)
  - Write Current less than 0.5 mA (3.6V)
  - Read Current less than 0.2 mA (3.6V)
- Byte and Page (up to 16 bytes) Write Operations
  - Partial Page-writes permitted
- Random and Sequential Read modes
- Self-Time Write Cycle (5ms, max)
- Data Protection Features Reversible Software Protection for four individual 128-Byte block
- Filtered Inputs for Noise Suppression
- More than 1 million Erase/Write Endurance Cycles
- More than 100 years Data Retention
- Packages: UDFN, TSSOP and SOIC copper wire package
- Operating Temperature range: -40°C to +125°C

2. General Description

The GT34C04 is a 4K-bit Serial Presence Detect (SPD) EEPROM, which is fully compatible to industrial standard I^2C/SMBus interface and compliant to the JEDEC JC42.4 (EE1004-v) specification. The EEPROM memory is organized as two pages of 256 bytes each or 512 bytes of total memory. Each page is comprised of two 128-byte blocks. The devices are able to selectively lock the data in any or all of the four 128-byte blocks.

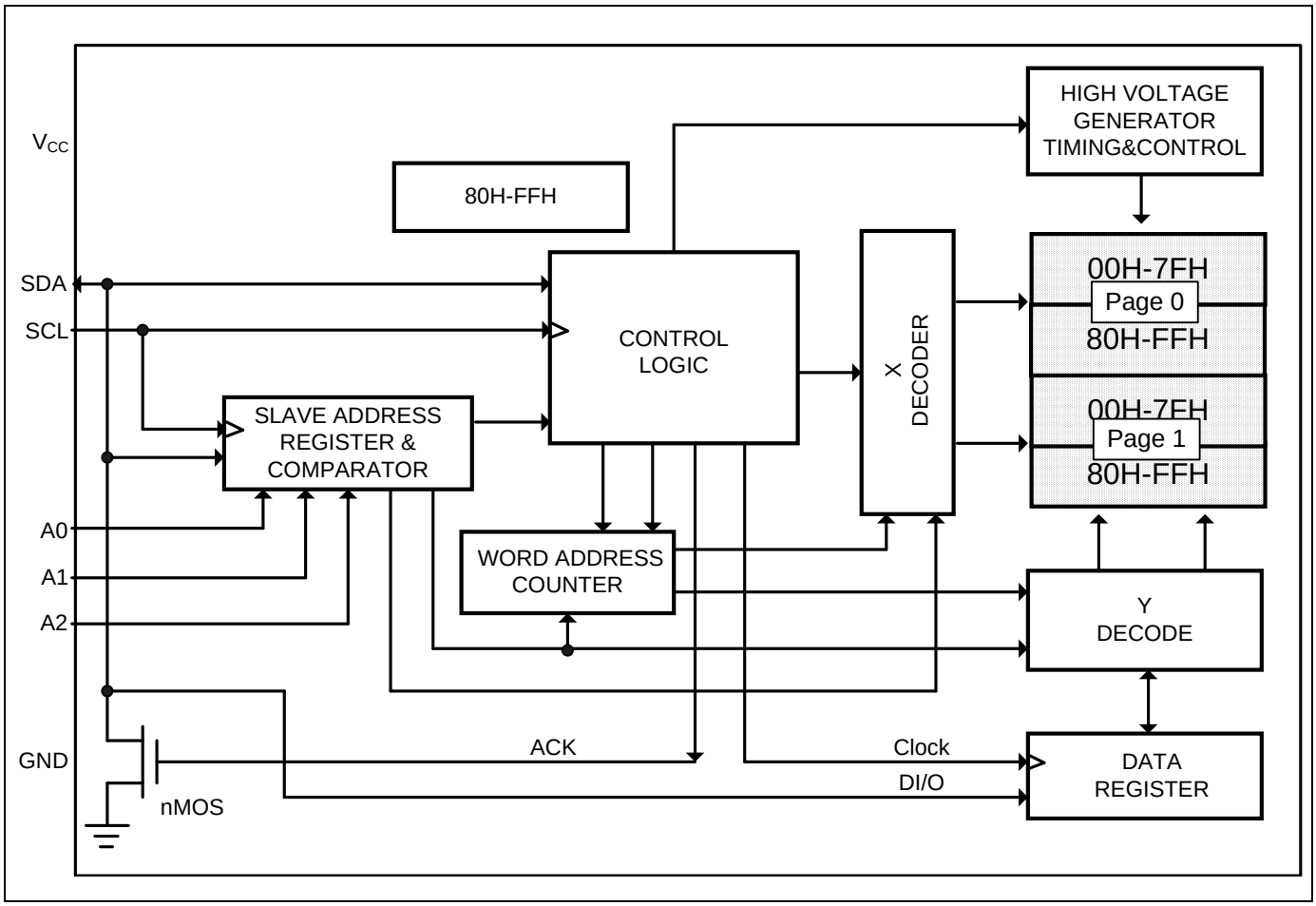
This product is designed for memory module applications in most PC and Server platforms, as well as other related applications. All the information concerning the DRAM module configuration (such as its access speed, its size, and its organization) can be kept write protected in one or more of the blocks of memory.

The GT34C04 is protocol-compatible with the previous generation of 2-Kbit devices, GT34C02A. The page selection method allows commands used with legacy devices such as GT34C02A to be applied to the lower or upper pages of the EEPROM.

The GT34C04 operate the SMBus bus in the 1.7 V - 3.6 V voltage range, with a maximum of 1 MHz transfer rate. The operating temperature range is from -40°C to +125°C. The device is offered in Lead-free, RoHS, halogen free or Green package.

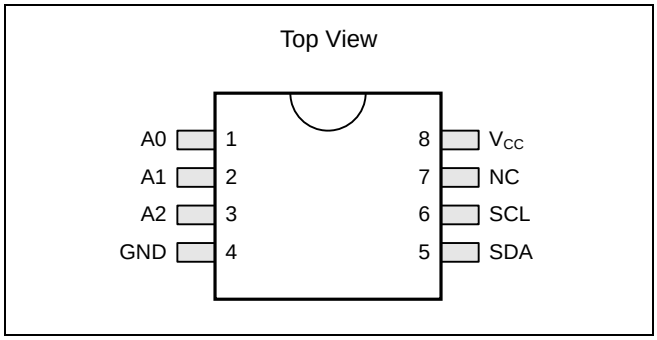
In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, the device does not respond to any instructions until the supply voltage (VCC) has reached an acceptable stable level above the reset threshold voltage. Once VCC passes the power on reset threshold, the device is reset and enters into the Standby mode. This would also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once VCC drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is not recommended to send an command until the VCC reaches its operating level.

3. Functional Block Diagram

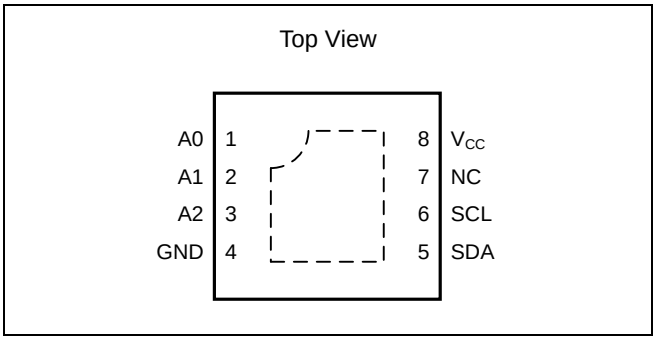


4. Pin Configuration

4.1 8-Pin SOIC and TSSOP



4.2 8-Lead UDFN



4.3 Pin Definition

Pin No.	Pin Name	I/O	Definition
1	SA0	I	Device Address Input
2	SA1	I	Device Address Input
3	SA2	I	Device Address Input
4	GND	-	Ground
5	SDA	I/O	Serial Address, Data input and Data output (Open drain)
6	SCL	I	Serial Clock Input
7	NC	-	Not connected internally
8	V_{CC}	-	Power Supply

Note: Thermal sensing devices also have a heat paddle, typically connected to the application ground plane.

4.4 Pin Descriptions

SCL

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor can be connected from Serial Clock (SCL) to V_{CC}. (Figure 4.1 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

SDA

The bi-directional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-ORed with other open drain or open collector signal on the bus. A pull up resistor must be connected from Serial Data (SDA) to the most positive V_{CC} in the I^2C Bus chain. (Figure 4.1 indicates how the value of the pull-up resistor can be calculated).

SA0, SA1, SA2

These input signals are used to create the Logical Serial Address LSA that is compared to the three least significant bits(b3, b2, b1) of the 7-bit Slave Address.(Pls refer to table 5.1 for details on LSA encoding).

The SA0 input is also used to detect the V_{HV} voltage when decoding a SWPn or CWP instruction. (Pls refer to table5.1 for decode details).

NC

The NC pin is not bonded to a die pad.

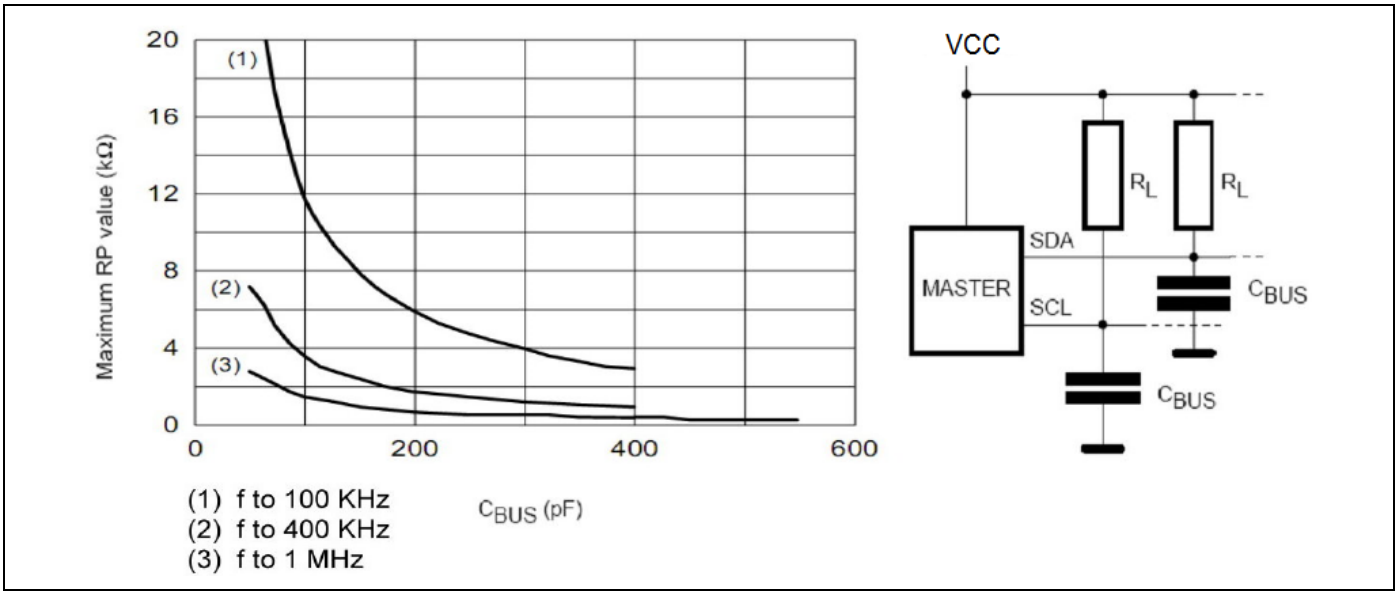
GND

Ground of supply voltage.

.**Vcc**

Supply voltage.

Figure 4.1 Maximum RL Value Versus Bus Capacitance (CBUS) for an I²C Bus



5. I²C / SMBus Serial Interface

5.1 Serial bus interface

The GT34C04 behaves as a slave device in the I²C Bus protocol, with all operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and R/$\overline{W}$ bit (as described in Table5.1), terminated by an acknowledge bit. GT34C04 shall not initiate clock stretching, which is an optional I²C Bus feature.

In accordance with the I²C Bus definition, the GT34C04 use three (3) built-in, 4-bit Device Type Identifier Codes (DTIC) and a 3-bit Select Address to generate an I²C Bus Slave Address.

The EE memory may be accessed using a DTIC of (1010), and to perform the SWPn, RSPn, or CWP operations a DTIC of (0110) is required.

5.2 I²C / SMBus Communication

When writing data to the memory, an acknowledge bit is inserted during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Bus Master generated STOP condition after an Ack for WRITE, and after a NoAck for READ. Violations of the command protocol result in unpredictable operation.

5.3 Start Condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the High state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

5.4 Stop Condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven High. A Stop condition terminates communication between the device and the bus master.

A Read command that is followed by NoAck can be followed by a Stop condition to force the EE into Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

5.5 Acknowledge

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it is bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) Low to acknowledge the receipt of the eight data bits. The no-acknowledge bit is used to indicate the completion of a block read operation, or an attempt to modify a write-protected register. The bus master releases Serial Data (SDA) after sending eight bits of data, and during the 9th clock pulse period, and does not pull Serial Data (SDA) Low.

5.6 Slave address

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the Device Select Code, shown in Table 5.2 (on Serial Data (SDA), most significant bit first). The Device Select Code consists of a 4-bit Device Type Identifier, and a 3-bit Select Address. To address the EE memory array, the 4-bit Device Type Identifier is 1010b; to access the write protection settings or EE page address, it is 0110b. Additionally, writing or clearing the reversible EE write protect requires that SA0 be raised to the V_{HV} voltage level.

Up to eight devices can be connected on a single I²C Bus. Each one is given a unique 3-bit Logical Serial Address code. The LSA is a decoding of information on the SA pins SA0, SA1, and SA2 as described in Table 5.2. When the Device Select Code is received, the device only responds if the Select Address is the same as the Logical Serial Address. Write Protection commands SWPn, CWP, and RPSn, and the EE Page Address commands SPAn and RPA, do not use the Select Address or Logical Serial Address, therefore all devices on the I²C Bus will act on these commands simultaneously. Since it is impossible to determine which device is responding to RPSn or RPA commands, for example, these functions are primarily used

for external device programmers rather than in-system applications.

The 8th bit is the Read/Write bit (R/$\overline{W}$). This bit is set to 1 for Read and 0 for Write operations. If a match occurs on the Device Select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the Device Select code, the EE section deselects itself from the bus, and goes into Standby mode. The I^2C Bus operating modes are detailed in Table 5.1.

5.7 Power-Up and Reset States

5. 7.1 Power-Up Condition

In order to prevent inadvertent operations during power up, a Power On Reset (POR) circuit is included. On cold power on, V_{CC} must rise monotonically between V_{PON} and V_{CC}(min) without ring back to ensure proper startup. Once V_{CC} has passed the V_{PON} threshold, the device is reset.

Prior to selecting the memory and issuing instructions, a valid and stable V_{CC} voltage must be applied, and no command may be issued to the device for T_{INIT}. The supply voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (T_W).

At power down (phase during which V_{CC} decreases continuously), as soon as V_{CC} drops from the normal operating voltage below the minimum operating voltage, the device stops responding to commands. On warm power cycling, V_{CC} must remain below V_{POFF} for T_{POFF}, and must meet cold power on reset timing when restoring power.

The devices are delivered with all bits in the EEPROM memory array set to '1' (each byte contains 0xFF).

5. 7.2 Software reset

The GT34C04 contains a reset function in case the 2-wire bus transmission on is accidentally interrupted (e.g. a power loss), or needs to be terminated mid-stream. The reset is initiated when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

Table 5.1 I²C Bus Operating Mode

Mode	R/$\overline{W}$ Bit	Bytes	Initial Sequence
EEPROM Current Address Read	1	1	START, Device Select, R/$\overline{W}$ =1
EEPROM Random Address Read	0	1	START, Device Select, R/$\overline{W}$ =0, Address
	1		reSTART, Device Select, R/$\overline{W}$ =1
EEPROM Sequential Read	1	≥1	Similar to Current or Random Address Read
EEPROM Byte Write	0	1	START, Device Select, R/$\overline{W}$ =0, Data, STOP
EEPROM Page Write	0	≤16	START, Device Select, R/$\overline{W}$ =0, Data, STOP

Table 5.2 Device Select Code

Function	Abbr	Device Type Identifier[1]				Select Address[2,4]			R/$\overline{W}$	SA0 Pin[3]
		B7	B6	B5	B4	B3	B2	B1		
Read EE Memory	RSPD	1	0	1	0	LSA2	LSA1	LSA0	1	0 or 1
Write EE Memory	WSPD								0	
Set Write Protection, Block0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, Block1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, Block2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, Block3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, Block0	RPS0					0	0	1	1	0,1, or V_{HV}
Read Protection Status, Block1	RPS1					1	0	0	1	0,1, or V_{HV}
Read Protection Status, Block2	RPS2					1	0	1	1	0,1, or V_{HV}
Read Protection Status, Block3	RPS3					0	0	0	1	0,1, or V_{HV}
Set EE Page Address to 0[5]	SPA0					1	1	0	0	0,1, or V_{HV}
Set EE Page Address to 1[5]	SPA1					1	1	1	0	0,1, or V_{HV}
Read EE Page Address to 0[6]	RPA					1	1	0	1	0,1, or V_{HV}
Reserved	--					All Other Encodings				

Note: [1] The most significant bit, b7, is sent first.

[2] Logical Serial Addresses (LSA) are generated by the combination of inputs on the SA pins

[3] SA0 pin is driven to 0 = GND, 1 = V_{CC}, or V_{HV}

[4] For backward compatibility with previous devices, the order of block select bits (b3 and b1) are not a simple binary encoding of the block number.

[5] Set EE page address to 0 selects the lower 256 bytes of EEPROM, setting to 1 selects the upper 256 bytes of EEPROM. Subsequent Read EE or Write EE commands operate on the selected EE page.

[6] Reading the EE page address results in Ack when the current page is 0 and NoAck when the current page is 1.

[7] Permanent Write Protect features have been eliminated from the devices.

[8] GT34C04 Only

Figure 5.1 V_{CC} Ramp Up and Ramp Down

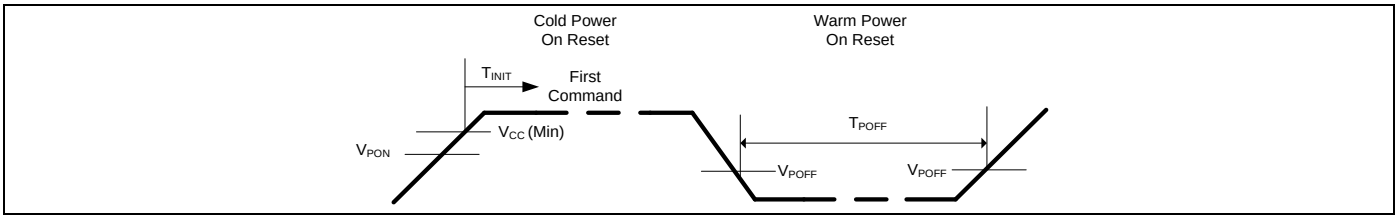


Figure 5.2. Typical System Bus Configuration

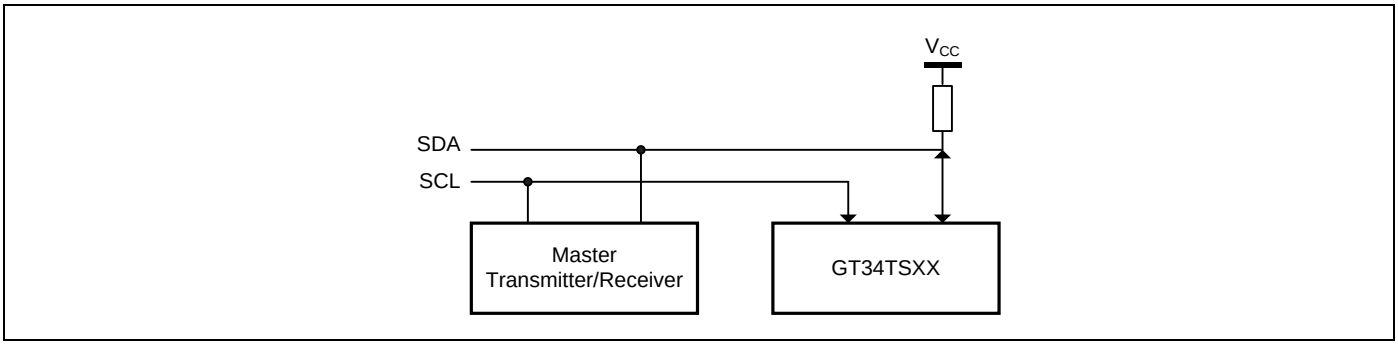


Figure 5.3. Start and Stop Conditions

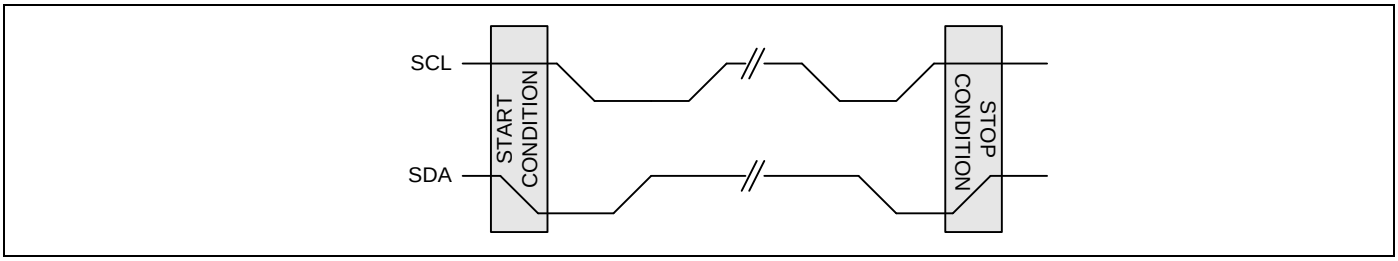


Figure 5.4. Data Validity Protocol

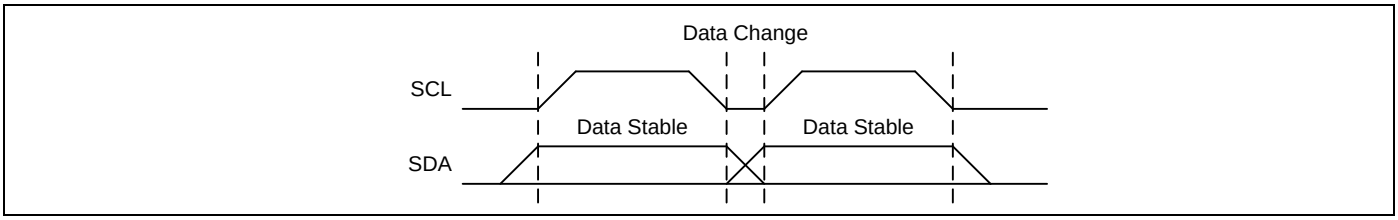


Figure 5.5. Output Acknowledge

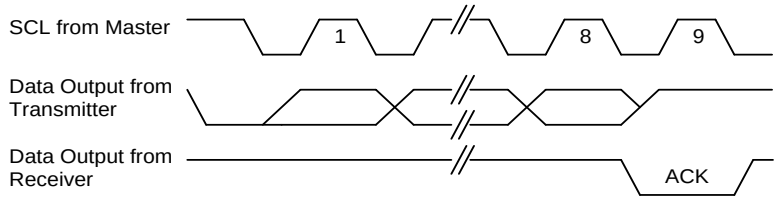


Figure 5.6. Bus Timing

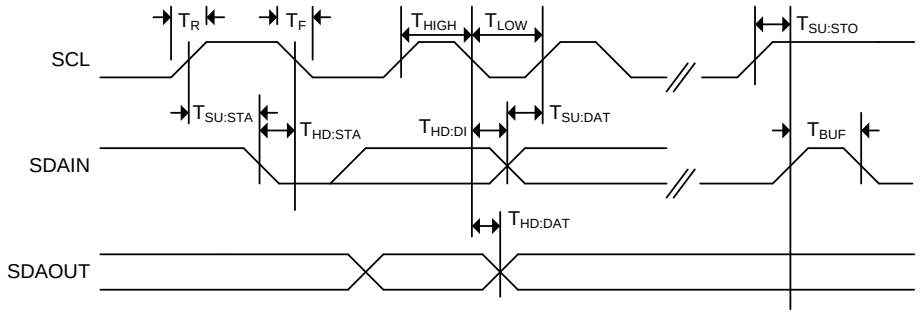


Figure 5.7. Write Cycle Timing

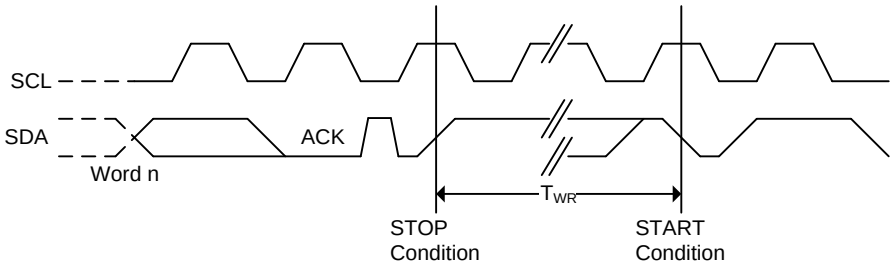
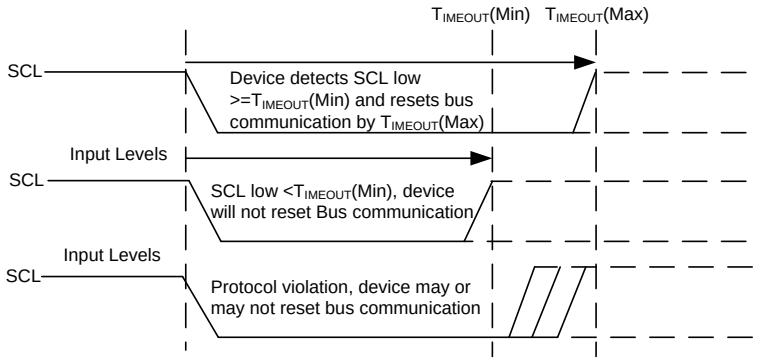


Figure 5.8. Bus Timeout Waveform



6. EEPROM Functional Description

6.1 Write Operation

Following a Start condition the bus master sends a Device Select Code with the R/$\overline{W}$ bit reset to 0. The device acknowledges this, as shown in Figure 6.1 and 6.2, and waits for an address byte. The device responds to the address byte with an acknowledge bit, and then waits for the data byte.

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

During the internal Write cycle, Serial Data (SDA) and Serial Clock (SCL) are ignored by the EE, and the EE device does not respond to any requests.

The device has an internal address counter which is incremented each time a byte is written. If a Write operation is performed to a protected block, the internal address counter is not incremented.

6.1.1 Byte Write

After the Device Select Code and the address byte, the bus master sends one data byte. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. After the byte is transferred, the internal byte address counter is incremented unless the block is write protected. The bus master terminates the transfer by generating a Stop condition, as shown in Figure 6.1.

6.1.2 Page Write

The Page Write mode allows up to 16 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits are the same. If more bytes are sent than will fit up to the end of the page, a condition known as "roll-over' occurs. This should be avoided, as data starts to be over-written in an implementation dependent fashion.

The bus master sends from 1 to 16 bytes of data, each of which is acknowledged by the device. If the addressed location is write-protected, the device replies to the data byte with NoAck, and the locations are not modified. After each byte is transferred, the internal byte address counter is incremented unless the block is write-protected. The transfer is terminated by the bus master generating a Stop condition, as shown in Figure 6.2.

6.1.3 Write Cycle Polling Using ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (T_W) is shown in AC Electric characteristic table, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in Figure 6.9, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a Device Select Code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, NoAck will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

6.2 Read Operation

Read operations are performed independent of the software protection state.

The device has an internal address counter which is incremented each time a byte is read.

6.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in Figure 6.3) but without sending a Stop condition. Then, the bus master sends another Start condition, and repeats the Device Select Code, with the R/$\overline{W}$ bit set to 1. The device acknowledges this,

and outputs the contents of the addressed byte. The bus master must not acknowledge the byte, and terminates the transfer with a Stop condition.

6.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a Device Select Code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in Figure 6.4, without acknowledging the byte.

6.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master does acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must not acknowledge the last byte, and must generate a Stop condition, as shown in Figure 6.5.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 0x00.

6.2.4 Acknowledge In Read Mode

For all Read commands to the SPD, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) Low during this time, the device terminates the data transfer and returns to an idle state to await the next valid START condition. This has no effect on the TS operational status, as shown in Table 6.2.

6.3 Write Protection

6.3.1 Software Write Protection

The devices have three software commands for setting, clearing, or interrogating the write-protection status.

- SWPn: Set Write Protection for Block n
- CWP: Clear Write Protection for all blocks
- RPSn: Read Protection Status for Block n

There are four independent memory blocks, and each block may be independently protected. The memory blocks are:

- Block 0 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 0
- Block 1 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 0
- Block 2 = memory addresses 0x00 to 0x7F (decimal 0 to 127), SPD Page Address = 1
- Block 3 = memory addresses 0x80 to 0xFF (decimal 128 to 255), SPD Page Address = 1

The level of write-protection (set or cleared) that has been defined using these instructions, remains defined even after a power cycle.

6.3.2 Set and Clear Write Protection

If the software write-protection has been set with the SWPn instruction, it may be cleared again with a CWP instruction. SWPn acts on a single block as specified in the SWPn command, but CWP clears write protection for all blocks, as shown in Figure 6.6 and Table 6.1.

6.3.3 Read Protection Status

The controller issues a RPSn command specifying which block to report upon. If Software Write Protection has not been set, the device replies to the data byte with an Ack. If Software Write Protection has been set, the device replies to the data byte with a NoAck, as shown in Figure 6.7 and Table 6.2.

6.3.4 Read SPD Page Address

The controller issues an RPA command to determine if the currently selected SPD page is 0 (device returns Ack) or 1 (device returns NoAck).

6.3.5 Set SPD Page Address

The controller issues an SPAn command to select the lower 256 bytes (SPA0) or upper 256 bytes (SPA1) as shown in figure 6.8. After a cold or warm power-on reset, the SPD Page Address is always 0, selecting the lower 256 bytes.

Figure 6.1 Byte Write

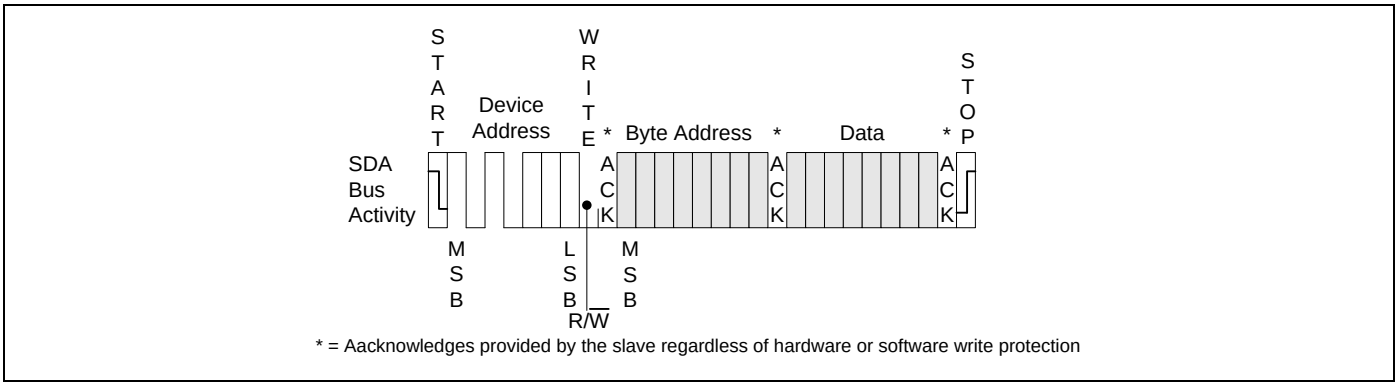


Figure 6.2 Page Write

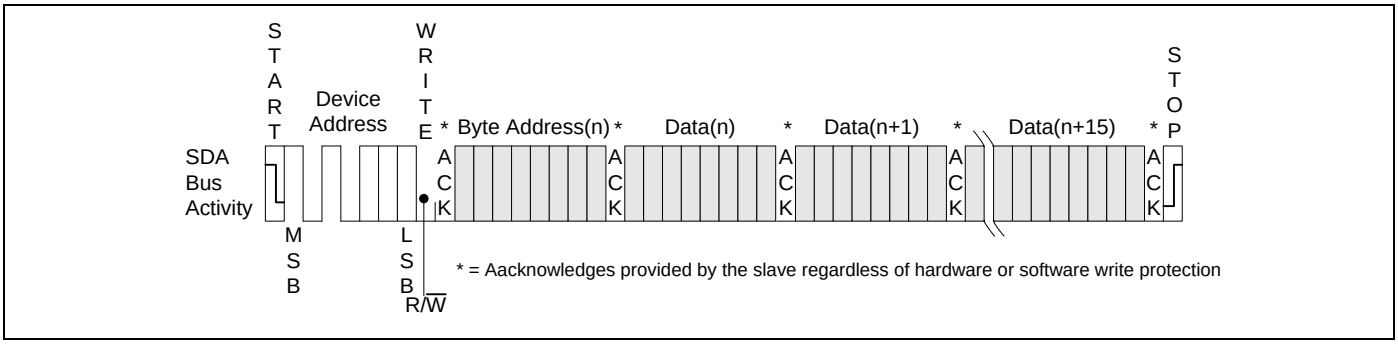


Figure 6.3 Random Address Read

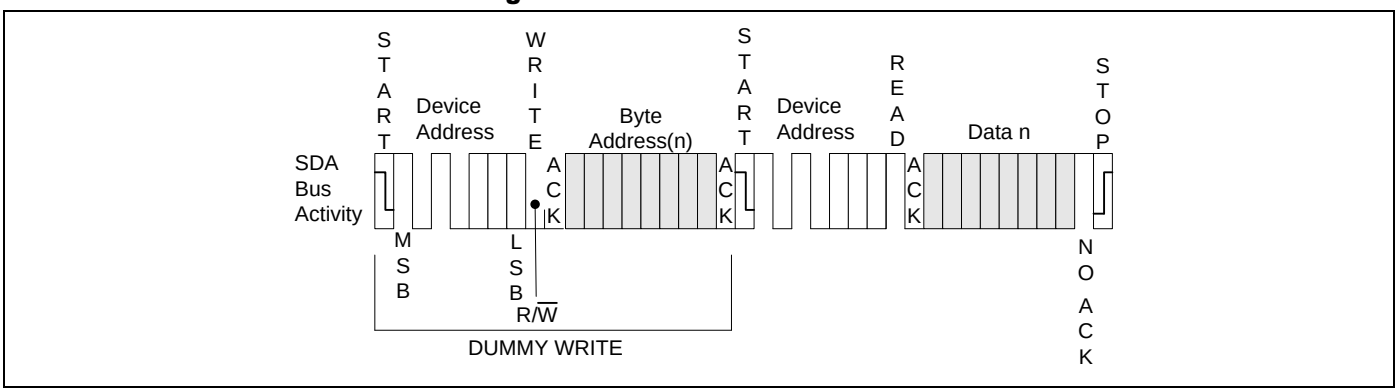


Figure 6.4 Current Address Read

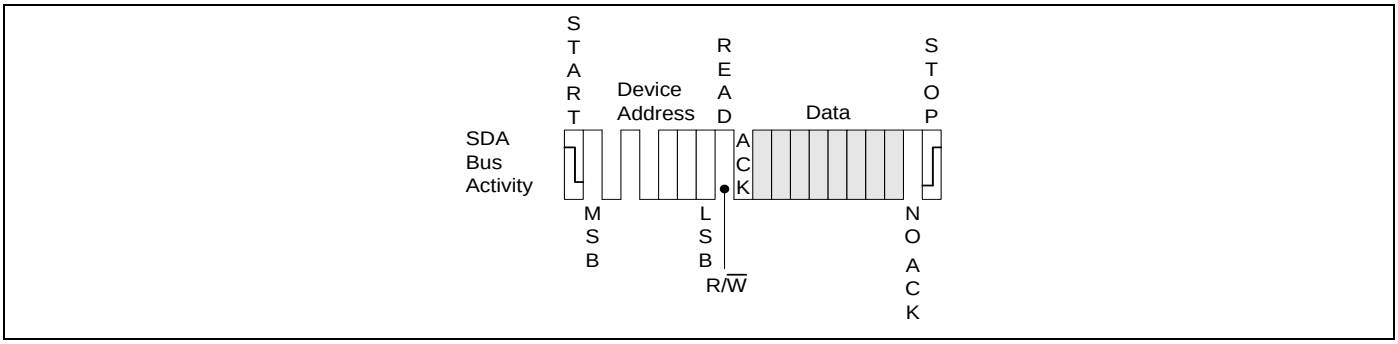


Figure 6.5 Sequential Read

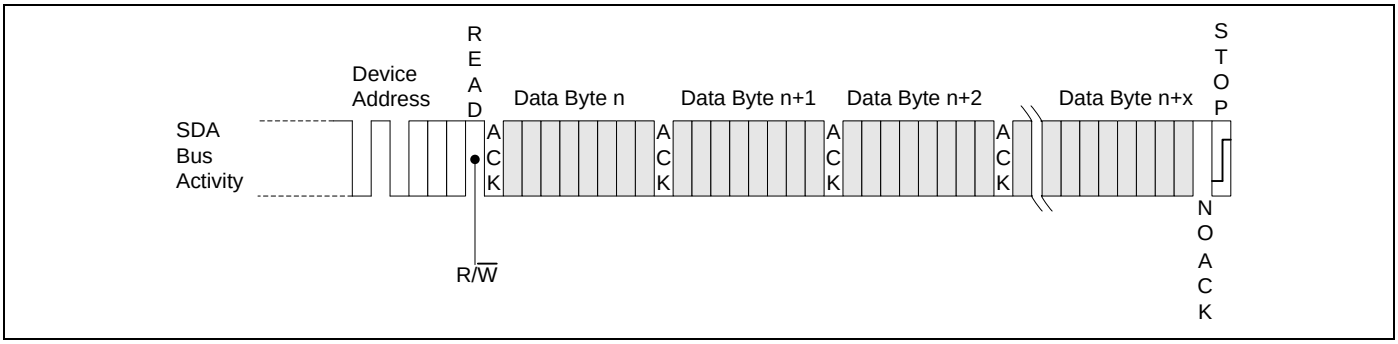


Figure 6.6 Set and Clear Write Protection

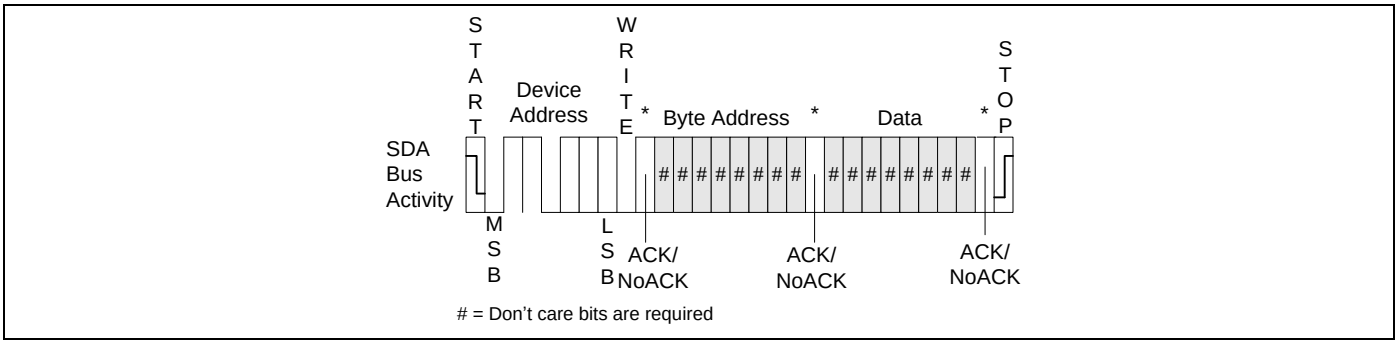


Figure 6.7 Read Write Protection Status

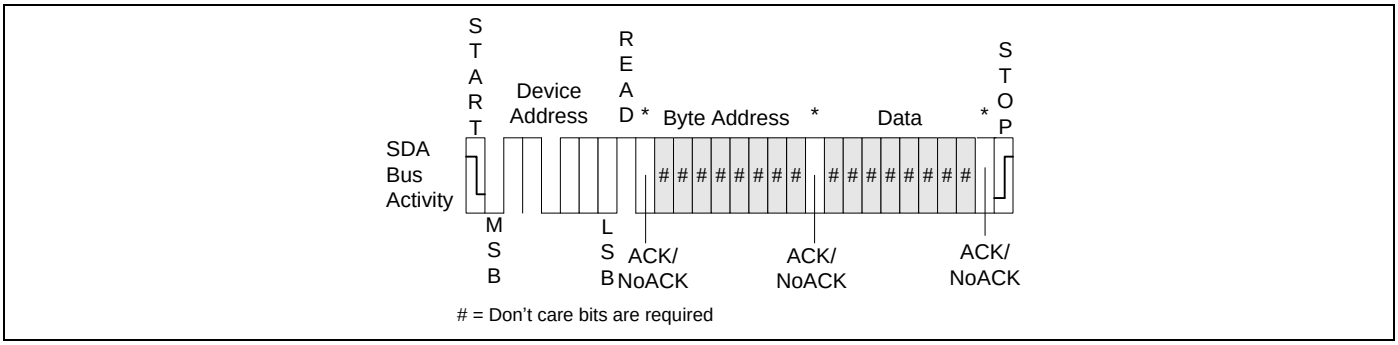


Figure 6.8 Set Page Address

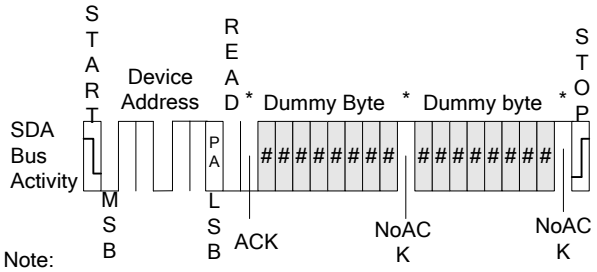


Figure 6.9 Write Cycle Polling Flowchart for EE using ACK

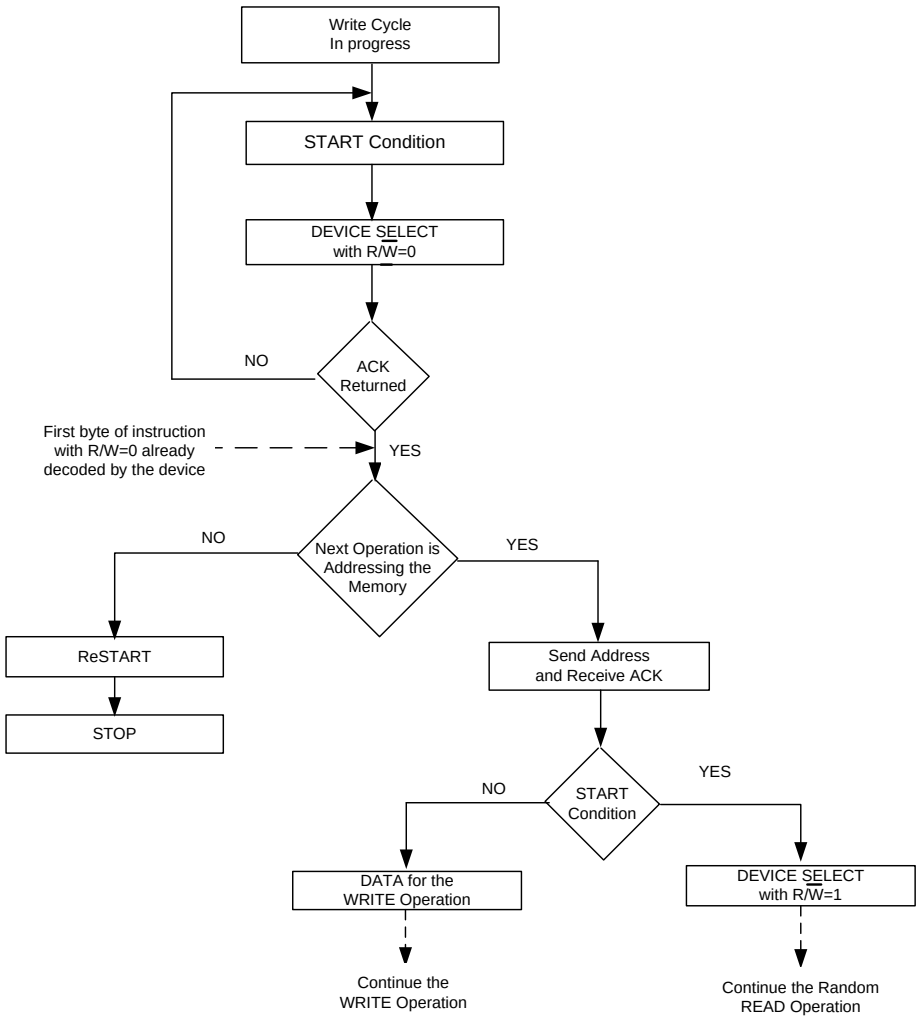


Table 6.1 Acknowledge When Writing Data or Defining Write Protection

Status	Instruction	ACK	Address	ACK	Data Byte	ACK	Write Cycle (T_W)
Protected with SWPn	SWPn	NoACK	Not signaificant	NoACK	Not signaificant	NoACK	No
	CWP	ACK	Not signaificant	ACK	Not signaificant	ACK	Yes
	Page or byte write in protected block	ACK	Address	ACK	Data	NoACK	No
Not Protected	SWPn or CWP	ACK	Not signaificant	ACK	Not signaificant	ACK	Yes
	Page or byte write	ACK	Address	ACK	Data	ACK	Yes

Table 6.2 Acknowledge When Reading the Protection Status

SWPn Status	Instruction	ACK	Address	ACK	Data Byte	ACK
Set	RPSn	NoACK	Not signaificant	NoACK	Not signaificant	NoACK
Not Set	RPSn	ACK	Not signaificant	NoACK	Not signaificant	NoACK

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to + 4.3	V
V_N	Voltage on Input Pins	–0.5 to + 4.3	V
V_{SA0}	Voltage on pin SA0	-0.5 to +10	V
$T_{J(max)}$	Maximum Junction Temperature	150	°C
T_{stg}	Storage Temperature	–65 to +150	°C

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

7.2 Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Industrial	-40°C to +125°C	1.7V to 3.6V

Note: Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

7.3 Capacitance

Symbol	Parameter[1, 2]	Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	--	--	6	pF
$C_{I/O}$	Input / Output Capacitance	--	--	8	pF
Z_{EIL}	Ei (SA0, SA1, SA2) input impedance	V_{IN}<0.3*V_{CC}	30	--	KΩ
Z_{EIH}	Ei (SA0, SA1, SA2) input impedance	V_{IN}>0.7*V_{CC}	800	--	KΩ
T_{SP}	Pulse width of spikes which must be suppressed by the input filter	Single glitch, f≤100KHz	--	--	ns
		Single glitch, f≥100KHz	0	50	

Notes: [1] Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
[2] Test conditions: T_A = 25°C, f = 400 KHz, V_{CC} = 2.2V to 3.6V, unless otherwise specified.

7.4 AC Measurement Conditions

Symbol	Parameter	Min	Max	Units
C_L	Load capacitance	100		pF
	Input rise and fall times	--	50	ns
	Input levels	0.2*V_{CC} to 0.8*V_{CC}		V
	Input and output timing reference levels	0.3*V_{CC} to 0.7*V_{CC}		V

7.5 DC Electrical Characteristic

V_{CC} = 1.7V to 3.6V, T_{amb} = -40 °C to +125 °C, unless otherwise specified

Symbol	Parameter[1]	Conditions	f≤400KHz		F≥400KHz		Unit
			Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage current(SCL, SDA)	V_{IN}=V_{CC} or GND	--	±5	--	±5	μA
I_{LO}	Output leakage current	V_{OUT}=V_{CC} or GND, SDA in Hi-Z	--	±5	--	±5	μA
I_{CC}	Supply current	V_{CC}=3.V, f_C=100KHz (rise/fall time<30ns)	--	2	--	2	mA
I_{SB1}	Standby supply current	V_{IN}=V_{CC} or GND, $V_{CC<}$=2.2V	--	1	--	1	μA
I_{SB2}	Standby supply current	V_{IN}=V_{CC} or GND, $V_{CC>}$=2.2V		2		2	μA
V_{IH}	Input High Voltage	SCL, SDA	0.7* V_{CC}	V_{CC}+0.5	0.7* V_{CC}	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	SCL, SDA	-0.5	0.3* V_{CC}	-0.5	0.3* V_{CC}	V
V_{HV}	SA0 High Voltage	V_{HV} - V_{CC} ≥ 4.8V	7	10	7	10	V
V_{OL1}	Output Low Voltage [2] open-drain or open-collector	I_{OL}=3mA, V_{CC}>2.2V	--	0.4	--	0.4	V
V_{OL2}		I_{OL}=2mA, V_{CC}≤2.2V	--	0.2	--	0.2	
I_{OL}	Output Low Sink Current[3]	V_{OL}=0.4V	3		20		mA
		V_{OL}=0.6V	6		--		mA
V_{PON}	Power On Reset threshold	Monotonic rise between V_{PON} and V_{CC}(min) without ringback	1.6	--	1.6	--	V
V_{POFF}	Power Off threshold for warm power on cycle	No ringback above V_{POFF}	--	0.9	--	0.9	V

Notes: [1] The parameters are characterized but not 100% tested.

[2] The same resistor value to drive 3mA at 3.0V, V_{CC} provides the same RC time constant when using<2V, V_{CC} with a smaller current draw

[3] In order to drive full bus load at 400KHz, 6mA IOL is required at 0.6V VOL. Parts not meeting this specification can still function, but not at 400KHz and 400pF.

7.6 AC Electrical Characteristic

V_{CC} = 1.7V to 3.6V, T_{amb} = -40~+125°C, unless otherwise specified

Symbol	Parameter [11]	V_{CC}[4]<1.7V		V_{CC}≥1.7V				Unit
		100KHz[10]		400KHz[9]		1000KHz		
		Min.	Max.	Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	10	100	10	400	10	1000	kHz
T_{LOW}[6]	Low period of SCL clock	4700		1300		500		ns
T_{HIGH}	High period of SCL clock	4000		600		260		ns
T_{BUF}	Bus free time between a Stop and a Start conditions	4700		1300		500		ns
$T_{SU;STA}$[1]	Start condition Setup time	4700		600		260		ns
$T_{HD;STA}$	Start condition Hold time	4000		600		260		ns
$T_{SU;STO}$	Stop condition Setup time	4000		600		260		ns
$T_{SU;DAT}$	Data In Setup time	250		100		50		ns
$T_{HD;DI}$[2]	Data In Hold time	0		0		0		ns
$T_{HD:DAT}$	Data Out Hold Time	200	3450	200	900	0	350	ns
T_W	Write Cycle		5		5		5	ms
T_R[2]	Rise time of SDA	--	1000	20	300	--	120	ns
T_F[2]	Fall time of SDA	--	300	20	300	--	120	ns
T_{INIT}	Time from power on to first command	10		10		10		ns
T_{POFF}	Warm power cycle off time	1		1		1		ms
$T_{time\text{-}out}$[5,7]	Detect clock low timeout	25	35	25	35	25	35	ms

Notes: [1] For a reSTART condition, or following a write cycle.

[2] Guaranteed by design and characterization, not necessarily tested.

[3] To avoid spurious START and STOP conditions, a minimum delay is placed between falling edge of SCL and the falling or rising edge of SDA.

[4] Unlike previous EE generations, EE1004-v and TSE2004av families must support bus timeout on EE accesses.

[5] EE1004-v and TSE2004av family devices shall not initiate clock stretching, which is an optional I2C Bus feature.

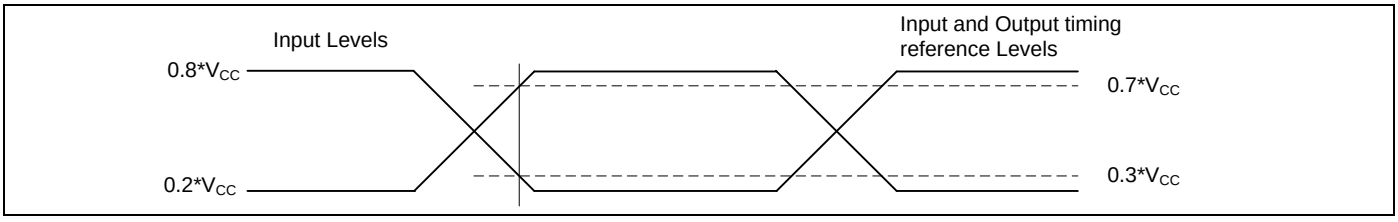
[6] I2C bus masters can terminate a transaction in process and reset device communication on the bus by asserting SCL low for $T_{TIMEOUT}$,MAX or longer. EE/TSE devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $T_{TIMEOUT}$,MAX. EE/TSE devices will not reset if SCL stretching is less than $T_{TIMEOUT}$, MIN. See EE/TSE Bus Timeout Waveforms.

[7] 400 KHz timing defined for compatibility with EE1002(A) and TSE2002av applications.

[8] 100 KHz timing compliant with SMBus 2.0 specifications.

[9] Not all parameters are 100% tested .

Figure 7.1 AC Measurement I/O Waveform



8. Ordering Information

Industrial Grade: -40°C to +125°C, Lead-free

Voltage Range	Part Number*	Package (8-pin)*
1.7V to 3.6V	GT34C04-2UDLI-TR	2 x 3 x 0.55 mm Ultra-thin DFN
	GT34C04-2ZLI-TR	3 x 4.4 mm TSSOP
	GT34C04-2GLI-TR	150-mil SOIC

*

1. Contact Giantec Sales Representatives for availability.
2. The listed part numbers are packed in tape and reel “-TR”. UDFN is 5K per reel.
3. Refer to Giantec website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. Giantec offers Industrial grade for Commercial applications (0°C to +70°C).

9. Top Markings

9.1 UDFN Copper Package

GT: Giantec Logo

62: GT34C04-2UDLI-TR

YWW: Date Code, Y=year, WW=week

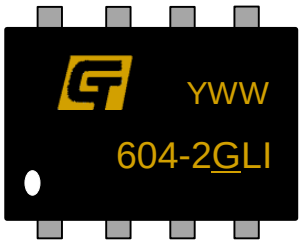
9.2 TSSOP Copper Package

GT: Giantec Logo

604-2ZLI: GT34C04-2ZLI-TR

YWW: Date Code, Y=year, WW=week

9.3 SOIC Copper Package



GT: Giantec Logo

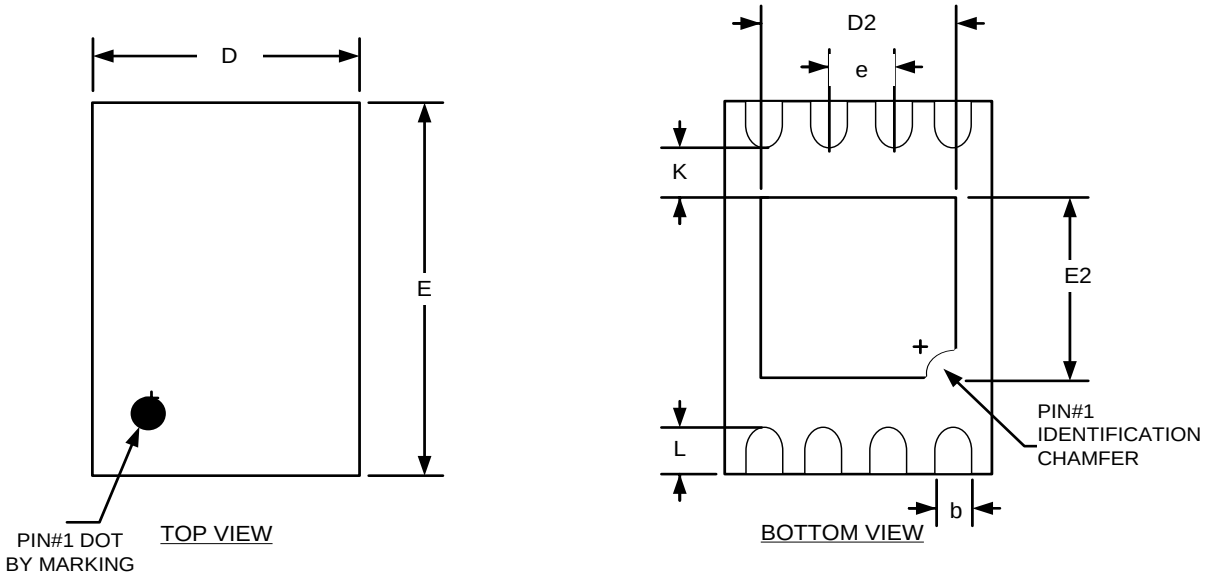
604-2GLI: GT34C04-2GLI-TR

YWW: Date Code, Y=year, WW=week

10. Package Information

10.1 UDFN

8L 2x3mm UDFN Package Outline



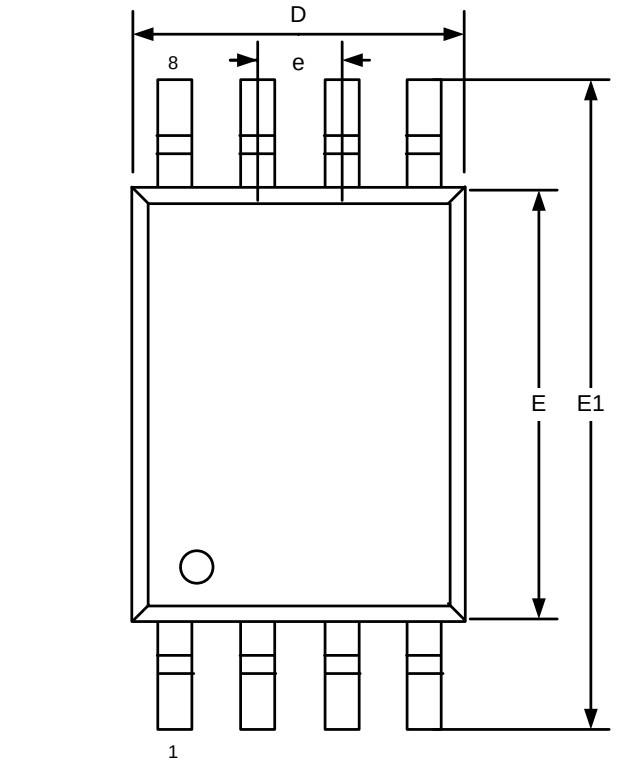
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

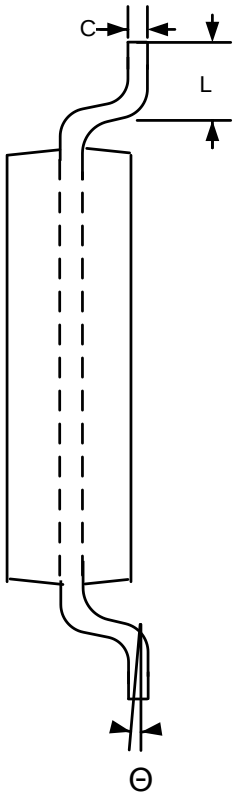
Note:

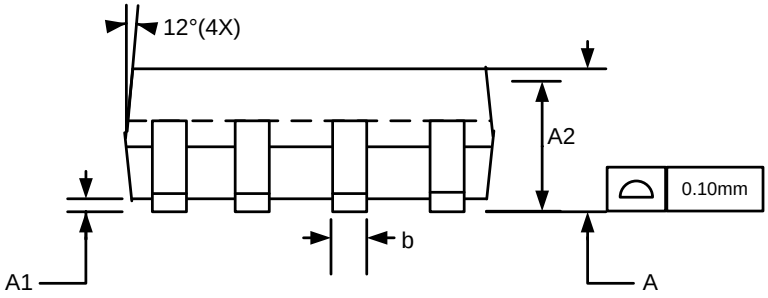
1. Controlling Dimension:MM
2. Drawing is not to scale

10.2 TSSOP

8L 3x4.4mm TSSOP Package Outline





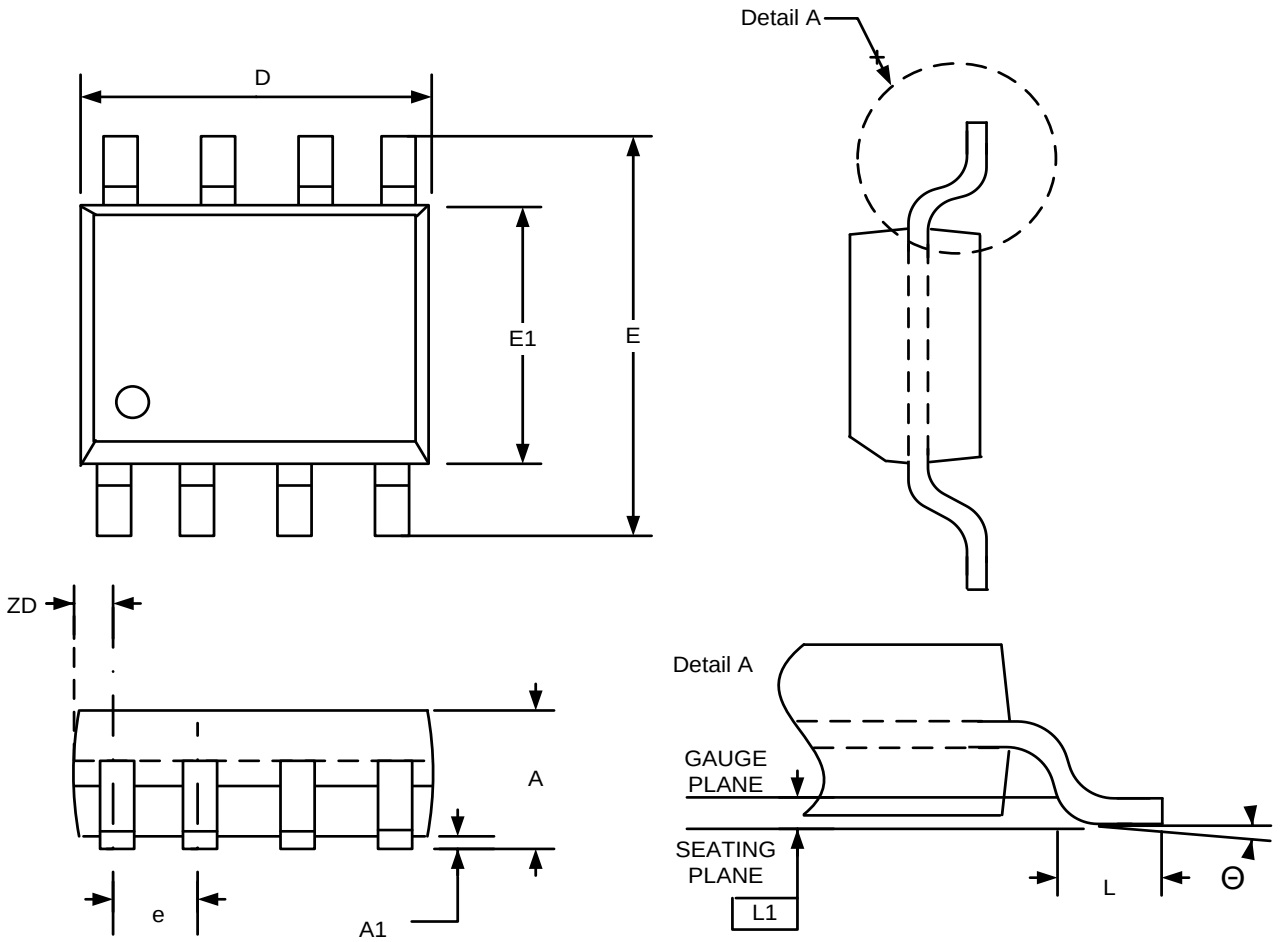


Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.4 BSC			0.252 BSC		
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

10.3 SOIC

8L 150mil SOIC Package Outline



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

Note:

1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

11. Revision History

Revision	Date	Descriptions
A0	Mar. 2015	Initial version
A1	Oct. 2016	Remove WP pin function
A2	May.2017	Add Figure 6.8 set page address