TOSHIBA Insulated Gate Bipolar Transistor Silicon N Channel IGBT

GT45F123

For PDP-TV Applications

- 5th generation (trench gate structure) IGBT
- Enhancement-mode
- Low input capacitance: Cies = 2700pF (typ.)
- Peak collector current: ICP = 200 A (max)
- TO-220SIS package

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Collector-emitter voltage		V _{CES}	300	$\langle \rangle$
Gate-emitter voltage		V _{GES}	± 30	X
Collector current	Pulse (Note 1)	I _{CP}	200	> A
Collector power dissipation	Tc=25°C	Pc	26	W
	Ta=25°C	F C	2	
Junction temperature		T _j	150	⟨⟨°C
Storage temperature range		T _{stg}	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e.

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Weight: 2 g (typ.)

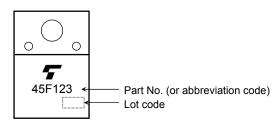
operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Rating	Unit
Thermal resistance , junction to case (Tc = 25°C)	Rth.(j-c)	4.8	°C/W
Thermal resistance , junction to ambient (Ta = 25°C)	R _{th} (j-a)	62.5	°C/W

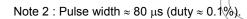
Marking



Note 1: I_{CP} maximum rating(200A) is limited by pulse width (3 μs).

Electrical Characteristics (Ta = 25°C)

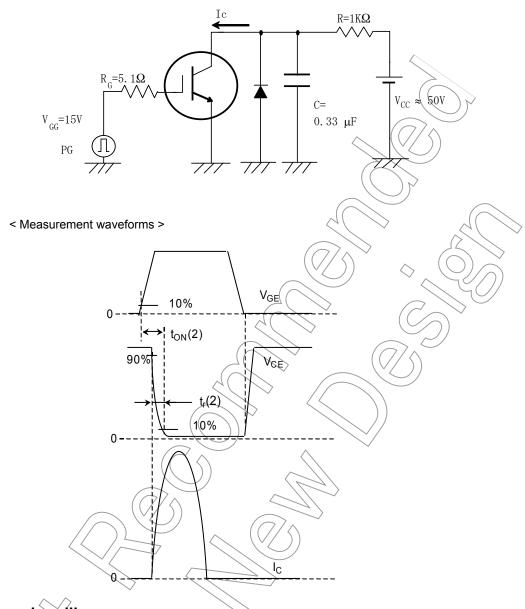
Charac	teristics	Symbol	Test Condition	Min	Тур.	Max	Unit	
Gate leakage curre	nt	I _{GES}	$V_{GE} = \pm 30 \text{ V}, V_{CE} = 0 \text{V}$	_	_	± 100	nA	
Collector cut-off cu	rrent	I _{CES}	V _{CE} = 300 V, V _{GE} = 0V	_	_	0.5	mA	
Emitter-collector vo	ltage	V _{ECS}	I _E = 0.5A, V _{GE} = 0V (Note2)	15	_		V	
Gate-emitter cut-of	f voltage	V _{GE} (OFF)	I _C = 10 mA, V _{CE} = 5 V	3.0	4.5	5.5	V	
Collector-emitter sa	aturation voltage	V _{CE} (sat) (1)	I _C = 45 A, V _{GE} = 15 V	(F)1.35	1.6	V	
Collector-emitter sa	aturation voltage	V _{CE} (sat) (2)	I _C = 120 A, V _{GE} = 15 V) _K	1.95	2.4	V	
Collector-emitter sa	aturation voltage	V _{CE} (sat) (3)	I _C = 200 A, V _{GE} = 15 V	\mathcal{P}	2.6	3.3	V	
Input capacitance		C _{ies}			2700	_		
Reverse transfer capacitance		C _{res}	V _{CE} = 10 V, V _{GE} = 0V, f = 1 MHz	_	155	_	pF	
Output capacitance		C _{oes}		_	225	_		
Switching time (Resistance load)	Rise time	t _{r (1)}	15 V C=80A -		180			
	Turn-on time	t _{on(1)}	0 5,1\(\Omega\) \$\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	_((230) —		
	Fall time	t _f	V_{IN} : $t_r \le 100 \text{ ns}$ $t_f \le 100 \text{ ns}$		200	300	ns	
	Turn-off time	t _{off}	Duty cycle ≤ 1% ≈ 250 V	\bigcirc	290			
Switching time (Discharge mode)	Rise time	t _{r (2)}	$V_{CC} \approx 50V, V_{CP} = 100A$ $V_{GG} = 15V/0V, R_{G} = 5.1\Omega$) —	125	ı	ne	
	Turn-on time	t _{on(2)}	(Note 3)	_	150	_	ns	
Total gate charge gate-drain)	(gate-emitter plus	Qg	V _{CE} = 300 V, V _{GE} = 15V, I _C = 120 A	_	110	_	nC	





Note 3: Switching time measurement circuit and input/output waveforms.

< Switching circuit of discharge mode>



Caution on handling

This MOS gate device is sensitive to electrostatic discharge (ESD).

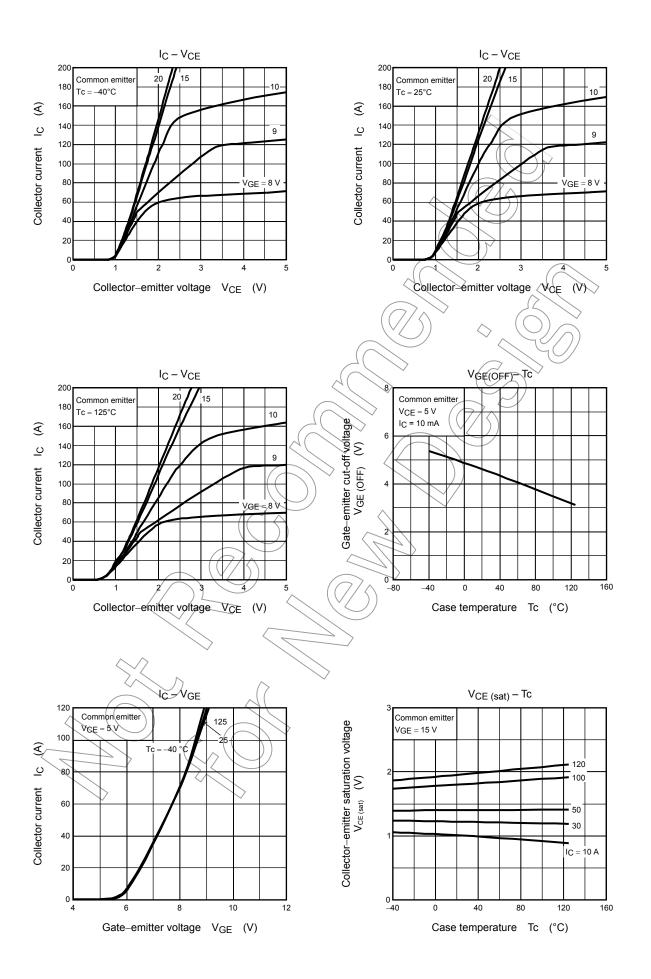
When handling the device, be sure that the environment is protected against static electricity.

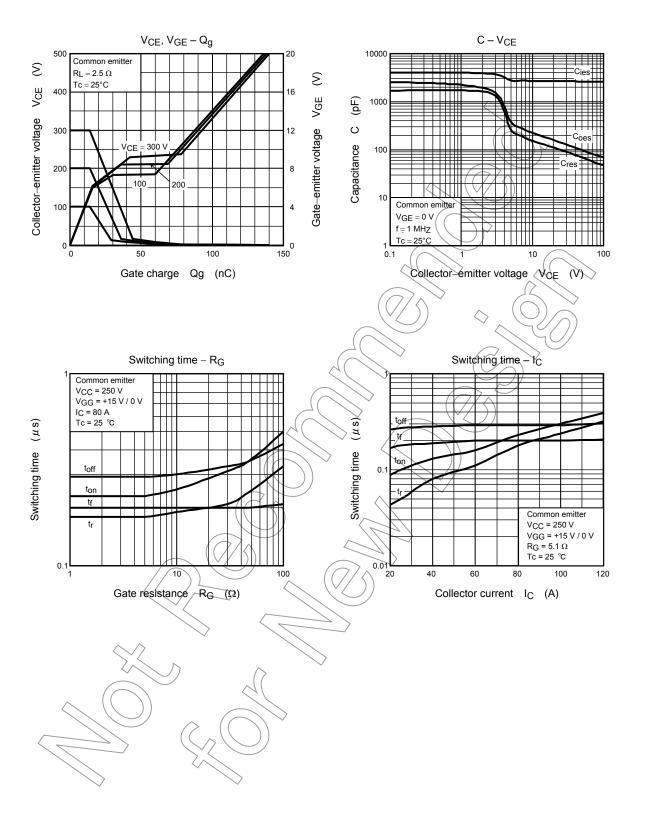
Caution in design

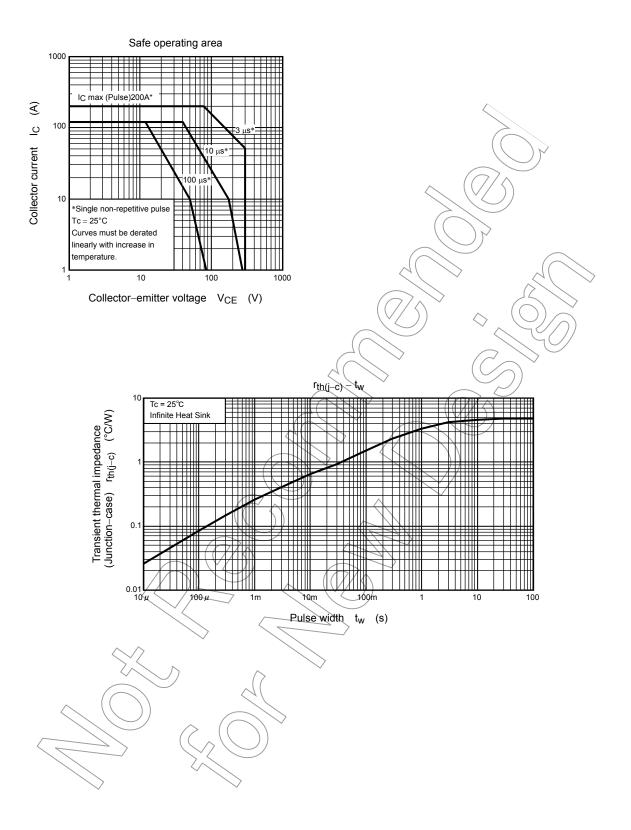
This devise is designed for use in PDP-TVs.

Please contact our sales section if the device is intended for any other use.

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• The information contained herein is subject/to change without notice.

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Handbook" etc.

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