

# GT7111



## 200MHz, High Speed, CMOS, Rail-to-Rail Operational Amplifier

**Advanced**

### 1. Features

- Single-Supply Operation from +2.5V ~ +5.5V
- Rail-to-Rail Input / Output
- Gain-Bandwidth Product: 200MHz (Typ.)
- Low Input Bias Current: 10pA (Typ.)
- Low Offset Voltage: 5mV (Max.)
- Quiescent Current: 2.8mA (Typ.)
- Operating Temperature: -40°C ~ +125°C
- Available in SOT23-5 and SOP8 Packages

### 2. General Description

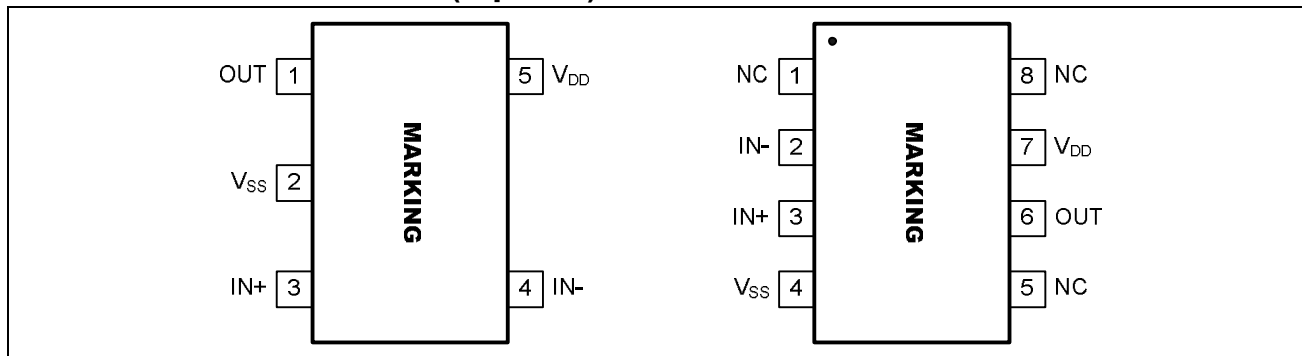
The GT7111 is wideband, low-noise, low-distortion operational amplifier, that offer rail-to-rail output and single-supply operation down to 2.5V. They draw 2.8mA of quiescent supply current, as well as low input voltage-noise density (13nV/ $\sqrt{\text{Hz}}$ ) and low input current-noise density (400fA/ $\sqrt{\text{Hz}}$ ). These features make the devices an ideal choice for applications that require low distortion and low noise. The GT7111 has output which swing rail-to-rail and their input common-mode voltage range includes ground and offer wide bandwidth to 200MHz (G=+1). They are specified over the extended industrial temperature range (-45°C ~ 125°C). The single GT7111 is available in space-saving, SOT23-5 and SOP-8 packages.

### 3. Applications

- Portable Equipment
- Mobile Communications
- Smoke Detector
- Sensor Interface
- Medical Instrumentation
- Handheld Test Equipment
- Imaging/video

### 4. Pin Configuration

#### 4.1 GT7111 SOT23-5 and SOP8 (Top View)



**Figure 1. Pin Assignment Diagram (SOP23-5 and SOP8 Package)**

**Note:** Please see section “Part Markings” for detailed Marking Information.

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## 5. Application Information

### 5.1 Size

GT7111 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. The small footprints of the GT7111 series packages save space on printed circuit boards and enable the design of smaller electronic products.

### 5.2 Power Supply Bypassing and Board Layout

GT7111 series operates from a single 2.5V to 5.5V supply or dual  $\pm 1.25\text{V}$  to  $\pm 2.75\text{V}$  supplies. For best performance, a  $0.1\mu\text{F}$  ceramic capacitor should be placed close to the  $V_{\text{DD}}$  pin in single supply operation. For dual supply operation, both  $V_{\text{DD}}$  and  $V_{\text{SS}}$  supplies should be bypassed to ground with separate  $0.1\mu\text{F}$  ceramic capacitors.

### 5.3 Low Supply Current

The low supply current (typical 2.8mA) of GT7111 series will help to maximize battery life. They are ideal for battery powered systems

### 5.4 Operating Voltage

GT7111 series operate under wide input supply voltage (2.2V to 5.5V). In addition, all temperature specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Most behavior remains unchanged throughout the full operating voltage range. These guarantees ensure operation throughout the single Li-Ion battery lifetime

### 5.5 Rail-to-Rail Input

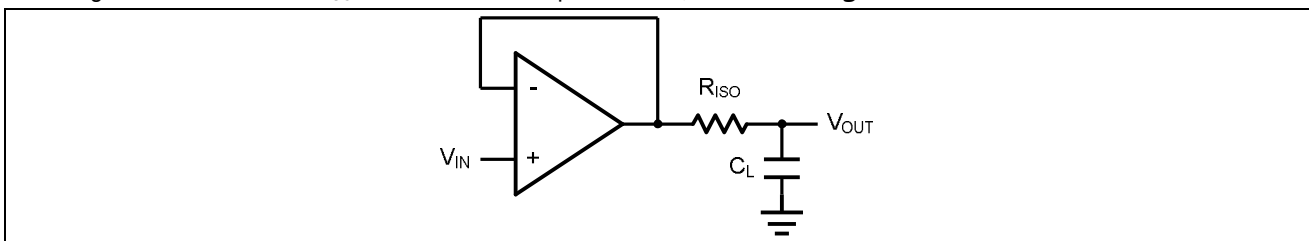
The input common-mode range of GT7111 series extends 5mV beyond the supply rails ( $V_{\text{SS}}-0.1\text{V}$  to  $V_{\text{DD}}+0.1\text{V}$ ). This is achieved by using complementary input stage. For normal operation, inputs should be limited to this range.

### 5.6 Rail-to-Rail Output

Rail-to-Rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating in low supply voltages. The output voltage of GT7111 series can typically swing to less than 10mV from supply rail in light resistive loads ( $>100\text{k}\Omega$ ), and 60mV of supply rail in moderate resistive loads ( $10\text{k}\Omega$ ).

### 5.7 Capacitive Load Tolerance

The GT7111 series can directly drive 250pF capacitive load in unity-gain without oscillation. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. In unity-gain configurations, the capacitive load drive can be improved by inserting an isolation resistor  $R_{\text{ISO}}$  in series with the capacitive load, as shown in **Figure 2**.

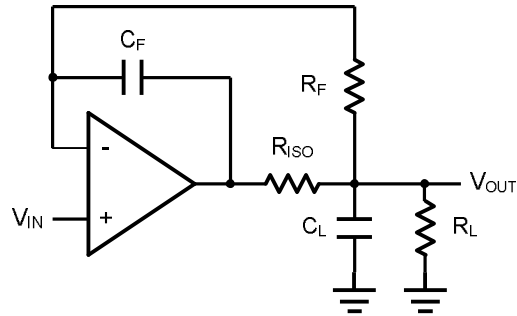


**Figure 2. Indirectly Driving a Capacitive Load Using Isolation Resistor**

The bigger the  $R_{\text{ISO}}$  resistor value, the more stable  $V_{\text{OUT}}$  will be. However, if there is a resistive load  $R_L$  in parallel with the capacitive load, a voltage divider (proportional to  $R_{\text{ISO}}/R_L$ ) is formed, this will result in a gain error.

The circuit in **Figure 3** is an improvement to the one in **Figure 2**.  $R_F$  provides the DC accuracy by feed-forward the  $V_{\text{IN}}$  to  $R_L$ .  $C_F$  and  $R_{\text{ISO}}$  serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving the phase margin in the overall feedback loop. Capacitive drive can be increased

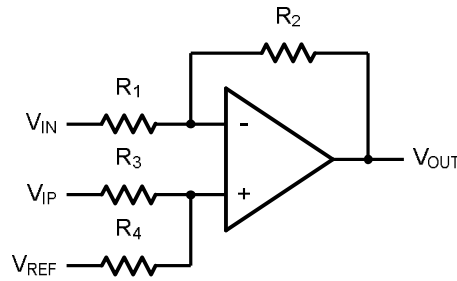
by increasing the value of  $C_F$ . This in turn will slow down the pulse response.



**Figure 3. Indirectly Driving a Capacitive Load with DC Accuracy**

## 5.8 Differential amplifier

The differential amplifier allows the subtraction of two input voltages or cancellation of a signal common to the two inputs. It is useful as a computational amplifier in making a differential to single-end conversion or in rejecting a common mode signal. **Figure 4.** shows the differential amplifier using GT7111.



**Figure 4. Differential Amplifier**

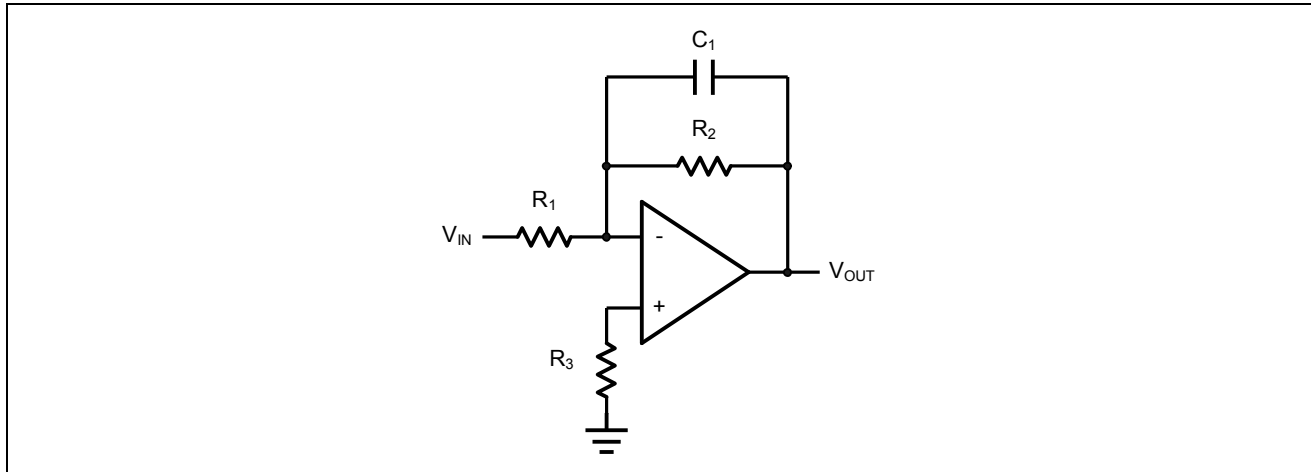
$$V_{OUT} = \left( \frac{R_1 + R_2}{R_3 + R_4} \right) \frac{R_4}{R_1} V_{IN} - \frac{R_2}{R_1} V_{IP} + \left( \frac{R_1 + R_2}{R_3 + R_4} \right) \frac{R_3}{R_1} V_{REF}$$

If the resistor ratios are equal (i.e.  $R_1 = R_3$  and  $R_2 = R_4$ ), then

$$V_{OUT} = \frac{R_2}{R_1} (V_{IP} - V_{IN}) + V_{REF}$$

## 5.13 Low Pass Active Filter

The low pass active filter is shown in **Figure 8**. The DC gain is defined by  $-R_2/R_1$ . The filter has a -20dB/decade roll-off after its corner frequency  $f_c=1/(2\pi R_3 C_1)$ .



**Figure 8. Low Pass Active Filter**

## 5.14 Sallen-Key 2<sup>nd</sup> Order Active Low-Pass Filter

GT7111 can be used to form a 2<sup>nd</sup> order Sallen-Key active low-pass filter as shown in **Figure 9**. The transfer function from  $V_{IN}$  to  $V_{OUT}$  is given by

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{\frac{1}{C_1 C_2 R_1 R_2} A_{LP}}{S^2 + S \left( \frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} \right) + \frac{A_{LP}}{C_1 C_2 R_1 R_2}}$$

Where the DC gain is defined by  $A_{LP}=1+R_3/R_4$ , and the corner frequency is given by

$$\omega_C = \sqrt{\frac{1}{C_1 C_2 R_1 R_2}}$$

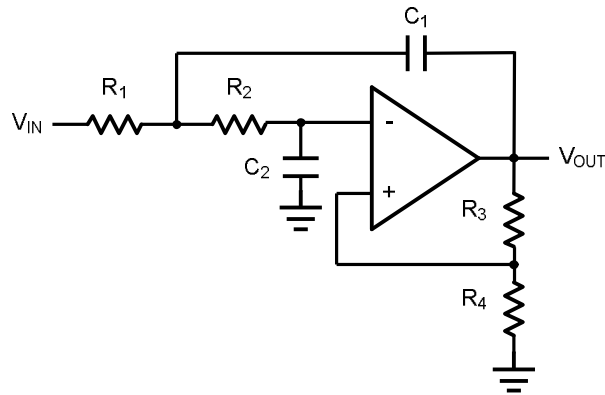
The pole quality factor is given by

$$\frac{\omega_C}{Q} = \frac{1}{C_1 R_1} + \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} - \frac{A_{LP}}{C_2 R_2}$$

Let  $R_1=R_2=R$  and  $C_1=C_2=C$ , the corner frequency and the pole quality factor can be simplified as below

$$\omega_C = \frac{1}{CR}$$

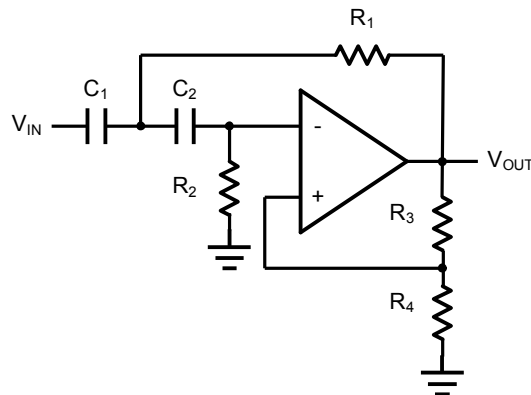
And  $Q=2-R_3/R_4$



**Figure 9. Sallen-Key 2nd Order Active Low-Pass Filter**

## 5.15 Sallen-Key 2<sup>nd</sup> Order high-Pass Active Filter

The 2<sup>nd</sup> order Sallen-key high-pass filter can be built by simply interchanging those frequency selective components  $R_1$ ,  $R_2$ ,  $C_1$ , and  $C_2$  as shown in **Figure 10**.



**Figure 10. Sallen-Key 2nd Order Active High-Pass Filter**

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{S^2 A_{HP}}{S^2 + S\left(\frac{1}{C_1 R_1} + \frac{1}{C_2 R_2} + \frac{1 - A_{HP}}{C_1 R_1}\right) + \frac{1}{C_1 C_2 R_1 R_2}}$$

Where  $A_{HP} = 1 + R_3/R_4$



## 6. Electrical Characteristics

### 6.1 Absolute Maximum Ratings

Condition	Min	Max
Power Supply Voltage ( $V_{DD}$ to $V_{SS}$ )	-0.5V	+7V
Analog Input Voltage ( $IN+$ or $IN-$ )	$V_{SS}-0.5V$	$V_{DD}+0.5V$
PDB Input Voltage	$V_{SS}-0.5V$	+7V
Operating Temperature Range	-40°C	+125°C
Junction Temperature	+150°C	
Storage Temperature Range	-65°C	+150°C
Lead Temperature (soldering, 10sec)	+300°C	
Package Thermal Resistance ( $T_A=+25^{\circ}C$ )		
SOP23-5, $\theta_{JA}$	190°C	
SOP8, $\theta_{JA}$	130°C	

**Note:** Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



## 6.2 Electrical Characteristics

( $V_{DD} = +5V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = 0V$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_L = 100K$  tied to  $V_{DD}/2$ ,  $SHDNB = V_{DD}$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Notes 1,2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply-Voltage Range	$V_{DD}$	Guaranteed by the PSRR test	2.5	-	5.5	V
Quiescent Supply Current (per Amplifier)		$V_{DD} = 5V$	-	2.8	3.5	mA
Input Offset Voltage	$V_{OS}$	$T_A = 25^{\circ}C$	-	$\pm 1$	-	mV
		$T_A = -40^{\circ}C \sim +85^{\circ}C$	-	$\pm 8$	-	
		$T_A = -40^{\circ}C \sim +125^{\circ}C$	-	-	$\pm 10$	
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$		-	$\pm 2$	-	$\mu V/^{\circ}C$
Input Bias Current	$I_B$	(Note 3)	-	$\pm 10$	$\pm 100$	pA
Input Offset Current	$I_{OS}$	(Note 3)	-	$\pm 10$	$\pm 100$	pA
Input Common-Mode Voltage Range	$V_{CM}$	Guaranteed by the $T_A = 25^{\circ}C$ CMRR test, $T_A = -40^{\circ}C \sim +125^{\circ}C$	-0.1	-	$V_{DD} + 0.1.5$	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} - 0.1V \leq V_{CM} \leq V_{DD} + 0.1V$ $T_A = 25^{\circ}C$	-	75	-	dB
		$V_{SS} \leq V_{CM} \leq 5V_{DD}$ $T_A = 25^{\circ}C$	72	90	-	
		$V_{SS} - 0.1V \leq V_{CM} \leq V_{DD} + 0.1V$ $T_A = -40^{\circ}C \sim +125^{\circ}C$	-	68	-	
Power-Supply Rejection Ratio	PSRR	$V_{DD} = +2.5V$ to $+5.5V$	75	90	-	dB
Open-Loop Voltage Gain	$A_V$	$R_L = 10k\Omega$ to $V_{DD}/2$ $V_{OUT} = 100mV$ to $V_{DD} - 125mV$	90	100	-	dB
		$R_L = 1k\Omega$ to $V_{DD}/2$ $V_{OUT} = 200mV$ to $V_{DD} - 250mV$	80	95	-	
		$R_L = 500\Omega$ to $V_{DD}/2$ $V_{OUT} = 350mV$ to $V_{DD} - 500mV$	70	80	-	
Output Voltage Swing	$V_{OUT}$	$ V_{IN+} - V_{IN-}  \geq 10mV$ $V_{DD} - V_{OH}$	-	10	30	mV
		$R_L = 10k\Omega$ to $V_{DD}/2$ $V_{OL} - V_{SS}$	-	10	35	
		$ V_{IN+} - V_{IN-}  \geq 10mV$ $V_{DD} - V_{OH}$	-	80	50	
		$R_L = 1k\Omega$ to $V_{DD}/2$ $V_{OL} - V_{SS}$	-	30	50	
		$ V_{IN+} - V_{IN-}  \geq 10mV$ $V_{DD} - V_{OH}$	-	100	140	
		$R_L = 500\Omega$ to $V_{DD}/2$ $V_{OL} - V_{SS}$	-	100	140	
Output Short-Circuit Current	$I_{SC}$	Sinking or Sourcing	-	$\pm 100$	-	mA
-3 dB Gain Bandwidth Product	GBW	$A_V = +1V/V$	-	200	-	MHz
Slew Rate	SR	$A_V = +1V/V$	-	125	-	V/ $\mu s$



Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Differential Phase error (NTSC)	DP	$G=2, R_L=150\Omega$	-	0.03	-	deg
Differential Gain error (NTSC)	DG	$G=2, R_L=150\Omega$	-	0.09	-	dB
Settling Time	$t_s$	To 0.01%, $V_{OUT} = 2V$ step $A_V = +1V/V$	-	42	-	ns
Over Load Recovery Time		$V_{IN} \times \text{Gain} = V_S$	-	35	-	ns
Input Voltage Noise Density	$e_n$	$f = 1\text{MHz}$	-	16	-	nV/ $\sqrt{\text{Hz}}$
Total Harmonic Distortion plus Noise	THD+N	$f_C=5\text{MHz}, V_{OUT}=2V_{p-p}, G=+2$	-	-60	-	dB

**Note 1:** All devices are 100% production tested at  $T_A = +25^\circ\text{C}$ ; all specifications over the automotive temperature range is guaranteed by design, not production tested.

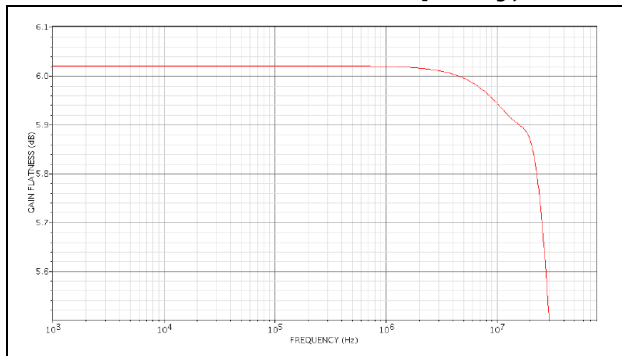
**Note 2:** Parameter is guaranteed by design.

**Note 3:** Peak-to-peak input noise voltage is defined as six times rms value of input noise voltage.

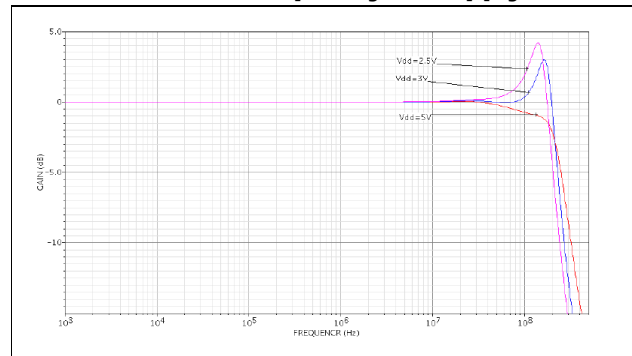


## 6.3 Typical characteristics

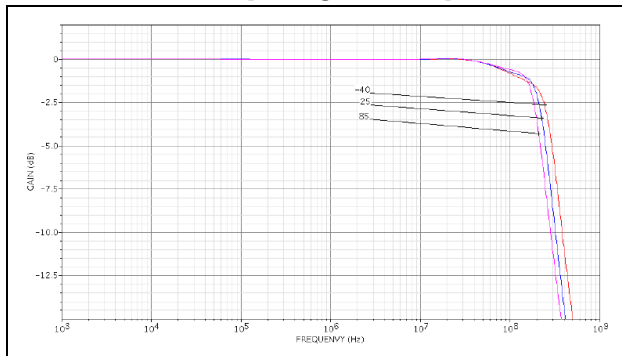
**0.1dB Gain Flatness vs. Frequency; G=+2**



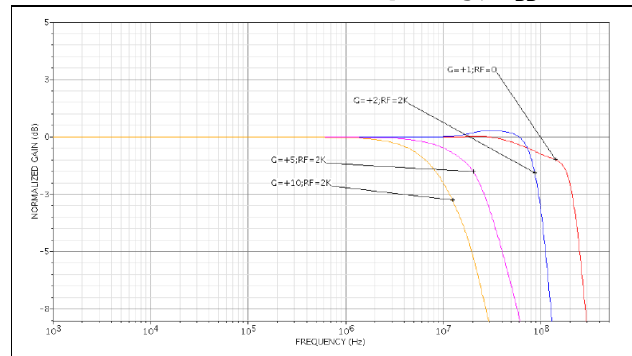
**Gain vs. Frequency vs Supply**



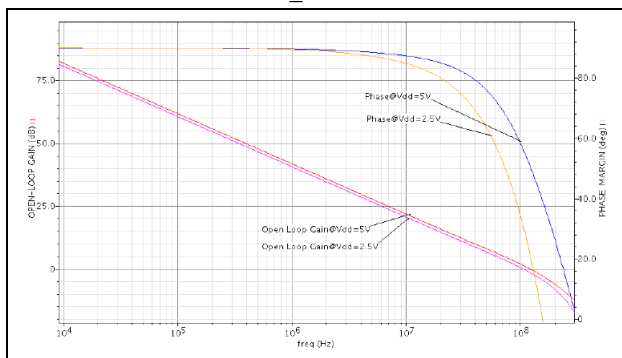
**Gain vs. Frequency vs Temperature**



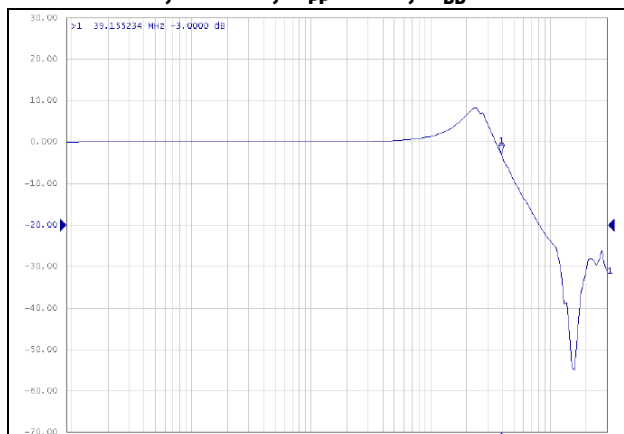
**Normalized Gain vs. Frequency;  $V_{DD}=5V$**



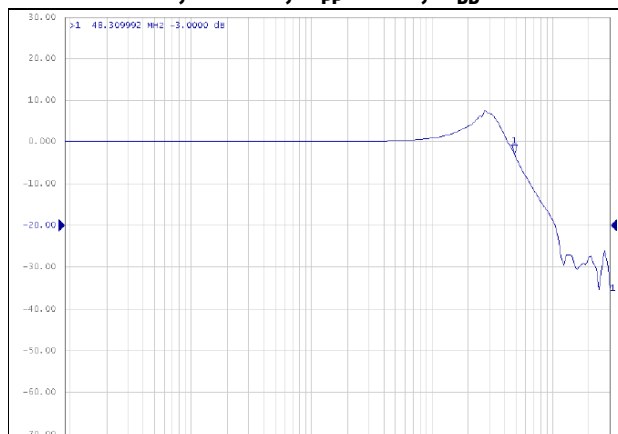
**STB\_RL=2K**



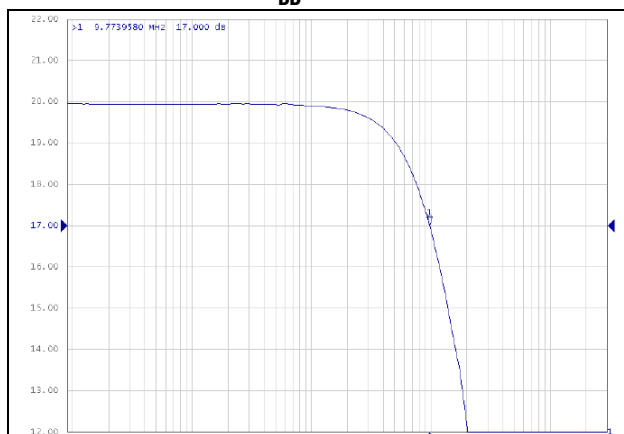
**G=+1; RF=2K; V<sub>pp</sub>=0.2V; V<sub>DD</sub>=2.5V**



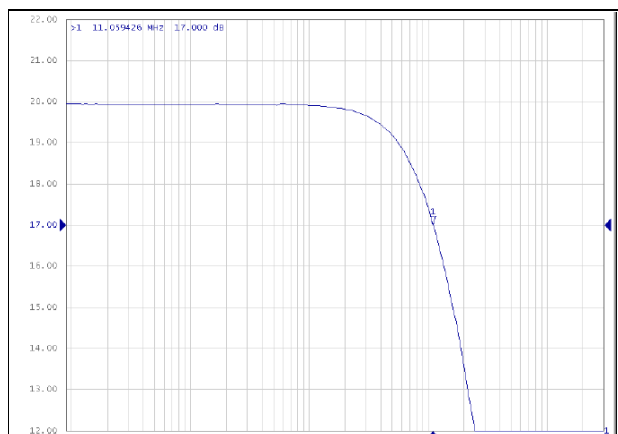
**G=+1; RF=2K; V<sub>pp</sub>=0.2V; V<sub>DD</sub>=5V**



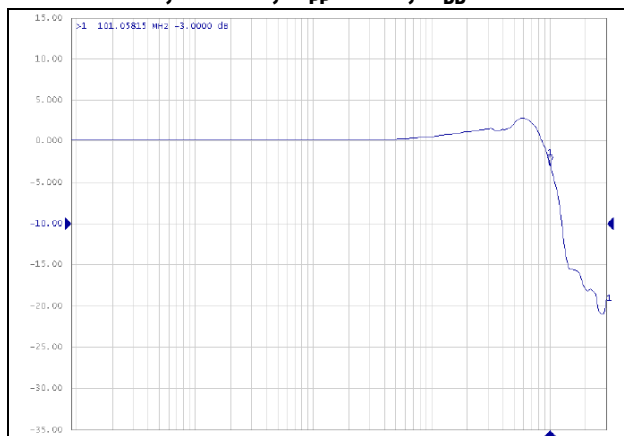
**G=+2; RF=100Ω; RI=150 Ω V<sub>pp</sub>=0.2V;  
V<sub>DD</sub>=2.5V**



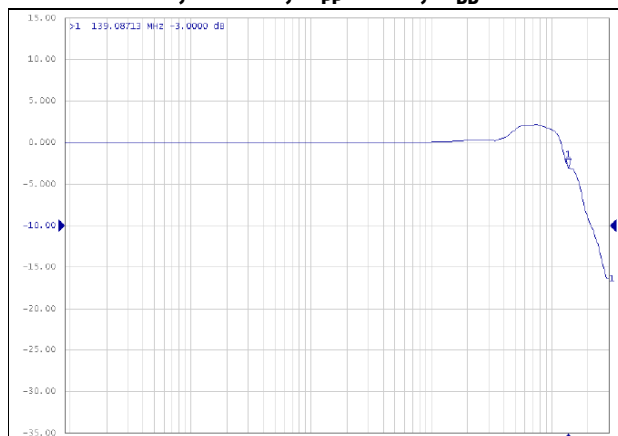
**G=-10; RF=2K; V<sub>pp</sub>=0.2V; V<sub>DD</sub>=5V**



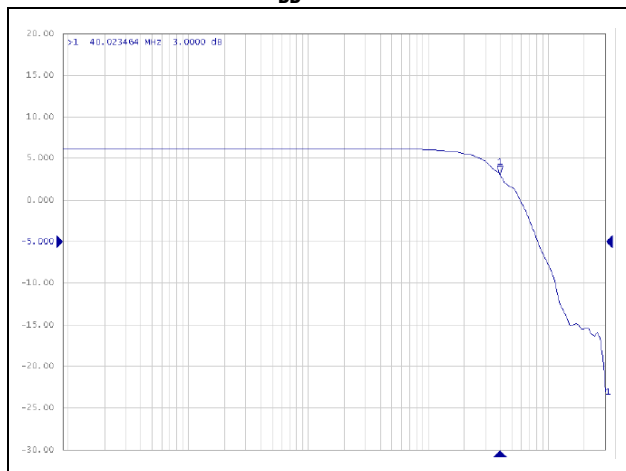
**G=+1; RF=2K; V<sub>pp</sub>=0.2V; V<sub>DD</sub>=2.5V**



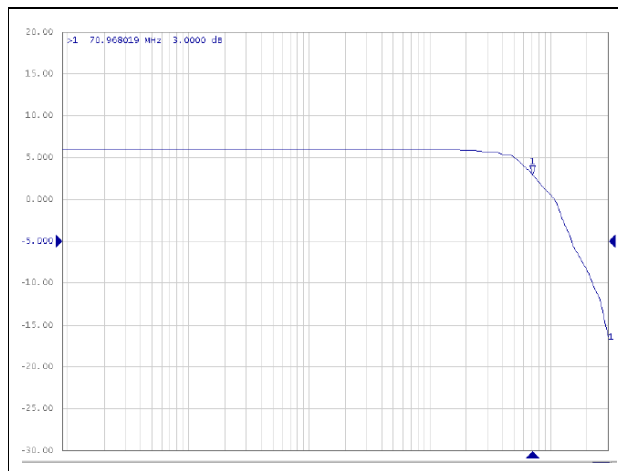
**G=+1; RF=2K; V<sub>pp</sub>=0.2V; V<sub>DD</sub>=5V**



**G=+2; RF=100  $\Omega$ ; RI=150  $\Omega$  V<sub>pp</sub>=0.2V;  
V<sub>DD</sub>=2.5V**



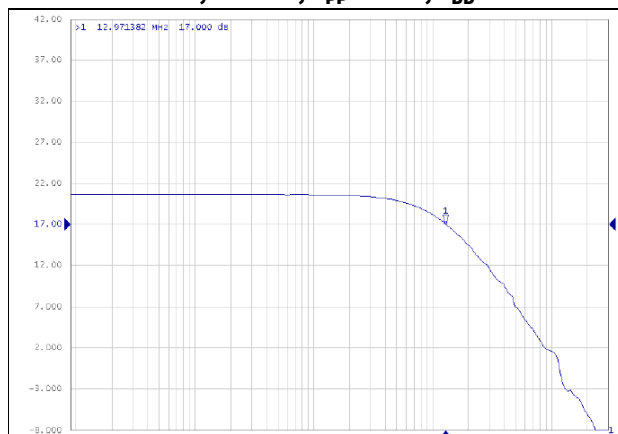
**G=+2; RF=100  $\Omega$ ; RI=150  $\Omega$  V<sub>pp</sub>=0.2V; V<sub>DD</sub>=5V**



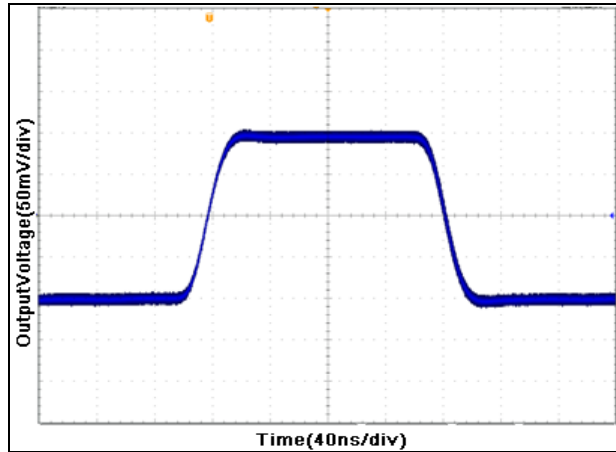
**G=+10; RF=2K; V<sub>pp</sub>=0.2V; V<sub>DD</sub>=2.5V**



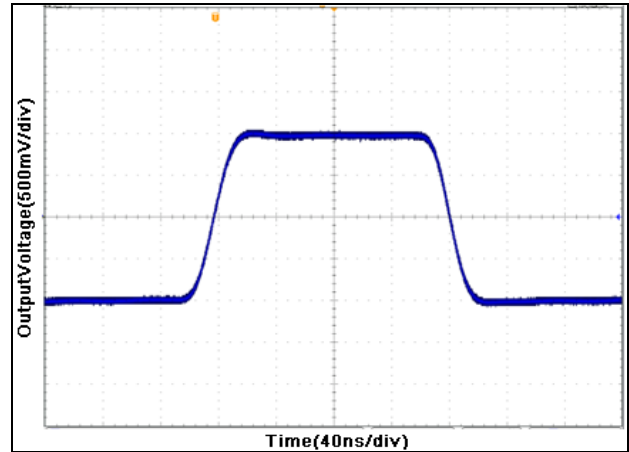
**G=+10; RF=2K; V<sub>pp</sub>=0.2V; V<sub>DD</sub>=5V**



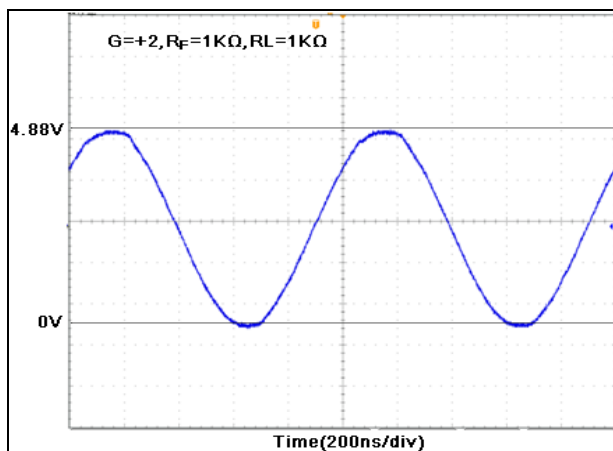
**Non-Inverting Small Signal Step Response**



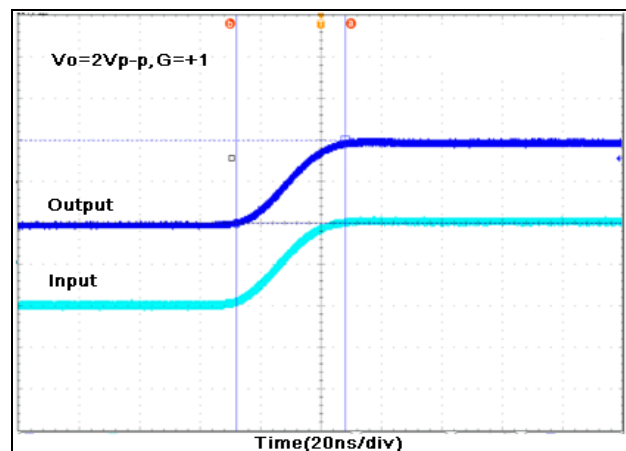
**Non-Inverting Large Signal Step Response**



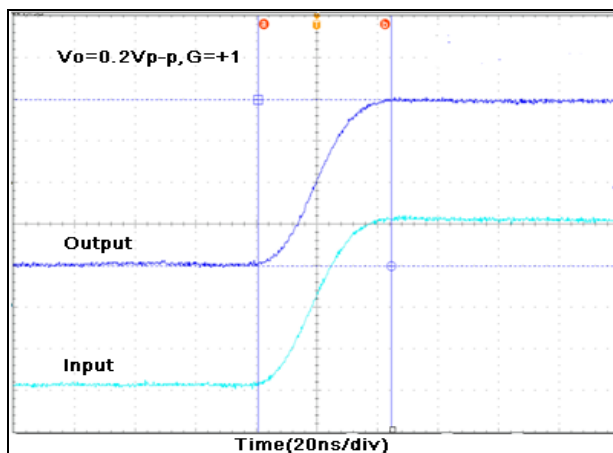
**Rail-To-Rail**



**Output Settling Time(large signal)**

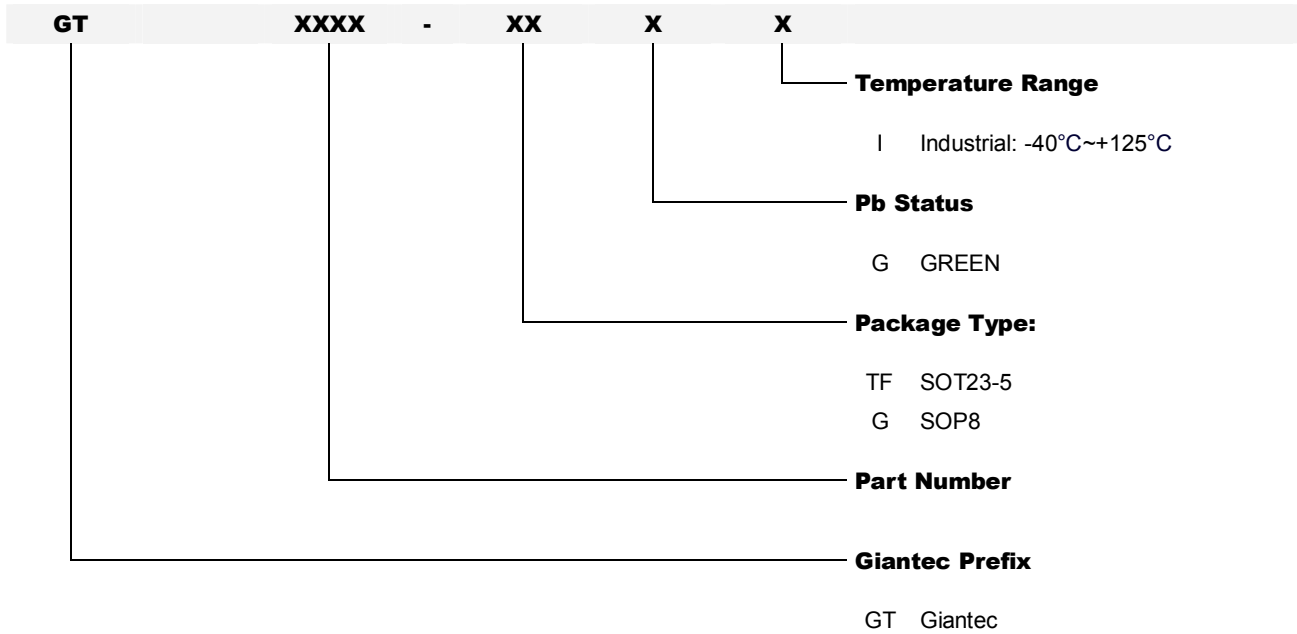


**Output Settling Time(small signal)**





## 7. Ordering Information



Order Number	Package Description	Package Option
GT7111-TFGI-TR	SOT23-5	Tape and Reel 3000
GT7111-GGI-TR	SOP8	Tape and Reel 4000



## 8. Part Markings

### 8.1 GT7111-TFGI (Top View)

		<u>1</u>	<u>1</u>	<u>1</u>	<u>Y</u>	<u>W</u>	
--	--	----------	----------	----------	----------	----------	--

<b>111</b>	GT7111-TFGI		
●	Pin 1 Indicator		
<b>Y</b>	Seal Year	<b>W</b>	Seal Week
2010 (1st half year)	A	Week 01	A
2010 (2nd half year)	B	Week 02	B
2011 (1st half year)	C	.....	
2011 (2nd half year)	D	Week 26	Z
2012 (1st half year)	E	Week 27	A
2012 (2nd half year)	F	Week 28	B
.....	.....	.....	.....
2022 (2nd half year)	Z	Week 52	Z



# GT7111

## 8.2 GT7111-GGI (Top View)

<u>G</u>	<u>T</u>	<u>7</u>	<u>1</u>	<u>1</u>	<u>1</u>	<u>G</u>	<u>G</u>	<u>I</u>
—	—	—	—	Lot Number		—	—	—
•		<u>Y</u>	<u>Y</u>	<u>W</u>	<u>W</u>	<u>S</u>	<u>V</u>	

### GT7111GGI

#### Lot Number

States the last 9 characters of the wafer lot information

•

Pin 1 Indicator

#### YY

Seal Year

00 = 2000

01 = 2001

99 = 2099

#### WW

Seal Week

01 = Week 1

02 = Week 2

.

.

.

51 = Week 51

52 = Week 52

#### S

Subcon Code

J = ASESH

L = ASEKS

#### V

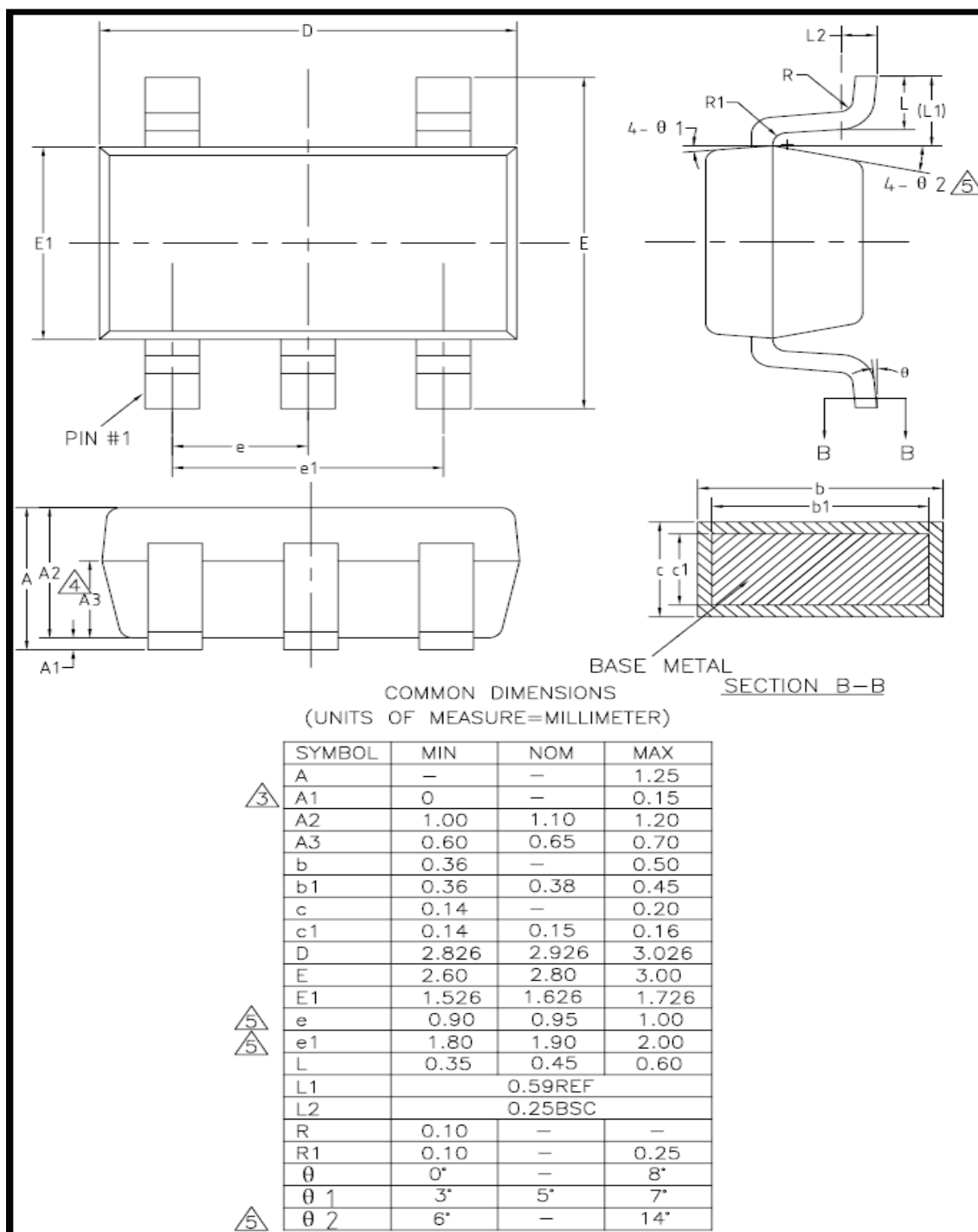
Die Version



# GT7111

## 9. Package Information

### 9.1 SOP23-5

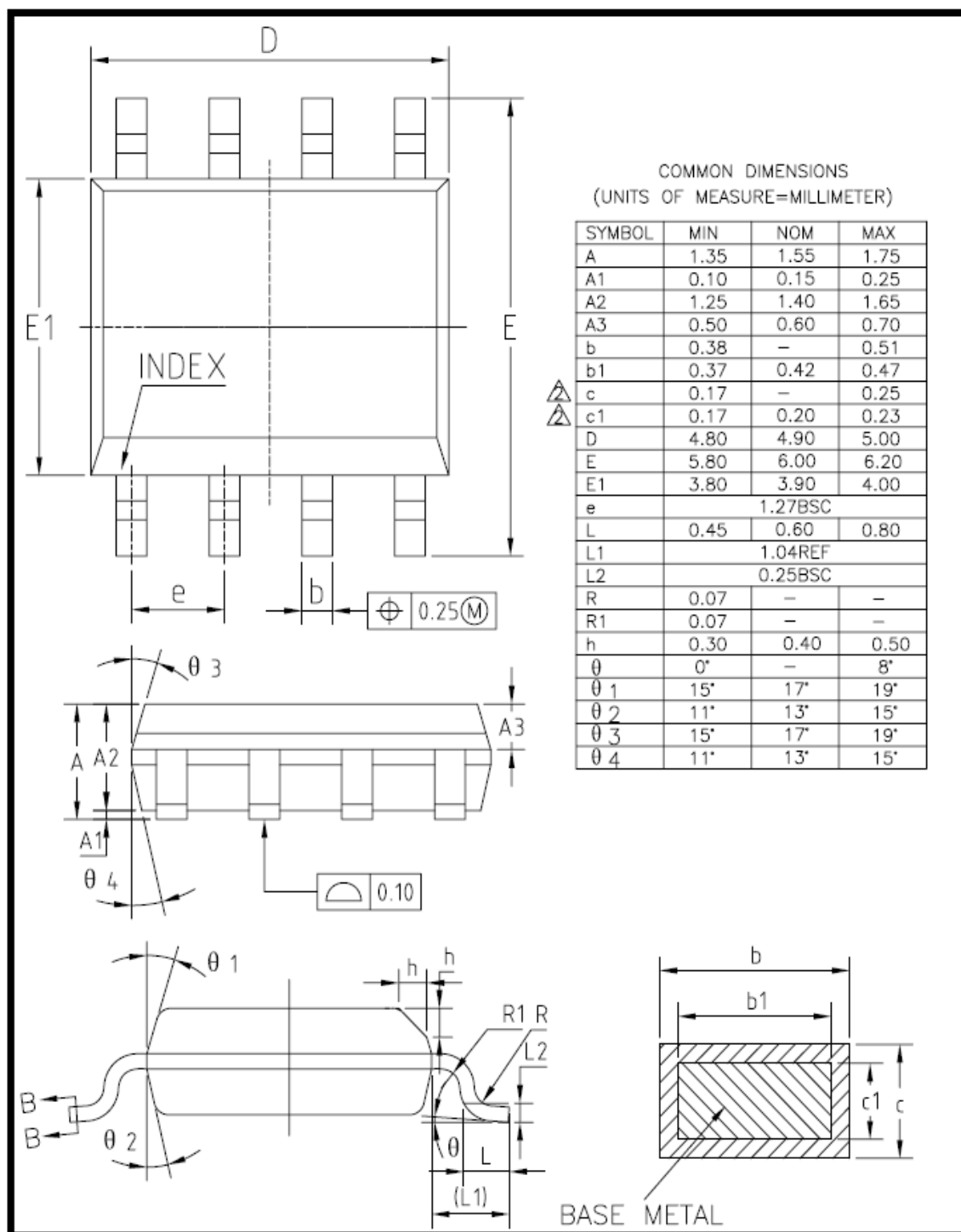






# GT7111

## 9.2 SOP8





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## 10. Revision History

Revision	Date	Descriptions
A0	Sept.,2011	Initial Version