GT7131 Single/GT7132 Dual

350 kHz, Low Power, Zero-Drift, CMOS, Rail-to-Rail Operational Amplifier with RF Filter

Advanced

1. Features

- Single-Supply Operation from +2.5V ~ +5.5V
- Rail-to-Rail Input / Output
- Gain-Bandwidth Product: 350 kHz (Typ.)
- Quiescent Current per Amplifier: 20μA (Typ.)
- Zero Drift: 0.05μV/°C (Max.)
- Low Offset Voltage: 20μV (Max. @25°C)
- Low Input Bias Current: 10pA (Typ. @25°C)
- Slew Rate: 0.1V/μs (Typ.)
- Total Harmonic Distortion plus Noise: 0.005 % (Typ.)
- Embedded RF Anti-EMI Filter
- Operating Temperature: -40°C ~ +125°C
- GT7131 Available in SOT23-5 and SOP8 Packages
- GT7132 available in SOP8 and MSOP8 Packages
-

2. General Description

The GT7131/GT7132 amplifier is single/dual supply, micro-power, zero-drift CMOS operational amplifiers, the amplifiers offer bandwidth of 350 kHz, rail-to-rail inputs and outputs, and single-supply operation from 2.5V to 5.5V. GT7131/GT7132 uses chopper stabilized technique to provide very low offset voltage (less than 20μV maximum) and near zero drift over temperature. Low quiescent supply current of 20μA per amplifier and very low input bias current of 10pA make the devices an ideal choice for low offset, low power consumption and high impedance applications.

The GT7131 is available in SOT23-5 and SOP8 packages. And the GT7132 is available in SOP8 and MSOP8 packages. The extended temperature range of -40°C to +125°C over all supply voltages offers additional design flexibility.

3. Applications

- Portable Equipment
- Mobile Communications
- Filter and Buffer
- Sensor Interface
- Medical Instrumentation
- Battery-Powered Instruments
- Handheld Test Equipment

4. Pin Configuration

4.1 GT7131 SOT23-5 and SOP8 (Top View)

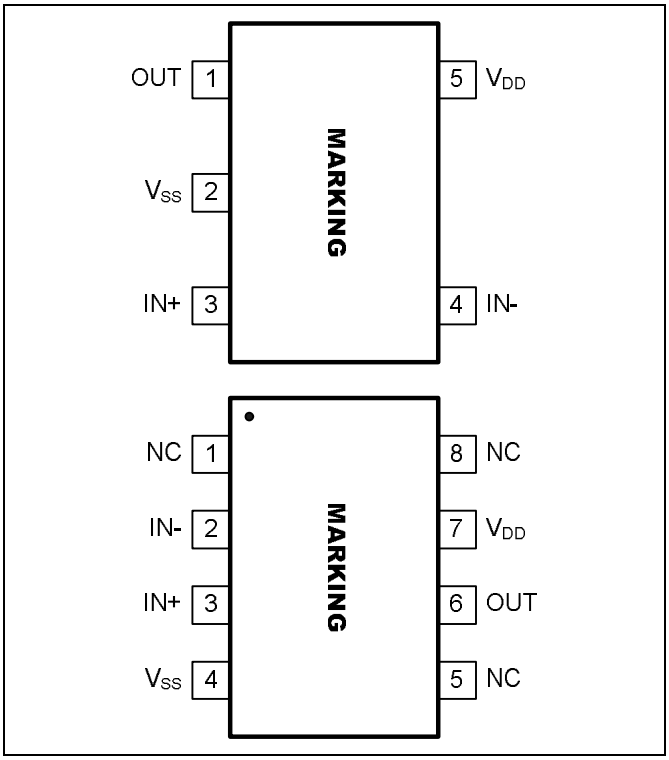


Figure 1-a. Pin Assignment Diagram (SOT23-5 and SOP8 Package)

4.2 GT7132 SOP8 and MSOP8 (Top View)

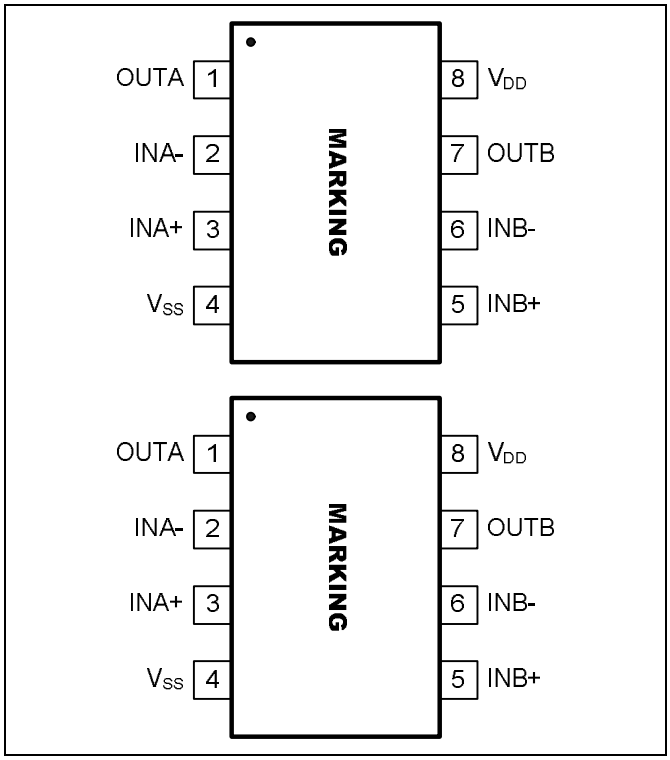


Figure 2-b. Pin Assignment Diagram (SOP8 and MSOP8 Package)

Note: Please see section "**Part Markings**" for detailed Marking Information.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Condition	Min	Max
Power Supply Voltage (V_{DD} to Vss)	-0.5V	+7V
Analog Input Voltage (IN+ or IN-)	Vss-0.5V	V_{DD}+0.5V
PDB Input Voltage	Vss-0.5V	+7V
Operating Temperature Range	-40°C	+125°C
Junction Temperature	+150°C	
Storage Temperature Range	-65°C	+150°C
Lead Temperature (soldering, 10sec)	+300°C	
Package Thermal Resistance (T_A=+25°C)		
SOP23-5, θ_{JA}	190°C	
SOP8, θ_{JA}	130°C	
MSOP8, θ_{JA}	210°C	

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.2 Electrical Characteristics

(V_{DD} = +5V, Vss = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, R_L=10K tied to V_{DD}/2, SHDNB = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A =+25°C.) (Note 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply-Voltage Range	V_{DD}	Guaranteed by the PSRR test	2.5	-	5.5	V
Quiescent Supply Current (per Amplifier)	I_Q	V_{DD} = 5V	14	20	26	μA
Input Offset Voltage	V_{OS}		-	-	±20	μV
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$		-	-	0.05	μV/°C
Input Bias Current	I_B	(Note 2)	-	10	-	pA
Input Offset Current	I_{OS}	(Note 2)	-	100	-	pA
Input Common-Mode Voltage Range	V_{CM}		-0.1	-	V_{DD}+0.1	V
Common-Mode Rejection Ratio	CMRR	V_{DD}=5.5 Vss-0.1V≤V_{CM}≤V_{DD}+0.1V	90	110	-	dB
		Vss≤V_{CM}≤5V	95	115	-	dB
Power-Supply Rejection Ratio	PSRR	V_{DD} = +2.5V to +5.5V	85	105	-	dB
Open-Loop Voltage Gain	A_V	V_{DD}=5V, R_L=10kΩ, 0.05V≤V_O≤4.95V	100	120	-	dB

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Voltage Swing	V_{OUT}	$\|V_{IN+}-V_{IN-}\| \geq 10mV$, R_L = 100kΩ to $V_{DD}/2$, $V_{DD}-V_{OH}$	-	6	-	mV
		$\|V_{IN+}-V_{IN-}\| \geq 10mV$, R_L = 100kΩ to $V_{DD}/2$, $V_{OL}-V_{SS}$	-	6	-	mV
		$\|V_{IN+}-V_{IN-}\| \geq 10mV$, R_L = 5kΩ to $V_{DD}/2$, $V_{DD}-V_{OH}$	-	60	-	mV
		$\|V_{IN+}-V_{IN-}\| \geq 10mV$, R_L = 5kΩ to $V_{DD}/2$, $V_{OL}-V_{SS}$	-	60	-	mV
Output Short-Circuit Current	I_{SC}	Sinking or Sourcing	-	±5	-	mA
Gain Bandwidth Product	GBW	A_V = +1V/V	-	350	-	kHz
Slew Rate	SR	A_V = +1V/V	-	0.1	-	V/μs
Settling Time	t_S	To 0.1%, V_{OUT} = 2V step A_V = +1V/V	-	20	-	μs
Over Load Recovery Time		$V_{IN} \times Gain=V_S$	-	100	-	μs
Input Voltage Noise Density	e_n	f = 1kHz	-	70	-	nV/√Hz
		f = 10kHz	-	60	-	
Total Harmonic Distortion plus Noise	THD+N	V_{OUT} = $2V_{PP}$,Av = +1V/V, R_L = 10kΩ to GND, f = 1kHz	-	0.005	-	%
		V_{OUT} = $2V_{PP}$,Av = +1V/V, R_L =10kΩ to GND, f = 10kHz	-	0.1	-	

Note 1: All devices are 100% production tested at T_A = +25°C; all specifications over the automotive temperature range is guaranteed by design, not production tested.

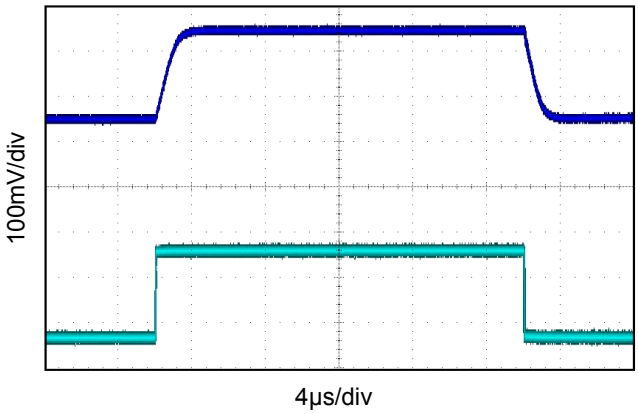
Note 2: Parameter is guaranteed by design.

5.3 Typical characteristics

(T_A=+25°C, R_L=10 kΩ connected to V_S/2 and V_{OUT}= V_S/2, unless otherwise noted.)

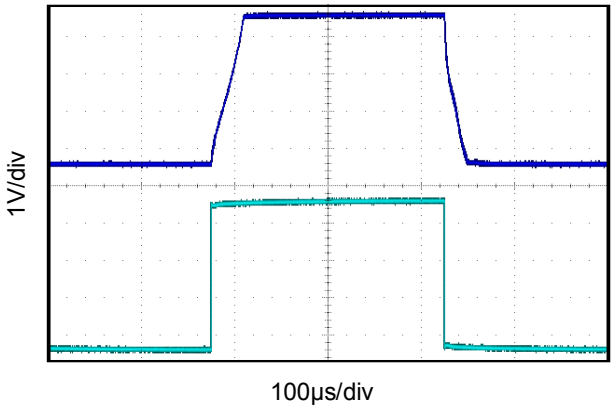
Small Signal Step Response

G=+1V/V,RL=10kΩ,CL=0pF

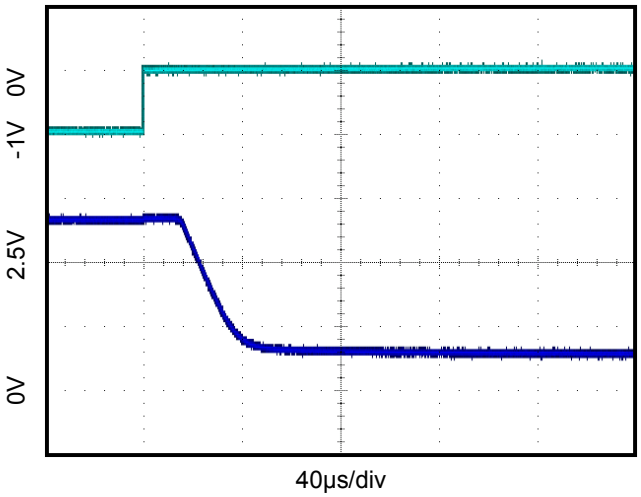


Large Signal Step Response

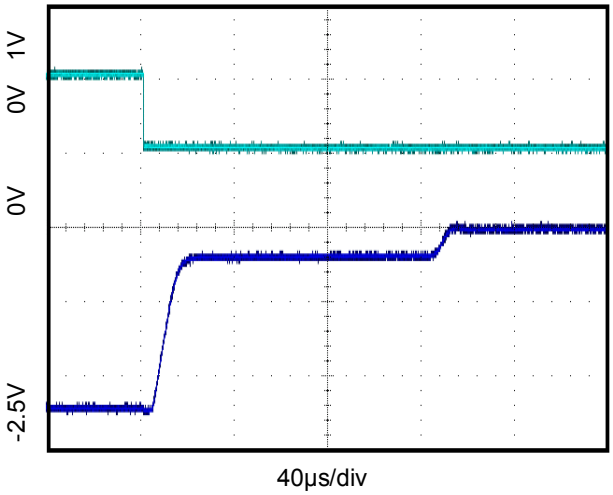
G=+1V/V,RL=100kΩ,CL=100pF



Positive Over-Voltage Recovery

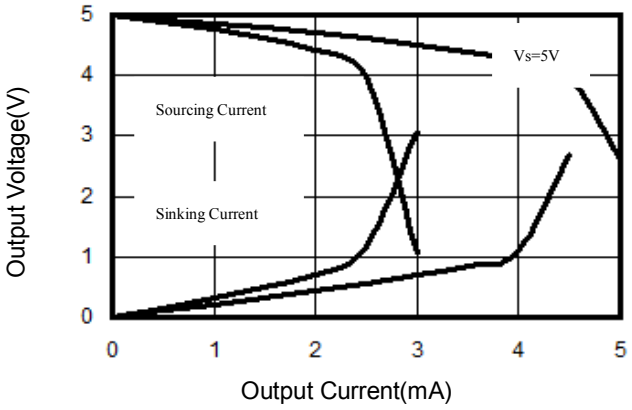


Negative Over-Voltage Recovery

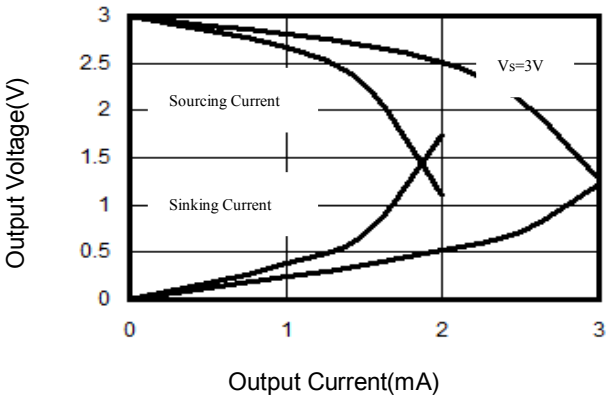


Typical characteristics (Continued)

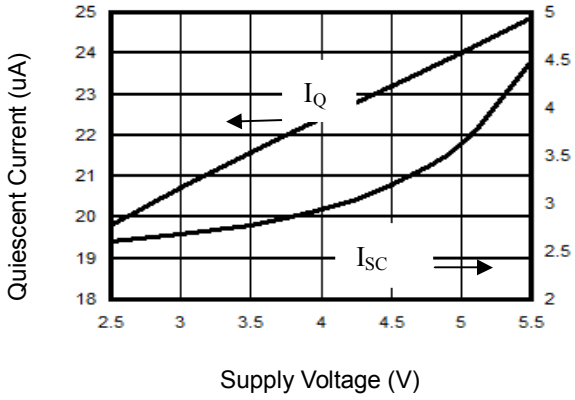
Output Voltage Swing vs. Output Current



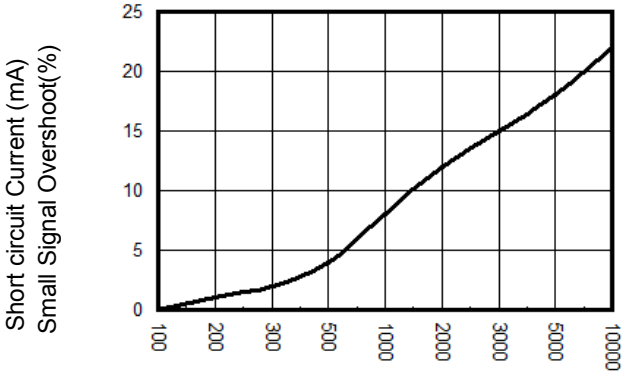
Output Voltage Swing vs. Output Current



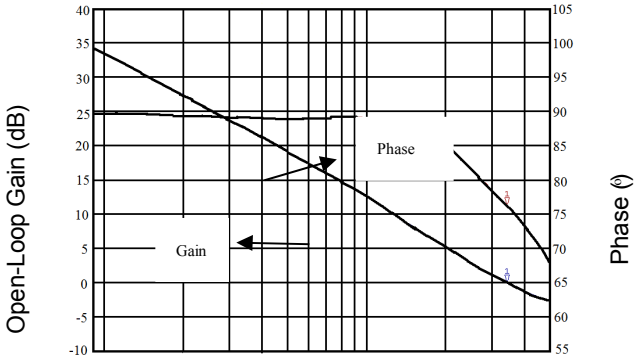
Quiescent and Short-Circuit Current vs. Supply Voltage



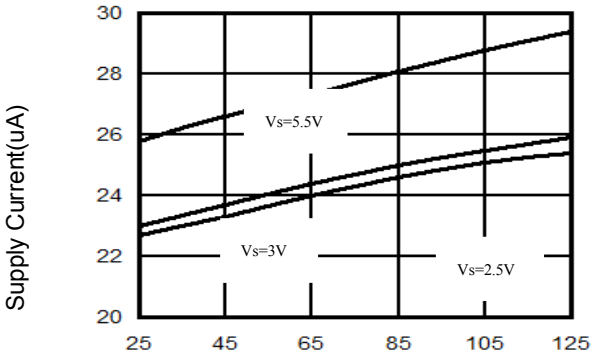
Small Signal Overshoot vs. Load Capacitance



Open-Loop Gain And Phase vs. Frequency



Supply Current vs. Temperature



6. Application Information

6.1 Size

GT7131/GT7132 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. The small footprints of the GT7131/GT7132 series packages save space on printed circuit boards and enable the design of smaller electronic products.

6.2 Power Supply Bypassing and Board Layout

GT7131/GT7132 series operates from a single 2.5V to 5.5V supply or dual ±1.25V to ±2.75V supplies. For best performance, a 0.1μF ceramic capacitor should be placed close to the V_{DD} pin in single supply operation. For dual supply operation, both V_{DD} and V_{SS} supplies should be bypassed to ground with separate 0.1μF ceramic capacitors.

6.3 Low Supply Current

The low supply current (typical 20μA/40μA) of GT7131/GT7132 series will help to maximize battery life. They are ideal for battery powered systems

6.4 Operating Voltage

GT7131/GT7132 series operate under wide input supply voltage (2.5V to 5.5V). In addition, all temperature specifications apply from -40 °C to +125 °C. Most behavior remains unchanged throughout the full operating voltage range. These guarantees ensure operation throughout the single Li-Ion battery lifetime

6.5 Rail-to-Rail Input

The input common-mode range of GT7131/GT7132 series extends 100mV beyond the supply rails (V_{SS}-0.1V to V_{DD}+0.1V). This is achieved by using complementary input stage. For normal operation, inputs should be limited to this range.

6.6 Rail-to-Rail Output

Rail-to-Rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating in low supply voltages. The output voltage of GT7131/GT7132series can typically swing to less than 10mV from supply rail in light resistive loads (>100kΩ), and 60mV of supply rail in moderate resistive loads (5kΩ).

6.7 Capacitive Load Tolerance

The GT7131/GT7132 series can directly drive 250pF capacitive load in unity-gain without oscillation. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. In unity-gain configurations, the capacitive load drive can be improved by inserting an isolation resistor R_{ISO} in series with the capacitive load, as shown in ***Figure 2***.

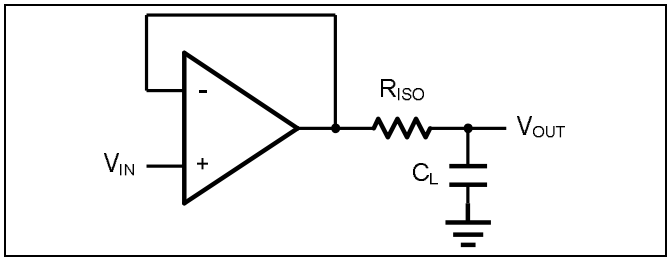


Figure 2. Indirectly Driving a Capacitive Load Using Isolation Resistor

The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. However, if there is a resistive load R_L in parallel with the capacitive load, a voltage divider (proportional to R_{ISO}/R_L) is formed, this will result in a gain error.

The circuit in ***Figure 3*** is an improvement to the one in ***Figure 2***. R_F provides the DC accuracy by feed-forward the V_{IN} to R_L. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving the phase margin in the overall feedback loop. Capacitive drive can be increased by increasing the value of C_F. This in turn will slow down the pulse response.

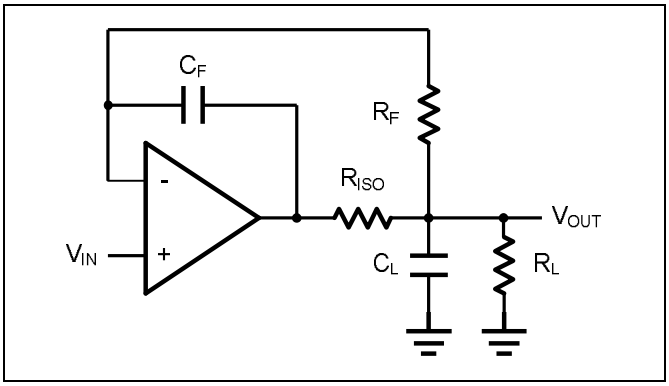


Figure 3. Indirectly Driving a Capacitive Load with DC Accuracy

6.8 Differential amplifier

The differential amplifier allows the subtraction of two input voltages or cancellation of a signal common the two inputs. It is useful as a computational amplifier in making a differential to single-end conversion or in rejecting a common mode signal. ***Figure 4.*** shown the differential amplifier using GT7131/GT7132.

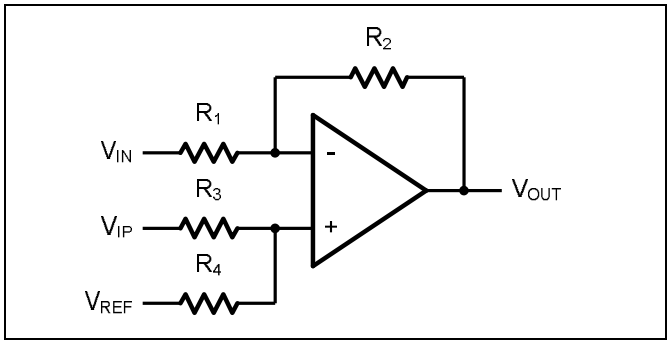


Figure 4. Differential Amplifier

$$V_{OUT}=(\frac{Rl+R2}{R3+R4})\frac{R4}{Rl}V_{IN}-\frac{R2}{Rl}V_{IP}+(\frac{Rl+R2}{R3+R4})\frac{R3}{Rl}V_{REF}$$

If the resistor ratios are equal (i.e. R_1=R_3 and R_2=R_4), then

$$V_{OUT}=\frac{R2}{R1}(V_{IP}-V_{IN})+V_{REF}$$

6.9 Instrumentation Amplifier

The input impedance of the previous differential amplifier is set by the resistors R1, R2, R3, and R4. To maintain the high input impedance, one can use a voltage follower in front of each input as shown in the following two instrumentation amplifiers.

6.10 Three-Op-Amp Instrumentation Amplifier

The dual GT7132 can be used to build a three-op-amp instrumentation amplifier as shown in ***Figure 5***.

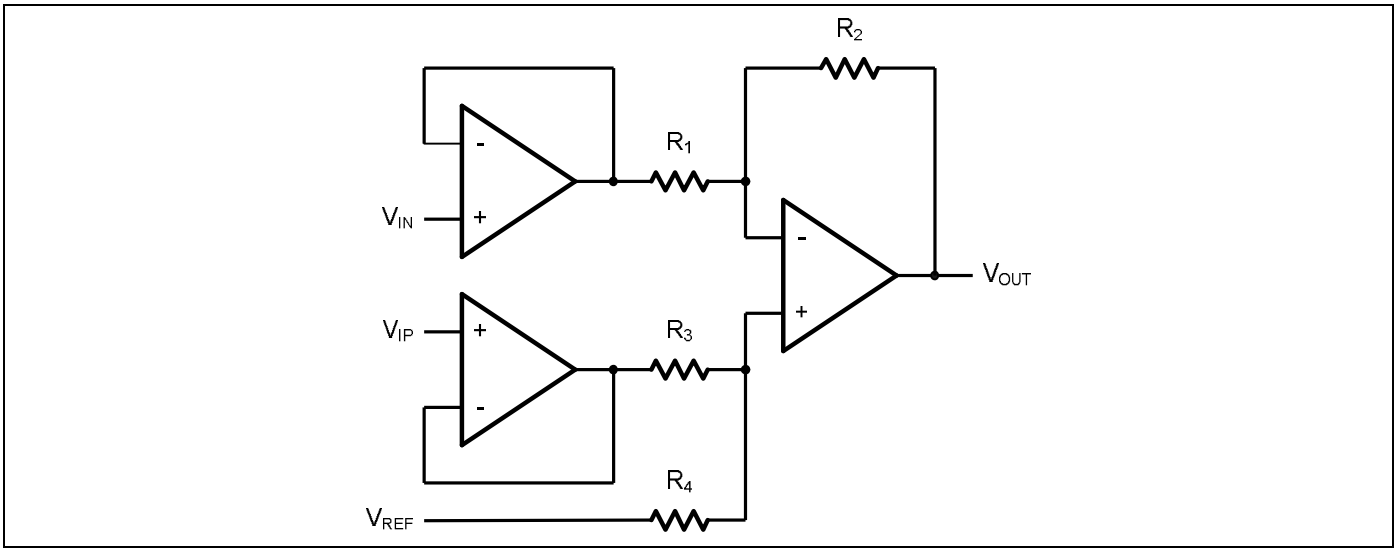


Figure 5. Three-Op-Amp Instrumentation Amplifier

The amplifier in ***Figure 5*** is a high input impedance differential amplifier with gain of R_2/R_1. The two differential voltage followers assure the high input impedance of the amplifier.

$$V_{OUT} = (1 + \frac{R4}{R3})(V_{IP} - V_{IN})$$

6.11 Two-Op-Amp Instrumentation Amplifier

GT7131/GT7132 can also be used to make a high input impedance two-op-amp instrumentation amplifier as shown in ***Figure 6***.

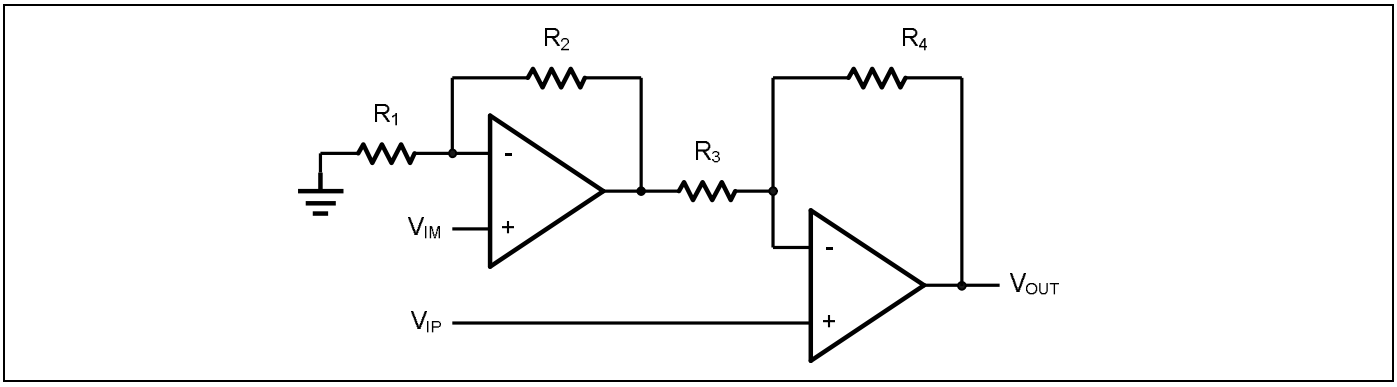


Figure 6. Two-Op-Amp Instrumentation Amplifier

Where $R_1=R_3$ and $R_2=R_4$. If all resistors are equal, then $V_{OUT}=2(V_{IP}-V_{IN})$

6.12 Single-Supply Inverting Amplifier

The inverting amplifier is shown in ***Figure 7***. The capacitor C_1 is used to block the DC signal going into the AC signal source V_{IN}. The value of R_1 and C_1 set the cut-off frequency to $f_C=1/(2\pi R_1 C_1)$. The DC gain is defined by $V_{OUT}=-(R_2/R_1)V_{IN}$

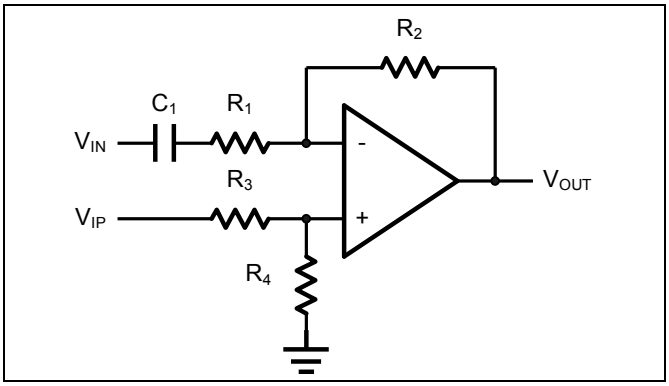


Figure 7. Single Supply Inverting Amplifier

6.13 Low Pass Active Filter

The low pass active filter is shown in ***Figure 8***. The DC gain is defined by $-R_2/R_1$. The filter has a -20dB/decade roll-off after its corner frequency $f_C=1/(2\pi R_3 C_1)$.

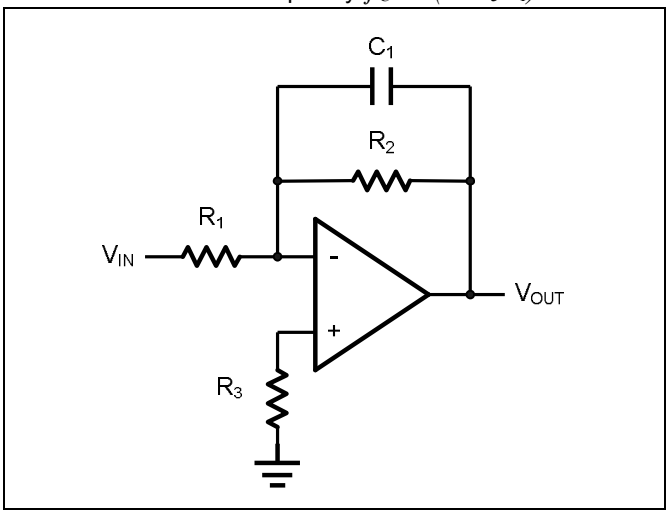


Figure 8. Low Pass Active Filter

6.14 Sallen-Key 2nd Order Active Low-Pass Filter

GT7131/GT7132 can be used to form a 2nd order Sallen-Key active low-pass filter as shown in ***Figure 9***. The transfer function from V_{IN} to V_{OUT} is given by

$$\frac{V_{OUT}}{V_{IN}}(S)=\frac{\frac{1}{C_1C_2R_1R_2}A_{LP}}{S^2+S(\frac{1}{C_1R_1}+\frac{1}{C_1R_2}+\frac{1}{C_2R_2}-\frac{A_{LP}}{C_2R_2})+\frac{1}{C_1C_2R_1R_2}}$$

Where the DC gain is defined by $A_{LP}=1+R_3/R_4$, and the corner frequency is given by

$$\omega C=\sqrt{\frac{1}{C_1C_2R_1R_2}}$$

The pole quality factor is given by

$$\frac{\omega C}{Q}=\frac{1}{C_1R_1}+\frac{1}{C_1R_2}+\frac{1}{C_2R_2}-\frac{A_{LP}}{C_2R_2}$$

Let R1=R2=R and C1=C2=C, the corner frequency and the pole quality factor can be simplified as below

$$\omega_C=\frac{1}{CR}$$

And $Q=2-R_3/R_4$

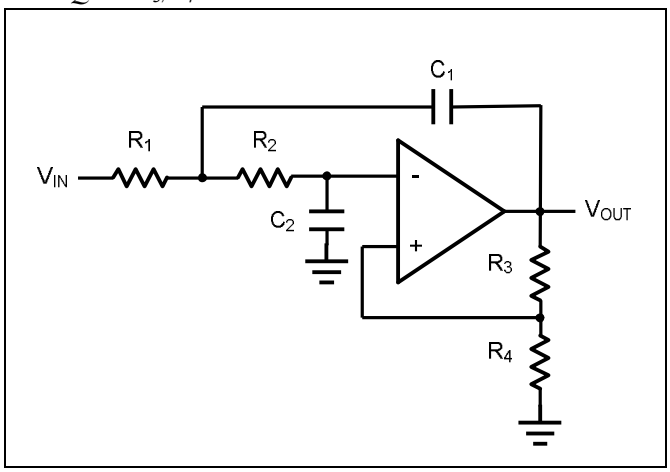


Figure 9. Sanllen-Key 2nd Order Active Low-Pass Filter

6.15 Sallen-Key 2nd Order high-Pass Active Filter

The 2nd order Sallen-key high-pass filter can be built by simply interchanging those frequency selective components R_1, R_2, C_1, and C_2 as shown in ***Figure 10***.

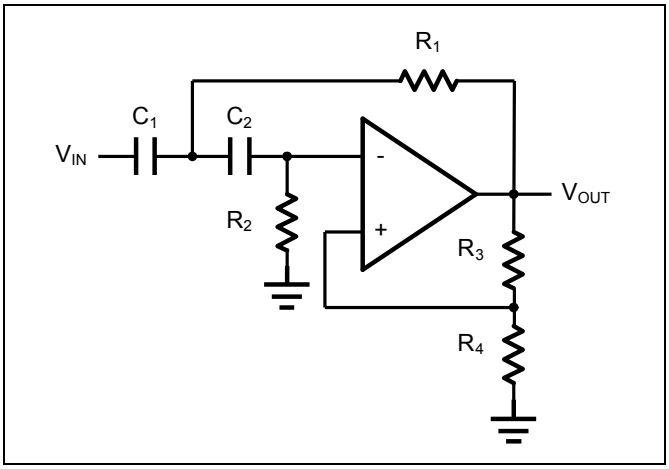


Figure 10. Sanllen-Key 2nd Order Active High-Pass Filter

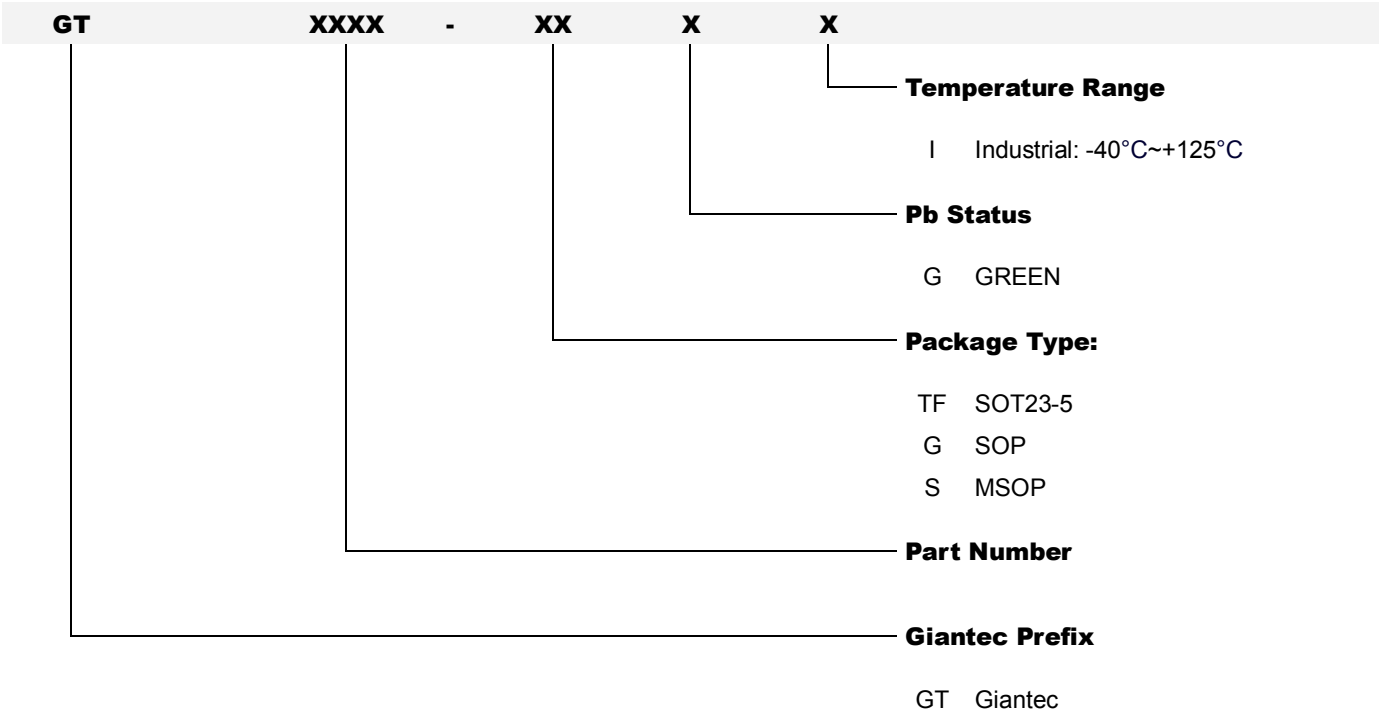
$$\frac{V_{OUT}}{V_{IN}}(S)=\frac{S^2 A_{HP}}{S^2+S(\frac{1}{C_1R_1}+\frac{1}{C_2R_2}+\frac{1-A_{HP}}{C_1R_1})+\frac{1}{C_1C_2R_1R_2}}$$

Where $A_{HP}=1+R_3/R_4$

6.16 Input Offset Cancellation

The GT7131/GT7132 series opamps use internal chopping stabilized technique to cancel dc offset and flick noise. Since the offset temperature drift is a dc parameter, it is also cancelled by the chopping technique. The amplifier requires approximately 100μs to achieve the specified V_{os} accuracy.

7. Ordering Information



Order Number	Package Description	Package Option
GT7131-TFGI-TR	SOT23-5	Tape and Reel 3000
GT7131-GGI-TR	SOP8	Tape and Reel 4000
GT7132-GGI-TR	SOP8	Tape and Reel 4000
GT7132-SGI-TR	MSOP8	Tape and Reel 4000

8. Part Markings

8.1 GT7131-TFGI (Top View)

1	3	1	Y	W

131	GT7131-TFGI		
●	Pin 1 Indicator		
Y	Seal Year	**W**	Seal Week
2010 (1st half year)	A	Week 01	A
2010 (2nd half year)	B	Week 02	B
2011 (1st half year)	C	……	
2011 (2nd half year)	D	Week 26	Z
2012 (1st half year)	E	Week 27	A
2012 (2nd half year)	F	Week 28	B
……	……	……	……
2022 (2nd half year)	Z	Week 52	Z

8.2 GT7131-GGI (Top View)

G	T	7	1	3	1	G	G	I
				Lot Number				
●		Y	Y	W	W	S	V	

GT7131GGI			02 = Week 2
Lot Number	States the last 9 characters of the wafer		.
	lot information		.
●	Pin 1 Indicator		.
YY	Seal Year		51 = Week 51
	00 = 2000		52 = Week 52
	01 = 2001	**S**	Subcon Code
	99 = 2099		J = ASESH
WW	Seal Week		L = ASEKS
	01 = Week 1	**V**	Die Version

8.3 GT7132-GGI (Top View)

G	T	7	1	3	2	G	G	I
				Lot Number				
●		Y	Y	W	W	S	V	

GT7132GGI

Lot Number	States the last 9 characters of the wafer lot information		02 = Week 2 . . .
●	Pin 1 Indicator		
YY	Seal Year 00 = 2000 01 = 2001 99 = 2099		51 = Week 51 52 = Week 52
WW	Seal Week 01 = Week 1	**S** **V**	Subcon Code J = ASESH L = ASEKS Die Version

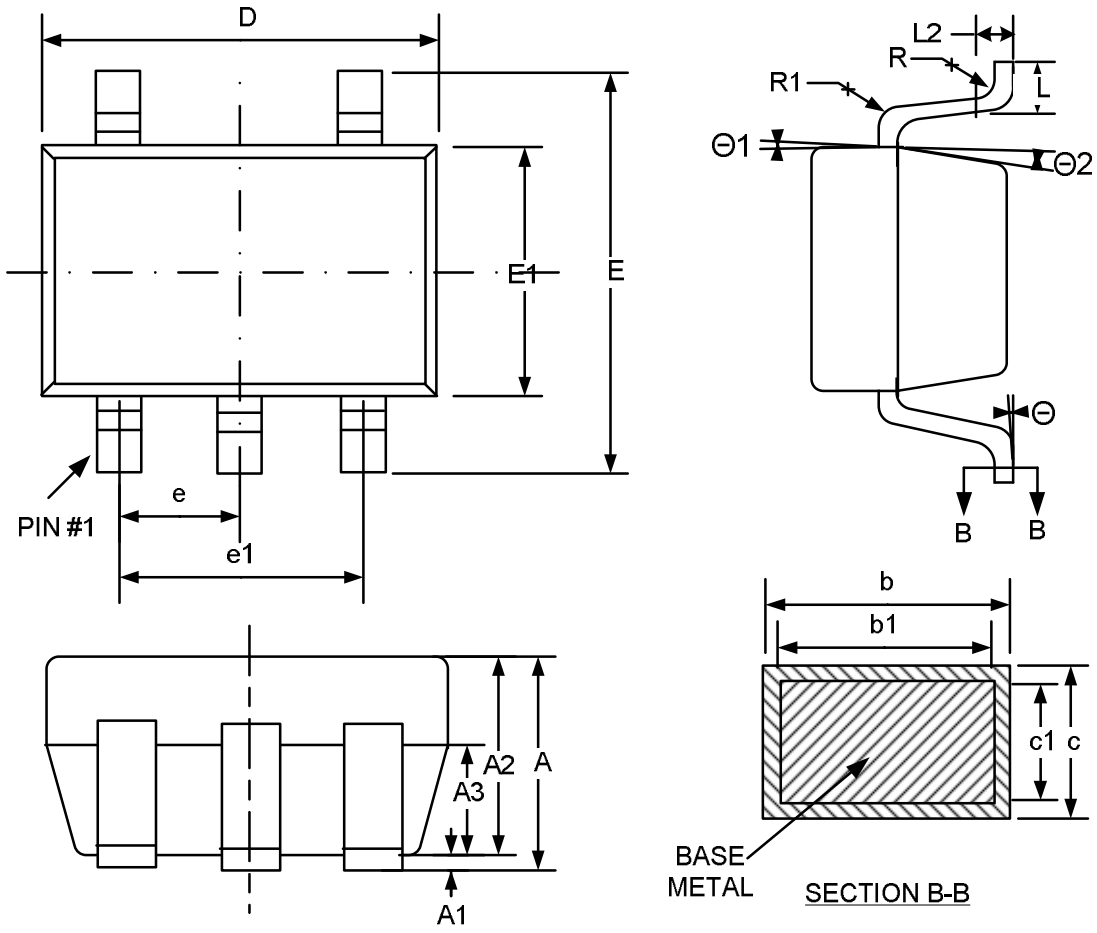
8.4 GT7132-SGI (Top View)

G	T	7	1	3	2		
				Lot Number			
●		Y	Y	W	W	S	V

GT7132	GT7132-SGI		02 = Week 2
Lot Number	States the last 9 characters of the wafer lot information		. .
●	Pin 1 Indicator		.
YY	Seal Year 00 = 2000 01 = 2001 99 = 2099		51 = Week 51 52 = Week 52
WW	Seal Week 01 = Week 1	**S** **V**	Subcon Code J = ASESH L = ASEKS Die Version

9. Package Information

9.1 SOP23-5

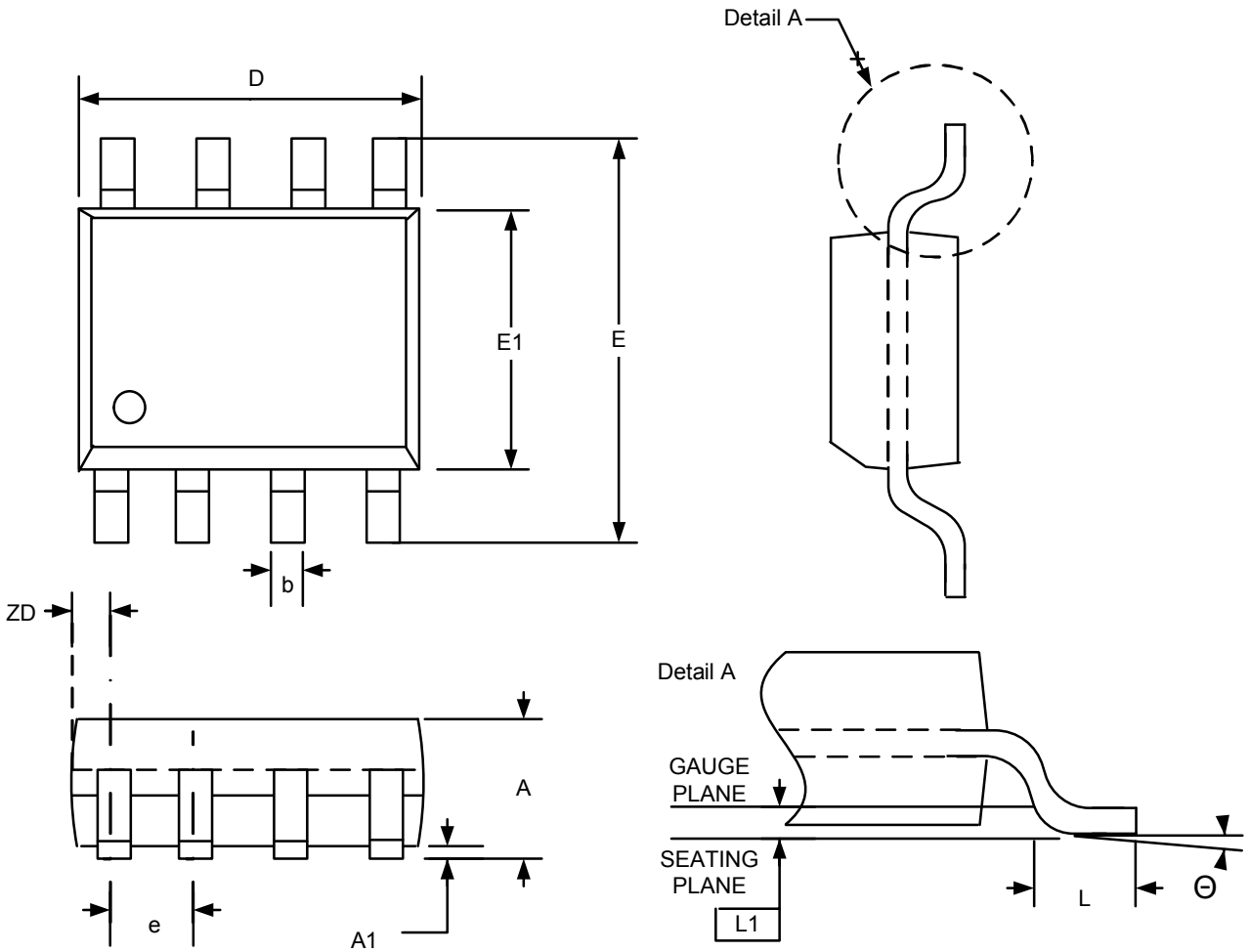


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.25	--	--	0.049
A1	0.00	--	0.15	0.000	--	0.006
A2	1.00	1.10	1.20	0.039	0.043	0.047
A3	0.60	0.65	0.70	0.024	0.026	0.028
b	0.36	--	0.50	0.014	--	0.020
b1	0.36	0.38	0.45	0.014	0.015	0.018
c	0.14	--	0.20	0.006	--	0.008
c1	0.14	0.15	0.16	0.006	0.006	0.006
D	2.826	2.926	3.026	0.111	0.115	0.119
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.526	1.626	1.726	0.060	0.064	0.068
e	0.90	0.95	1.00	0.035	0.037	0.039
e1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.35	0.45	0.60	0.014	0.018	0.024
L1	0.59REF			0.023REF		
L2	0.25BSC			0.010BSC		
R	0.10	--	--	0.004	--	--
R1	0.10	--	0.25	0.004	--	0.010
Θ	0°	--	8°	0°	--	8°
Θ1	3°	5°	7°	3°	5°	7°

Note:

1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MO-178 AA
5. Drawing is not to scale

9.2 SOP8

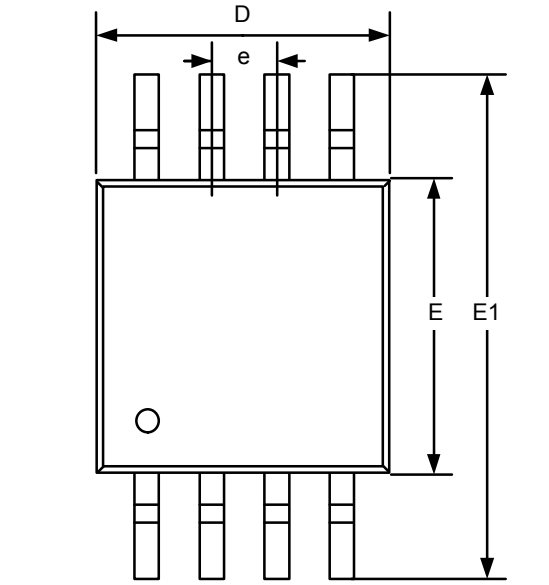


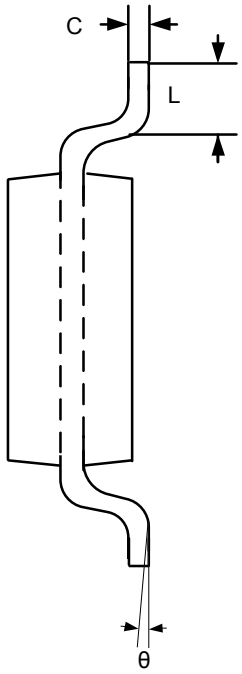
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

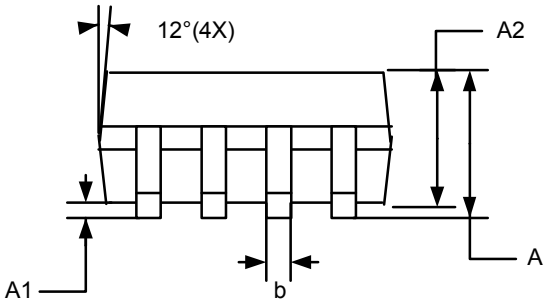
Note:

1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

9.3 MSOP8







SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.10	--	--	0.043
A1	0.05	--	0.15	0.002	--	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.25	--	0.40	0.010	--	0.016
C	0.13	--	0.23	0.005	--	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	4.90 BSC			0.193 BSC		
e	0.65 BSC			0.026 BSC		
L	--	--	0.55	--	--	0.022
Θ	0	--	7°	0	--	7°

Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Refer to Jedec standard MO187
4. Drawing is not to scale

10. Revision History

Revision	Date	Descriptions
A0	Oct.,2011	Initial Version