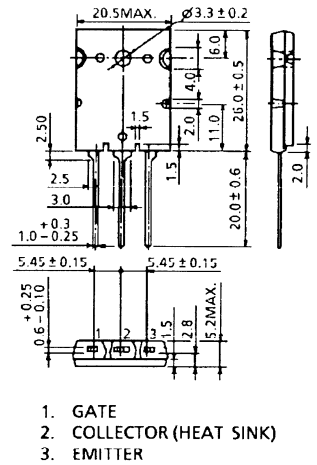
TOSHIBA Insulated Gate Bipolar Transistor Silicon N Channel IGBT

GT80J101B

High Power Switching Applications

- Enhancement mode type
- High speed: t_f = 0.40 μs (max) (I_C = 80 A)
- Low saturation voltage: $V_{CE\ (sat)}$ = 2.9 V (max) (I_C = 80 A)

Unit: mm



1. GATE
2. COLLECTOR (HEAT SINK)
3. EMITTER

JEDEC	?
JEITA	?
TOSHIBA	2-21F2C

Weight: 9.75 g (typ.)

Maximum Ratings (Ta = 25°C)

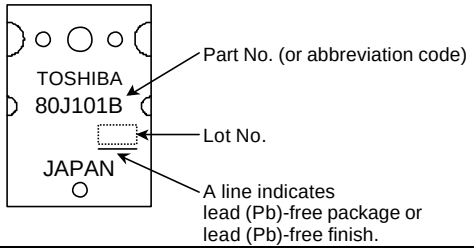
Characteristics		Symbol	Rating	Unit
Collector-emitter voltage		V_{CES}	600	V
Gate-emitter voltage		V_{GES}	±20	V
Continuous collector current	@Tc = 100°C	I_C	33	A
	@Tc = 25°C		80	
Pulsed collector current (Note 1)		I_{CP}	160	A
Collector power dissipation	@Tc = 100°C	P_C	80	W
	@Tc = 25°C		200	
	@Ta = 25°C		3.5	
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	−55~150	°C
Screw torque		—	0.8	N·m

Note 1: The Maximum rating of I_{CP}=160A is limited by pulse (1ms).
Refer to the graph of safe operating area for the detail.

Thermal Characteristics

Characteristics	Symbol	Rating	Unit
Thermal resistance , junction to case (Tc = 25°C)	$R_{th\ (j\text{-}c)}$	0.625	°C/W
Thermal resistance , junction to air (Ta = 25°C)	$R_{th\ (j\text{-}a)}$	35.7	°C/W

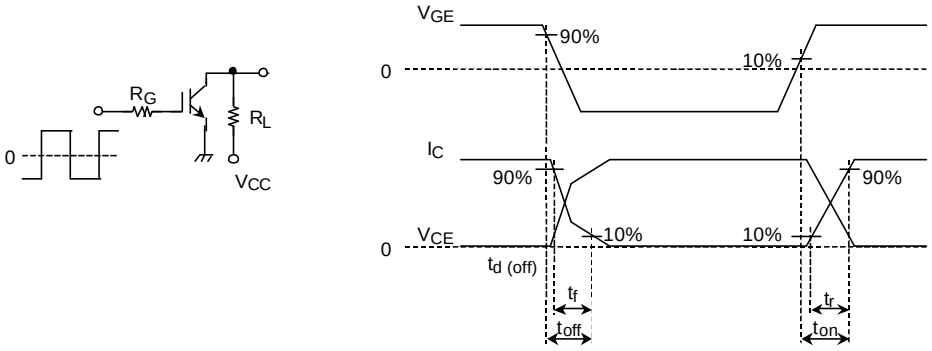
MARKING



Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GES}	V_{GE} = ±25 V, V_{CE} = 0	—	—	±500	nA
Collector cut-off current		I_{CES}	V_{CE} = 600 V, V_{GE} = 0	—	—	1.0	mA
Gate-emitter cut-off voltage		$V_{GE\ (OFF)}$	V_{CE} = 5 V, I_C = 80 mA	3.0	—	6.0	V
Collector-emitter saturation voltage		$V_{CE\ (sat)}$ (1)	I_C = 10 A, V_{GE} = 15 V	—	—	2.0	V
		$V_{CE\ (sat)}$ (2)	I_C = 80 A, V_{GE} = 15 V	—	2.4	2.9	
Input capacitance		C_{ies}	V_{CE} = 10 V, V_{GE} = 0, f = 1 MHz	—	5500	—	pF
Switching time	Rise time	t_r	Resistive load V_{CC} = 300 V, I_C = 80 A V_{GG} = ±15 V, R_G = 33Ω (Note 2)	—	0.3	—	µs
	Turn-on time	t_{on}		—	0.5	—	
	Fall time	t_f		—	0.25	0.40	
	Turn-off time	t_{off}		—	0.7	—	

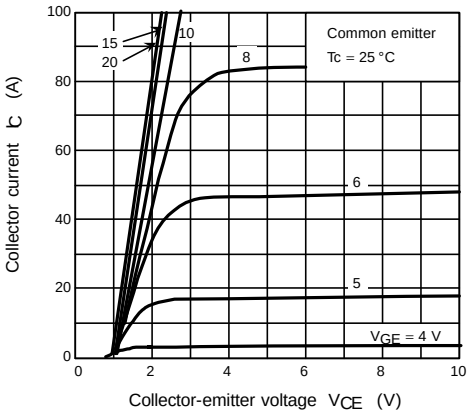
Note 2: Switching time measurement circuit and input/output waveforms.



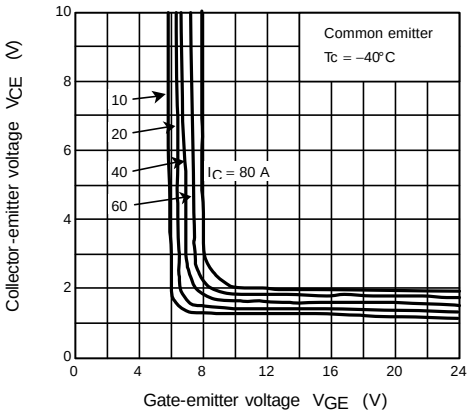
Caution on handling

This device is MOS gate type. Therefore, please care about ESD when use.

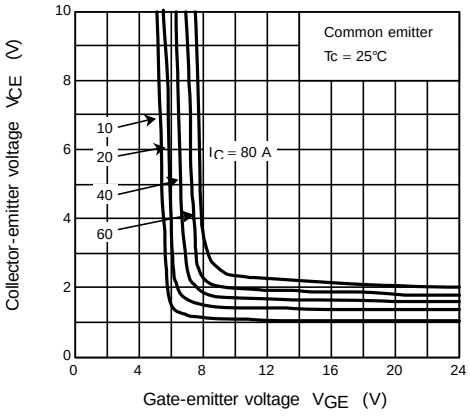
$I_C - V_{CE}$



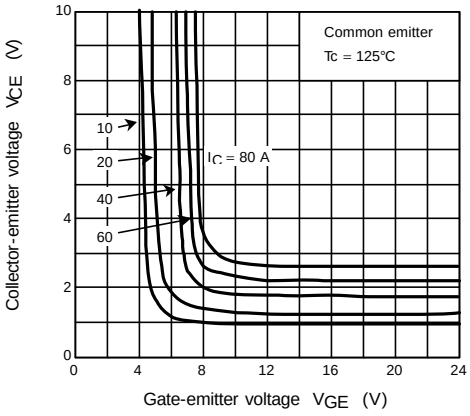
$V_{CE} - V_{GE}$



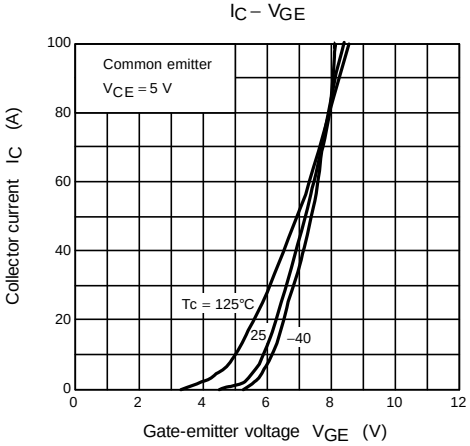
$V_{CE} - V_{GE}$



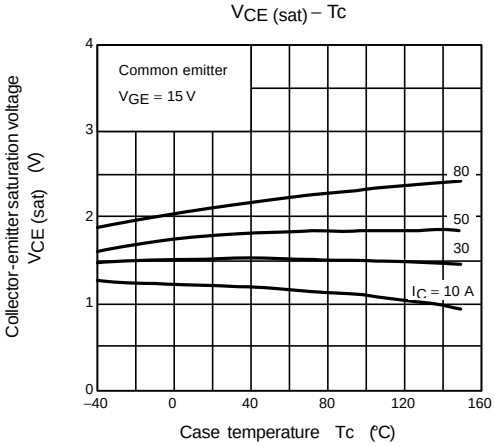
$V_{CE} - V_{GE}$



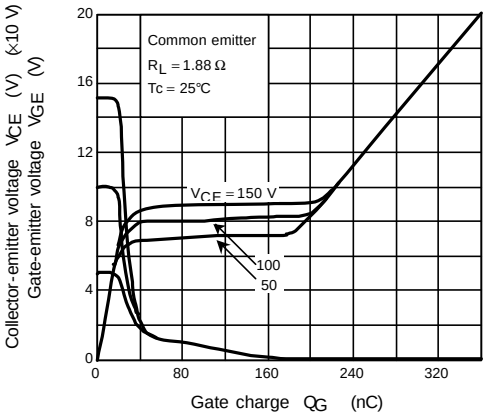
$I_C - V_{GE}$



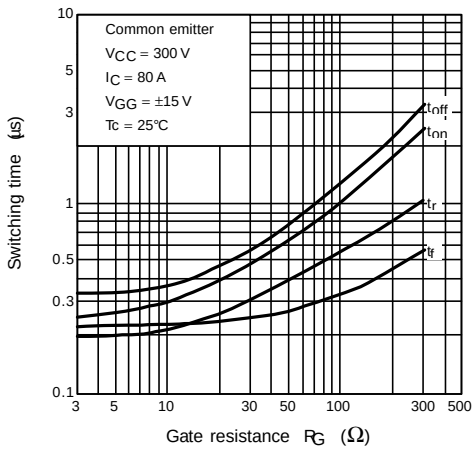
$V_{CE\ (sat)} - Tc$



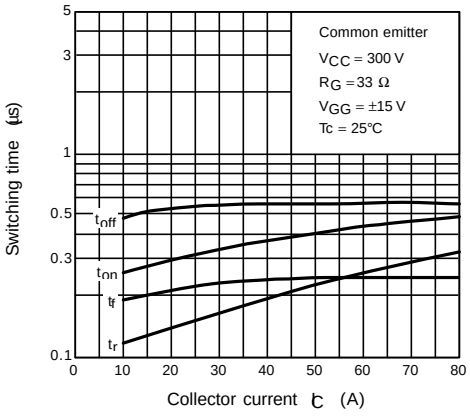
V_{CE}, V_{GE} – Q_G



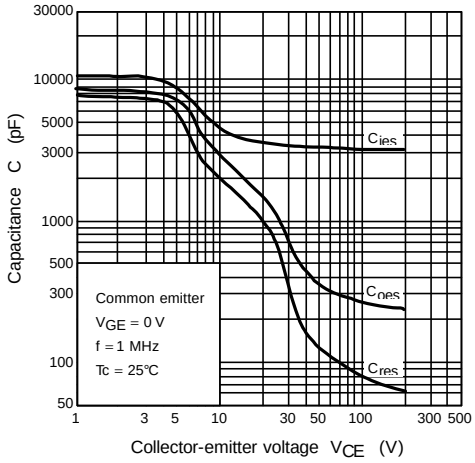
Switching time – R_G



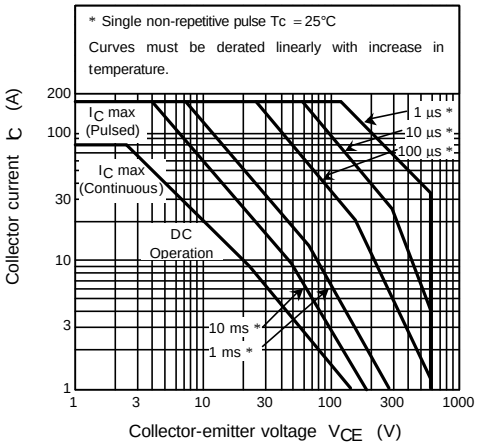
Switching time – I_C



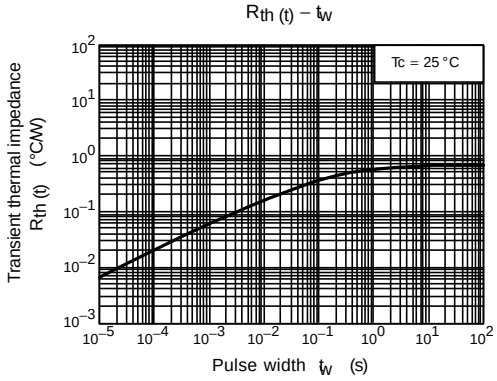
C – V_{CE}



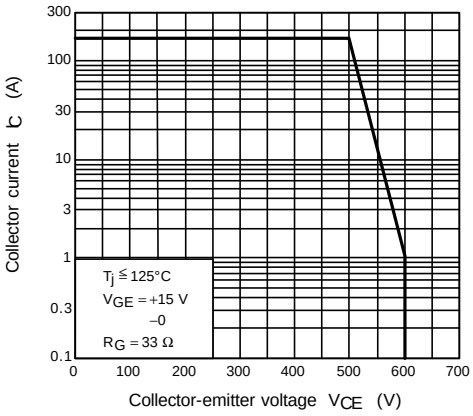
Safe Operating Area



$R_{th\ (t)}$ – t_w



Reverse Bias SOA



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