APPLICATION NOTE

GTV4000
2Fh TV receiver with TDA9321H and TDA933xH

AN98079

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Abstract

An application of the TDA9321H (High performance Input Processor) and TDA933xH (High performance Output Processor) a double line frequency TV receiver is described.

To convert the video signal to the double line frequency a BESIC module IPQ-MK8 or IPQ-MK9 module is used.

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Summary

In a 100Hz (2Fh) TV receiver the incoming signal is a normal 50Hz (1Fh) video signal. This signal is converted to the double frequency in the feature box. The outgoing signals of the feature box are on double the line frequency and also the line deflection is running on 2fh.

The TDA9321H contains the following functions: Sound IF, Vison IF and Demodulation, PAL / SECAM / NTSC colour decoding, Sync processing, Source switching and RGB to YUV matrix.

All out going signals are converted into YUV signals which are fed to the feature box. This box converts the YUV signals to YUV signals with the double line frequency and double field frequency or single field frequency in case of progressive scan mode.

The output YUV signals from the feature box are fed to the TDA933xH. The TDA933xH contains the YUV to RGB conversion, the RGB processing and deflection processing of the set. The output signals from the TDA933xH drive the RGB output stages, vertical deflection and horizontal deflection. It is also possible to feed to the TDA9332H a VGA signal from an external source (PC).

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1. Introduction

The purpose of this 2Fh demonstration TV receiver is to show the functionality of the TDA9321H, TDA933xH and an IPQ module in a more or less realistic 100Hz environment and not just an assembly of separate test boards. Second priority was to show PIP with the SAB9077 and picture improvement with the TDA9178. It would have been nice if sound could also have been implemented. In such a receiver also more or less realistic EMC tests can be done.The first two goals have been met. PIP shows with embedded software only minimum functionality, but the TV set is made in such a way that with the aid of a PC the rest of the PIP functions can be tested.

The TV set is hardware prepared for sound but due to other priorities not been tested. Also the sound software is not yet implemented. This demonstration TV does absolutely not pretend to be a production ready model but only to be a demonstration of a more or less realistic functionality. A lot of work still has to be done and every TV setmaker will have its own wishes which functions are or are not to be implemented.

In a 2Fh TV receiver the incoming signal is a normal (1Fh) video signal. This signal is converted to the double line frequency in the feature box. The outgoing signals of the feature box are on double the line frequency and also the line deflection is running on 2Fh.

The TDA9321H is the input processor: it contains the following functions: sound IF, vison IF and demodulation, PAL / SECAM / NTSC colour decoding, Sync processing, Source switching and RGB to YUV matrix.

All out going signals are converted into YUV signals which are fed to the feature box. This box converts the YUV signals to YUV signals with the double line frequency and double field frequency or single field frequency in case of progressive scan mode.

The output YUV signals from the feature box are fed to the output processor TDA933xH. The TDA933xH contains the YUV to RGB conversion, the RGB processing and deflection processing of the TV set. The output signals from the TDA933xH drive the RGB output stages, vertical deflection and horizontal deflection.
Types of output processors are:
TDA9330H TV only; no VGA mode. DAC output (pin 25) I^2C bus controlled.
TDA9332H TV and VGA mode. DAC output (pin 25) I^2C bus controlled in both modes.

2. Block diagram HIP TDA9321H

The block diagram is given in fig 1.

The input processor TDA9321H contains 2 IF circuits, one for the sound part and one for the vision part.

The sound IF signal is obtained from the tuner via 2 SAW filters which are switched for the different systems. The output of the sound circuit is a QSS IF signal for the FM systems and an audio signal for the AM sytems. The output signals are combined on one pin.

The vision IF signal is obtained from the tuner via a switchable double nyquist edge type SAW filter. The nyquist edge on 38.9MHz is used for all systems exept SECAM L'. The bandwidth of the SAW filter can be switched for M/N systems and BG systems. The BG position is also used for DK/I/L. The theoretical bandwidth loss is accepted in this set. The nyquist edge on 33.9MHz is only used for SECAM L'.

After demodulation the internal CVBS signal is fed to the sound traps to remove the sound carrier from the CVBS signal; the sound traps are switchable for the different systems. The CVBS signal is now fed to the group delay circuit which allows the user to adjust the group delay for the B/G system, so a SAW filter with a flat group delay can be used. The signal is fed into the TDA9321H as internal CVBS.

There are 2 more CVBS inputs CVBS1 and CVBS2. Furthermore there are 2 Y/C inputs, Y3/C3 and Y4/C4; these Y3 and Y4 can also be used as CVBS3 and CVBS4 inputs. The internal switches allow independant

switching of the output signals CVBS (to Comb filter), CVBS TXT and CVBS PIP to any of the incoming CVBS signals. In case of Y/C input Y and C are added at the CVBS-TXT and PIP output.

From the CVBS to the comb filter SAA4961 the Y and C signal are separated and fed to the multi standard colour decoder. When the comb filter is not used the CVBS signals or external Y/C signals are directly connected to the colour decoder. The colour decoder outputs are YUV signals which are fed to the picture improvement IC's and to the feature box.

The TDA9321H has also 2 RGB and fast blanking inputs; the RGB inputs are also converted to YUV signals and can be switched to the YUV outputs via the fastblanking inputs BL1 and BL2.

The TDA9321H delivers horizontal sync. pulse HA, vertical sync. pulse VA and a sandcastle pulse; these signals are used for the picture improvement IC's and in the feature box.

3. Block diagram HOP TDA933xH.

The block diagram is given in fig 2.

The 2Fh YUV signals from the feature box (via picture improvement IC's) are fed to the YUV inputs of the TDA933xH; the 2Fh line sync pulse HD and the 1Fv or 2Fv vertical sync pulse VD are also obtained from the feature box and fed to the TDA933xH for syncronisation.

The RGB3 input can be used as VGA input (from PC); in this case the H and V sync pulses from the VGA signal source are connected to the H and V sync inputs of the TDA9331/2H via the external switches.

The RGB4 and BL4 is used to insert the OSD from the micro controller in the RGB output signals and also for TXT.

Other input signals are:

LPSU, Low Power Start-Up: when this pin is connected to a supply voltage the horizontal output will deliver drive pulses to start the horizontal deflection circuit.

Flash, Flash detection: When the picture tube gets a flash over the horizontal drive pulses can be stopped.

DHcomp; Dynamic horizontal phase compensation.

EHT: Beamcurrent information from horizontal deflection to compensate for EHT variations.

BCL: Beamcurrent information from horizontal deflection to limit the maximum beamcurrent.

HFB: Horizontal flyback voltage input used for synchronisation and sand castle generation.

The incoming YUV signals are converted in to RGB signals to drive the RGB amplifiers. The RGB amplifiers deliver the information for the dark current stabilisation circuit. All adjustments for the picture tube can be done via the I^2C bus; such as white point, maximum drive level, gain etc.

The TDA933xH delivers the following output pulses:

Vertical drive to drive the vertical deflection amplifier.

Sandcastle output pulse; this pulse is required for some of the picture improvement IC's. The sandcastle pulse is combined with the vertical guard pulse. The guard circuit detect if something is not correct in the vertical deflection and in that case the picture is blanked.

Horizontal drive to drive the horizontal deflection circuit.

EW drive to drive the EW output amplifier which drive the diode modulator in the horizontal deflection circuit.

All geometry corrections required for the picture tube can be done via the I^2C bus for vertical as well as for horizontal direction.

Note: Two critical components connected to the TDA933xH are R196 on pin 16 (Iref) and C174 on pin 15 (Vsaw) these components must be low tolerance 2% and low must have a low temperature coefficient.

4. Block diagram of total TV receiver (vision part).

The block diagram is given in fig 3.

In the total receiver concept the incoming antenna signal is fed to an active splitter. The output signals are fed to the main tuner and to the sub tuner on the PIP module.

The sound IF signal from the main tuner is fed to the sound IF input via 2 SAW filters which are switched for the different systems. The output of the sound circuit is a QSS IF signal for the FM systems and an audio signal for the AM sytems. The output signals SIF out and AM out are combined on one pin and fed to the sound section of the receiver.

The vision IF signal from the main tuner is fed to a switchable double nyquist edge SAW filter. The nyquist edge on 38.9MHz is used for all systems exept SECAM L' .The band width of the SAW filter can be switched for M/N sysems and BG systems. The BG position is also used for DK/I/L. For system DK/I/L the bandwidth is limited to the bandwidth for BG this loss in bandwidth is accepted in this set. The nyquist edge on 33.9MHz is only used for SECAM L'.

After demodulation the internal CVBS signal is fed to the sound traps to remove the sound carrier from the CVBS signal; the sound traps are swichable for the different systems. The CVBS signal is now fed to the group delay circuit which allows the user to adjust the group delay for the B/G system so a SAW filters with flat delay can be used. The signal is fed into the TDA9321H as internal CVBS.

Other input signals for the TDA9321H are:

From SCART1: video signal CVBS1, status signal AV1, R1-G1-B1 and fast blanking signal BL1.

From SCART2: video signal CVBS2, status signal AV2, R2-G2-B2 and fast blanking signal BL2.

SVHS1 input: Y3 and C3 or via CINCH connector CVBS3.

SVHS2 input: Y4 and C4 or via CINCH connector CVBS4.

The internal switches allow switching of the output signals CVBS (to Comb filter), CVBS TXT and CVBS PIP to any of the incoming CVBS signals. In this receiver the CVBS (to Comb filter) is also fed to the text decoder (CVBS TXT). Therefore the text decoder will always display the text from the displayed picture. The CVBS TXT output of the TDA9321H is fed to the SCART 2 connector. CVBS - SCART 1 out is always the internal CVBS. The CVBS PIP output is fed to the PIP module.

From the CVBS to the comb filter SAA4961 the Y and C signal are separated and fed to the multi standard colour decoder. When the comb filter is not used the CVBS signals or external Y/C signals are directly connected to the colour decoder. The colour decoder outputs are YUV signals which are fed to the 1Fh feature connectors.

The 2 RGB inputs from SCART 1 and 2 are also converted to YUV signals and can be switched to the YUV outputs via the fastblanking inputs BL1 and BL2.

In the 1Fh feature connectors all kind of picture improvements and PIP modules can be plugged in, which work on 1Fh line frequency. In this receiver the PIP module is inserted in this connectors. The output YUV signals from the 1Fh connectors are fed to the Feature box

The TDA9321H delivers Horizontal sync. pulse HA, vertical sync. pulse VA and a sandcastle pulse. These signals are used for the picture improvement IC's and in the feature box.

In the feature box IPQ-MK8 or IPQ-MK9 the frequency of the incoming YUV is converted to 2 times the line frequency 2Fh. The line sync pulse HD is also converted to 2Fh; the vertical sync pulse VD is converted to 2Fv for 100Hz/120Hz mode and in the progressive scan mode the vertical sync pulse VD is on 1Fv.

The 2Fh YUV signals from the feature box are fed to the YUV inputs of the 2Fh feature connectors. In this receiver the TDA9178 is used to incorporate the picture improvements of this IC.

The 2Fh line sync pulse HD and the 1Fv or 2Fv vertical sync pulse VD as well as the 2Fh sandcastle pulse are also fed to the 2Fh feature connectors.The 2Fh YUV output signals from the 2Fh feature connectors are fed to the TDA933xH. For synchronisation the HD and VD sync pulses from the feature box are fed to the TDA933xH via external switches.

The RGB3 input can be used as VGA input (from PC), In this case the H and V sync pulses from the VGA signal source are connected to the H and V sync inputs of the TDA9331/2H via the external switches. In non VGA mode the HD and VD sync signals are connected to the H and V sync inputs of the TDA933xH via the external switches.

The RGB4 and BL4 is used to insert the OSD from the micro controller in the RGB output signals and is also used for TXT insertion.

The input signals: Low power start-up, Flash detection and Dynamic horizontal phase compensation are not used in this setup.

EHT, Beamcurrent information from horizontal deflection to compensate for EHT variations.

BCL, Beamcurrent information from horizontal deflection to limit the maximum beamcurrent.

HFB, Horizontal flyback voltage input used for synchronisation and sand castle generation.

The incoming 2Fh YUV signals are converted in to RGB signals to drive the RGB amplifiers. The RGB amplifiers deliver the information for the dark current stabilisation circuit. All adustments for the picture tube can be done via the I^2C bus such as white point, maximum drive level, gain etc.

The TDA933xH delivers the following output pulses:

Vertical drive to drive the vertical deflection amplifier.

Sandcastle output pulse; this pulse is required for some of the picture improvement IC's. The sandcastle pulse is combined with the vertical guard pulse which detect if something is not correct in the vertical deflection and in that case the picture is blancked.

Horizontal drive to drive the horizontal deflection circuit.

EW drive to drive the EW output amplifier which drives the diode modulator in the horizontal deflection circuit.

All geometry corrections required for the picture tube can be done via the I^2C bus for vertical as well as for horizontal direction.

5. IPQ-MK8 and IPQ-MK9 modules.

The feature box converts the normal 1Fh video signal (YUV) into a video signal (YUV) with double the line frequency. The MK8 module is the simple and cost-effective solution; the IPQ-MK9 module is the feature box with more features build in.

In the feature box the analog YUV input signals are converted to digital signals by an analog to digital converter. Then the digital signal is converted to the double line frequency. For this conversion field memories are used. With the use of the field memory also some picture improvements can be realised. After the conversion the digital signals are converted back to analog by a D/A converter and on the output the 2Fh analog YUV signals are available, which are fed to the TDA933xH.

5.1 IPQ-MK8 module.

The block diagram of the IPQ-MK8 module is shown in fig 4.

The MK8 module is a scan converter based on the video processing IC SAA4977 and one 2M9 field memory. The A/D and D/A converters are incorporated in the SAA4977.

Features of the MK8 module:

- Scan conversion from 50/60Hz to 100/120Hz A-A-B-B mode (field repetition)
- Still picture.
- Horizontal compression.
- Digital colour transient improvement.
- Luminance peaking.

When the MK8 module is equipped with the SAA4990 and a second field memory (see fig 5) the following extra features are possible:

- Scan conversion with line flicker reduction (LFR) in A-A*-B*-B mode.
- Progressive scan.
- Frame repetition mode for movie sources.
- Advanced still picture (A-A*-A-A*).
- Noise reduction.

For more detailed information on the BESIC MK8 module see Ref1 report AN98043.

5.2 IPQ-MK9 module.

Block diagram of the IPQ MK9 module is shown in fig 6.

This module is the high end scan converter: it contains more display possibilities compared to the MK8 module.

The extra display modes are:

- Motion-vector compensated line flicker reduction.
- Motion-vector compensated field rate upconversion.
- Motion -vector compensated film processing (conversion from 25 to 50 movement phases).
- Variable vertical zoom.

For more detailed information on the IPQ-MK9 module see Ref2 report AN98041.

6. Functional description total receiver.

The total circuit diagram of the small signal part is given in figs 7a, b, c, d.

6.1 Tuner and SAW filter switching.

Tuner and SAW filter circuit diagram is shown in fig 7a.

The tuner TN2 has the type number UV1316AS. It is a PLL tuner which is controlled via the I^2C bus pins 4 and 5. The supply voltage pin 7 is 5V and the tuning voltage pin 9 is 33V. This tuning voltage is obtained from the not stabilised 45V via a resistive divider. The AGC control pin 1 of the tuner is obtained from pin 62 of the TDA9321H; the control range is 4V to 0.3V.

The IF output signal pin 11 is fed to a buffer TR3; this buffer is required because the capacitance of the connected SAW filters is to high to be driven by the tuner output directly.

For the sound part 2 SAW filters are used; FL1 and FL2.

FL1 is a switchable SAW filter OFW K9462M; if pin 2 is connected to ground and pin 1 is used as input, the filter is suitable for the M and N system. When pin 1 is grounded and pin 2 is used as input, the filter is suitable for BG,I, DK and L system. FL2 is a SAW filter OFW L9353M for L' system. The output pins 4 and 5 of FL1 and FL2 are connected in parallel and fed to the sound IF inputs of the TDA9321H pins 63 and 64.

The switching of the SAW filters is done with the switch out pins 19 and 22 of the TDA9321H via transistors TR4, TR5 and TR6. When switch out pin 22 is low TR6 is not conducting and TR4 and TR5 are conducting; this results in not conducting diodes D1 and D2 and FL1 does not receive input signal. D3 is conducting and FL2 receives the IF input signal from the tuner and the sound system is switched for L'.

When pin 22 is high TR6 is conducting; therefore D3 is not conducting and FL2 does not receive an input signal. In this case with switch out pin 19 SAW filter FL1 can be switched between M/N and BG,DK,I,L. When pin 19 is high TR4 is conducting and pin 2 of FL1 is connected to ground and input 1 is used. In this case the M/N system is chosen. When pin 19 is low TR4 is not conducting and TR5 is conducting; now pin 1 is grounded and pin 2 is used as input and therefore the systems BG,DK,I and L are chosen.

For the vision part only 1 switchable SAW filter FL3 (OFW K6263K) is used. When switch out pin 19 of the TDA9321H is high TR7 is conducting and pin 10 of FL3 is grounded then the filter has a bandpass for the M and N system. When pin 19 is low TR7 is not conducting now D4 is conducting and therefore pin 1 and pin 10 of FL3 are connected; in that case a filter with double nyquist edge is selected and can be used for the systems BG,DK,I, L,L'. The output pins 4 and 5 of FL3 are connected to the vision IF input pins 2 and 3 of the TDA9321H.

Switching status:

pin 19 low, pin 22 low: system L'

pin 19 high, pin 22 low: system not valid (sound is M/N and vision is L')

pin 19 low, pin 22 high: system BG, DK, I and L.

pin 19 high, pin 22 high: system M and N.

6.2 IF circuits and sound traps.

The circuit diagram of the IF circuits and sound traps are shown in fig 7a.

For the sound part the IF amplifiers and AM demodulator are build in the TDA9321H. In case of system BG, DK, I, M and,N the QSS sound signal is present on pin 5 of the TDA9321H; in case of system L and L' the AM demodulated signal is present on this pin. The signals are connected to the sound connector P31; the QSS

signal is connected to pin 5 via a high pass filter C151 and R183, the AM signal is connected to pin 6 via a low pass filter R175 and C161.

The vision IF signal is amplified in the IF amplifiers and fed to the PLL demodulater. The VCO coil is connected to pins 7 and 8 of the TDA9321H. The adjustment of the VCO frequency is done via the I^2C bus for the systems BG, DK, I, L, M, and N. The VCO is adjusted for 38.9MHz; in case of L' the VCO is adjusted for 33.9MHz.

The demodulated CVBS signal is available on pin 10 of the TDA9321H. The amplitude of the signal is reduced to 1Vpp by the resistive divider R29 (1k) and R286 (3k3). The signal is fed to 4.5MHz sound trap FL5 via emitterfollower TR10 and to the double sound trap FL4 of 5.5MHz and 5.74MHz via emitterfollower TR9. Two emitterfollowers are used to avoid influence of the 4.5MHz trap on the 4.4MHz chroma frequencies in the BG, DK, I, L and L' CVBS signals. On the output of the sound traps a switch is present; when switch out pin 19 of TDA9321H is high TR11 is switched on and TR8 is switched off. The CVBS signal will pass through the 4.5MHz trap and the sound carrier for system M and N will be removed. When pin 19 is low the TR8 is switched on and TR11is switched off in this case 5.5MHz and 5.74MHz will be removed from the CVBS signal; this is suitable for system BG. For the systems I, DK, L and L' no traps are required; the sound carriers are already sufficient suppressed in the SAW filters used. From the switch the signal is fed to the group delay input pin 12 of the TDA9321H which allows the user to adjust the group delay for the B/G system, so a SAW filters with flat delay can be used. The group delay out signal on pin13 is fed into the TDA9321H as internal CVBS on pin 14 and to SCART connector 1 (p14) pin19 via an output amplifier T12 and T13.

6.3 Video input and output signals.

See fig 7a and 7b.

The TDA9321H can switch between 5 input signals, the selected one is displayed on the screen:

- CVBS int in pin 14 is CVBS from the front end part.
- CVBS1 in pin 16 is CVBS input signal from SCART 1 connector p14 pin 20.
- CVBS2 in pin 18 is CVBS input signal from SCART 2 connector p15 pin 20.
- CVBS3 in pin 20 is CVBS input signal from CINCH p44-1.
- Y3 in pin 20 is connected to Y input of the SVHS connector p16 in parallel to CVBS3.
- Chroma 3 in pin 21 is connected to C input of the SVHS connector p 16.
- CVBS4 in pin 23 is CVBS input signal from CINCH p44-2.
- Y4 in pin 23 is connected to Y input of the SVHS connector p17 in parallel to CVBS4.
- Chroma 4 in pin 24 is connected to C input of the SVHS connector p 17.

SCART 1 connector (p14)

pin

1 Sound out Right from Sound connector p37 pin 9

2 Sound in Right to Sound connector p37 pin 7.

3 Sound out Left from Sound connector p37 pin 8.

4 Ground.

5 Ground.

6 Sound in Left to Sound connector p37 pin 6.

7 Blue 1 in from TDA9321H pin 38.

8 AV1 in (status signal) to TDA9321H pin 15.

9 Ground.

10 N.C.

11 Green 1 in to TDA9321H pin 37.

12 N.C.

13 Ground.

14 Ground.

15 Red 1 in to TDA9321H pin 38.

16 Fast blanking 1 in to TDA9321H pin 39.

17 Ground.

18 Ground.

19 Internal CVBS out.

20 CVBS 1 in to TDA9321H pin 16.

21 Ground.

SCART 2 connector (p15)

pin

1 Sound out Right from Sound connector p22 pin 6

2 Sound in Right to Sound connector p22 pin 9.

3 Sound out Left from Sound connector p22 pin 7.

4 Ground.

5 Ground.

6 Sound in Left to Sound connector p22 pin 10.

7 Blue 2 in to TDA9321H pin 43.

8 AV 2 in (status signal) to TDA9321H pin 17.

9 Ground.

10 N.C.

11 Green 2 in to TDA9321H pin 42.

12 N.C.

13 Ground.

14 Ground.

15 Red 2 in to TDA9321H pin 41.

16 Fast blanking 2 in to TDA9321H pin 40.

17 Ground.

18 Ground.

19 Selected CVBS out (CVBS TXT) from TDA9320 pin 34 via buffer TR1.

20 CVBS 2 in to TDA9321H pin 18.

21 Ground.

SVHS (Y3/C3) connector p16.

pin:

1 Ground.

2 Ground.

3 Y3 input to TDA9321H pin 20. The signal is connected in parallel to CINCH p44-1 CVBS3 input.

4 C3 input to TDA9321H pin 21.

SVHS (Y4/C4) connector p17.

pin:

1 Ground.

2 Ground.

3 Y4 input to TDA9321H pin 23. The signal is connected in parallel to CINCH p44-2 CVBS4 input.

4 C4 input to TDA9321H pin 24.

CINCH input connector p44-1

Yellow connector: CVBS3 input

White connector: Left sound 3 input

Red connector: Right sound 3 input

CINCH input connector p44-2

Yellow connector: CVBS4 input

White connector: Left sound 4 input

Red connector: Right sound 4 input

CINCH input connector p44-3

Yellow connector: Not used

White connector: Left sound input VGA

Red connector: Right sound input VGA

VGA input connector p24

pin:

1 Red input VGA to TDA933xH pin 30

2 Green input VGA to TDA933xH pin 31

3 Blue input VGA to TDA933xH pin 32

4 N.C.

5 Ground

6 Ground

7Ground

8 Ground

9 N.C.

10 Ground

11 N.C.

12 N.C.

13 Horizontal sync. VGA to IC5 pin 1

14 Vertical sync. VGA to IC5 pin4

15 N.C.

On all in and out going pins of all connectors spark gaps and low pass filters are connected. The sparkgap limits the voltage on the pins in case of an electric static discharge (ESD) the series resistors of the low pass filters limits the currents which can flow into the IC's on an ESD. The low pass filter reduce the incoming high frequency signals picked up by the connected wires in case of an high electromagnetic field (EMC).

The internal switches allow switching of the output signals CVBS Comb filter out (TDA9321H pin 25), CVBS TXT (TDA9321H pin 34) and CVBS PIP out (TDA9321H pin 32) to any of the incoming CVBS signals. In this receiver the CVBS Comb filter out is also fed to the Text decoder. Therefore the text decoder will always display the text from the displayed picture. The CVBS TXT output is fed to the SCART 2 connector. CVBS - SCART 1 out is always connected to the internal CVBS. The CVBS PIP out is fed to the PIP module.

6.4 Colour decoder and comb filter.

Colour decoder and comb filter circuits are shown in figs 7a and 7b.

The selected CVBS on CVBS Comb filter out (TDA9321H pin 26) is fed to the comb filter IC 1 SAA4961 input pin 17. The comb filter is automatically switched to the correct standard by the system switch lines from the TDA9321H system 1 (pin 25) and system 2 (pin 27). The comb filter needs also a subcarrier signal which is present on TDA9321H pin 30. In the comb filter the Y and chroma signal are separated and fed back to the TDA9321H; Y on pin 28 and chroma on pin 29. The Y and chroma signals are fed to the Multi standard colour decoder. When the comb filter is not used the CVBS signals or external Y/C signals are directly connected to the colour decoder. The colour decoder outputs are YUV signals which are available on the TDA9321H; Y out on pin 49, U out on pin 50 and V out on pin 51.The YUV signals are fed to the 1Fh feature connectors. To the colour decoder 4 X tals can be connected for the different colour standards.

Pin 54 X1 = 4.433169MHz for system PAL/SECAM BG, DK, I, L and L'.

Pin 55 X2 = 3.582056MHz for system PAL N.

Pin 56 X3 = 3.575611MHz for system PAL M.

Pin 57 X4 = 3.579545MHz for system NTSC M.

When not all systems are used, the corresponding Xtal can be left out and the TDA9321H has to be programmed via the I^2C bus which Xtals are used.

The 2 RGB inputs from SCART 1 and 2 are also converted to YUV signals and can be switched to the YUV outputs via the fastblanking inputs BL1 and BL2.

RGB2 has priority over RGB1.

6.5 50Hz feature connectors.

The 50Hz feature connectors (see fig 7a) can be used to insert into the YUV path a picture improvement module or Picture In Picture (PIP) module. In this receiver only the PIP module is inserted in the 50Hz feature connectors. In the not used connectors the YUV input and output signals have to be interconnected because the feature connectors are connected in series for the YUV signals. This is done with a contra connector with interconnections. There are 2 pairs of connectors p2, p5 and p3, p6 the in and output signals are:

Connectors p2 and p3:

pin

1. V out
2. U out
3. Ground
4. U in
5. V in
6. Ground.
7. Sandcastle in, from TDA9321H pin 59
8. SDA, I^2C bus
9. SCL, I^2C bus
10. +8V supply voltage
11. Y out
12. Y in

Connectors p5 and p6:

pin

1, 2. N.C.

3. +45V_vert, Tuning voltage for the tuner on the PIP module
4. FBpip, Fast blanking from the PIP module
5. VA, Vertical sync pulse from TDA9321H pin 61
6. HA, Horizontal sync pulse from TDA9321H pin 60
7. +5V supply voltage

8, 9, 10. N.C.

11. Ground

12. CVBS pip in, from TDA9321H pin 32

The output signals Y, U, V, HA, VA and FBpip from the 50Hz connectors are fed to the feature box connectors via lowpass filters of 100 ohm and 27 pF. These filters are used to remove high frequency components in the YUV signals which can be generated in the digitizing part of the PIP module; the filters are also used to reduce the feedback from high frequency signals from the digitizing part of the feature box to the YUV, sync and fast blanking signals to the PIP module.

6.6 Feature box.

The feature box (1Fh to 2Fh convertor) is plugged into 5 connectors of 7 pins (see fig 7a). In this connectors different feature boxes can be connected dependant on the functions and features required for the receiver. In this receiver demo software is made for BESIC IPQ MK8 module and the feature box with more possibilities IPQ MK9.

In and out going signals are:

Connector p1:

pin

1. Ground

2. V out, to 100Hz features connector p11 pin 5

3. Ground

4. U out, to 100Hz features connector p11 pin 4

5. Ground

6. Y out, to 100Hz features connector p11 pin 12

7. Ground

Connector p4:

pin

1. Ground

2. Y in, from 50Hz features connector p2 pin 11

3. Ground

4. U in, from 50Hz features connector p2 pin 2

5. Ground

6. V in, from 50Hz features connector p2 pin 1

7. Ground

Connector p7:

pin

1. Ground
2. N.C.
3. Ground
4. N.C.
5. HA Horizontal sync from TDA9321H pin 60
6. VA Vertical sync from TDA9321H pin61
7. FBpip Fastblanking from 50Hz feature connectors (pin 4 of p5 and p6).

Connector p8:

pin

1. +5V supply voltage
2. +5V supply voltage
3. Ground
4. +8V supply voltage
5. Ground
6. +8V supply voltage
7. Ground

Connector p9:

pin

1. N.C.
2. Ground
3. HD, Horizontal sync pulse to the 100Hz feature connectors and text module.
4. VD, Vertical sync pulse to the 100Hz feature connectors and text module.

Via switches IC7 HD and VD are also fed to the HOP and micro controller (OSD).

5. Ground
6. SCL, I^2C bus
7. SDA, I^2C bus

6.7 100Hz feature connectors.

In the 100Hz feature connectors (see fig 7a) one feature board is used the picture improvement IC TDA9178. The connections from the connectors are exactly the same as in the 50Hz (1Fh) feature connectors, all incoming and outgoing signals are now 100Hz (2Fh).

6.8 Teletext.

The main board of the set is provided with two connectors p18 and p23 (see fig 7a) in which a teletext module can be plugged. In this set no teletext module is used.

In and out going signals from the TXT board.

Connector p18:

pin

1.CVBS_in, CVBS signal from the displayed picture (CVBS comb filter out TDA9321H pin 26 via buffer)

2. Ground

3. Rtxt, Red signal from teletext to RGB switch IC9

4. Gtxt, Green signal from teletext to RGB switch IC9

5. Btxt, Blue signal from teletext to RGB switch IC9

6. FBtxt, Fast blanking signal from teletext to RGB switch IC9

7, 8. N.C.

9. +5V supply

10. Ground

11. SCL, I^2C bus

12. SDA, I^2C bus

Connector p23:

pin

1. +12V supply

2. Ground

3. N.C.

4. Ground

5. N.C.

6. Ground

7. Ground

8. N.C.

9. Ground

10. HD, Horizontal sync from feature box connector p9 pin 3

11. VD, Vertical sync from feature box connector p9 pin 4

12. N.C.

6.9 VGA mode.

The external signals from VGA sources (PC's) can be connected to the VGA connector p24 (see fig 7c) . The RGB signals are connected to the TDA9331/2H directly and the horizontal and vertical sync pulses are connected to IC5. The sync pulses can have a positive or negative polarity. In IC5 the polarity of the incoming sync is transformed to positive sync pulses independent on the polarity of the incoming sync pulses. Then the sync pulses are fed to the TDA933xH and micro controller via the sync switches IC7.

The sync pulses from IC5 are also fed to IC4; with this IC is checked if both sync pulses are present; when no sync pulses are present the output signal is low. This output signal is fed to the micro controller IC15 pin7 (VGA_Ident). In monitor applications it is common to switch the set into stand by when for a certain time no sync pulses are present. In this set the sync is switched to TV sync and the message "No picture" is displayed.

The horizontal sync pulse of IC5 is also fed to IC3; in this IC the repetition time of the incoming sync pulse is compared to an adjusted time (adjustable with R130). When the incoming sync frequency is higher than the adjusted frequency, the output signal on pin 9 of IC3 is high. The signal is fed to the micro controller IC15 pin 8. Because the deflection circuit in this TV receiver is designed for 32KHz the micro controller switches to the TV sync pulses and displays "VGA error" on the screen. This function is build in to protect the deflection output stage to (mall)function on too high line frequencies.

note: If the outputs of IC3 and IC4 are used to switch to stand by, then IC3, IC4 and IC5 should be supplied from the +5V_standby!

6.10 Micro controller and N.V. memory.

The micro controller used is IC15 type number P87C766 (see fig 7c).

The micro controller is a 64K programmable micro filled with demo software.

The Non Volatile memory IC13 type number PCF85116-3 has a capacity of 2K*8 (2048*8).

In the micro controller use is made of 3 different I^2C buses.

I^2C is used for all I^2C bus devices except volatile memory IC13, TDA933xH IC11and PIP controller.

I^2C-1 is used to control the non volatile memory IC13 and the TDA933xH IC11 to avoid problem with the other IC's because in stand-by mode and during start-up only these two IC's are connected to the stand-by supply voltage.

I^2C-2 is used to initialize the PIP controller during start-up, this bus is free during normal operation and than the PIP controller can be controlled with an external PC..

Functions of the micro controller pins:

pin:

1, 2, 3. Not used.

4. Sound mute: a high level on this pin is used to mute the sound output amplifiers.

5. Prot_Mode, Protection mode is active when the pin is high (J5 open). In this situation the set will be switched off (stand-by mode) when one of the protections is activated e.g. overvoltage, flash etc. When J5 is closed the protections are switched off except for the VGA protection.

6. VGA_Select, this signal drives the sync switch IC7; when the signal is high the H and V sync signals from the VGA source are connected to the sync inputs of the TDA933xH and micro controller.

7. VGA_ident, the signal from the sync detector IC4 is connected to this pin; when no sync pulses are present the signal level is low and than the set can be switched to stand by. This feature is not incorporated in this software. In the demo set “Blue back” is switched on and the message “no picture” is displayed. The sync’s are then switched to the IPQ module (or TV mode).

8. VGA_Prot, when the incoming sync signal has a too high frequency for the deflection circuit used, the signal from the maximum frequency detector IC3 is high and the set is switched to the TV mode to protect the deflection circuit running on a too high frequency which could cause damage of the deflection circuit. Blue back is switched on with the message “VGA Error”.

9, 10, 11, 12. Not used.

13. On_Noff, when the signal is low the set is switched into stand-by mode. The signal is fed to the local key board via p42 pin 5. Via transistor TR21 the signal is inverted and fed to the large signal PCB via connector p41 pin 5.

14. SCL2, clock line of I^2C bus 2.

15. SDA2, data line of I^2C bus 2. The I^2C bus 2 is only used to control the PIP module.

16, 17, 18, 19. Keyb0 to Keyb3, scanning lines of the local key board.

20. LedN, LED drive on the local key board via connector p42 pin 8. When the signal is low the LED is on.

21. Ground.

22. OSD_B, Blue OSD output.

23. OSD_G, Green OSD output.

24. OSD_R, Red OSD output.

The OSD drive levels are reduced to 0.7V by resistive dividers; the signals are fed to the RGB 2 inputs of the TDA933xH via the OSD/TXT switch IC9.

25. OSD_FBL, Fast blanking signal from the OSD. The signal is fed to the fast blanking input of the OSD/TXT switch IC9 pin 14 and control input pin 5.

26. OSD_Hsync, Horizontal sync for OSD signal.

27. OSD_Vsync, Vertical sync for OSD signal.

The OSD sync signals come from IPQ or VGA via the sync switch IC7.

28. AVcc, Analog supply voltage +Vmicro (+5V). The voltage is obtained from the +5V stand-by. The voltage is extra filtered with L13, C197 and C198 to become a clean supply voltage for the analog part of the micro controller.

29. Ground.

30. Not used.

31. XTALIN, oscillator input.

32. XTALOUT, oscillator output.

The oscillator uses a 12MHz Xtal between the pins 31 and 32.

33. RESET, on this pin an external reset circuit is added; as long as the supply voltage (+5Vstb) is below about 4.3V (3.6V of Z3 + BE voltage of TR17) TR17 is not conducting and therefore TR18 is conducting and pin 33 is connected to the supply voltage. This is the reset condition of the micro controller.

When the supply voltage rises over the 4.3V the TR17 starts conducting and TR18 stops conducting and the voltage on pin 33 will decrease with the time constant of C181, R234 and the internal resistance of pin 33, after some time the reset condition will be released and the micro starts working.

The voltage of pin 33 is also used to switch the supply voltage of the non volatile memory IC13; as long as the voltage on pin 33 is higher than 0.7V (Vbe of TR22) TR22 will conduct and the supply voltage of IC13 will be zero, when the voltage on pin 33 becomes lower than 0.7V the micro controller is working correctly and than the supply voltage for the non volatile memory IC13 is switched on.

34. Not used.

35. Service\WP, when this pin is connected to ground the micro controller is set in the factory mode. In this mode all settings of the set can be done and the settings can be stored into the non volatile memory via the I^2C bus. When the set is in the factory mode the micro controller is set in the slave mode and therefore an external controller (PC) can control the set. When the pin is connected to ground for more than 250mS and released again the micro is set into the service mode. In this mode all adjustments of the service menu can be changed and stored in the non volatile memory with the remote control hand set or the local key board.

The content of the non volatile memory can only be changed when the service line is low; in the factory mode it is always low, therefore it is always possible to write in the memory. In the service mode the micro controller will make the service pin low during write operations.

36. SCL1, clock line of I^2C bus 1.

37. RC5N, RC5 code input from the remote control receiver.

38. SDA1, data line of I^2C bus 1.

I^2C bus 1 is used to control the non volatile memory IC13 and the TDA933xH IC11.

39. SCL, clock line of I^2C bus.

40. SDA, data line of I^2C bus.

This I^2C bus controls all other I^2C bus controlled IC's present in the set.

41. Not used.

42. Vcc, supply voltage +Vmicro is obtained from +5Vstb via filter components C160, L9 and C159.

6.11 RGB and sync switches.

The RGB signals from the TXT board and the RGB from OSD are switched in the external switch IC9 TDA8601 (see fig 7c). The RGB signals from TXT are connected to pins 2, 3 and 4 via coupling capacitors. The RGB signals from OSD are connected to pins 6, 7 and 8 also via coupling capacitors. The output RGB signals from pins 12, 11 and 10 are connected to TDA933xH pins 35, 36 and 37. On pin 16 a clamping pulse is connected; for this purpose the sandcastle pulse of the TDA933xH is used. When the fast blanking from OSD is high (pin 5 and 14) the OSD is displayed on the screen independant on the level of the fast blanking of the TXT signal. When the fast blanking of OSD (pin 15) is low and the fast blanking of TXT is high the TXT is displayed on the screen.

The sync pulses from the feature box (HD pin2 and VD pin5) and from the VGA input (H pin3 and V pin6) are switched in sync switch IC7. The output pulses are present on Hsync pin4 and Vsync pin7. These sync pulses are fed to the micro controller and to the sync input of the TDA933xH. Pin1 of IC7 is connected to VGA_Select pin6 of the micro controller. When this pin is high the sync pulses from the VGA source are switched to the output and when this pin is low the sync signals of the feature box are present on the output.

6.12 Vertical deflection.

In the lay-out of the receiver 2 different vertical deflection output amplifiers can be used (see fig 7d); IC12 the TDA8351 and IC10 the TDA8354. In the present receiver the TDA8351 is used; for later versions the successor TDA8354 will be used.

Circuit with TDA8351:

In the circuit diagram all components for both IC are drawn; in case the TDA8351 is used the following components can be left out:

R177, R186, R227, C177, C193 and C194.

R215 and R222 are zero ohm.

R203 = 33 ohm.

Pin:

1. Positive drive input from TDA933xH pin 2.

2. Negative drive input from TDA933xH pin 1.

The vertical drive currents from the TDA933xH are converted to a differential input voltage by R223 and fed to the input pins 1 and 2.

3. Supply voltage +16V (scan).

4. Output B (scan part of output voltage).

5. Ground.

6. Supply voltage +45V (flyback).

7. Output A (scan + flyback voltage).

8. Guard, this pin is connected to the sandcastle pulse and blanks the picture when there is a malfunctioning of the vertical deflection stage.

9. Feedback voltage input.

The output current of pin 4 flows through R181 and R182 (parallel) and the deflection coil to the output A pin 7. Across R181 and R182 a voltage is present which depend on the value of R181 and R182 and the deflection current flowing; this voltage is connected to pin 9 and is internally used as a feed back voltage.

Drive current Idr * R223 = The deflection current Id * R181//R182

voltage across R223 = the voltage across R181//R182, Vdrive = Vfeedback.

Circuit with TDA8354:

In case the TDA8354 is used the following components can be left out:

R188, R223, C173, C176 and C183.

R203 = 1 ohm.

Pin:

1. Guard, this pin is connected to the sandcastle pulse and blanks the picture when there is a mall functioning of the vertical deflection stage

2. Vm, input measuring resistor, feedback voltage.

3. Vcon, input conversion resistor.

The conversion of the input drive current to a drive voltage is realized with R186.

4. Supply voltage +16V (scan). With this IC a 12V supply could be used.

5. Output B (scan part of output voltage).

6. Ground.

7. Supply voltage +45V (flyback).

8. Ground.

9. Output A (scan + flyback voltage).

10. Supply voltage +16V (scan). With this IC a 12V supply could be used.

11. Negative drive input from TDA933xH pin 1.

12. Positive drive input from TDA933xH pin 2.

In this IC the drive currents are directly fed into the inputs of the amplifier; there is no conversion from current to voltage on the input pins.

13. Icomp, input for damping resistor compensation current.

For loop stability R180 (330 ohm) is connected in parallel to the vertical deflection coil. During the flyback the current in R180 is much higher than during scan. This results in a too low scan current at the begin of scan. To compensate for this error an extra feedback is made via R227 to pin13.

The output current of pin 5 flows through R181 and R182 (parallel) and the deflection coil to the output A pin 9. Across R181 and R182 a voltage is present which depend on the value of R181 and R182 and the deflection current flowing, this voltage is connected to pin 2 and is internally used as a feed back voltage.

2 * drive current Idr * R186 = deflection current Id * R181//R182.

6.13 Horizontal drive and EW drive.

The horizontal drive pulses are obtained from the TDA933xH pin 8 (see fig 7d). The output stage is an open drain. For that reason a pull up resistor is required on this pin. When a pull up resistor is present on the large signal board, jumper j8 can be open. The drive pulse is fed to the large signal part via connector p40 pin 8.

The EW drive from the TDA933xH pin 3 is fed to EW amplifier TR23 and R249. The output voltage on the drain of TR23 is given by EW drive current * R249. The output voltage is connected to the large signal board via p40 pin 3.

6.14 Sound connectors.

In the sound connectors on the main board the sound boards can be connected (see fig 7d). Depending on the system solution the sound board is equipped with stereo, dolby surround etc.

The main board has 4 sound connectors.

Connector p31:

pin

1, 2, 3, 7, 8, 11, and 12 are not connected.

4. +5V supply voltage.

5. QSS signal from frontend.

6. AM sound signal from frontend.

9. +8V supply voltage.

10. Ground.

Connector p37:

pin

1. Lmain, Left output signal to output amplifier.

2. Rmain, Right output signal to output amplifier.

3. SurrSub, Surround output signal to output amplifier.

4. Center, Center output signal to output amplifier.

5. Ground.

6. Lin, Left channel input from SCART 1 connector p14.

7. Rin, Right channel input from SCART 1 connector p14.

8. Lout, Left channel output to SCART 1 connector p14.

9. Rout, Right channel output to SCART 1 connector p14.

10. Ground.

11. SCL, Clock line of I^2C bus.

12. SCA, Data line of I^2C bus.

Sound-Top connector p22.

This connector is one to one connected to a top connector on the sound board.

pin

1, 2, 4 and 5 are not connected.

3. Ground.

6. Rout Av2, Right channel output to SCART 2 connector p15.

7. LoutAv2, Left channel output to SCART 2 connector p15.

8. Ground.

9. RinAv2, Right channel input from SCART 2 connector p15.

10. LinAv2, Left channel input from SCART 2 connector p15.

11. RinAv3, Right channel input from sound switches.

12. LinAv3, Left channel input from sound switches.

Connector p26.

This connector is used to select sound source of the sound switches. The connector is one to one connected to a connector on the sound board.

pin

1. Ground.

2. LED1.

3. LED2.

4, 5 and 6 not connected.

6.15 Sound switches.

The sound switching (see fig 7d) for the input signals frontend, AV1 and AV2 is done on the sound boards used. When the video signal of AV3 (Y/C3), AV4 (Y/C4) or AV5 (VGA) is selected, on the sound board input AV3 is selected and the switching is done with the external switch IC6. The output signals from the external switch is connected to the Av3 input of the sound connectors p22 pins 11 and 12. With the signals from the sound board LED1 and LED2 the different sources are selected.

LED1 Low, LED2 Low; PIP sound is selected.

LED1 Low, LED2 High; AV5 (VGA) sound is selected.

LED1 High, LED2 Low; AV4 (Y/C4) sound is selected.

LED1 High, LED2 High; AV3 (Y/C3) sound is selected.

All input signals are AC coupled to the switch and the DC of the inputs is set to 2.5V with divider R150 and R163. The sound signals from AV5 (VGA) have to be amplified by a factor of 3 because the VGA sound is only 150mV.

6.16 Sound output amplifiers.

In the set 4 sound output amplifiers are used (see fig 7d), The 4 amplifiers are build up with 2 stereo amplifier IC's TDA2616Q IC8 and IC14. The supply voltage +Vsnd = +29V is obtained from the large signal board via connector p41 pin 9. The used speakers have an impedance of 8 ohm and the output power per channel is 12W d=0.5%. The drive signals are obtained from the sound boards via the sound connector p37 pins 1 to 4. The amplifiers for the right and left channel are situated in IC8; the phase of the right channel is inverted with TR16. In this way it is possible to create a signal to drive the subwoofer speaker between the outputs of the right and left channel without using a separate amplifier for this speaker. The phase of the right channel is corrected again at the speaker connector. When surround sound is used, the surround and centre speakers are driven by the output amplifiers of IC14.

During switch on and switch off the output amplifiers are muted by the mute signal from the micro controller. To mute the output amplifiers a current of 300 micro Amps has to be drawn from pin 2 of IC8 and IC14; this is realized with TR24.

7. Software description

The software used in the set is made just for demo purposes, it is not finished.

The software supports the following IC's:

TDA9321H

TDA933xH

Tuner UV1316

NV memory PCF85116-3

TDA9178

Feature box; IPQ MK8 or IPQ MK9.

The PIP module is initialized during start up, only few controls can be done. The controls which are incorporated are PIP on/off, 4 PIP positions on the screen and source switching program 1 and AV 1 to AV4 in a carrousel. During normal operation the I^2C bus 2 is free to access with an external PC to control all functions on the PIP IC.

The demo software does not support the sound part of the receiver yet.

7.1 Start up procedure.

At switch on all devices are initialized via the I^2C bus with the values which are stored in the non volatile memory. When the IPQ module does not give an acknowledge the set will switch to the stand-by condition. When the PIP module or the picture improvement module with TDA9178 does not give an acknowledge, the software will exclude these modules and the menus will not show the functions of these modules.

On the PIP module the tuner is tuned to program 1 of the main tuner. After this action I^2C bus 2 is not driven any more by the micro controller and all functions of the PIP IC can be controlled with an external PC.

At start up only the stand-by voltages +5Vstb for micro and NV memory and +8Vstb for TDA933xH are present. The micro starts up when the stand-by pin 13 of the micro gets high and the power supply starts to operate; on the same time the micro sends the data from the NV memory to the TDA933xH. The TDA933xH will deliver line drive pulses. The supply voltage for the line is available and now the line deflection parts starts operating. All supply voltages for all devices are now available and the micro will initialize all I^2C bus devices and send the data from the NV memory to each device; the set is in normal operation condition.

7.2 Short description of the software functions

The software is menu driven. The menus can be selected by pressing the **menu** button. In a menu an item can be selected with the **up** and **down** keys and the value or setting can be changed with the **left** and **right** keys.

When we push the menu button the items for controlling the SOUND part are displayed, such as:

Volume, Balance, AVL, Loudness and Preset.

In this version of the demo software these functions are not working.

By pushing the menu button again the PICTURE menu is displayed. With this the normal display controls can be controlled such as:

Brightness, Contrast, Colour, Sharpness, Hue and Preset.

By pushing the menu button again the IMPROVE PICTURE menu is displayed: in this menu the picture improvement settings can be set such as:

White pnt, Skin tone, Blue str, Green enh, VDC, CDS, CTI, Demo and Preset.

By pushing the menu button again the 2Fh menu is displayed: in this menu the settings of the feature box can be set such as:

For MK8 the 2Fh mode can be: AABB, LFR and P.scan; Functions: DNR, DNR demo and Freeze.

For MK9 the 2Fh mode can be: AABB, LFR, P.scan and MOTION; Functions: DNR, DNR demo and Freeze.

By pushing the menu button again the PICTURE SIZE menu is displayed. In this menu the picture size can be set such as:

Format: 16:9, 14:9, Centre, Left, Right, Expand and Exp.+lift.

By pushing the menu button again the OTHERS menu is displayed. In this menu other settings can be set such as:

Perm. OSD, Clock, Switch at, Switch to, Sleeptimer and Lock.

When the menu button is pressed for more than 2 seconds the INSTALLATION menu will appear. The following items can be controlled:

Programme, System, Sound, Frequency, AFC, Store and Auto store.

When the menu button is pressed the PROGRAMME EDIT menu will appear. In this menu can be controlled:

Program, Move to, Name, Hide and Lock.

When the menu button is pressed the SET UP menu will appear. In this menu can be controlled:

Lock code, Tuning, Language, Mute, Power on, AV1, AV2-out and Max volume.

A menu can always be left by pressing the “TV” key.

7.3 Service menu.

To reach the service menu the **service** button on the local key board has to be pressed for more than 250mS. On the screen there will appear one line of text or two lines of text depending on the item selected.

When there is one line of text, first an abbreviation of 3 or 4 characters will be present followed by a value and than the range in which the value can be set.

When there are two lines of text, the first line displays an abbreviation of 3 or 4 characters followed by an indication (high, low, inside, outside etc.).

On the second line an abbreviation of 3 or 4 characters will be present followed by a value and than the range in which the value can be set. In this case it always influences the results on the first line.

Only the menu items which have relation to the display picture on the screen will be displayed. For instance when a 50Hz (100Hz) PAL picture is displayed on the screen the settings for 60Hz (120Hz), SECAM, NTSC, VGA etc. will not be displayed and can not be changed.

An item can be selected with the **up** and **down** keys and the value or setting can be changed with the **left** and **right** keys. To leave the service menu “TV” mode has to be pressed.

When the service menu is active, with the following RCkeys we can go to particular part of the service settings.

key:

0. Main IF-PLL adjustment, Main AGC take over, Main Y delays and Main Y gain.

1: Sub IF-PLL adjustment, Sub AGC take over, Sub Y delay and Sub Y gain. Sub = devices on PIP board.

2. PIP adjustments.

3. TDA9178 adjustments.

4. TDA933X (HOP) adjustments.

5. 50Hz adustments.

6. 60Hz adjustments.

7. VGA settings.

8. OSD position, Teletext position and Option bytes.

9. Initialisation to default values. **Do not use this function. All programmed settings will be lost.**

Red. TDA933xH White point R.

Green. TDA933xH White point G.

Blue. TDA933xH White point B.

TV. Exit service mode (Not in Menu Carrousel).

7.4 Abbreviations used in the service menu.

Special conditions are present for the following items:

5IV1, 5OV1, 5VW1, 5VZ1, 6IV1, 6OV1, 6VW1 and 6VZ1. Used if SFM mode not active or 4:3 to 16:9 format and horizontal compress formats when SFM mode is active.

5IV2, 5OV2, 5VW2, 5VZ2, 6IV2, 6OV2, 6VW2 and 6VZ2. Used with 4:3 to 16:9 format when SFM mode active.

5IV3, 5OV3, 5VW3, 5VZ3, 6IV3, 6OV3, 6VW3 and 6VZ3. Used with expand format when SFM mode active.

5IV4, 5OV4, 5VW4, 6IV4, 6OV4 and 6VW4. Used with expand +lift when SFM mode active.

Abbreviation:

5EWC. 50Hz E-W Corner parabola.

5EWE. 50Hz E-W EHT Compensation.

5EWP. 50Hz E-W Parabola width.

5EWT. 50Hz E-W Trapezium.

5EWW. 50Hz E-W Width.

5HP. 50Hz Parallelogram.

5HS. 50Hz Horizontal shift.

5IH1. 50Hz IPQ Horizontal write delay.

5IV1 50Hz IPQ Vertical write delay1.

5IV2. 50Hz IPQ Vertical write delay 2.

5IV3. 50Hz IPQ Vertical write delay 3.

5IV4. 50Hz IPQ Vertical write delay 4.

5OV1. 50Hz OSD position 1.

5OV2. 50Hz OSD position 2.

5OV3. 50Hz OSD position 3.

5OV4. 50Hz OSD position 4.

5SC. 50Hz Vertical S correction.

5VA. 50Hz Vertical amplitude.

5VC. 50Hz Vertical scroll.

5VS. 50Hz Vertical shift.

5VSL. 50Hz Vertical slope.

5VW1. 50Hz Vertical wait 1.

5VW2. 50Hz Vertical wait 2.

5VW3. 50Hz Vertical wait 3.

5VW4. 50Hz Vertical wait 4.

5VZ1. 50Hz Vertical zoom 1.

5VZ2. 50Hz Vertical zoom 2.

5VZ3. 50Hz Vertical zoom 3.

6EWC. 60Hz E-W Corner parabola.

6EWE. 60Hz E-W EHT Compensation.

6EWP. 60Hz E-W Parabola width.

6EWT. 60Hz E-W Trapezium.

6EWW. 60Hz E-W Width.

6HP. 60Hz Parallelogram.

6HS. 60Hz Horizontal shift.

6IH1. 60Hz IPQ Horizontal write delay.

6IV1 60Hz IPQ Vertical write delay1.

6IV2. 60Hz IPQ Vertical write delay 2.

6IV3. 60Hz IPQ Vertical write delay 3.

6IV4. 60Hz IPQ Vertical write delay 4.

6OV1. 60Hz OSD position 1.

6OV2. 60Hz OSD position 2.

6OV3. 60Hz OSD position 3.

6OV4. 60Hz OSD position 4.

6SC. 60Hz Vertical S correction.

6VA. 60Hz Vertical amplitude.

6VC. 60Hz Vertical scroll.

6VS. 60Hz Vertical shift.

6VSL. 60Hz Vertical slope.

6VW1. 60Hz Vertical wait 1.

6VW2. 60Hz Vertical wait 2.

6VW3. 60Hz Vertical wait 3.

6VW4. 60Hz Vertical wait 4.

6VZ1. 60Hz Vertical zoom 1.

6VZ2. 60Hz Vertical zoom 2.

6VZ3. 60Hz Vertical zoom 3.

HCDL. HOP (TDA933xH) Cathode drive level.

HPWL. HOP (TDA933xH) Peak white limiting.

HSCL. HOP (TDA933xH) Soft clipping level peak white limiter.

HWPB. HOP (TDA933xH) White point B.

HWPG. HOP (TDA933xH) White point G.

HWPR. HOP (TDA933xH) White point R.

INIT. Initialisation to default values. **Do <u>not</u> use this function. All programmed settings will be lost.**

MAG. Main AGC take over point.

MIF. Main IF-PLL adjustment for non SECAM-L'.

MIF1. Main IF-PLL adjustment for SECAM-L'.

MYFN. Main Y delay front end NTSC.

MYFP. Main Y delay front end PAL.

MYFS. Main Y delay front end SECAM.

MYG. Main Y gain.

OH. OSD Horizontal position.

OP1. Option byte 1.

OP_PAL_BG	Bit 0	1=PAL-BG allowed	0=PAL-BG not allowed
OP_PAL_DK	Bit 1	1=PAL-DK allowed	0=PAL-DK not allowed
OP_PAL_I	Bit 2	1=PAL-I allowed	0=PAL-I not allowed
OP_PAL_M	Bit 3	1=PAL-M allowed	0=PAL-M not allowed
OP_PAL_N	Bit 4	1=PAL-N allowed	0=PAL-N not allowed
OP_NTSC_M	Bit 5	1=NTSC-M allowed	0=NTSC-M not allowed
OP_NTSC_443	Bit 6	1=NTSC-443 allowed	0=NTSC-443 not allowed
OP_SECAM_BG	Bit 7	1=SECAM-BG allowed	0=SECAM-BG not allowed

OP2. Option byte 2.

OP_SECAM_DK	Bit 0	1=SECAM-DK allowed	0=SECAM-DK not allowed
OP_FRANCE	Bit 1	1=SECAM-L/L' allowed	0=SECAM-L/L' not allowed
OP_TN_THREE_BANDS	Bit 2	1=VHF-L, VHF-H, UHF	0=UHF
OP_COMBFILTER	Bit 3	1=Use comb filter	0=Do not use comb filter
OP_DL_PHASE	Bit 4	1=0.5H delay in second field	0=0.5H delay in first field
RESERVED	Bit 5		
RESERVED	Bit 6		
RESERVED	Bit 7		

OP3. Option byte 3.

OP_CURSOR_KEYS	Bit 0	1=Separate cursor keys	0=P+/- and Vol+/-cursor key
OP_PROZONIC	Bit 1	1=PROZONIC present	
OP_MELZONIC	Bit 2	1=MELZONIC present	
OP_VOLBAR	Bit 3	1=Volume bar outside menu	0=no volume bar outside
OP_EXTERN_LS	Bit 4	1=External speakers	0=No external speakers
RESERVED	Bit 5		
OP_PRESETS	Bit 6	1=Five audio/video presets	0=One audio/video present
OP_LOCK	Bit 7	1=Parental lock	0=No parental lock

OP4. Option byte 4.

RESERVED	Bit 0	
OP_AV!_RGB	Bit 1	1=Allow RGB from AV1 when in FE mode
RESERVED	Bit 2	
RESERVED	Bit 3	
RESERVED	Bit 4	
RESERVED	Bit 5	
RESERVED	Bit 6	
RESERVED	Bit 7	

OP5. Option byte 5.

OP_CLOCK	Bit 0	1=Software RTC	0=No RTC hence no switch timer
OP_24_HRS_CLOCK	Bit 1	1=24 hrs clock	0=12 hrs clock (AM/PM)
RESERVED	Bit 2		
RESERVED	Bit 3		

OP_NTSC_MATRIX	Bit 4	1=USA matrix	0=Japanese matrix
RESERVED	Bit 5		
OP_TRAP	Bit 6	1=non M/N	0=M/N trap setting during search
OP_TUNER	Bit 7	1=UV1316 present	0=UV1336 present

PFBD. PIP Fast blanking delay.

PHAM. PIP Horizontal acquisition position main.

PHAS PIP Horizontal acquisition position Sub.

PHB. PIP Horizontal background position.

PUP. PIP U pedestal.

PVAM. PIP Vertical acquisition position main.

PVAS. PIP Vertical acquisition position sub.

PVB. PIP Vertical background position.

PVP. PIP V pedestal.

SAG. Sub AGC take over point.

SIF. Sub IF-PLL adjustment for non SECAM-L'.

SIF1. Sub IF-PLL adjustment for SECAM-L'.

SYFN. Sub Y delay front end NTSC.

SYFP. Sub Y delay front end PAL.

SYFS. Sub Y delay front end SECAM.

SYG. Sub Y gain.

TABS. TDA9178 Adaptive black stretch level.

TBSG. TDA9178 Blue stretch gain.

TBSS. TDA9178 Blue stretch size.

TDSA. TDA9178 Dynamic skin tone angle.

TDSS. TDA9178 Dynamic skin tone size.

TDSW. TDA9178 Dynamic skin tone width.

TGEG. TDA9178 Green enhancement gain.

TGES. TDA9178 Green enhancement size.

TGEW. TDA9178 Green enhancement width.

THPH. Teletext Horizontal position.

THPL. Teletext Horizontal position.

TLW. TDA9178 Line width.

TNLG. TDA9178 Non-linearity gain.

TS. TDA9178 Steepness.

TVG. TDA9178 Variable gamma.

TVP. Teletext Vertical position.

TYD. TDA9178 Y delay.

VEWC. VGA E-W Corner parabola.

VEWE. VGA E-W EHT Compensation.

VEWP. VGA E-W Parabola width.

VEWT. VGA E-W Trapezium.

VEWW. VGA E-W Width.

VHP. VGA Parallelogram.

VHS. VGA Horizontal shift.

VOV. VGA Vertical position if ident.

VOVN. VGA Vertical position if no ident.

VSC. VGA Vertical S correction.

VVA. VGA Vertical amplitude.

VVC. VGA Vertical scroll

VVS. VGA Vertical shift.

VVW. VGA Vertical wait.

VVZ. VGA Vertical zoom.

YAV. Y delay AV.

8. Adjustments.

8.1 Main IF PLL adjustment.

The IF PLL has to be adjusted to the vision IF frequency used. In this receiver SAW filters are used for an IF frequency of 38.9MHz for all systems exept SECAM L'. For SECAM L' the IF frequency is 33.9MHz.
The adjustment can be done in two different ways:

1. Feed a video modulated IF signal (38.9MHz) to the tuner IF output. The amplitude must be between 100mV and 1V pp. No signal should be connected to the antenna input of the tuner.
In the service menu the value of the MIF function can be changed till the indication shows AFC: inside high or inside low. Now the IF PLL is adjusted correctly.

For the adjustment of SECAM L' the IF frequency must be 33.9Mz. In the tuning menu the system must be set to FRANCE. In the service menu the value of the MIF1 function can be changed till the indication shows AFC: inside high or inside low. Now the IF PLL is adjusted correctly also for SECAM L'.

2. A second method is to feed an antenna signal to the tuner, tune in the tuning menu to this signal and store this setting. When the service menu is switched on the AFC from the main tuner and the PIP tuner is switched off. Go to the service menu and change the value of the MIF function till the indication shows AFC: inside high or inside low. Now the IF PLL is adjusted correctly. When the service menu is switched off the AFC will be set back to the position it was before the service menu was switched on.

For the adjustment of SECAM L' a SECAM L' signal has to be fed to the antenna input and, tune in the tuning menu to this signal. Set system to FRANCE and store these setting. Go to the service menu and change the value of the MIF1 function till the indication shows AFC: inside high or inside low. Now the IF PLL is adjusted correctly also for SECAM L'.

8.2 PIP IF PLL adjustment.

The adjustments for the PIP IF PLL can be done in the same way as described for the main IF PLL. In the service menu the function SIF is used for 38.9MHz adjustment and SIF1 is used for the SECAM L' (33.9MHz) adjustment.
At switch on the settings of the PIP module are copied from the main settings of program 1 in the tuning menu. For that reason all settings in the tuning menu have to be done on program 1 and the set must be switched off and on again to copy the settings to the PIP module: now the adjustment can be done as described for the main IF PLL.

8.3 Tuner AGC take over adjustment.

In a TV set the IF gain is controlled with 2 loops: one in the IF amplifier and one in the tuner. At low input levels the IF gain is controlling and the tuner gain is at its maximum. When the IF input voltage on the SAW filter is about 1Vpp the IF AGC stops regulating and the tuner gain takes over. The point that the tuner AGC starts working has to be adjusted with function Main AGC take over MAG in the service menu.

For the adjustment an antenna signal of 10mV to100mV is fed to the tuner: in the tuning menu the tuner is tuned to the signal. By varying function MAG in the service menu the IF voltage on the tuner output can be adjusted to 1Vpp: the adjustment is ready.

The PIP AGC take over point can be adjusted by feeding an antenna signal of 10mV to100mV to the tuner: in the tuning menu the tuner is tuned to the signal on program 1 when the set is switched off and on again. By varying function SAG in the service menu the IF voltage on the PIP tuner output can be adjusted to 1Vpp: the adjustment is ready.

8.4 Geometry.

To adjust the geometry of the picture a certain procedure has to be followed:

1. In the service mode functions 5VZ1 and 6VZ1 have to be set to value 19. The functions 5VC and 6VC have to be set to value 1F.

2. Vertical slope, in this mode the middle of the vertical deflection (zero deflection current) is adjusted to the middle of the video signal. The picture is blanked for have the scan by changing function 5VSL (for a 50Hz picture) and 6VSL (for a 60 Hz picture) the middle line of the video can be adjusted to the point that the blanking start in the middle of the screen.

3. Adjust now for Vertical amplitude 5VA and 6VA, Vertical shift 5VS and 6VS, Vertical S correction 5SC and 6SC.

4. Now the horizontal geometry can be adjusted. Horizontal width 5EWW and 6EWW, Horizontal shift 5HS and 6HS, Parabola 5EWP and 6EWP, Corner parabola 5EWC and 66EWC, Trapezium 5EWT and 6EWT, Horizontal parabola 5HP and 6HP.

When after the horizontal geometry adjustments changes are made in the vertical adjustments the horizontal geometry adjustments have to be repeated.

5. For VGA the same procedure has to be followed except for the slope function (not functional for VGA).

8.5 VGA maximum frequency.

To protect the horizontal deflection circuit a frequency detector is built-in for the VGA mode. When the incomming VGA signal has a higher frequency than the deflection can handle, the frequency detector IC3 gives a signal to the micro controller and this switches off the VGA sync pulses and the sync signals from the feature box are fed to the TDA933X: on the screen is displayed “VGA error”. The adjustment of the frequency detector can be done with R130. Feed a VGA signal into the VGA input of the maximum required frequency, turn on R130 until “VGA error” is displayed on the screen, turn back R130 a little until the VGA picture is displayed again. Now every frequency higher than the required frequency will be blocked.

9. Picture improvement TDA9178

The picture improvement IC TDA9178 has several possibilities to improve the picture (see fig 8). The board is connected into the 2Fh YUV path of the receiver. The inputs of the module are: 2Fh YUV, sandcastle and +8V. The output signals are the 2Fh improved YUV signals. The TDA9178 can be used for all TV standards.

Some of the picture improvements are:

1. Histogram function. The content of the picture is measured each frame. The signal is processed in such a way that in areas with low contrast the contrast is increased and in areas with high contrast the contrast is reduced. This results in a picture with more details even in very dark or very bright scenes. The result is that the picture gives the impression to be more sharp.

2. Variable gamma control. The variable gamma is a non linear gain control of the YUV signals. The black and the white are kept constant and the gain in between is made non linear. This allows the user to adjust for a picture which contains more brightness or less brightness without influencing the contrast of the picture. The gamma control can be seen as an improved brightness control.

3. Skin tone correction for the NTSC system. Skin tones are very sensitive for transmission (hue) errors, because we have an absolute feeling for the skin tones. To make a picture look free of hue error, the skin tones have to be on the correct colour. The circuit shifts the colour around the skin tone colour to the correct colour. The working area of the skin tone correction can be adjusted.

4. Green enhancement. The green enhancement circuit shifts low saturated green colour towards more saturated green colours. This results in a picture with trees or green grass in a picture with brighter green colours.

5. Blue stretch. The blue stretch circuit shifts colours near bright white towards more blueish colour white. A blueish white gives in a picture the impression to be brighter than normal white. The effect of this feature can very good be noticed with pictures in which the sun is shining on water or high lights on metal objects.

6. LTI. Luminance Transient Improvement.

7. Smart peaking.

8. CTI. Colour Transient Improvement.

Many more picture improvement features are present in the TDA9178; for more detailed information see Ref3 report AN97083.

In the PCB 3 resistors are added to the existing circuit; the resistors of 100K ohm are connected from pins 3, 4 and 5 to ground. In the layout Yin and Yout signals have to be separated.

10. Picture In Picture module with SAB9077.

The SAB9077 is a picture in picture controller for Multi-standard sets (see figs 9a and 9b). The circuit contains Analog to Digital Convertors, reduction circuitry, display and Digital to Analog Convertors.It inserts one or two live video signals with original or reduced sizes into a live video signal. All video signals are expected to be analog base band signals. The conversion into the digital environment and back to the analog environment is done on chip. Internal clocks are generated by two acquisition PLL's and a display PLL. The two PIP channels have a large external memory 2Mb offering a wide range of PIP modes. The emphasis is put on single PIP, double PIP, Split screen mode and many multi PIP modes.

For more detailed information see Ref4 report AN96041.

The circuit diagram of the PIP module is given in figs 9a and 9b.

The PIP module is build-up with 5 IC's:

IC1. TDA8601 output switches.

IC2. SAB9077H PIP circuit.

IC3. uPD482234 Memory, connected to the PIP circuit.

IC4. SAA4961 Comb filter.

IC5. TDA9321H high performance input processor.

The input circuit with tuner, SAW filters, comb filter and input processor are exactly the same as used in the main small signal part. The YUV output signals from IC5 and the horizontal HA and vertical VA sync pulses are fed to the sub inputs of the IC2. The YUV and the sync pulses HD and VD from the main picture are connected to the main inputs of IC2. The signals are processed in IC2 and the PIP picture is available on the output pins 86 (Y), 90 (U) and 88 (V). The output signals are fed to the video switches IC1. As long as the main picture is displayed the FBpip signal is low and the main YUV inputs (pins 2, 3, 4) of IC1 are connected with the outputs (pins 10, 11, 12) of IC1. During the time that the PIP picture is present on the outputs of IC2 (pins 6, 7, 8 of IC1) the FBpip signal is high and now the PIP picture is connected to the outputs of IC1. In this way the PIP picture is inserted in the main picture. The sandcastle pulse on pin 16 of IC 1 is used to clamp the incoming signals to a correct DC level.

On the circuit diagram there are 4 resistors marked R?; these resistors are added later on to the circuit. 3 resistors of 220 ohm on the YUV output pins 86, 88 and 90 of IC2 to terminate the outputs. One resistor of 3.3K ohm on the base of TR8 to ground to correct the video output amplitude.

On the PIP module two I^2C buses are used: SDA/SCL and SDA2/SCL2. SDA/SCL controls the tuner and IC5, SAD2/SCL2 control the PIP IC2. p1 or p2 must be connected to the main board p19; in this connection the +5V line should be removed. Only SCL2, Ground and SDA2 should be connected. (+5V stand-by and +5V would be connected and in that case the set will not start-up). In a later stage when the software is ready to control the PIP IC jumpers J1 and J2 can be closed and the PIP IC can be controlled via the normal bus and bus 2 can be removed. The other I^2C 2 connector can be used to control the PIP IC via a PC. The micro controller on the PIP-bus is only active at start-up and when a PIP command is given with the remote control.

11. Lay-out from small signal part.

The lay-out of the receivers is made as a demo set (see figs 10, 11 and 12). Use is made of plug-in modules to make it possible to demonstrate all kind of features and add on boards in an easy way. Therefore connectors are present for 2 times 1Fh features, different kind of featurebox, 2 times 2Fh features, teletext module and sound module.

The lay-out of the board is build up in such a way that the signal paths of the 1Fh and 2Fh do not interfere. The signal from the tuner goes via the SAW filters to the TDA9321H, the YUV output signals go to the 1Fh feature connectors, and than to the feature box in which the signals are converted to 2Fh. The total 1Fh signal path is located on the left hand side of the PCB.

The 2Fh YUV signals from the featurebox are flowing in the right hand side of the board. The signals go via the 2Fh feature connectors to the TDA933xH. The output RGB signals are connected to the picture tube PCB and the horizontal and EW drive pulses are fed to the deflection PCB via connector p40. The micro controller is also located on the 2Fh side of the board because the OSD is locked to the 2Fh display on the picture tube. The ground layers between the 1Fh and 2Fh parts are separated between TDA9321H (1Fh) and TDA933xH (2Fh). The grounds are connected under the featurebox.

Due to the lack of space under the picture tube the smaller components have to be located on the picture tube side of the board. The plug-in units are located in the middle of the board and the connectors for video, Y/C and sound in and out have to be located on the back side of the receiver. With this set up long tracks will be needed for video and Y/C in and outputs between SCART, Y/C connectors and TDA9321H. To avoid cross talk between the signals' the signal tracks are separated by a track which does not carry any signal. For instance the tracks can be separated like: video1 in, AV1 status signal, video2 out, ground, video2 in, +5V supply, video1 out, AV2 status signal, Y/C signal etc.

12. RGB output stages.

The RGB output stages are build-up around the video amplifier TDA6111Q (see fig 13). The small signal (60Vpp) bandwidth of the amplifiers is 16MHz, the large signal bandwidth (100Vpp) is 13MHz.

The pin functions of the TDA6111Q:

pin

1. Reference voltage (2.5V); the positive input of the differential amplifier.
2. +12V supply line.
3. Feedback pin; negative input of the differential amplifier.
4. Ground.
5. Black current output.
6. +200V supply line.
7. AC output pin.
8. DC output pin; cathode drive.
9. Feedback output pin.

The RGB input voltages from p3 are amplified by the gain which is set by the ratio of the input resistors R7,8, 9 and feedback resistors R18, 19, 20. In this application 68K/1.5K = 45. The input resistors are shunted with a capacitor of 8.2pF to increase the gain for higher frequencies to obtain a better flat frequency response. In series with the cathodes special resistors are connected to protect the amplifiers during a flash over of the picture tube.

The resistors have a low inductance and can withstand a high current for a short time. Each amplifier has his own decoupling of the +12V and +200V supply lines close to the IC's to avoid oscillations in the output stages.

The circuit around TR1 is used to suppress the beam current at switch off to avoid a bright white point on the screen which could damage the picture tube screen. On pin 1 of p4 a negative flyback voltage of 200Vpp is present. The scan part is rectified with D1 and results in a positive DC voltage of about 25V on C22, the negative part is rectified with D2 and results in a negative DC voltage of about 175V on C23. At normal operation TR1 is conducting and the collector is on about 0V. At switch off C22 is discharged fast with R34 and TR1 stops conducting. The negative voltage on C23 is not discharged because TR1 stops conducting and via R31 grid 1 of the picture tube is connected to the negative voltage and there fore no beam current can flow in the cathodes. When the beam current suppression is not used J1 has to be closed.

13. Local key board.

The local key board has only few control possibilities (see fig 14), from left to right:

(IR receiver), Program +, Program -, Control +, Control -, Source, Menu, (LED), Service and Stand-by.

By pressing the service button for longer than 250mS, the set goes into the service menu. This service button is mounted on the local key board only because this is a demo set. In a production set the button must be placed inside the cabinet only accessible for the service engineer.

When the set is in stand-by the D1 (LED-3R) is switched on.

The local key board is connected to the micro controller via p2 and the RC5 codes of the remote receiver are connected to the micro via p3. In p1 the remote receiver is connected: in this connector 2 types of remote receivers can be used.

14. Mains filter board.

The mains filter board contains the mains filter L1 and the degaussing circuit R1 (see fig 15). Connector p1 is connected to the mains voltage. p2 is connected to the mains input of the power supply and line deflection board. The degaussing coils are connected to p3. The connectors are marked p1, p2 and p3 on the circuit diagram and X1, X2 and X3 on the PCB.

15. Power supply and line deflection.

On the large signal board the SMPS and the line deflection circuit are combined. The power supply delivers all power required for the total receiver. The line deflection part is designed for 2Fh; the maximum working frequency is 35KHz.

15.1 Power supply.

In fig 16 the circuit diagram of the SMPS is shown. The circuit exists of two parts: the stand-by SMPS and the Main SMPS. The mains voltage connected to p800 is rectified by D800 to D803 and fed to the buffer elco C804

via R800 to limit the inrush current (TH800 is not conducting during start up). The rectified mains voltage +VB is used as supply voltage for the stand-by SMPS and the main SMPS.

The stand-by SMPS is a small self oscillating power supply which deliver the +5V stand-by voltages for the micro controller and error amplifier in the main SMPS. It also delivers the +8V stand-by voltage for the HOP (TDA933xH). The small SMPS is formed by the circuit around TR830 andT830. The output voltage of T830 is rectified with D830 and clamped to +8V by D831 and D832. This is possible in this way because the output of T830 acts as a kind of current source. The +8V is fed to a voltage regulator IC830 which delivers the +5V stand-by. For more detailed information on the self oscillating power supply see Ref5 report ETV/AN94015.

The main SMPS is also supplied by +VB from C804. The control of the main SMPS is done with IC800 TDA8380A.

The functions of the TDA8380A are:

pin

1. Positive drive output.
2. Supply voltage of drive output stage.
3. Demagnetization sense input.
4. Minimum Vcc threshold setting. Connected to ground in this application.
5. Supply voltage Vcc.
6. Reference current setting.
7. Feedback input.
8. Output error amplifier. Not used in this application.
9. Pulse width modulator input.
10. Oscillator capacitor.
11. Synchronisation input.
12. maximum duty factor (Dmax) setting for slow start.
13. Input current protection.
14. Ground.
15. Emitter of output sink transistor. Connected to ground.
16. Sink output.

The supply capacitor C820 of the control IC 800 is charged via R804 from +VB. The voltage on C820 increases till the starting level (17V) of IC800 is reached. The internal oscillator starts and the output drive pulses will appear. The duty cycle of the output drive pulses is increasing slowly due to the slow start function. The drive pulses drive the power transistor TR810 and the output voltages of transformer will increase till the nominal value. On the collector of TR810 damping networks are connected to limit the maximum voltage on the collector. The voltages present in the damping circuit are also used to drive thyristor TH800 which short-circuits R800. This is necessary when the power delivered by the SMPS is rising. The voltage drop on R800 would become very high and a lot off power would be waisted.

As soon as the output voltages of T800 are present, the supply voltage for the control IC800 is taken over via D817 and R817 as well as D818 and R818. An AC feedback is made from pin 10 of T800 to the demagnetization

sense input pin3 of IC800 to avoid switching on TR810 when the current in T800 is not zero. If TR810 is switched on when the current is not zero, the core can saturate and TR810 could be damaged.

The current in TR810 is measured with the series resistors R805 to R809 in parallel. The measured voltage is fed back to pin 13 of IC800; it switches off the drive for TR810 when the current in TR810 becomes too high.

The output voltages from T800 are:

+200V supply voltage for the video output amplifiers.

+150V supply voltage for the line deflection. This voltage is also used as feed back (SENSE) for the SMPS output voltages.

+29V supply voltage for the sound output stages. The ground of this supply voltage is connected to the main ground via R928 (1k ohm) to avoid disturbances from the large audio currents into the other circuits.

+16V low voltage supply.

The output voltages are stabilized by using the +150V as a sense voltage. The +150V is attenuated to about 7V with R887, R886, R884, VR880 and R885. The feedback voltage can be adjusted with VR880 and is fed to the error amplifier formed by D883 and TR880. The error amplifier current flows through an opto coupler OC880. The output of OC880 drives the pulse width modulator input pin 9 of IC800 via TR840 and with this the loop is closed be cause the duty cycle is regulated in such a way that the output voltage remains on the value adjusted with VR880.

When the set is switched to stand-by, the OFF signal from the micro controller is high and therefore TR881 is conducting. The current in the optocoupler is so high that the duty cycle of the control IC800 is zero and the output voltages of the SMPS will reduce to zero.

On the SYNC line a negative flyback voltage from the line output transformer is applied. The feedback voltage to the error amplifier is made lower during the horizontal flyback pulse and in this way the SMPS is synchronised with the line deflection.

15.2 Line deflection.

The circuit diagram of the line deflection part is given in fig 17.

The 2Fh horizontal drive pulses H-DRIVE from the TDA933xH drive the line driver. The driver circuit is build up around TR610 and T610; the supply voltage of the driver circuit is 150V. In the line driver circuit the base current for the line output transistor TR600 is generated. TR600 is the power switch of the line deflection part. The line deflection circuit is build up with line output transformer T600 and the so called diode modulator. A picture tube needs correction (EW correction) in the line deflection current to obtain a correct geometry on the screen. The diode modulator can modulate the line deflection current while the flyback voltage on the collector of TR600 still has the same amplitude. From this collector voltage the EHT is obtained via the up transformation in T600. From T600 also the Focus voltage and Vg2 are obtained. The beam current limiter information BCL is obtained from pin10 of T600. The beam current flows from +16V trough R660 to the EHT winding of T600. When the beam current rises the voltage on pin 10 will decrease and via the D660 the beam current limiter circuit in the TDA933xH the beam current will be limited.

When the beam current increases the EHT will reduce and with the same deflection current the picture will become larger. To compensate for this geometry distortion the information from the build-in EHT bleeder is used: the EHT information is available on pins 14, 15 and 16 of T600. The DC information is amplified via TR672 and the AC information is amplified via TR670. The information is combined in TR671 and fed to the EHT input of the TDA933xH. This IC drives the diode modulator via the EW drive and corrects the picture width dependant of the EHT variation.

The supply voltages for the vertical deflection +16V and +45V are also obtained from T600. By taking these voltages from the line output transformer the vertical deflection is automatically switched off when the line deflection is switched off (stand-by).

Parallel to the primary of T600 a second transformer T690 is connected. From this transformer the secondary voltages are scan rectified and deliver stabilized voltages of +12V and +5V. With a stabilizer IC690 a voltage of 8V is made. With a jumper on one of the positions J690 to J692 the output voltages can be adjusted to 3 levels and with a jumper on one of the positions J694 to J696 the output voltages can be adjusted to 3 levels and in the same time the EHT can be set to 3 levels.

The line deflection circuit contains a dynamic focus voltage circuit is build up around T611. This circuit is only used when a picture tube with DAF gun is used. A dynamic focus unit (FMP-PRT-DAF, 2322 460 91602) is connected to P602 and the focus voltage. From this unit the focus voltage(s) and Vg2 for the picture tube are obtained. Note that the upper flyback diodes D620 and D621 should be equipped with a heatsink. In practice R641 at the EW input should be deleted.

16. Interconnections.

The demo set is build up with the following PCB's (see fig 18):

Mains filter board PR33101.

Power supply and line deflection board PR32191.

Main small signal board PR31672.

Picture tube board PR30524.

Local key board PR31761.

PIP module board PR31731.

IPQ module MK8 T board H7VS04 or MK9.1 board H7VS31.

Picture improvement module with TDA9178 board PR31831.

The sound module is not used in the set because the software is not ready for this part. The module which will be used when the software is ready, is a Dolby surround sound module board PR31681.

The interconnections between the PCB's and the connections to the picture tube, degaussing coil and mains are shown in fig 18.

17. EMC

The TV set is tested on EMC behaviour in the Jacky test. The test is only done on video behaviour because the sound is not build in yet. The results are shown in fig 19. From the results can be seen that the requirements are not fulfilled completely but it is close to the limits. In a final receiver more tests and measures are required to fulfil the EMC requirements.

18. List of abbreviations

1Fh. Line frequency is 15625Hz for 50Hz systems and 15734Hz for 60Hz systems.

1Fv. 50Hz or 60Hz field frequency.

2Fh. Line frequency is 31250Hz for 50Hz (100Hz) systems and 32468 for 60Hz (120Hz) systems,

2Fv. 100Hz or 120Hz field frequency.

AC. Alternating Current.

A/D. Analog to Digital converter.

AFC. Automatic Frequency control.

AGC. Automatic Gain Control.

AM. Amplitude Modulation.

AV. Audio Video.

AVL. Automatic Volume Levelling.

BCL. Beam Current Limiter.

BL. BLanking signal.

CDS. Colour Dependant Sharpness.

CRS. Customer Requirement Specification.

CTI. Colour Transient Improvement.

CVBS. Composite Video Banking Sync.

D/A. Digital to Analog converter.

DC Direct Current.

DHcomp. Dynamic Horizontal phase compensation.

DNR. Dynamic Noise Reduction.

EEProm. Electrically Erasable Programmable Read Only Memory.

EHT. Extra High Tension.

EMC. Electro Magnetic Compatibility.

ESD. Electro Static Discharge.

EW. East West correction.

FB. Fast Blanking.

FBpip. Fast Blanking from the PIP module.

FBL. Fast BLanking.

FM. Frequency Modulation.

FRS. Functional Requirements Specification.

HA. Horizontal sync pulse Acquisition side.

HD. Horizontal sync pulse Deflection side.

HFB. Horizontal FlyBack.

HIP. High performance Input Processor.

HOP. High performance Output Processor.

HSI. Hardware Software Interface.

IC. Integrated Circuit.

I^2C bus. Inter IC bus.

IF. Intermediate Frequency.

IPQ MK8. Improved Picture Quality. (MKxx = version number)

IR. Infra Red.

L. Left sound signal.

LED. Light Emitting Diode.

LFR. Line Flicker Reduction.

LPSU. Low Power Start Up.

N.C. Not Connected.

NTSC. National Television System Committee.

NV. Non Volatile memory, EEProm.

OSD. On Screen Display.

PAL. Phase Alternating Line.

PC. Personal Computer.

PCB. Printed Circuit Board.

PIP. Picture In Picture.

PLL. Phase Locked Loop.

QSS. Quasi Split Sound.

R. Right sound signal.

RC5. Remote Control code 5.

RGB. Red Green Blue.

SAW. Surface Acoustic Wave filter.

SCL. Serial CLock of I^2C bus.

SDA. Serial DAta of I^2C bus.

SECAM. SEquencial Coleur Avec Memoire (Sequential Colour With Memory).

SIF. Sound Intermediate Frequency.

SFM. Single Field Memory mode.

SMPS. Switched Mode Power Supply.

SVGA. Super VGA.

SVHS. Super VHS.

TXT. Tele teXT.

TV. TeleVision.

U. colour difference signal -(B-Y).

V. colour difference signal -(R-Y).

VA. Vertical sync pulse Acquisition side.

VCO. Voltage Controlled Oscillator.

Vcon. Conversion resistor.

VD. Vertical sync pulse Display side.

VGA. Video Graphics Array.

VIF. Vision Intermediate Frequency.

Vm. Measuring resistor.

WP. Write Protect.

Xtal. Crystal.

Y. Luminance signal.

Y/C. Luminance / Chroma signal.

19. Appendix

19.1 Parts list of small signal board PR31672.

BOM file 31672.bom

ITEM	PART NO.	GEOMETRY	COUNT	DESCRIPTION	REFERENCE
1	210-535	VGA_BUS	1	VGA_B US_15p_sqr	P24
2	2222-037-58109	CASE_R11_m	2	CAP, 10uF, 20%	C176 C177
3	2222-037-58228	CASE_R11_m	1	CAP, 2.2uF, 20%	C47
4	2222-037-90047	CASE_R12	3	CAP, 100uF, 20%	C143 C171 C186
5	2222-122-57477	CASE_R2	1	CAP, 0.47uF, 20%	C51
6	2222-134-35109	CASE_R52_TFA	2	CAP, 10uF, 20%	C142 C185
7	2222-134-50109	CASE_R54_CA	1	CAP, 10uF, 20%	C75
8	2222-134-51108	CASE_R51_CA	1	CAP, 1uF, 20%	C28
9	2222-134-51109	CASE_R55_CA	2	CAP, 10uF, 20%	C73 C181
10	2222-134-53101	CASE_R55_CA	1	CAP, 100uF, 20%	C130
11	2222-134-55479	CASE_R55_CA	9	CAP, 47uF, 20%	C2 C32 C35 C49 C74 C91 C93 C164 C166
12	2222-136-61102	CASE_R19	4	CAP, 1000uF, 20%	C152 C162 C190 C196
13	2222-368-45104	C368_B	1	CAP, 100nF, 10%	C201
14	2222-370-11104	C370_A	4	CAP, 100nF, 10%	C14 C60 C179 C208
15	2222-370-11154	C370_B	1	CAP, 150nF, 10%	C206

16	2222-580-16632	C0805	5	CAP, 22nF, 10%	C76 C149 C158 C187 C195
17	2222-580-18712	C0805	64	CAP, 100nF, 20%	C3 C4 C5 C6 C7 C8 C9 C11 C12 C18 C20 C24 C26 C29 C34 C40 C41 C42 C44 C46 C52 C53 C54 C61 C62 C68 C92 C104 C106 C108 C109 C110 C124 C125 C126 C127 C128 C129 C131 C135 C139 C140 C144 C145 C146 C147 C150 C153 C154 C155 C159 C160 C163 C165 C167 C168 C169 C172 C174 C178 C189 C197 C198 C199
18	2222-590-16618	C0805	1	CAP, 2.2nF, 10%	C192
19	2222-590-16621	C0805	2	CAP, 3.3nF, 10%	C161 C191
20	2222-590-16627	C0805	6	CAP, 10nF, 10%	C31 C102 C120 C121 C132 C175
21	2222-629-03103	CER2_2B	1	CAP, 10nF, -20+80%	C209
22	2222-630-02472	CER1_4	1	CAP, 4.7nF, 10%	C30
23	2222-630-03332	CER2_3	1	CAP, 3.3nF, 10%	C13
24	2222-861-12101	C0805	1	CAP, 100pF, 5%	C64
25	2222-861-12102	C0805	18	CAP, 1nF, 5%	C57 C58 C65 C66 C83 C84 C85 C86 C87 C88 C89 C90 C136 C137 C157 C183 C193 C194
26	2222-861-12109	C0805	4	CAP, 10pF, 5%	C45 C50 C112 C133

27	2222-861-12189	C0805	6	CAP, 18pF, 5%	C16 C17 C23 C27 C184 C188
28	2222-861-12279	C0805	24	CAP, 27pF, 5%	C10 C21 C22 C37 C38 C39 C111 C113 C114 C115 C116 C117 C118 C122 C123 C138 C141 C148 C200 C203 C204 C205 C207 C210
29	2222-861-12331	C0805	1	CAP, 330pF, 5%	C151
30	2222-861-12479	C0805	18	CAP, 47pF, 5%	C55 C56 C59 C63 C67 C69 C70 C71 C72 C77 C78 C79 C80 C81 C82 C119 C156 C182
31	2222-921-16654	C1206	16	CAP, 220nF, 10%	C15 C94 C95 C96 C97 C98 C99 C100 C101 C105 C107 C134 C170 C173 C180 C202
32	2222-921-16655	C1206	1	CAP, 270nF, 10%	C103
33	2222-921-16656	C1206	6	CAP, 330nF, 10%	C1 C19 C25 C33 C36 C48
34	2322-180-73104	SFR16T	3	RES, 100k, 5%	R5 R212 R259
35	2322-180-73105	SFR16T	2	RES, 1M, 5%	R207 R211
36	2322-180-73108	SFR16T	2	RES, 1, 5%	R187 R203
37	2322-180-73153	SFR16T	1	RES, 15k, 5%	R10
38	2322-180-73154	SFR16T	1	RES, 150k, 5%	R270
39	2322-180-73181	SFR16T	3	RES, 180, 5%	R32 R70 R85
40	2322-180-73221	SFR16T	2	RES, 220, 5%	R110 R113
41	2322-180-73222	SFR16T	1	RES, 2.2k, 5%	R67
42	2322-180-73223	SFR16T	1	RES, 22k, 5%	R275
43	2322-180-73229	SFR16T	1	RES, 22, 5%	R188
44	2322-180-73273	SFR16T	1	RES, 27k, 5%	R271

45	2322-180-73331	SFR16T	1	RES, 330, 5%	R6
46	2322-180-73391	SFR16T	1	RES, 390, 5%	R28
47	2322-180-73684	SFR16T	1	RES, 680k, 5%	R264
48	2322-180-73759	SFR16T	1	RES, 75, 5%	R4
49	2322-180-73823	SFR16T	1	RES, 82k, 5%	R249
50	2322-186-16108	SFR25H	4	RES, 1, 5%	R172 R181 R182 R224
51	2322-186-16759	SFR25H	18	RES, 75, 5%	R40 R44 R50 R52 R59 R60 R61 R62 R88 R89 R90 R91 R92 R93 R111 R137 R138 R139
52	2322-186-16828	SFR25H	4	RES, 8.2, 5%	R174 R178 R228 R239
53	2322-194-13331	PR02	1	RES, 330, 5%	R180
54	2322-205-13108	SFR25H	1	RES, 1, 5%	R71
55	2322-482-40472	OMP10_h	1	RES, 4.7k, 20%	R130
56	2322-730-61101	R0805	72	RES, 100, 5%	R1 R2 R3 R7 R8 R12 R13 R14 R30 R33 R35 R36 R46 R47 R48 R49 R55 R58 R72 R74 R75 R76 R77 R78 R79 R82 R83 R131 R132 R133 R135 R140 R142 R143 R144 R145 R147 R149 R171 R173 R176 R179 R192 R193 R194 R199 R200 R201 R204 R205 R206 R208 R214 R215 R217 R222 R232 R233 R240 R245 R246 R247 R255

					R256 R260 R261
					R267 R268 R273
					R276 R284 R285
57	2322-730-61102	R0805	28	RES, 1k, 5%	R21 R29 R86 R87
					R95 R96 R97 R98
					R99 R100 R102 R150
					R154 R162 R163
					R169 R175 R183
					R197 R210 R229
					R236 R248 R258
					R279 R280 R281
					R282
58	2322-730-61103	R0805	19	RES, 10k, 5%	R25 R26 R27 R41
					R42 R53 R57 R120
					R134 R141 R216
					R219 R225 R226
					R238 R242 R244
					R263 R278
59	2322-730-61104	R0805	12	RES, 100k, 5%	R114 R116 R118
					R119 R121 R122
					R146 R148 R151
					R152 R156 R283
60	2322-730-61105	R0805	1	RES, 1M, 5%	R155
61	2322-730-61109	R0805	1	RES, 10, 5%	R19
62	2322-730-61123	R0805	1	RES, 12k, 5%	R54
63	2322-730-61124	R0805	1	RES, 120k, 5%	R125
64	2322-730-61152	R0805	6	RES, 1.5k, 5%	R51 R69 R73 R127
					R129 R186
65	2322-730-61153	R0805	20	RES, 15k, 5%	R94 R101 R103 R104
					R105 R106 R107
					R108 R165 R168
					R195 R209 R213
					R221 R231 R250
					R251 R252 R253
					R257

66	2322-730-61181	R0805	1	RES, 180, 5%	R84
67	2322-730-61221	R0805	1	RES, 220, 5%	R243
68	2322-730-61222	R0805	8	RES, 2.2k, 5%	R15 R16 R17 R22 R38 R157 R158 R161
69	2322-730-61223	R0805	5	RES, 22k, 5%	R126 R128 R166 R167 R266
70	2322-730-61224	R0805	1	RES, 220k, 5%	R230
71	2322-730-61272	R0805	1	RES, 2.7k, 5%	R262
72	2322-730-61273	R0805	3	RES, 27k, 5%	R112 R170 R218
73	2322-730-61302	R0805	1	RES, 3k, 5%	R223
74	2322-730-61331	R0805	7	RES, 330, 5%	R63 R64 R65 R66 R159 R164 R272
75	2322-730-61332	R0805	10	RES, 3.3k, 5%	R31 R45 R56 R136 R177 R184 R185 R198 R202 R286
76	2322-730-61333	R0805	2	RES, 33k, 5%	R80 R153
77	2322-730-61392	R0805	2	RES, 3.9k, 5%	R37 R43
78	2322-730-61393	R0805	1	RES, 39k, 5%	R234
79	2322-730-61472	R0805	2	RES, 4.7k, 5%	R115 R117
80	2322-730-61473	R0805	6	RES, 47k, 5%	R68 R123 R124R235 R241 R254
81	2322-730-61479	R0805	2	RES, 47, 5%	R11 R23
82	2322-730-61562	R0805	7	RES, 5.6k, 5%	R9 R189 R190 R191 R269 R274 R277
83	2322-730-61563	R0805	1	RES, 56k, 5%	R109
84	2322-730-61682	R0805	1	RES, 6.8k, 5%	R160
85	2322-730-61684	R0805	1	RES, 680k, 5%	R227
86	2322-730-61822	R0805	2	RES, 8.2k, 5%	R34 R39
87	2322-730-61823	R0805	1	RES, 82k, 5%	R81
88	2322-734-63903	R0805	1	RES, 39k, 1%	R196
89	2422-021-98731	JUMPER_2p	5	JUMPER_2p	J5 J6 J7 J8 J9
90	2422-024-04008	-9967	1		
91	2422-549-13266	7127	1		
92	2422-549-13272	24221	1		
93	2422-549-13654	24221	1		

94	3111-101-41211	31112	1		
95	4330-030-38081	WBC_2.5r	2	CHOKE, WBC_2.5_R	L9 L13
96	4330-030-41051	WBC_2rt	2	CHOKE, WBC_2_RT	L8 L10
97	4822-267-10094	EURO_SCART	2	EURO_SCART	P14 P15
98	9331-176-80153	SOD27	1	BZX79C	Z3
99	9331-177-50153	SOD27	1	BZX79C	Z2
100	9335-447-20112	TO92	1	BF370	TR3
101	9335-896-10215	SOT23	17	BC848	TR1 TR2 TR4 TR5
					TR6 TR7 TR8 TR9
					TR10 TR11 TR13
					TR14 TR15 TR16
					TR20 TR21 TR22
102	9335-896-30215	SOT23	1	BC848B	TR24
103	9335-897-70215	SOT23	6	BC858	TR12 TR17 TR18
					TR19 TR25 TR26
104	9336-247-30113	SOD68	1	BAT81	D9
105	9339-139-10115	SOD80C	9	BAS32L	D1 D2 D3 D4 D5 D6
					D7 D8 D10
106	9339-555-50127	SOT186	1	BUK444_200A	TR23
107	9350-554-00112	SOT131_heat._c	1	TDA8351_N1	IC12
108	9390-288-60112	28366	1		
109	9922-520-00477	HC49_u13	1	XTAL, 3.582056MHz	X2
110	9922-520-00478	HC49_u13	1	XTAL, 3.579545MHz	X4
111	9922-520-00479	HC49_u13	1	XTAL, 3.575611MHz	X3
112	9922-520-00481	HC49_u13	1	XTAL, 4.433619MHz	X1
113	9922-520-12MHz	HC49_u13	1	XTAL, 12MHz	X6
114	B39339-L9353-M100	SIP_5K	1	OFW_L9353M	FL2
115	B39389-K6263-P100	DIP_10	1	OFW_K6263	FL3
116	B39389-K9462-M100	SIP_5K	1	OFW_K9462M	FL1
117	CST12.0MTW	SFE_3p	1	CST12.0MTW	X5
118	DIL8	SOT97_s	1	PCF85116-3	IC13
119	DIL16	SOT38_s	1	HEF4052B	IC6
119a	DIL16	SOT38_s	1	HCT157	IC7
119b	DIL16	SOT38_s	1	TDA8601	IC9
120	DIL28	SOT117_s	1	SOT117	IC1

121	DIL42SHR	SOT270_s	1	SAA4961	IC15
122	DIL_SHR_42p		1	DIL_SHR_42p_SOCKET	
123	IC149-064-101-S510		1		
124	IEC149-044-152-S510		1		
125	K177-AC-81912		1		
126	LAL02NA100K	uChoke_2e	2	CHOKE, 10uH, 10%	L6 L7
127	LAL03NA330K	uChoke_3e	6	CHOKE, 33uH, 10%	L1 L2 L3 L5 L11 L12
128	MKS3733-1-0-303	MKS3730_3p	9	MKS3730_3p	P25 P30 P32 P33 P34 P38 P39 P43 P45
129	MKS3734-1-0-404	MKS3730_4p	3	MKS3730_4p	P19 P20 P21
130	MKS3735-1-0-505	MKS3730_5p	1	MKS3730_5p	P35
131	MKS3736-1-0-606	MKS3730_6p	1	MKS3730_6p	P26
132	MKS3737-1-0-707	MKS3730_7p	5	MKS3730_7p	P1 P4 P7 P8 P9
133	MKS3738-1-0-808	MKS3730_8p	1	MKS3730_8p	P42
134	MKS3740-1-0-1010	MKS3730_10p	1	MKS3730_10p	P40
135	MKS3744-1-0-1414	MKS3730_14p	1	MKS3730_14p	P41
136	MKS4230-1-0-1212	MKS4230_12p	13	MKS4230_12p	P2 P3 P5 P6 P10 P11 P12 P13 P18 P22 P23 P31 P37
137	PN-TDA8354	SOT141_heat._c	1	TDA8354	IC10
138	QFP44S10	SOT307_EMU_ ADAPTER	1	SOT37	IC11
139	QFP64REC	SOT319_EMU_ ADAPTER	1	SOT319	IC2
140	SIL9	SOT131	2	TDA2616Q	IC8 IC14
141	SO14	SOT108	1	74HCT86D	IC5
142	SO16	SOT109	2	74HCT4538D	IC3 IC4
143	SOLD-JUMPER_2p	SOLD_JUMPER	1	SOLD_JUMPER_2p	J10
144	SPARK-GAP	SPARK_GAP	15	SPARK_GAP	F9 F10 F11 F12 F13 F14 F15 F16 F31 F32 F33 F34 F35 F36 F37
145	TOKO-5KM	TOKO_5km	1	TOKO_5km	L4

146	TPS4.5MB2	SFE_3p	1	TPS4.5MB2	FL5
147	TPW04B	SFE_3p	1	TPW04B	FL4
148	UV1316	TUNER	1	UV1316	TN2
149	YKC21-2531-9P-3-switch		1		
		14X15_RA_3L9P_TYPE_3S			P44
150	YKF51-5508		2		
		RAC_1.5_TYPE_SQUARE			P16 P17

19.2 Parts list of picture improvement module PR31831.

BOM file 31831.bom

ITEM	PART NO.	GEOMETRY	COUNT	DESCRIPTION	REFERENCE
1	2222-037-58479	CASE_R13_m	1	CAP, 47uF, 20%	C2
2	2222-580-18712	C0805	2	CAP, 100nF, 20%	C1 C3
3	2322-730-61101	R0805	2	RES, 100, 5%	R1 R2
4	2422-021-98731	JUMPER_3p	1	JUMPER_3p	J1
6	DIL24SHR	SOT234_s	1	TDA9178	IC1
7	DIL_SHR_24p_SOCKET		1	DIL_SHR_24p_SOCKET	
8	MKF1512-1-0-1212	MKF1500_12p	1	MKF1500_12p	P3
9	MKS3733-1-0-303	MKS3730_3p	1	MKS3730_3p	P1
10	MKS3734-1-0-404	MKS3730_4p	1	MKS3730_4p	P2

19.3 Parts list of PIP module PR31731.

BOM file 31732.bom

ITEM	PART NO.	GEOMETRY	COUNT	DESCRIPTION	REFERENCE
1	2222-037-58228	CASE_R11_m	1	CAP, 2.2uF, 20%	C81
2	2222-122-57477	CASE_R2	1	CAP, 0.47uF, 20%	C85
3	2222-134-50109	CASE_R54_CA	1	CAP, 10uF, 20%	C93
4	2222-134-51108	CASE_R51_CA	2	CAP, 1uF, 20%	C23 C69

5	2222-134-51109	CASE_R55_CA	1	CAP, 10uF, 20%	C91
6	2222-134-53229	CASE_R53_CA	1	CAP, 22uF, 20%	C10
7	2222-134-55109	CASE_R52_CA	6	CAP, 10uF, 20%	C5 C9 C24 C33 C47 C51
8	2222-134-55479	CASE_R55_CA	5	CAP, 47uF, 20%	C53 C73 C76 C83 C92
9	2222-370-11104	C370_A	2	CAP, 100nF, 10%	C57 C88
10	2222-580-18712	C0805	45	CAP, 100nF, 20%	C6 C7 C8 C11 C12 C16 C17 C18 C19 C20 C21 C22 C25 C26 C27 C30 C31 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C48 C49 C50 C54 C55 C61 C63 C65 C67 C70 C75 C78 C80 C87 C89
11	2222-590-16621	C0805	1	CAP, 3.3nF, 10%	C95
12	2222-590-16627	C0805	1	CAP, 10nF, 10%	C72
13	2222-590-16632	C0805	1	CAP, 22nF, 10%	C94
14	2222-590-16641	C0805	8	CAP, 100nF, 10%	C1 C13 C14 C15 C28 C29 C32 C86
15	2222-630-02472	CER1_4	1	CAP, 4.7nF, 10%	C71
16	2222-630-03332	CER2_3	1	CAP, 3.3nF, 10%	C56
17	2222-861-12109	C0805	2	CAP, 10pF, 5%	C79 C84
18	2222-861-12181	C0805	3	CAP, 180pF, 5%	C2 C3 C4
19	2222-861-12189	C0805	4	CAP, 18pF, 5%	C59 C60 C64 C68
20	2222-861-12331	C0805	1	CAP, 330pF, 5%	C90
21	2222-921-16654	C1206	1	CAP, 220nF, 10%	C58
22	2222-921-16656	C1206	6	CAP, 330nF, 10%	C52 C62 C66 C74 C77 C82
23	2322-180-73104	SFR16T	1	RES, 100k, 5%	R17
24	2322-180-73153	SFR16T	1	RES, 15k, 5%	R19
25	2322-180-73181	SFR16T	4	RES, 180, 5%	R33 R51 R60 R61

26	2322-180-73222	SFR16T	1	RES, 2.2k, 5%	R47
27	2322-180-73391	SFR16T	1	RES, 390, 5%	R30
28	2322-186-16338	SFR25H	2	RES, 3.3, 5%	R1 R14
29	2322-205-13108	SFR25H	1	RES, 1, 5%	R52
30	2322-730-61101	R0805	9	RES, 100, 5%	R4 R5 R15 R16 R42
					R46 R53 R56R57
31	2322-730-61102	R0805	3	RES, 1k, 5%	R31 R43 R55
32	2322-730-61103	R0805	12	RES, 10k, 5%	R3 R12 R13 R27 R28
					R29 R35 R36R39
					R40 R45 R50
33	2322-730-61109	R0805	1	RES, 10, 5%	R24
34	2322-730-61123	R0805	1	RES, 12k, 5%	R41
35	2322-730-61152	R0805	3	RES, 1.5k, 5%	R38 R49 R54
36	2322-730-61222	R0805	5	RES, 2.2k, 5%	R21 R22 R23 R25
					R34
37	2322-730-61332	R0805	3	RES, 3.3k, 5%	R32 R37 R44
38	2322-730-61333	R0805	1	RES, 33k, 5%	R58
39	2322-730-61473	R0805	1	RES, 47k, 5%	R48
40	2322-730-61479	R0805	2	RES, 47, 5%	R20 R26
41	2322-730-61562	R0805	1	RES, 5.6k, 5%	R18
42	2322-730-61823	R0805	1	RES, 82k, 5%	R59
43	2322-734-61008	R0805	2	RES, 1, 1%	R2 R11
44	2322-734-62209	R0805	5	RES, 22, 1%	R6 R7 R8 R9 R10
45	2422-021-98731	JUMPER_2p	3	JUMPER_2p	J1 J2 J3
46	2422-021-98731	JUMPER_3p	1	JUMPER_3p	J4
51	9335-447-20112	TO92	1	BF370	TR1
52	9335-896-10215	SOT23	8	BC848	TR2 TR3TR4 TR5
					TR6TR7 TR8TR9
53	9339-139-10115	SOD80C	5	BAS32L	D1 D2 D3 D4 D5
54	9922-520-00477	HC49_u13	1	XTAL, 3.582056MHz	X2
55	9922-520-00478	HC49_u13	1	XTAL, 3.579545MHz	X4
56	9922-520-00479	HC49_u13	1	XTAL, 3.575611MHz	X3
57	9922-520-00481	HC49_u13	1	XTAL, 4.433619MHz	X1
58	B39339-L9353-M100	SIP_5K	1	OFW_L9353M	FL2
59	B39389-K6263-P100	DIP_10	1	OFW_K6263	FL3

60	B39389-K9462-M100	SIP_5K	1	OFW_K9462M	FL1
61	DIL28	SOT117_s	1	SAA4961	IC4
62	IC149-064-101-S510		1		
63	LAL02NA100K	uChoke_2e	2	CHOKE, 10uH, 10%	L10 L11
64	LAL02NA4R7K	uChoke_2e	4	CHOKE, 4.7uH, 10%	L1 L2 L3 L4
65	LAL03NA330K	uChoke_3e	4	CHOKE, 33uH, 10%	L5 L6 L7 L9
66	MKF1512-1-0-1212	MKF1500_12p	2	MKF1500_12p	P3 P4
67	MKS3734-1-0-404	MKS3730_4p	3	MKS3730_4p	P1 P2 P5
68	NEC-uPD482234	SOJ40	1	uPD482234	IC3
69	PN-SAB9077H	SOT317	1	SAB9077H	IC2
70	PN-TDA8601	SOT38_s	1	TDA8601	IC1
71	QFP64REC	SOT319_EMU_ADAPTER			
			1	TDA9321H	IC5
72	TOKO-5KM	TOKO_5km	1	TOKO_5km	L8
73	TPS4.5MB2	SFE_3p	1	TPS4.5MB2	FL5
74	TPW04B	SFE_3p	1	TPW04B	FL4
75	UV1316	UV1316	1	TUNER	TN1

19.4 Parts list of RGB output stages board PR30524.

BOM file PR30524.bom

ITEM	PART NO.	GEOMETRY	COUNT	DESCRIPTION	REFERENCE
1	2222-037-58109	CASE_R11_m	1	CAP, 10uF, 20%	C1
2	2222-037-90047	CASE_R12	1	CAP, 100uF, 20%	C16
3	2222-042-13109	CASE_A00	1	CAP, 10uF, -10/+50%	C15
4	2222-368-45104	C368_B	3	CAP, 100nF, 10%	C9 C10 C11
5	2222-370-11104	C370_A	6	CAP, 100nF, 10%	C6 C7 C8 C19 C20 C21
6	2222-371-41104	C371_C	2	CAP, 100nF, 10%	C22 C23
7	2222-376-92912	C376_H	1	CAP, 9.1nF, 5%	C18
8	2222-630-02561	CER1_1	3	CAP, 560pF, 10%	C12 C13 C14
9	2222-638-09828	CER2_1	3	CAP, 8.2pF, 0.25pF	C2 C3 C4
10	2322-180-73102	SFR16T	1	RES, 1k, 5%	R10
11	2322-180-73109	SFR16T_3e	1	RES, 10, 5%	R26

12	2322-180-73152	SFR16T	6	RES, 1.5k, 5%	R7 R8 R9 R12 R13 R14
13	2322-180-73223	SFR16T	1	RES, 22k, 5%	R33
14	2322-180-73392	SFR16T	1	RES, 3.9k, 5%	R11
15	2322-180-73472	SFR16T	1	RES, 4.7k, 5%	R34
16	2322-180-73479	SFR16T	1	RES, 47, 5%	R22
17	2322-186-16105	SFR25H	1	RES, 1M, 5%	R31
18	2322-186-16473	SFR25H	1	RES, 47k, 5%	R32
19	2322-186-16683	SFR25H	3	RES, 68k, 5%	R18 R19 R20
20	2322-329-34688	AC04	1	RES, 6.8, 10%	R30
21	2422-021-98731	JUMPER_2p	1	JUMPER_2p	J1
22	3122-128-76273	TUBE_SOCKET	1	TUBE-SOCKET-45AX	P5
23	4022-007-45420	SOLDER_PIN	2	SOLDER-PIN_large	P1 P2
24	9332-593-60112	TO92	1	BF423	TR1
25	9337-234-10113	SOD81	2	BYD33G	D1 D2
26	9350-205-30112	SOT111	3	TDA6101Q	IC1 IC2 IC3
27	AB-EB6815	BRADLEY	5	RES, 680, 5%	R23 R24 R25 R28 R35
28	MKS3735-1-0-505	MKS3730_5p	1	MKS3730_5p	P3
29	MKS3737-1-0-707	MKS3730_7p	1	MKS3730_7p	P4

19.5 Parts list of local key board PR31761.

BOM file 31761.bom

ITEM	PART NO.	GEOMETRY	COUNT	DESCRIPTION	REFERENCE
1	05-88-1736AR	RAY_BUS	1	ARRAY_BUS_H_1x5p	P1
2	2222-030-34229	CASE_A2	1	CAP, 22uF, -10/+50%	C1
3	2322-180-73101	SFR16T_3e	1	RES, 100, 5%	R1
4	2322-180-73102	SFR16T_3e	1	RES, 1k, 5%	R4
5	2322-180-73153	SFR16T	1	RES, 15k, 5%	R3
6	2322-180-73222	SFR16T_3e	1	RES, 2.2k, 5%	R2
7	LED-3R	SOD53	1	LED, LED-3R	D1
8	MKS3733-1-0-303	MKS3730_3p	1	MKS3730_3p	P3
9	MKS3738-1-0-808	MKS3730_8p	1	MKS3730_8p	P2

10	RODELCO-4973-012M				
		INI_SWITCH-v	8	SKHHLS	S1 S2 S3 S4 S5 S6 S7, S8

19.6 Parts list of mains filter board PR33101.

BOM file 33101.bom

ITEM	PART NO.	GEOMETRY	COUNT	DESCRIPTION	REFERENCE
1	2222-378-62104	C378_C	1	CAP, 100nF, 5%	C3
2	2222-379-54334	C379_F	2	CAP, 330nF, 5%	C1 C2
3	2322-662-96116	DUAL_PTC	1	RES, DUAL_PTC_24_750_3K, 5%	R1
4	2412-086-28239	GLAS_HOLDER	1	FUSE, 2A	F1
5	3111-138-53860	AT4043_93	1	AT4043_93	L1
6	MKS3733-1-0-303	MKS3730	3	MKS3730_2p_220V	P1 P2 P3

19.7 Parts list of power supply and line deflection board PR32191.

BOM file 32191.bom

ITEM	PART NO.	GEOMETRY	COUNT	DESCRIPTION	REFERENCE
1	2222-037-51681	CASE_R18	1	CAP, 680uF, 20%	C833
2	2222-037-58109	CASE_R11_m	1	CAP, 10uF, 20%	C661
3	2222-037-58478	CASE_R11_m	1	CAP, 4.7uF, 20%	C825
4	2222-037-60221	CASE_R14	1	CAP, 220uF, 20%	C696
5	2222-037-61471	CASE_R12_m	2	CAP, 470uF, 20%	C871 C872
6	2222-037-64472	CASE_R19	2	CAP, 4700uF, 20%	C690 C691
7	2222-037-65221	CASE_R13_m	1	CAP, 220uF, 20%	C836
8	2222-037-65222	CASE_R18	1	CAP, 2200uF, 20%	C692
9	2222-037-66331	CASE_R14	1	CAP, 330uF, 20%	C820
10	2222-037-66471	CASE_R15	2	CAP, 470uF, 20%	C662 C860
11	2222-037-66479	CASE_R11_m	1	CAP, 47uF, 20%	C840
12	2222-037-90047	CASE_R12	1	CAP, 100uF, 20%	C612

13	2222-042-11101	CASE_A03	2	CAP, 100uF, -10/+50%	C852 C853
14	2222-044-62101	CASE_R20	1	CAP, 100uF, 20%	C603
15	2222-044-63479	CASE_R13	1	CAP, 47uF, 20%	C891
16	2222-057-58221	CASE_3040	1	CAP, 220uF, 20%	C804
17	2222-336-60222	C336_A	6	CAP, 2.2nF, 20%	C800 C801 C802 C803 C898 C899
18	2222-368-25474	C368_E	1	CAP, 470nF, 10%	C640 Changed to 1uF
19	2222-368-45334	C368_F	1	CAP, 330nF, 10%	C610
20	2222-368-55393	C368_D	1	CAP, 39nF, 10%	C602
21	2222-370-11104	C370_A	4	CAP, 100nF, 10%	C600 C672 C841 C842
22	2222-370-11105	C370_D	4	CAP, 1uF, 10%	C670 C671 C815 C816
23	2222-370-11224	C370_B	1	CAP, 220nF, 10%	C660
24	2222-370-11334	C370_B	4	CAP, 330nF, 10%	C694 C695 C834 C835
25	2222-370-11683	C370_A	1	CAP, 68nF, 10%	C673
26	2222-370-41333	C370_B	1	CAP, 33nF, 10%	C881
27	2222-376-72682	C376_B	1	CAP, 6.8nF, 5%	C811
28	2222-376-82153	C376_G	1	CAP, 15nF, 5%	C622
29	2222-376-92222	C376_C	1	CAP, 2.2nF, 5%	C813
30	2222-376-92272	C376_C	1	CAP, 2.7nF, 5%	C805
31	2222-376-92562	C376_F	2	CAP, 5.6nF, 5%	C620 C621
32	2222-378-64684	C378_L	1	CAP, 680nF, 5%	C630 changed to 470nF
33	2222-427-26801	C42x_A	1	CAP, 680pF, 5%	C823
34	2222-629-03102	CER2_1	1	CAP, 1nF, -20+80%	C832
35	2222-629-03103	CER2_2B	2	CAP, 10nF, -20+80%	C814 C883
36	2222-630-03471	CER2_1	2	CAP, 470pF, 10%	C861 C870
37	2222-631-10109	CER1_1	1	CAP, 10pF, 2%	C826
38	2222-631-58221	CER1_4	1	CAP, 220pF, 2%	C822
39	2222-638-34151	CER2_4	1	CAP, 150pF, 2%	C831
40	2222-650-10339	CER2_2B	2	CAP, 33pF, 2%	C829 C830
41	2222-655-03101	CER2_1	2	CAP, 100pF, 10%	C824 C882
42	2222-655-03221	CER2_1	2	CAP, 220pF, 10%	C851 C890
43	2222-655-03222	CER2_4	1	CAP, 2.2nF, 10%	C837

44	2222-655-03471	CER2_2A	2	CAP, 470pF, 10%	C611 C810
45	2222-655-03681	CER2_2B	1	CAP, 680pF, 10%	C850
46	2322-156-14322	MRS25	1	RES, 4.32k, 1%	R826
47	2322-156-17503	MRS25	1	RES, 75k, 1%	R886
48	2322-186-16101	SFR25H	1	RES, 100, 5%	R885
49	2322-186-16102	SFR25H	6	RES, 1k, 5%	R613 R801 R802 R815 R834 R928
50	2322-186-16103	SFR25H	3	RES, 10k, 5%	R819 R840 R882
51	2322-186-16104	SFR25H	2	RES, 100k, 5%	R669 R672
52	2322-186-16105	SFR25H	1	RES, 1M, 5%	R675
53	2322-186-16109	SFR25H	3	RES, 10, 5%	R601 R679 R833
54	2322-186-16122	SFR25H	1	RES, 1.2k, 5%	R841
55	2322-186-16124	SFR25H	1	RES, 120k, 5%	R824
56	2322-186-16125	SFR25H	1	RES, 1.2M, 5%	R832
57	2322-186-16152	SFR25H	2	RES, 1.5k, 5%	R881 R887
58	2322-186-16153	SFR25H	2	RES, 15k, 5%	R602 R612
59	2322-186-16154	SFR25H	1	RES, 150k, 5%	R650
60	2322-186-16181	SFR25H	1	RES, 180, 5%	R671
61	2322-186-16182	SFR25H	1	RES, 1.8k, 5%	R880
62	2322-186-16183	SFR25H	2	RES, 18k, 5%	R674 R677
63	2322-186-16221	SFR25H	1	RES, 220, 5%	R823
64	2322-186-16223	SFR25H	2	RES, 22k, 5%	R670 R825
65	2322-186-16228	SFR25H	1	RES, 2.2, 5%	R817
66	2322-186-16303	SFR25H	2	RES, 30k, 5%	R827 R888
67	2322-186-16332	SFR25H	2	RES, 3.3k, 5%	R835 R884
68	2322-186-16333	SFR25H	2	RES, 33k, 5%	R678 R883
69	2322-186-16394	SFR25H	1	RES, 390k, 5%	R681
70	2322-186-16472	SFR25H	6	RES, 4.7k, 5%	R611 R663 R673 R830 R831 R842
71	2322-186-16479	SFR25H	1	RES, 47, 5%	R814
72	2322-186-16684	SFR25H	1	RES, 680k, 5%	R676
73	2322-186-16822	SFR25H	1	RES, 8.2k, 5%	R660
74	2322-186-16824	SFR25H	1	RES, 820k, 5%	R680
75	2322-186-16828	SFR25H	1	RES, 8.2, 5%	R818
76	2322-193-90072	PR01	3	RES, 0.22, 5%	R860 R870 R890

77	2322-194-13104	PR02	1	RES, 100k, 5%	R804
78	2322-194-13109	PR02	2	RES, 10, 5%	R811 R822
79	2322-194-13223	PR02	1	RES, 22k, 5%	R851
80	2322-194-13271	PR02	1	RES, 270, 5%	R810
81	2322-194-13331	PR02	1	RES, 330, 5%	R850
82	2322-194-13339	PR02	1	RES, 33, 5%	R820
83	2322-194-13828	PR02	1	RES, 8.2, 5%	R821
84	2322-195-13128	PR03	1	RES, 1.2, 5%	R600
85	2322-195-13331	PR03	1	RES, 330, 5%	R630
86	2322-195-13339	PR03	1	RES, 33, 5%	R640
87	2322-195-13473	PR03	1	RES, 47k, 5%	R812
88	2322-205-13108	SFR25H	5	RES, 1, 5%	R805 R806 R807 R808 R809
89	2322-205-13153	SFR25H	1	RES, 15k, 5%	R828
90	2322-205-13227	SFR25H	2	RES, 0.22, 5%	R661 R662
91	2322-242-13475	VR37	1	RES, 4.7M, 5%	R899
92	2322-329-04109	AC04	1	RES, 10, 5%	R800
93	2322-329-04152	AC04	1	RES, 1.5k, 5%	R610
94	2322-329-07102	AC07	1	RES, 1k, 5%	R813
95	2322-329-07151	AC07	1	RES, 150, 5%	R641
96	2322-329-44478	AC10	1	RES, 4.7, 10%	R871
97	2322-482-40471	OMP10_h	1	RES, 470, 20%	VR880
98	2422-024-04008	JUMPER_2p	6	JUMPER_2p	J690 J691 J692 J694 J695 J696
99	2422-062-43241		6	JUMPER_CAP	
100	2422-549-13266		1	DIL_SOCKET_16p	
101	3111-138-26060	AT4043_87A	1	AT4043_87A	T610
102	3112-338-30521	AT4043_96	1	AT4043_96	L690
103	3112-338-32021	AT4043_78	1	AT4043_78	L640
104	3112-338-32253	AT4043_32B	1	AT4043_32B	T690
105	3112-338-33151	AT3020_01A	1	AT3020_01A	T800
106	3119-101-01700		2	SPRING-CLIP	
107	3122-138-51020	CU11B2	1	CU11B2, CU11B2	L850
108	3122-138-57081	ADJ_LC_C	1	AT4042_32A	L630
109	3122-268-30671	AT2091_32S	1	AT2091_32S	T600

110	3128-138-32291	AT4043_67A	1	AT4043_67A	L891
111	3128-138-32801	CE136ds	1	AT3006_300A	T830
112	4330-030-38081	WBC_2.5r	2	CHOKE, WBC_2.5_R	L870 L890
113	9330-229-10153	SOD27	2	BAX18	D818 D830
114	9330-839-90153	SOD27	7	1N4148	D814 D815 D816 D880 D881 D884 D885
115	9331-012-20112	SOD27	2	BAW62	D611 D660
116	9331-177-40153	SOD27	2	BZX79C6.2V	D882 D883
117	9331-892-10153	SOD27	1	BAV21	D610
118	9331-976-40112	TO92	1	BC548	TR881
119	9331-976-70112	TO92	5	BC548C	TR670 TR671 TR834 TR840 TR880
120	9331-977-50112	TO92	1	BC558B	TR672
121	9332-715-70112	TO126	1	BUX87	TR830
122	9333-636-10153	SOD57	4	BYW54	D800 D801 D802 D803
123	9333-878-80127	SOT186	1	BT151_500R	TH800
124	9333-912-80127	TO220_ac	1	BYW29-100	D690
125	9334-946-70127	SOT93	1	BUW13	TR810
126	9335-001-50153	SOD64	1	BYW95C	D850
127	9335-001-60112	SOD64	1	BYW96E	D890
128	9335-198-50682	TO220_vc	1	LM7805CT	IC830
129	9335-536-10112	SOD64	1	BYV28-200	D691
130	9336-620-20127	TO220_ac	1	BYV29-500	D870
130a			1	BYR29F800	d622
131	9337-036-90112	SOD57	2	BYV26D	D812 D813
132	9337-234-00113	SOD81	6	BYD33D, 200V	D600 D661 D662 D817 D851 D860
133	9337-533-70153	SOD81	2	VREG, 8.2V	D831 D832
134	9338-846-80127	SOT231	1	CNX82A	OC880
135	9339-524-00113	SOD64	2	BY328	D620 D621
136	9340-089-30112	TO92	1	BSN274	TR610
137	9340-154-00127	SOT199	1	BU2525AF	TR600
138	DE0707391K	CER3_1	1	CAP, 390pF, 10%	C601

139	DE0807681K	CER3_1	1	CAP, 680pF, 10%	C674
140	DIL16	SOT38_s	1	SOT38	IC800
141	K177-AC-819		2	ISOLATION-AVE	
142	LAL03NA2R2M	uChoke_3e	1	CHOKE, 2.2uH, 10%	L820
143	MKS3733-1-0-303	MKS3730	2	MKS3730_2p_220V	P602 P800
144	MKS3737-1-0-707	MKS3730_7p	1	MKS3730_7p	K600
145	MKS3738-1-0-808	MKS3730_8p	1	MKS3730_8p	K601
146	MKS3740-1-0-1010	MKS3730_10p	1	MKS3730_10pK491	
147	MKS3744-1-0-1414	MKS3730_14p	1	MKS3730_14pK891	
148	PN-L7808CV	TO220_vc	1	L7808CV	IC690
149	2322 460 91602	FMP-PRT-DAF	1	Focus unit connected to P602	

20. References.

Ref1:

Report: AN98043.

Title: Improved Picture Quality Module MK8.

Author: Heinrich Waterholter.

Ref2:

Report: AN98041.

Title: Improved Picture Quality Module MK9.

Author: Heinrich Waterholter.

Ref3:

Report: AN97083.

Title: Application of the TDA9178: YUV one chip picture improvement processor.

Autor: G.C.M.Rossen.

Ref4:

Report: AN96041.

Title: Application information for picture in picture controller SAB9077.

Author: G. Bauhuis.

Ref5:

Report: ETV/AN94015.

Title: Miniature stand-by power supply.

Author: H Simons.

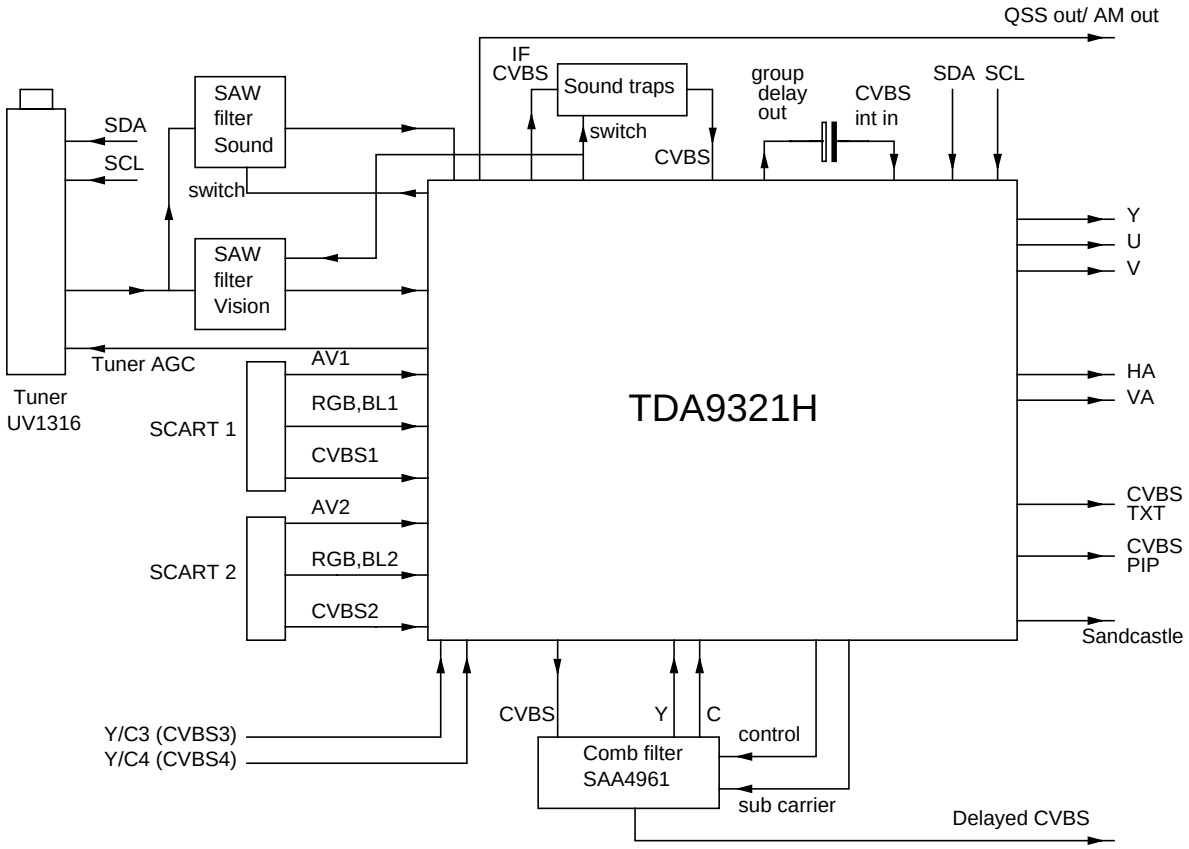

Fig 1: HIP block diagram

PHILIPS SEMICONDUCTORS PS-SLE TV Receivers	Engineer: Bergmans	Philips Semiconductors B.V. Eindhoven The Netherlands	
	Drawn by: H.v.Dingenen	Sheet Name: Fig 1	Size: A4
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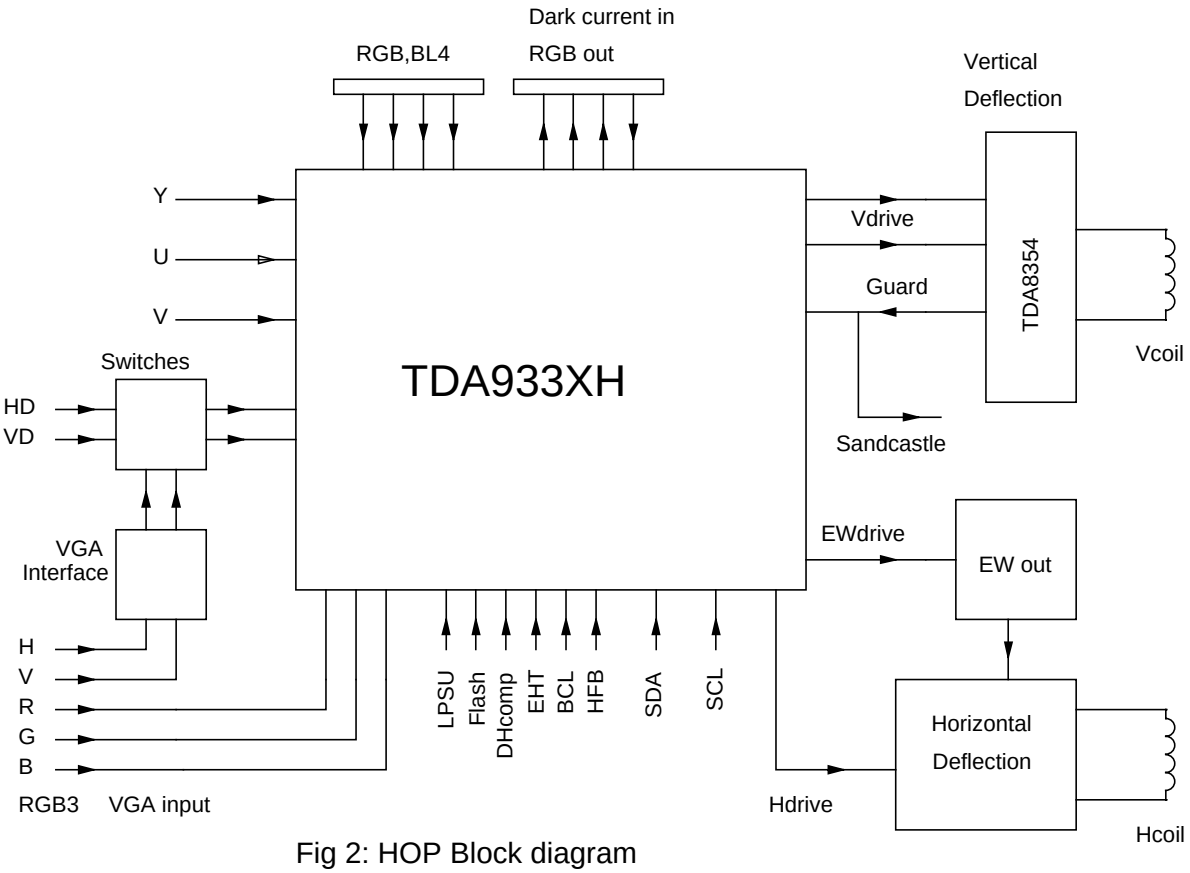

Fig 2: HOP Block diagram

PHILIPS SEMICONDUCTORS PS-SLE TV Receivers	Engineer: Bergmans	Philips Semiconductors B.V. Eindhoven The Netherlands	
	Drawn by: H.v.Dingenen	Sheet Name: Fig 2	Size: A4
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Date Changed: Friday, August 14, 1998	Time Changed: 8:20:15 am	Project: HIPHOP	Drwg: Fig 2

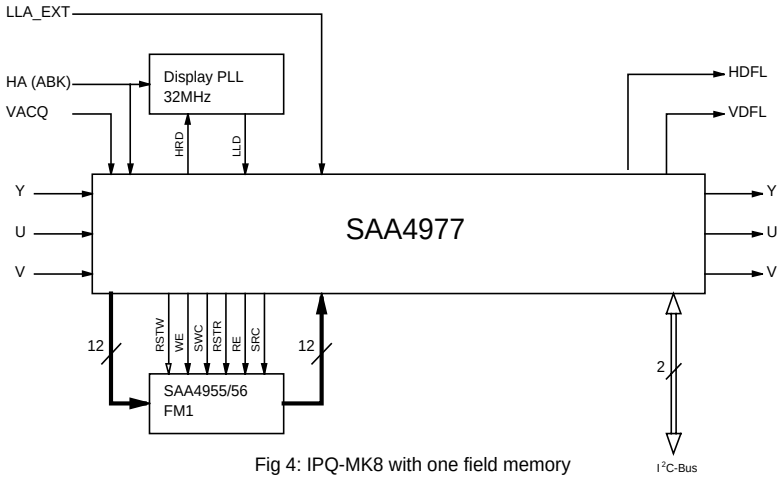

Fig 4: IPQ-MK8 with one field memory

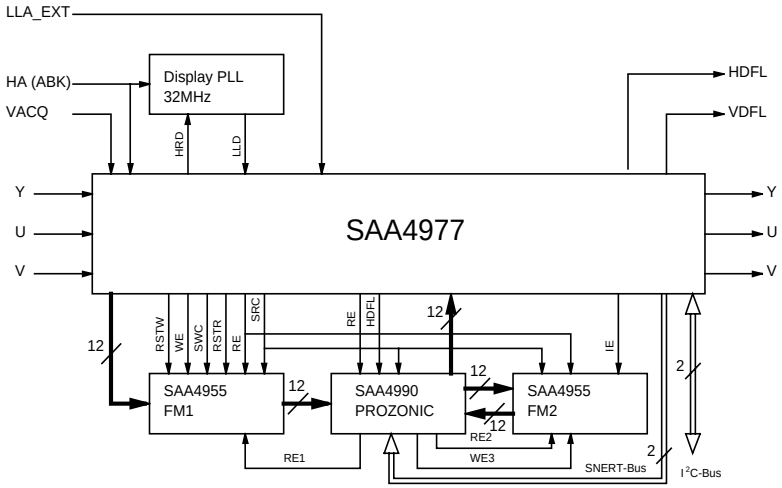

Fig 5: IPQ-MK8 with two field memories

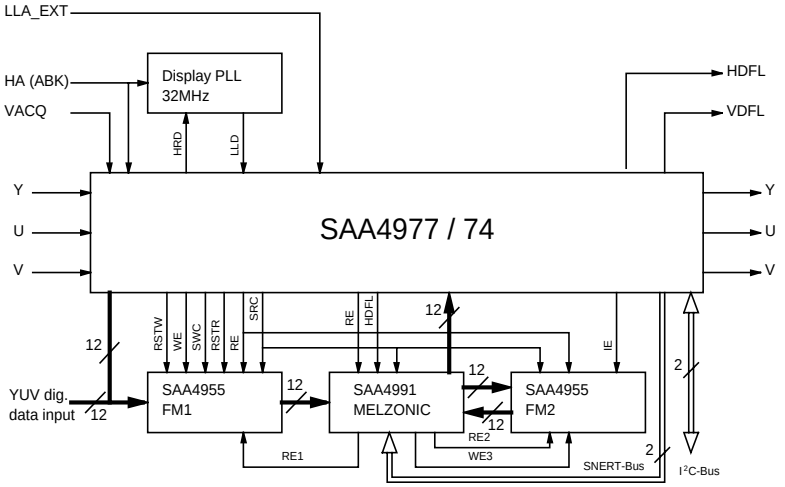

Fig 6: IPQ-MK9

PHILIPS SEMICONDUCTORS PS-SLE TV Receivers	Engineer: Bergmans	Philips Semiconductors B.V. Eindhoven The Netherlands	
	Drawn by: H.v.Dingenen	Sheet Name: Fig 4, 5, 6	Size: A4
	Changed by: Bergmans		
Date Changed: Friday, August 14, 1998	Time Changed: 8:20:15 am	Project: HIPHOP	Drwg: Fig 4, 5, 6

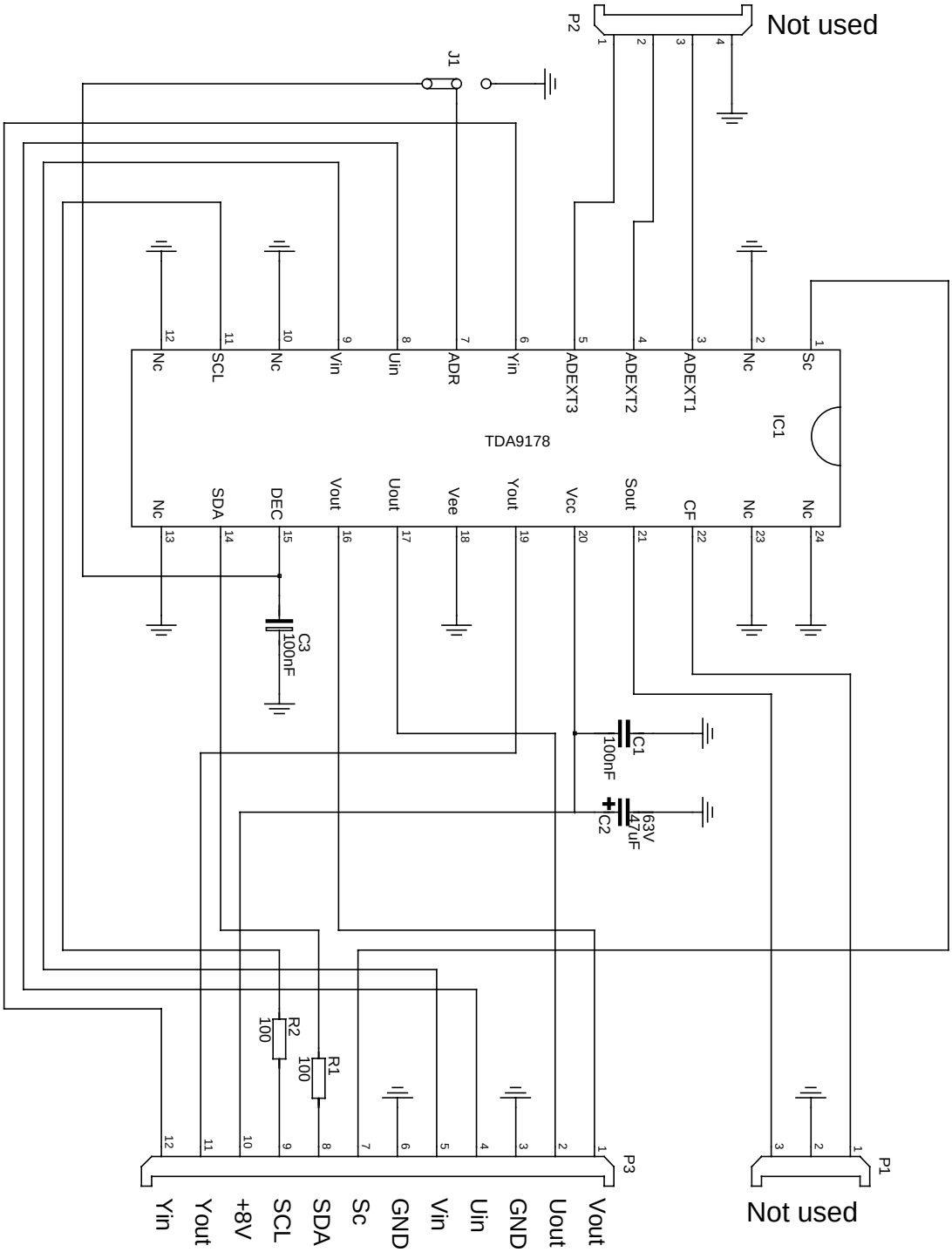

Fig 8: Picture improvement module TDA9178

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	Drawn by: H.v.Dingenen	Sheet Name: Fig 8	Size: A4
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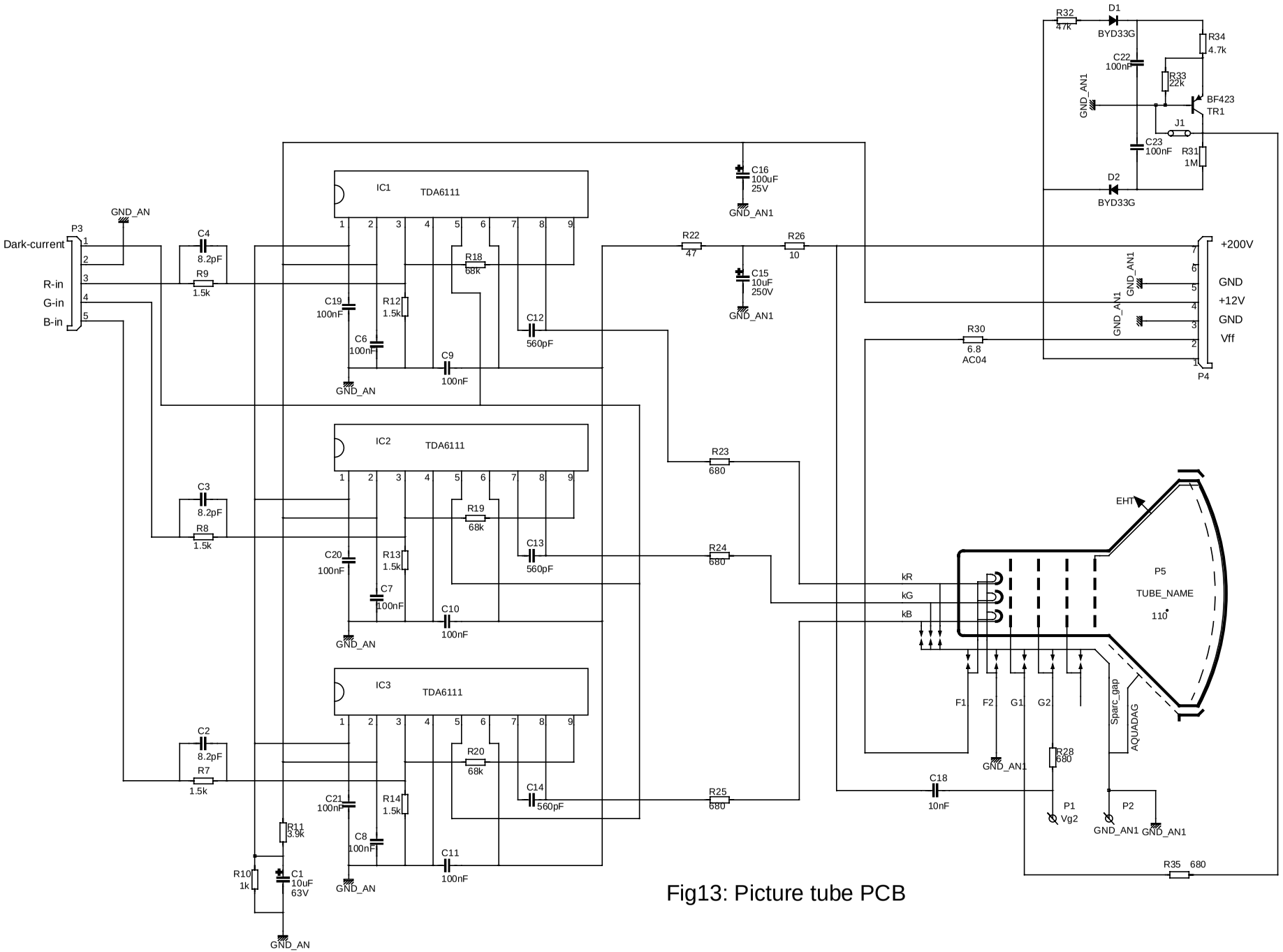

Fig13: Picture tube PCB

Date Changed: Friday, August 14, 1998	PHILIPS SEMICONDUCTORS PS-SLE TV Receivers	Engineer: Bergmans
Time Changed: 8:20:15 am	Drawn by: H.v.Dingenen Changed by: Bergmans	Philips Semiconductors B.V. Eindhoven The Netherlands
Project: HIPHOP	Sheet Name: Fig 13	Size: A4
Dwg: Fig 13		

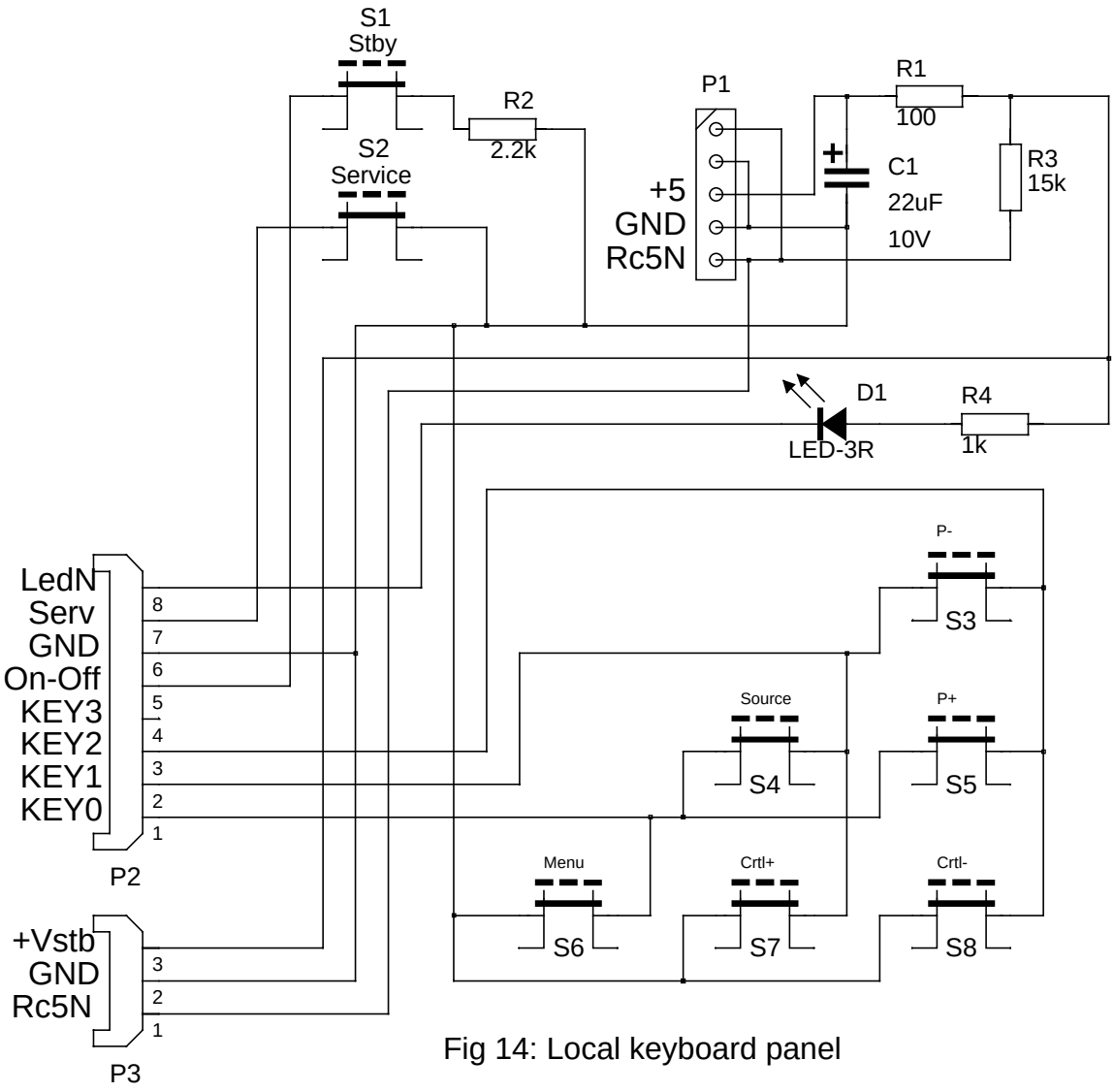

Fig 14: Local keyboard panel

PHILIPS SEMICONDUCTORS PS-SLE TV Receivers	Engineer: Bergmans	Philips Semiconductors B.V. Eindhoven The Netherlands	
	Drawn by: H.v.Dingenen	Sheet Name: Fig 14	Size: A4
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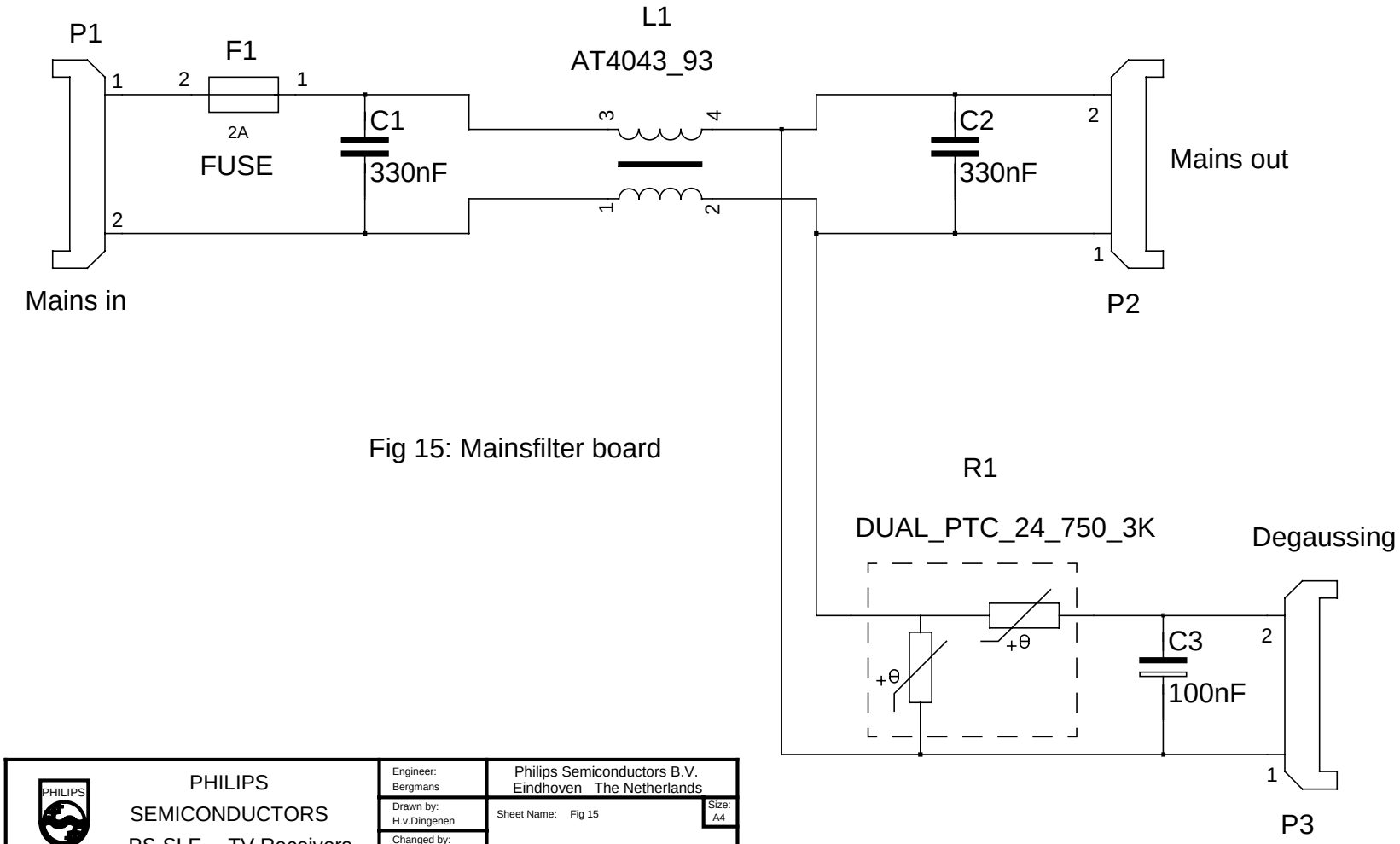

Fig 15: Mainsfilter board

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	Drawn by: H.v.Dingenen	Sheet Name: Fig 15	Size: A4
	Changed by: Bergmans		
Date Changed: Friday, August 14, 1998	Time Changed: 8:20:15 am	Project: HIPHOP	Drwg: Fig 15

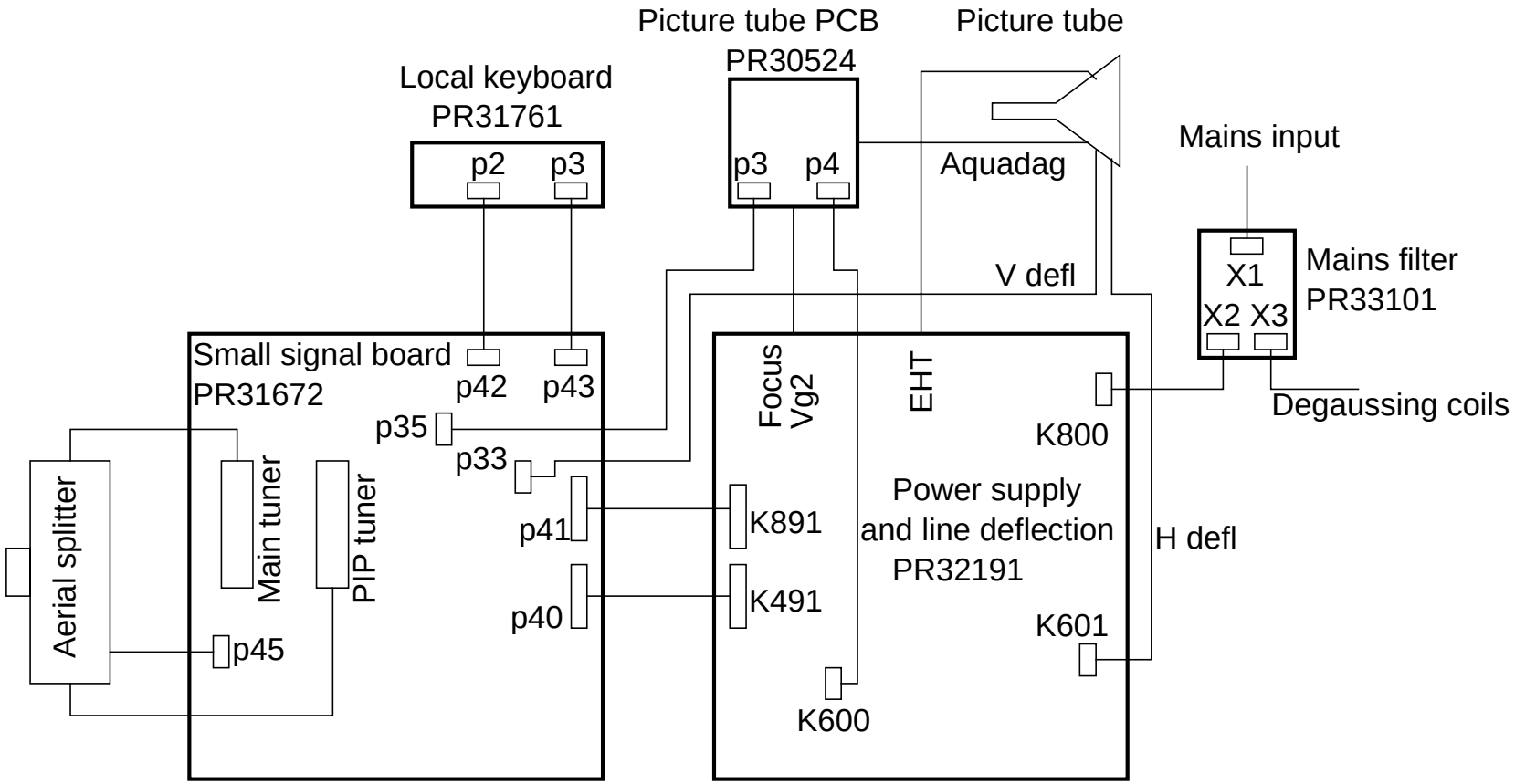

Fig 18: Interconnections

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	Drawn by: H.v.Dingenen	Sheet Name: Fig 18	Size: A4
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Date Changed: Friday, August 14, 1998	Time Changed: 8:20:15 am	Project: HIPHOP	Drwg: Fig 18

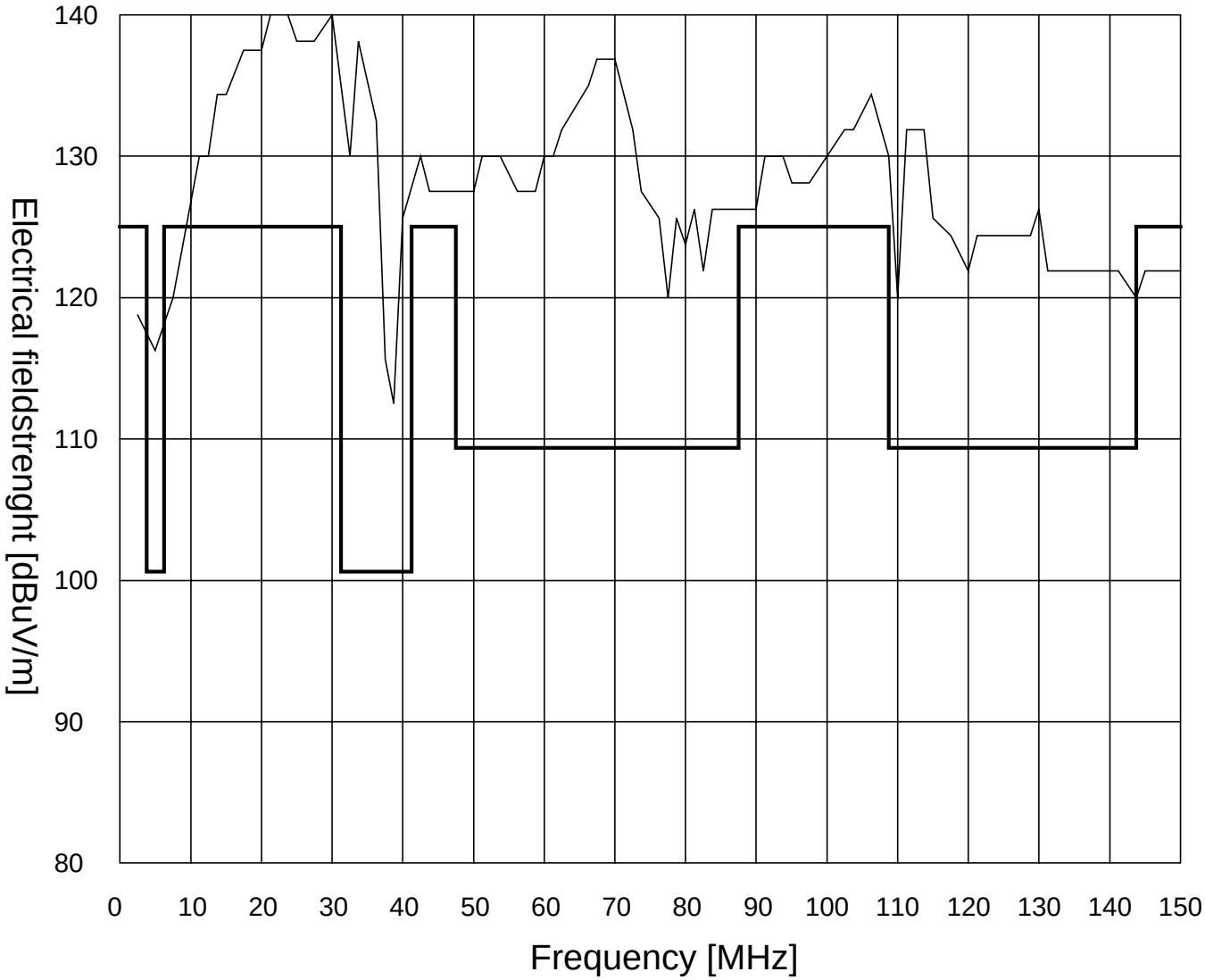

Fig 19a: EMC measurement on GTV4000 in SECAM L mode

PHILIPS SEMICONDUCTORS
PS-SLE TV Receivers

Engineer: Bergmans
Drawn by: H.v.Dingenen
Changed by: Bergmans
Time Changed: 8:20:15 am
Date Changed: Friday, August 14, 1998

Philips Semiconductors B.V.
Eindhoven The Netherlands

Sheet Name: Fig 19a
Project: HIPHOP
Drwg: Fig 19a
Size: A4

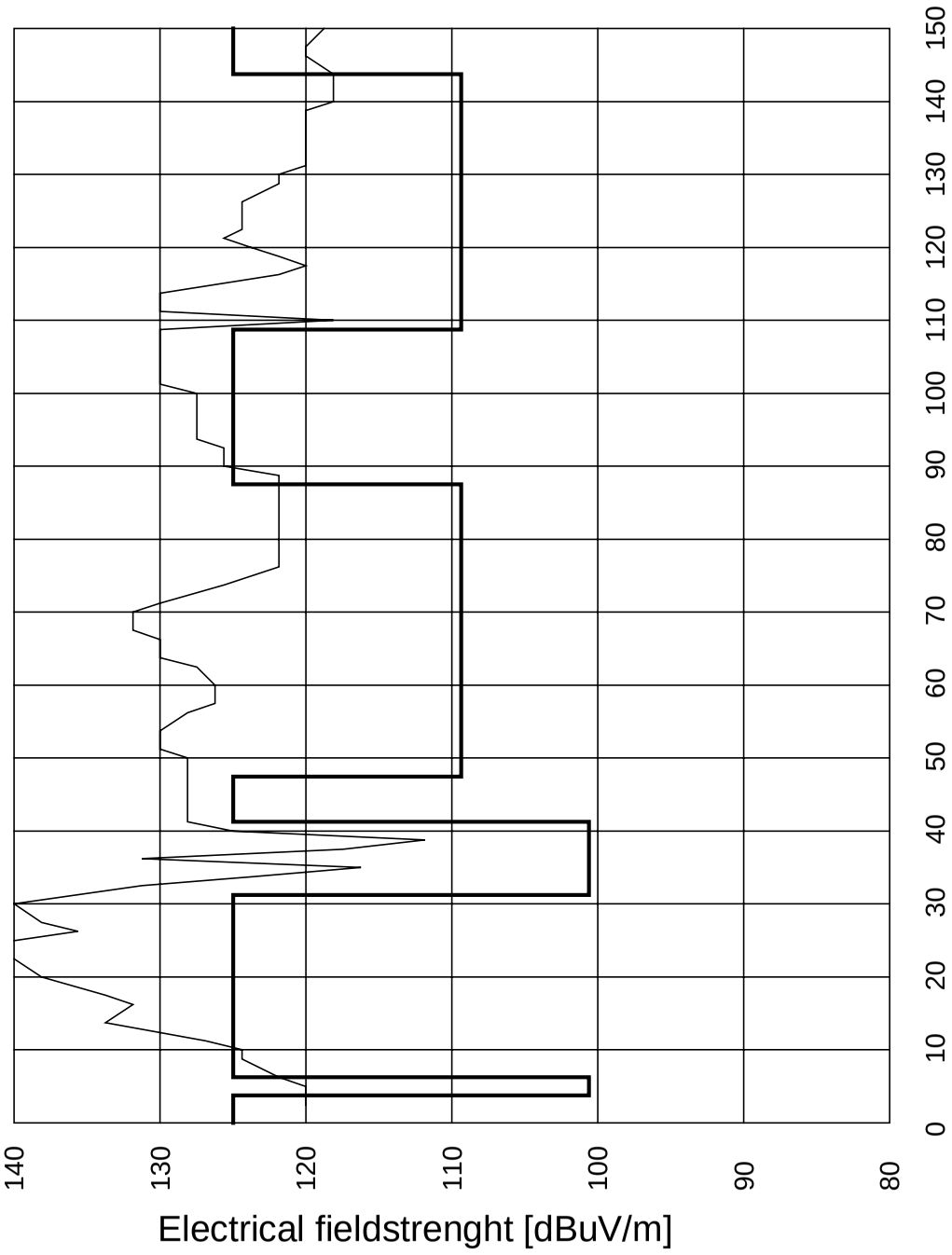

Fig 19b: EMC measurement on GTV4000 in PAL B/G mode

PHILIPS SEMICONDUCTORS PS-SLE TV Receivers	Engineer: Bergmans	Philips Semiconductors B.V. Eindhoven The Netherlands	
	Drawn by: H.v.Dingenen	Sheet Name: Fig 19b	Size: A4
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Date Changed: Friday, August 14, 1998	Time Changed: 8:20:15 am	Project: HIPHOP	Drwg: Fig 19b

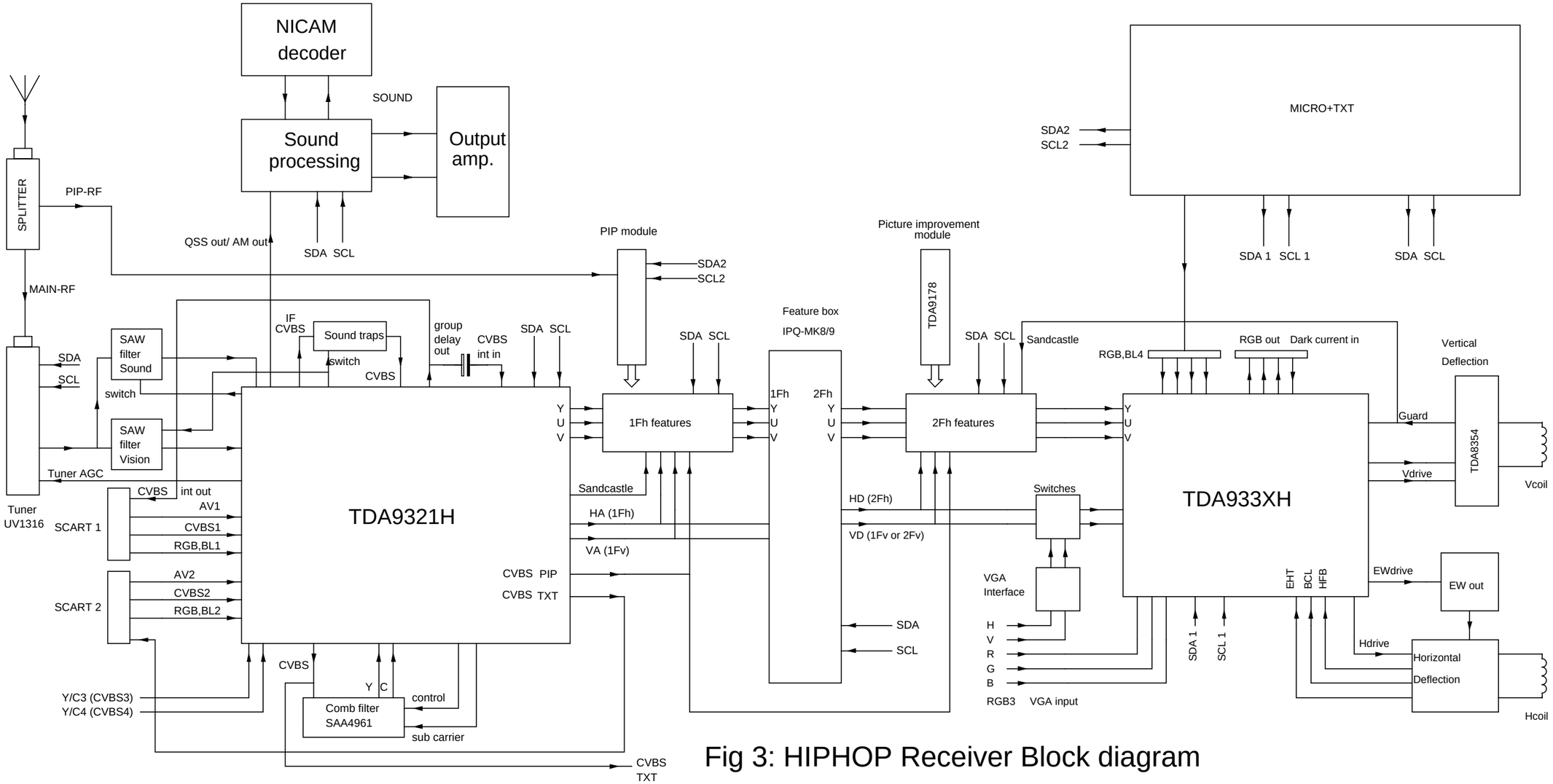

Fig 3: HIPHOP Receiver Block diagram

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	Drawn by: H.v.Dingenen	Sheet Name: Fig 3	Size: A3
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PHILIPS SEMICONDUCTORS PS-SLE TV Receivers | Engineer: Bergmans | Drawn by: H.v.Dingenen | Changed by: Bergmans | Philips Semiconductors B.V. Eindhoven The Netherlands | Sheet Name: Fig 7a | Size: A3 | Date Changed: Friday, August 14, 1998 | Time Changed: 8:20:15 am | Project: HIPHOP | Drwg: Fig 7a

IPQ

50Hz features

FEAT.2

PIP

PIP SAB9077 + tuner + HIP

100Hz features

TDA9178 PIP

TXT

IF buffer

System witches

Splitter supply

Sound traps

CVBS (PIP)

TDA9321H

IC2

M/N=1

L' = 0

Fig7a: Main board part a

TDA9321H

IC2

CVBS output buffer

Comb filter

SAA4961

Sound trap switches

Sound traps

SCART 1

SCART 2

Int CVBS output ampl.

Fig 7b: Main board part b

Philips Semiconductors B.V. Eindhoven The Netherlands	Size: A3
Sheet Name: Fig 7b	
Engineer: Bergmans	Drawn by: H.v.Dingenen
Changed by: Bergmans	
PHILIPS SEMICONDUCTORS PS-SLE TV Receivers	
Project: HIPHOP	Drwg: Fig 7b
Time Changed: 8:20:15 am	
Date Changed: Friday, August 14, 1998	

PHILIPS SEMICONDUCTORS PS-SLE TV Receivers	Engineer: Bergmans	Philips Semiconductors B.V. Eindhoven The Netherlands	
	Drawn by: H.v.Dingenen	Sheet Name: Fig 7c	Size: A3
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Date Changed: Friday, August 14, 1998	Time Changed: 8:20:15 am	Project: HIPHOP	Drwg: Fig 7c

TDA933XH
IC11

TDA9330AH + NV memory

Fig 7c: Main board part c

VGA sound Aplifiers

Sound switches

From sound board

LPS

Low power start up

Xtal out

Xtal in

Ground

Bandgap

Vcc

I ref

V saw

Dynamic phase shift in

H flyback

H select

Vertical deflection

EW amplifier

DEFLECTION

SUPPLY

Sound

Sound output amplifiers

Fig 7d: Main board part d

PHILIPS SEMICONDUCTORS PS-SLE CONSUMER 1	Engineer: C. Bergmans	Philips Semiconductors B.V. Eindhoven The Netherlands	
	Drawn by: C. Bergmans	Sheet Name: Fig 7d	Size: A3
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	Changed by: Bergmans		
Date Changed: Friday, August 14, 1998	Time Changed: 8:20:15 am	Project: HIPHOP	Drwg: Fig9a

IC2

SAB9077H

IC3 uPD482234

IC1 TDA8601

Fig 9a: PIP module PIP part

IC5
TDA9321H

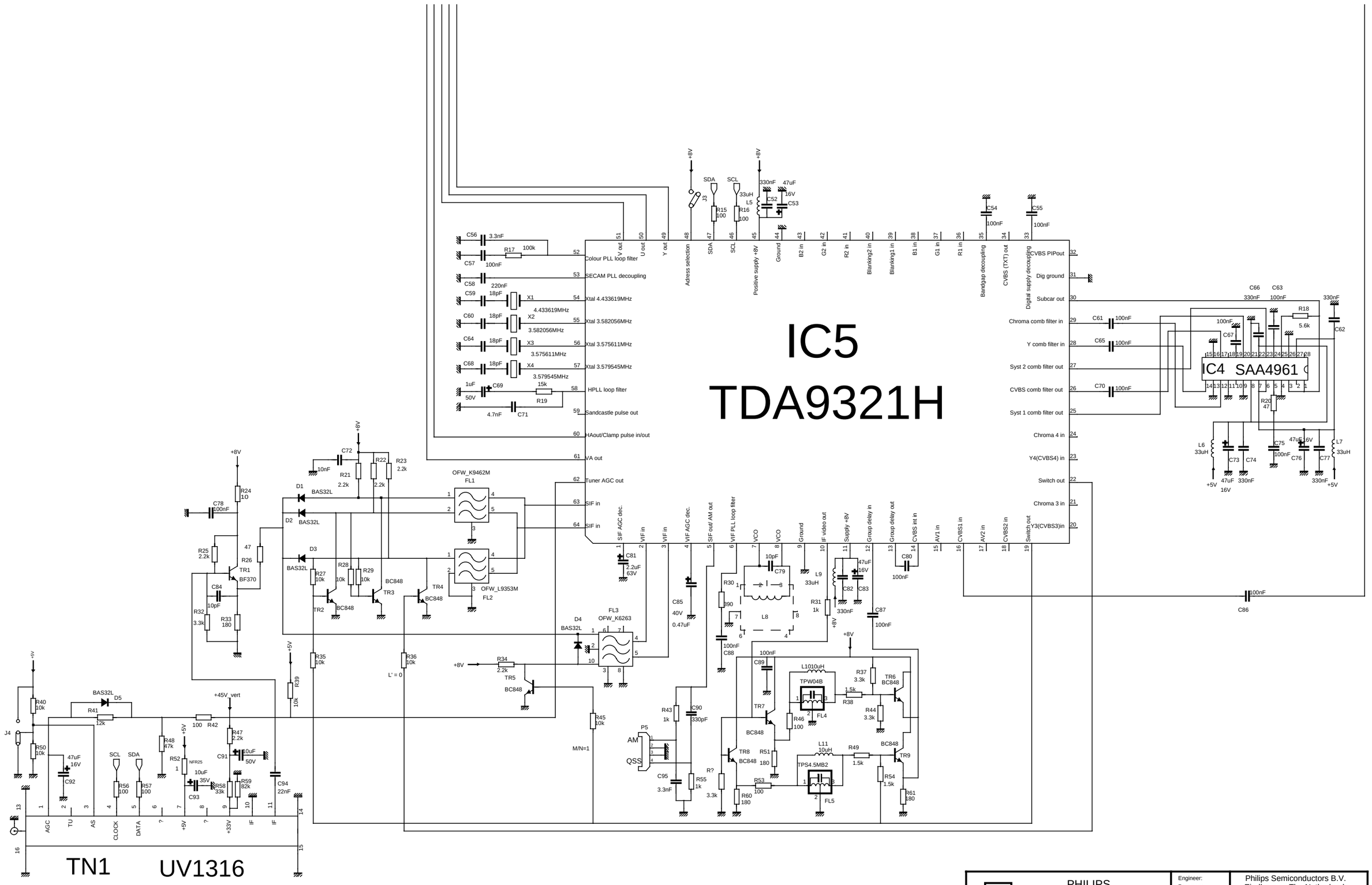

Fig 9b: PIP module frontend part

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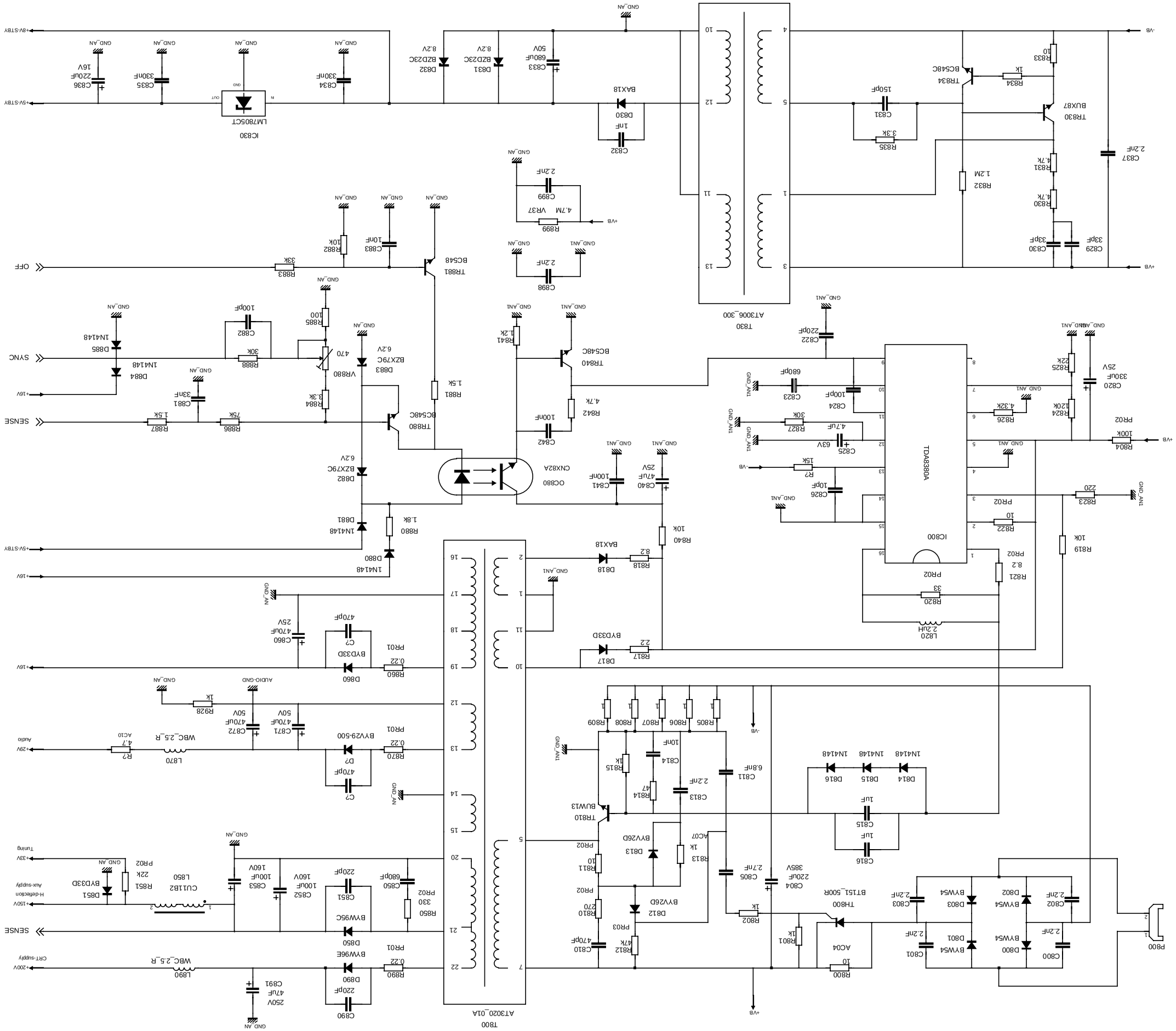
Fig 16: SMPS


PHILIPS
SEMICONDUCTORS
PS-SLE TV Receivers
Philips Semiconductors B.V.
Eindhoven The Netherlands
Engineer: Bergmans
Drawn by: H.v.Dingenen
Changed by: Bergmans
Date Changed: Friday, August 14, 1998
Time Changed: 8:20:15 am
Project: HIPHOP
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Size: A3
Dwg: Fig 16
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AT3006_30
T800
AT3020_01A
IC800
TDA8380A
IC830
LM7805CT
+8V-STBY
+5V-STBY
+16V
+29V
+200V
+150V
+35V
SENSE
SYNC
OFF
-VB
+VB
GND_AN
GND_AN1
GND_ANU1
AUDIO-GND

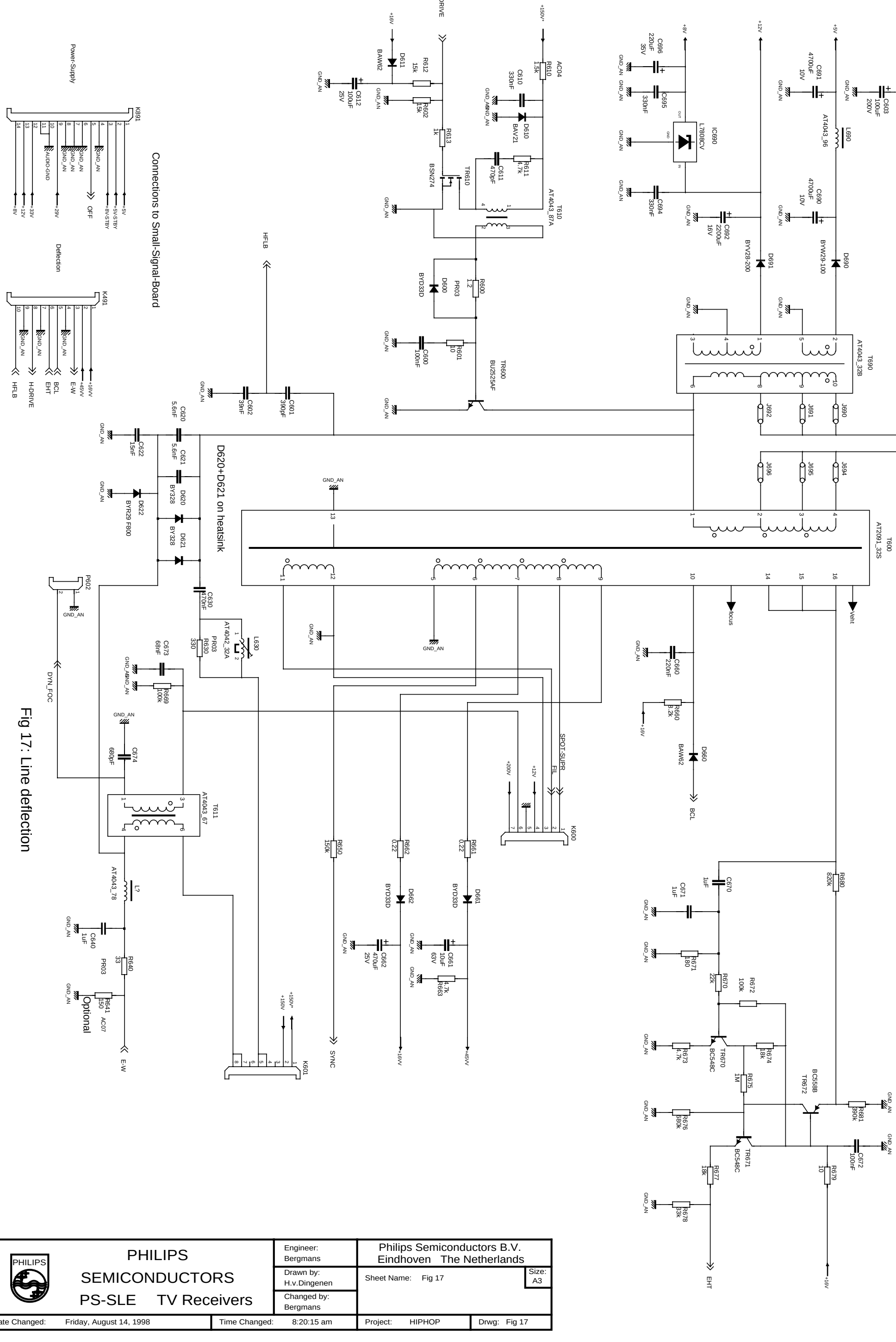

Fig 17: Line deflection

PHILIPS SEMICONDUCTORS PS-SLE TV Receivers	Engineer: Bergmans	Philips Semiconductors B.V. Eindhoven The Netherlands	
	Drawn by: H.v.Dingenen	Sheet Name: Fig 17	Size: A3
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Date Changed: Friday, August 14, 1998	Time Changed: 8:20:15 am	Project: HIPHOP	Drwg: Fig 17