Noritake itron

RoHS 2002/95/EC

Vacuum Fluorescent Display Module Specification

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1. General Description

1.1 Construction: A 160X32 dot BD-VFD single board display module consisting of an 8 bit micro-computer, character generator and a DC/DC converter.

1.2 Features: Simultaneous display of graphic and Simplified Chinese characters.
(Please refer to the Character cord table "DS-825-0002-XX)
Flexible Display and Editing Functions.
Compact design due to the application of a BD-VFD tube.

1.3 Dimensions: See attached drawings.

2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Input Voltage	VI	-0.5	—	Vcc +0.3	V	—
Power Supply Voltage	Vcc	0	—	6.5	VDC	—

3. Electrical Characteristics

Measurement Conditions: 25°C / Vcc=5.0V

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Input Voltage	"H"	VIH	4.0	—	—	VDC	IIH= 2 μA
	"L"	VIL	—	—	1.0		IIL= - 600 μA
Logic Output Voltage	"H"	VOH	4.7	—	—	VDC	IOH= - 300 μA
	"L"	VOL	—	—	0.3		IOL= 300 μA
Reset Input Voltage	"H"	VRH	4.0	—	—	VDC	IRH= 5 μA
	"L"	VRL	—	—	0.6	VDC	IRL= - 600 μA
Power Supply Voltage		Vcc	4.75	5.00	5.25	VDC	—
Power Supply Current		Icc	—	550	700	mA	VCC=+5V, All dots ON
			—	450	600		VCC=+5V, All dots OFF

Notes:

The rise time of **Vcc** should not exceed **100 ms**.

Icc may peak at power up may be more than twice the normal operating current

4. Optical Specifications

Number of dots: 5120 (160X32)
Display area: 101.45 mm x 20.17mm (X x Y)
Dot size: 0.485 mm x 0.485 mm (X x Y)
Dot pitch: 0.635 mm x 0.635 mm (X x Y)
Luminance: 350cd/m^2 (Min.)
Color of illumination: Green (Blue Green)

5. Environmental Specifications

Operating temperature: -40 to +85°C
Storage temperature: -40 to +85°C
Storage humidity: 20 to 80 % R.H(Non Condensation)
Vibration: 10-55-10Hz, all amplitude 1mm, 30Min., X-Y-Z (Non operating)
Shock: 539m/s^2 10mS (Non operating)

6. Description of Bus and Signals

This module has serial and 2 types of parallel interface.
Type of interface can be selected by jumper settings. Refer to 11 on page # 20 for details.

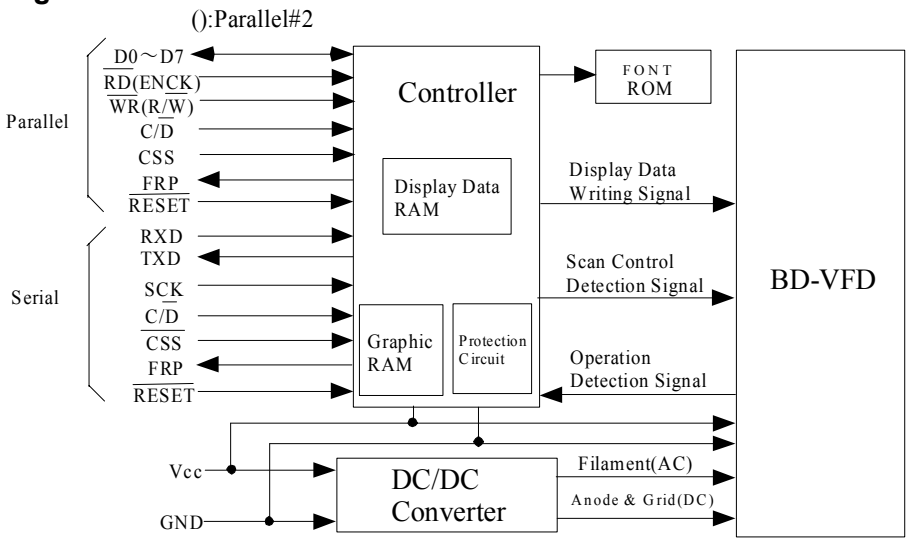
6.1 Parallel Interface

Data Line	Function
D0 ～ D7	Data Bus (Input / Output)
$\overline{WR}$ (R/$\overline{W}$)	Parallel #1: $\overline{\text{Write Signal}}$, Parallel #2: R/$\overline{W}$ (Input)
$\overline{RD}$ (ENCK)	Parallel #1: $\overline{\text{Read Signal}}$, Parallel #2: ENCK (Input)
$\overline{CSS}$	Chip Select (Input)
$\overline{C/D}$	Command / Data Select Signal (Input) C/$\overline{D}$ = "1" ⋯ Command C/$\overline{D}$ = "0" ⋯ Data
FRP	**Fr**ame **P**ulse Signal (**O**utput)
$\overline{RESET}$	$\overline{RESET}$="0"⋯ Reset (Input)
Vcc	Power Supply
GND	Ground

6.2 Serial Interface

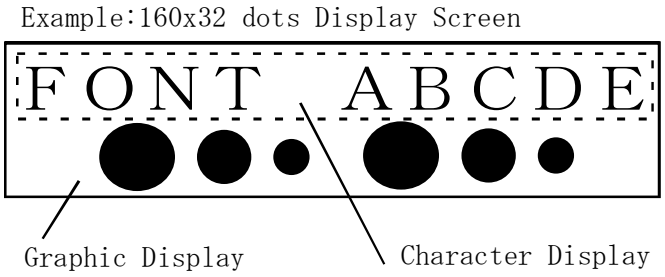
Data Line	Function
RXD	Serial Input
TXD	Serial Output
SCK	Clock (Input)
$\overline{CSS}$	Chip Select (Input)
$\overline{C/D}$	Command / Data Select Signal (Input) C/$\overline{D}$ = "1" ⋯ Command C/$\overline{D}$ = "0" ⋯ Data
FRP	Frame Pulse Signal (Output)
$\overline{RESET}$	$\overline{RESET}$="0"⋯ Reset (Input) Active Low
Vcc	Power Supply
GND	Ground

7. Block Diagram



8. Display Screen

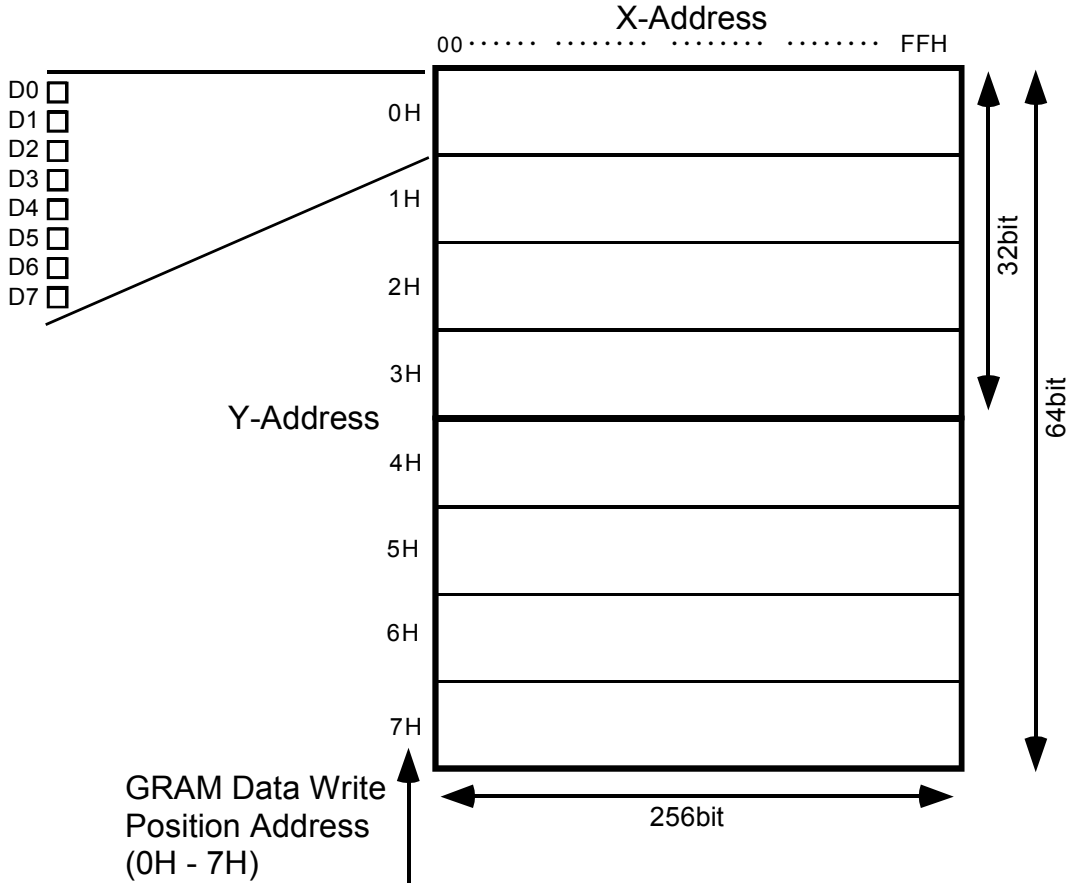
The Display screen consists of 5120 dots arranged as 160 by 32dots. It is divided into 40 display area blocks of 16 by 8 dots each. Each display area block can be assigned to GRAM or DDRAM by the Display Area Set command. Refer to Section 9.5 (page # 10) Display Area Set. The combination display of characters and graphics is possible by using this function described in the following figure. All display area blocks are set as DDRAM area as default.



8.1 Graphic Display (GRAM)

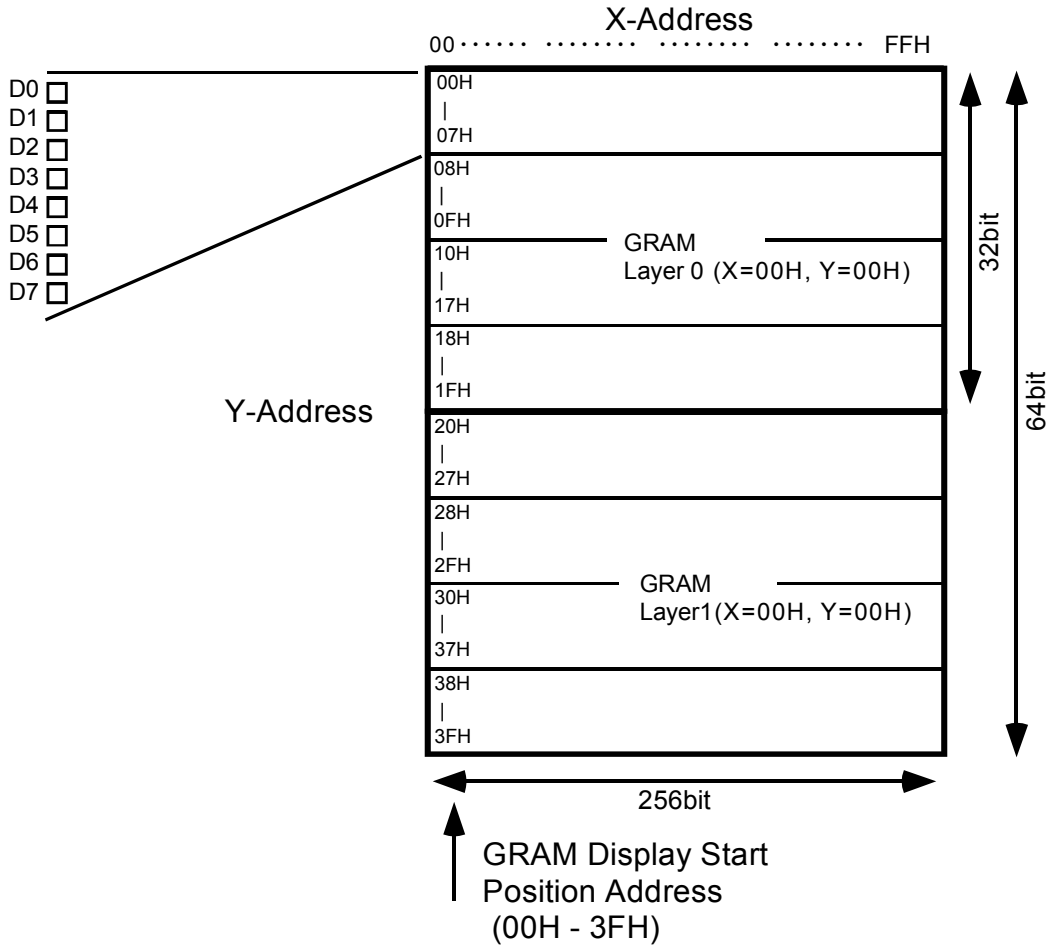
GRAM consists of 16,384 bits arranged in 256 by 64 bit blocks with access is structured as 8 bits of vertical data. The detail of GRAM is as follows:

GRAM Data Write Position Address



8.1 Cont'd

GRAM Display Start Position Address



This module has 2 layers - Layer 0 and Layer 1. Each layer in this display consists of 256 by 32 dots. Display merging using these 2 layers can be done with the Display ON/OFF command. Refer to 9.2 on page # 8 for details.

Layer 0 has an area of 256X32 dots that starts from top left point defined by the GRAM Start Position Address. The area of Layer 1 is the next 256X32 dots.

When the value of the GRAM Start Position Address X overflow = FFH, the next position goes to 00H.
When the value of the GRAM Start Position Address Y overflow = 3FH, the next position goes to 00H.

For example:
If the GRAM Start Position Address is set as X=02H, Y=08H, the area of Layer 0 is as follows;

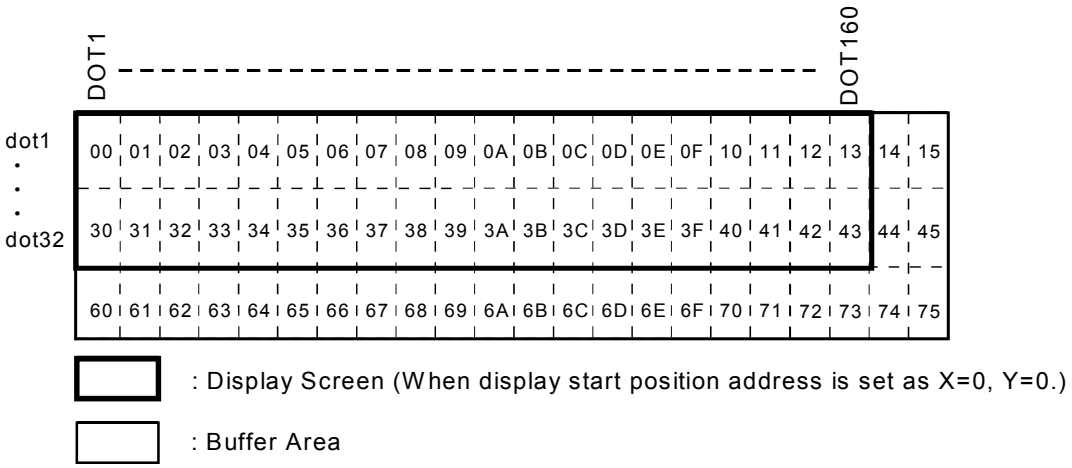
X=02H,03H,04H……FFH,00H,01H
Y=08H,09H……26H, 27H

In this case, the area of Layer1 is as follows;
X=02H,03H,04H……FFH,00H,01H
Y=28H,29H……06H,07H

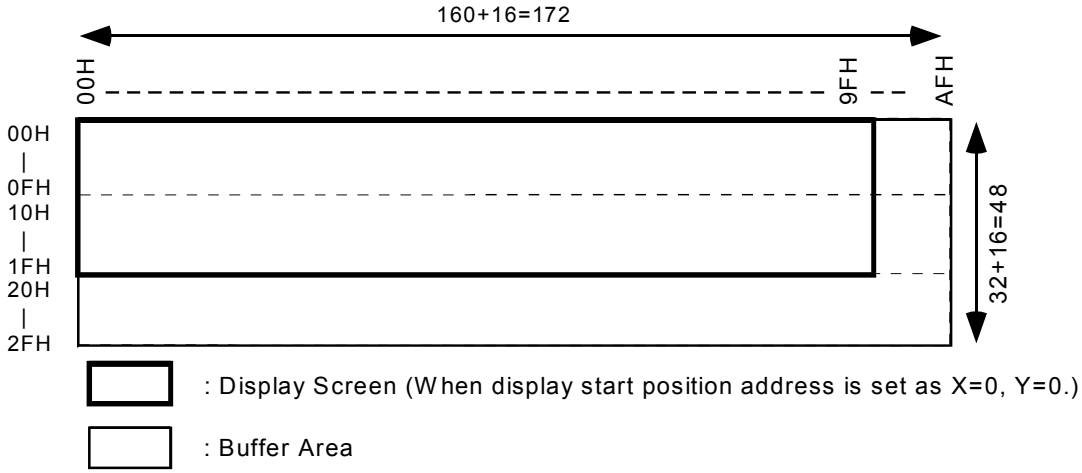
8.2 Character Display (DDRAM)

The DDRAM consists of “blocks” of either 16x16 dots, or 8x16 dots. This equates yields a width of either 11 *(16 pixels x 16 pixels)*, or 22 (8 x 16) characters x 3 lines. When 8 bits of data is sent twice, a character code can be written in a memory. The detail of DDRAM is as follows:

The DDRAM Data Write Position Address:



The DDRAM Display Start Position Address



When the value of the DDRAM Start Position Address X = Overflow AFH, the next position goes to 00H. Also, when value of the DDRAM Start Position Address Y = Overflow 2FH, the next position goes to 00H.

For example:

In the case of a DDRAM Start Position Address of X=30H, Y=20H, the Display screen area is as follows;

X=30H, 31H, 32H……AFH, 00H, 01H……1DH, 1EH, 1FH
Y=20H, 21H, 22H.....2FH, 00H, 01H.....0DH, 0EH, 0FH

9.0 Function

9.1 Commands

Command	C/$\overline{D}$	D7	D6	D5	D4	D3	D2	D1	D0	Comments	
Display ON/OFF	1	0	0	1	0	L1	L0	*	*	1st Byte	Display ON/OFF Control、2 Byte Command
		DS	GS	DRV	GRV	AND	EXOR	*	*	2nd Byte	
Brightness Set	1	0	1	0	0	BW3	BW2	BW1	BW0	1 Byte	1 Byte Command
Display Clear	1	0	1	0	1	G1C	G0C	DC	HM	1 Byte	1 Byte Command
Display Area SET	1	0	1	1	0	*	*	1	*	1st Byte	Display Area is assigned 3 Byte Command
		*	*	*	*	*	(A2～A0)			2nd Byte	
	0	D7	D6	D5	D4	D3	D2	D1	D0	3rd Byte	
Data Write Position Address Set	1	0	1	1	0	1	*	0	*	1st Byte	Character Display Address Set, 2 Byte Command
		DDRAM Address（DDA7～DDA0）								2nd Byte	
	1	0	1	1	0	0	1	0	*	1st Byte	Graphic Display X-Address Set, 2 Byte Command
		GRAM X-Address (GXA7～GXA0)								2nd Byte	
	1	0	1	1	0	0	0	0	*	1st Byte	Graphic Address Y-Address Set, 2-Byte Command
		*	*	*	*	0	GYA2	GYA1	GYA0	2nd Byte	
Display Start Position Address Set	1	0	1	1	1	*	*	*	*	1st Byte	Graphic Display Horizontal Shift, 2-Byte Command
		XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	2nd Byte	
	1	1	0	1	1	UD	S1	S0	*	1 Byte	Graphic Display Vertical Shift, 1 Byte Command
	1	1	0	1	0	*	*	*	0	1st Byte	Character Display Horizontal Shift, 2 Byte Command
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	2nd Byte	
	1	1	0	0	1	UD	S1	S0	*	1 Byte	Character Display Vertical Shift, 1 Byte Command
Address Mode Set	1	1	0	0	0	*	IGX	IGY	*	1 Byte	Address Increment, 1 Byte Command
Address Read	1	1	1	0	1	1	0	*	*	1st Byte	Character Display (DDRAM) Horizontal And Vertical Display Start Address, 3 Byte Command
		VD6	VD5	VD4	VD3	VD2	VD1	VD0	HD8	2nd Byte	
		HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	3rd Byte	
	1	1	1	0	1	0	1	*	*	1st Byte	Graphic Display (GRAM) Horizontal And Vertical Display Start Address, 3 Byte Command
		*	VG6	VG5	VG4	VG3	VG2	VG1	VG0	2nd Byte	
		HG7	HG6	HG5	HG4	HG3	HG2	HG1	HG0	3rd Byte	
ROM Transfer	1	1	1	1	0	*	*	*	*	1st Byte	Copy character in the Font ROM, 3 Byte Command
		AD19	AD18	AD17	AD16	AD15	AD14	AD13	AD12	2nd Byte	
		*	AD10	AD9	AD8	AD7	AD6	AD5	AD4	3rd Byte	
Data Write	0	WRITE DATA									Writes Data Char. Data is 2 Byte, Graphic Data is 1 Byte

* Either a “0” or a “1” is acceptable

9.2 Display On/Off (C/$\overline{D}$= "1")

The GRAM Layer is selected with the 1st Byte of data. DDRAM (**On/Off**), GRAM (**On/Off**), DDRAM (**reverse** or **normal** modes), GRAM (**reverse** or **normal** modes) and display merge are selected by the 2nd Byte. Reverse mode toggles the representation of green in the foreground and black in the background to the exact opposite - green to back and black to the foreground. This is similar to the concept of reverse video.

1st Byte:

MSB							LSB	
0	0	1	0	L1	L0	*	*	* Either a “0” or a “1” is acceptable
< ---------- >				< --------- >				
Command Select				Display Control Data				

L1= (**1** OR **0**) = GRAM Layer 1 (**Active** OR **Inactive**)
L0= (**1** OR **0**) = GRAM Layer 0 (**Active** OR **Inactive**)

2nd Byte:

MSB							LSB	
DS	GS	DRV	GRV	AND	EXOR	*	*	* Either a “0” or a “1” is acceptable
< ---------- ---------- >								
Display Control Data								

DS= (**1** OR **0**) Character Display Area (DDRAM) = (**On** OR **Off**)
GS= (**1** OR **0**) Graphic Display Area (GRAM) = (**On** OR **Off**)
DRV= (**1** OR **0**) Character Display Area (DDRAM) = (**Reverse** OR **Normal**)
GRV= (**1** OR **0**) Graphic Display Area (GRAM) = (**Reverse** OR **Normal**)

DS=”0”, GS= “0”: Stand-by mode

1st Byte		2nd Byte		Action
L1	L0	AND	EXOR	
*	*	1	*	AND Display of Layer 1& 0
*	*	0	1	EXOR Display of Layer 1& 0
1	1	0	0	OR Display of Layer 1& 0
1	0	0	0	Only Layer1 selected for display
0	1	0	0	Only Layer0 selected for display
0	0	0	0	Graphic Display Off

* Either a “0” or a “1” is acceptable

9.3 Brightness Set (C/D= "$\overline{1}$")

The Brightness level of the display screen can be scaled by the following four bit control. Please note that the brightness is consistent across the illuminated pixels. There is no scaling of individual pixels. The display self-initializes to 100% brightness.

MSB							LSB
0	1	0	0	BW3	BW2	BW1	BW0
< ---------- >				< ---------- >			
Command Select				Brightness Level Data			

9.3 Cont'd

Brightness levels are set by the following:

BW3	BW2	BW1	BW0	Brightness Level
0	0	0	0	100%(Light)
0	0	0	1	94%
0	0	1	0	87%
0	0	1	1	81%
0	1	0	0	75%
0	1	0	1	69%
0	1	1	0	62%
0	1	1	1	56%
1	0	0	0	50%
1	0	0	1	44%
1	0	1	0	37%
1	0	1	1	31%
1	1	0	0	25%
1	1	0	1	19%
1	1	1	0	12%
1	1	1	1	6%(Dark)

9.4 Display Clear (C/$\overline{D}$= "1") This command clears the GRAM and DDRAM.

This command should always be applied at power on or reset. In the period of 1mS following the issue of this command, the module requires internal processing and does not accept any commands.

MSB							LSB
0	1	0	1	G1C	G0C	DC	HM
< ---------- >				< ---------- >			
Command Select				Clear Control Code			

* Either a "0" or a "1" is acceptable

To clear the GRAM area, G1C or G0C bit must be asserted. By asserting HM bit, both data write position address and display start position address which selected by G1C, G0C, DC also be reset.

HM = (1 or 0) equals (Initialize data write position address and display start position address or Not initialize).

G1C= (1 or 0) equals (GRAM area 1 is cleared or GRAM area 1 not cleared)
G0C= (1 or 0) equals (GRAM area 0 cleared or GRAM area 0 not cleared)
GRAM area 1: X= 00H-FFH, Y=0H – 3H (Display data write position address)
GRAM area 2: X= 00H-FFH, Y=4H – 7H (Display data write position address)

DC= (1 or 0) equals (DDRAM cleared or DDRAM not cleared)
Example to clear both layers: 0101 1111

9.5 Display Area Set (C/$\overline{D}$="1")

This command sets the display area block as Graphic Display (GRAM) or Character display (DDRAM). Setup is performed by 3-byte command. A data-write position address set is required after switching display area, and before character or graphic data writing.

1st Byte: (C/$\overline{D}$="1") Command Select

MSB							LSB
0	1	1	0	*	*	1	*
< ---------- >							

Command Select

* Either a “0” or a “1” is acceptable

2nd Byte: (C/$\overline{D}$="1") Display Area Data Address Select

MSB							LSB
*	*	*	*	*	A2	A1	A0
					< ---------- >		

Display Area Data Address

* Either a “0” or a “1” is acceptable

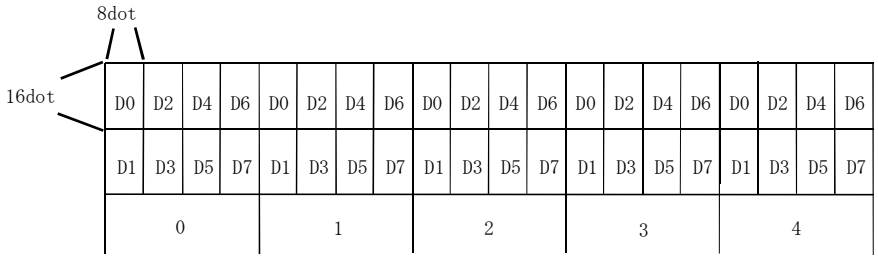
3rd Byte: (C/$\overline{D}$="0") Display Area Block Select

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
< ---------- >							

Display Data

D0 to D7 = "1": Graphic Display (GRAM)
D0 to D7 = "0": Character Display (DDRAM)

Display area block is assigned as follows on a screen.



Display Area Data Address (0 ～ 4H)

9.6 DDRAM Data Write Position Address Set (Character Display) (C/$\overline{D}$="1")

1st Byte: Command Select

MSB							LSB	
0	1	1	0	1	*	0	*	* Either a “0” or a “1” is acceptable
< ---------- >								

2nd Byte: DDRAM Data Write Position Address

MSB							LSB	
DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	* Either a “0” or a “1” is acceptable
< ---------- >								

The data write position address of DDRAM expressed with 8 bits (00Hex-75Hex) of DDA0-DDA7 is specified, and a character code is inputted after the 2nd Byte. Not to set addresses other than a sphere. Right end cannot write a 16x16 dots font in the place which is vacant only as for 8x16 dots. Refer to 8.2 Character Display (DDRAM) on Page #6

9.7 GRAM Data Write position Address Set (Graphic Display) (C/$\overline{D}$="1")

This command specifies both X & Y data write position address.

9.7.1 GRAM Data Write Position X Address Set

Data write position X address of GRAM expressed with 8 bits (00Hex-FFHex) is specified.
Refer to 8.1 Graphic Display (GRAM) on Page #4.

1st Byte: Command Select

MSB							LSB	
0	1	1	0	0	1	0	*	* Either a “0” or a “1” is acceptable
< ---------- >								

2nd Byte: GRAM Data Write Position X Address

MSB							LSB
GXA7	GXA6	GXA5	GXA4	GXA3	GXA2	GXA1	GXA0
< ---------- >							

9.7.2 GRAM Data Write Position Y Address Set

Data write position Y address of GRAM expressed with 4 bits (0Hex-7Hex) is specified.

1st Byte:

MSB							LSB	
0	1	1	0	0	0	0	*	* Either a “0” or a “1” is acceptable
< ---------- >								

Command Select

2nd Byte:

MSB							LSB	
*	*	*	*	0	GYA2	GYA1	GYA0	* Either a “0” or a “1” is acceptable
				< ---------- >				

9.8 GRAM Display Start Position Address Set ($\overline{C/D}$="1")

9.8.1 Horizontal Shift

This command specifies the address that a display pattern can be positioned to by **8 bits (00Hex to FFHex)**. DDRAM display area is not influenced. This is equivalent to an offset in the X-axis.

1st Byte:

MSB							LSB
0	1	1	1	*	*	*	*
< ---------- >							
Command Select							

* Either a "0" or a "1" is acceptable

2nd Byte:

MSB							LSB
XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0
< ---------- >							
GRAM Display Start Position Address							

9.8.2 Vertical Shift

This is equivalent to an offset Y-axis.

MSB							LSB
1	0	1	1	UD	S1	S0	*
< ---------- >				< ---------- >			
Command Select				Display Shift Data			

* Either a "0" or a "1" is acceptable

UD= "1": Display scrolled up.
UD= "0": Display scrolled down.
S1= "0", S0= "1": Display shift by 8 dots.
S1= "1", S0= "0": Display shift by 1 dot.
S1= "1", S0= "1": Display shift by 2 dots.

9.9 DDRAM Display Start Position Address Set ($\overline{C/D}$="1")

9.9.1 Horizontal Shift

1st Byte:

MSB							LSB
1	0	1	0	*	*	*	0
< ---------- >							*
Command Select							

* Either a "0" or a "1" is acceptable

* DDRAM Display Start Position Address

2nd Byte:

MSB							LSB
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
< ---------- >							
DDRAM Display Start Position Address							

* Either a "0" or a "1" is acceptable

This command specifies the address that a display pattern can be positioned to by **8bits** (00Hex to AFHex), and where the GRAM display area is not influenced. The Display start address is expressed as in the table that follows on the next page. A screen scrolls by setting a display start address with 00H and 01H one by one, and shifting in the horizontal direction.

9.9.2 Vertical Shift ($\overline{C/D}$="1")

MSB							LSB
1	0	0	1	UD	S1	S0	*
< ---------- >				< ---------- >			
Command Select				Display Shift Data			

* Either a "0" or a "1" is acceptable

Y-axis display shift of DDRAM display area is controlled.

UD= "1": Display scrolled up.
UD= "0": Display scrolled down.
S1= "0", S0= "1": Display shift by 8 dots.
S1= "1", S0= "0": Display shift by 1 dot.
S1= "1", S0= "1": Display shift by 2 dots.

9.10 Address Mode Set（$\overline{C/D}$="1"）

This command specifies the GRAM data write position address auto increment mode.

MSB							LSB	
1	0	0	0	*	IGX	IGY	*	* Either a “0” or a “1” is acceptable
< ---------- >				< ---------- >				
Command Select				Address Mode data				

IGX = "1" : X-Address +1(increment) when writing to GRAM.(It not affect to Y-Address.)
IGX = "0" : GRAM X address fixed mode
IGY = "1" : Y-Address +1(increment) when writing to GRAM.(It not affect to X-Address
IGY = "0" : GRAM Y address fixed mode.

9.11 Address Read （C/$\overline{D}$ ="1"）

This command reads both vertical and horizontal display start position addresses of DDRAM or GRAM *(Refer to sect. 8 - Display Screen on Page #4)*. On the parallel interface, the data bus outputs the address until $\overline{CSS}$ goes high after the READY signal goes active (Parallel #1:$\overline{RD}$=LOW, Parallel #2:R/$\overline{W}$=HIGH). The Data bus becomes an input when other. On the serial interface, TXD outputs the data from SCK rising after command is issued until the $\overline{CSS}$ goes high. Refer to 10.Interface on Page #17.

9.11.1 Vertical and Horizontal display start position address of character display (DDRAM)

1st Byte:

MSB							LSB	
1	1	0	1	1	0	*	*	* Either a “0” or a “1” is acceptable
< ---------- >								
Command Select								

	MSB							LSB	
2nd Byte:	VD6	VD5	VD4	VD3	VD2	VD1	VD0	HD8	(Read)
3rd Byte:	HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	(Read)
	< ---------- >								
	Vertical & Horizontal display start position address (DDRAM)								

VD0 to VD6: Vertical display start position address
HD0 to HD8: Horizontal display start position address

9.11.2 Vertical and Horizontal display start position address of graphic display (GRAM)

1st Byte:

MSB							LSB	
1	1	0	1	0	1	*	*	* Either a “0” or a “1” is acceptable
< ---------- >								
Command Select								

	MSB							LSB	
2nd Byte:	*	VG6	VG5	VG4	VG3	VG2	VG1	VG0	(Read)
3rd Byte:	HG7	HG6	HG5	HG4	HG3	HG2	HG1	HG0	(Read)
	< ---------- >								
	Vertical & Horizontal display start position address (GRAM)								

VG0 to VG6: Vertical display start position address
HG0 to HG7: Horizontal display start position address

9.12 ROM Transfer (C/$\overline{D}$="1")

This command copies the character font data in the Font ROM to the GRAM data write position address. Because transfer starts when RAM access completes, it is necessary to wait Min. 400uS. Also, it is not necessary to have the distinction of 16x16 dots, or 8x16 dots, and GRAM data write position address is automatically incremented.

1st Byte:

MSB							LSB	
1	1	1	0	*	*	*	*	* Either a “0” or a “1” is acceptable
< ---------- >								
Command Select								

2nd Byte:

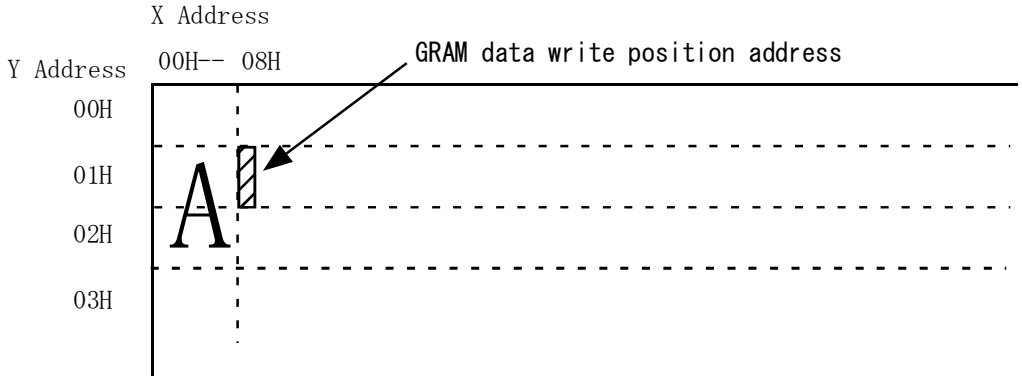
MSB							LSB
AD19	AD18	AD17	AD16	AD15	AD14	AD13	AD12
< ---------- >							
Upper address of character code							

3rd Byte:

MSB							LSB	
*	AD10	AD9	AD8	AD7	AD6	AD5	AD4	* Either a “0” or a “1” is acceptable
< ---------- >								
Lower address of character code								

Example: To show “A” (in 8x16 dot format) character as following.

GRAM data write position address is X=00H, Y=01H .
GRAM data write position address after copying character is X=08H, Y=01H.
(In case of 16x16 dots character: X=10H, Y=01H)



9.13 Data Write (C/$\overline{D}$="0")

9.13.1 Write to Character Display (DDRAM)

The DDRAM can be written to by setting a DDRAM data write position address with 2-byte writing. The 1st Byte is the upper address of character code, and the 2nd Byte is the lower address. For example, "A3Hex" is sent to the 1st Byte and "C1Hex" is sent to the 2nd Byte to display "A". At this time, the 2nd Byte is sent with the 1st Byte. An 8x16 dot font is also performed. Moreover, since an 8x16 dot font has 8 dots and 16 dots, a 16x16 dot font in a horizontal direction and a character is packed and displayed when a 16x16 dots font and a 8x16 dot font are mixed. The DRAM data write position moves to the right automatically by 8 dots in case of writing 8x16 dot font, and moves to the right automatically by 16dots in case of writing if 16x16dot font. Then, when it comes to right end, it returns to left end on same line after writing the font for the right end.

Refer to Character code table.

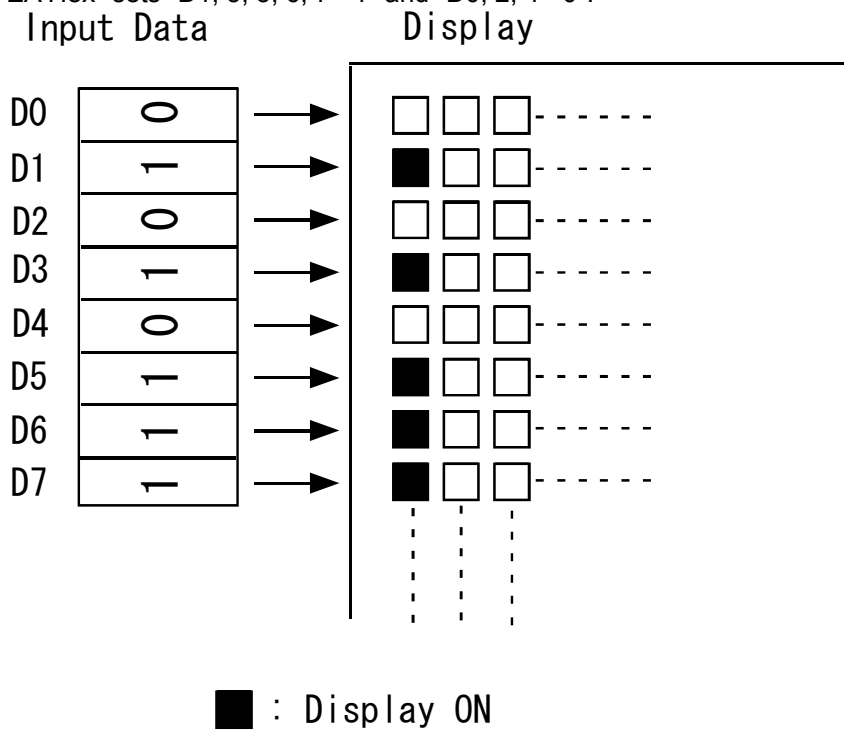
Font	Code
8x16 dots	2B00h – 2F7Fh
16x16 dots	A1A1h - FEFEh

The 16x16dots font of 2121h - 7E7Eh except the font of 2B00h - 2F7Fh is displayed as same as the font of A1A1h -FEFEh.

9.13.2 Write to Graphic Display(GRAM)

Can be written into GRAM by setting GRAM X or Y data write position address.

Example:
Writing "EA Hex" sets "D1, 3, 5, 6, 7 =1" and "D0, 2, 4 =0".

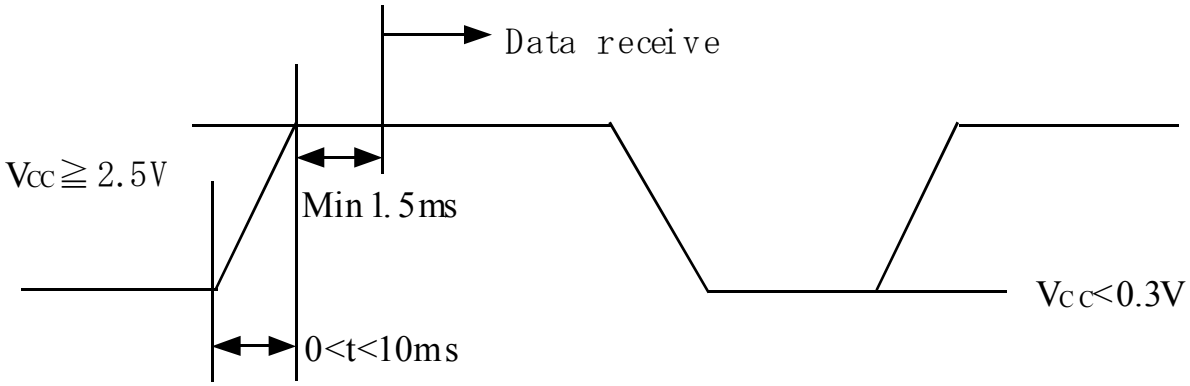


9.14 Default Status at Reset

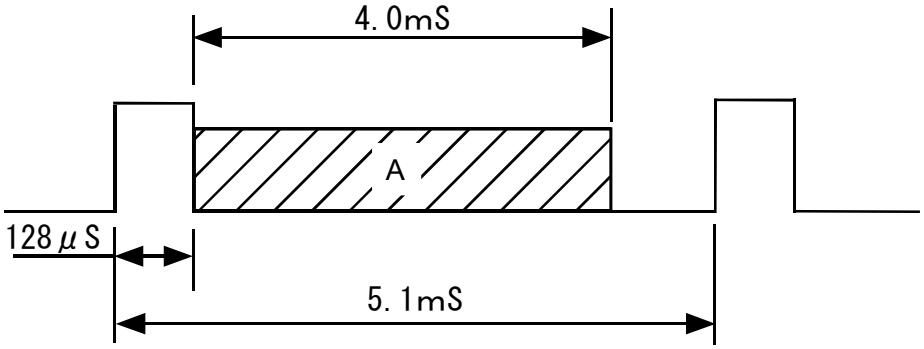
When the reset is applied, the display self-initializes into the following status:

GRAM Layer:	Layer (0)
Display ON/OFF:	Display (Off)
Display Area:	All DDRAM (Character display area)
Data write position address:	To set the “00” of DDRAM address
Display start position address:	To set the X=0 Y=0 of DDRAM address
Address Mode:	DDRAM increment mode
GRAM X-address:	Fixed mode
GRAM Y-address:	Fixed mode
Brightness Level:	100% Brightness

The following precautions should be observed at <u>power on</u>, and after a <u>reset:</u>
External Reset: After Vcc reaches 2.5V, the Reset level is "Low" for more than 1.5mS.
Power-Up: The following sequence occurs:



9.15 FRP (Frame Pulse)

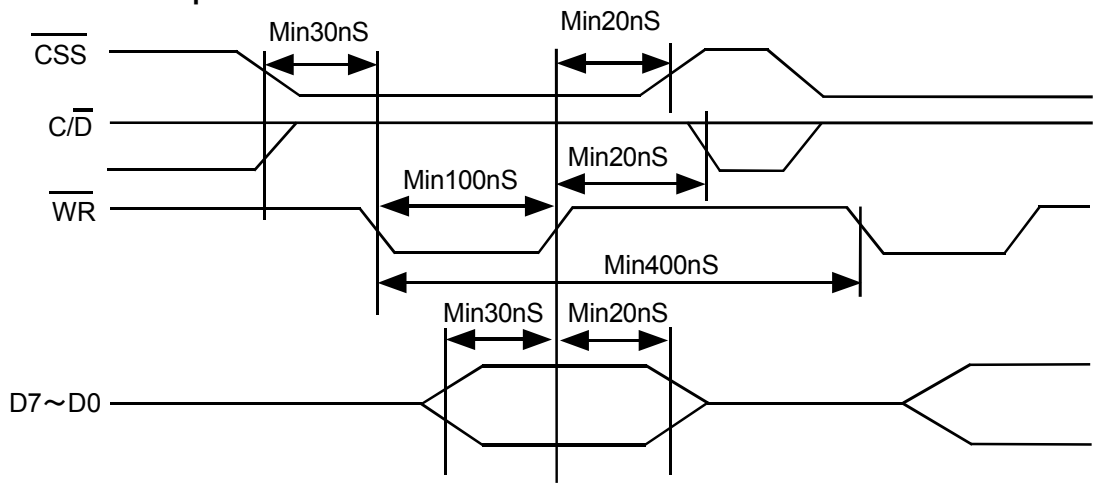


An FRP signal is triggered each time the display is refreshed by the module from its own memory. Smooth scrolling can be achieved by synchronizing the change of display start address with of the FRP signal from module. The area marked as “A” is optimal for writing commands.

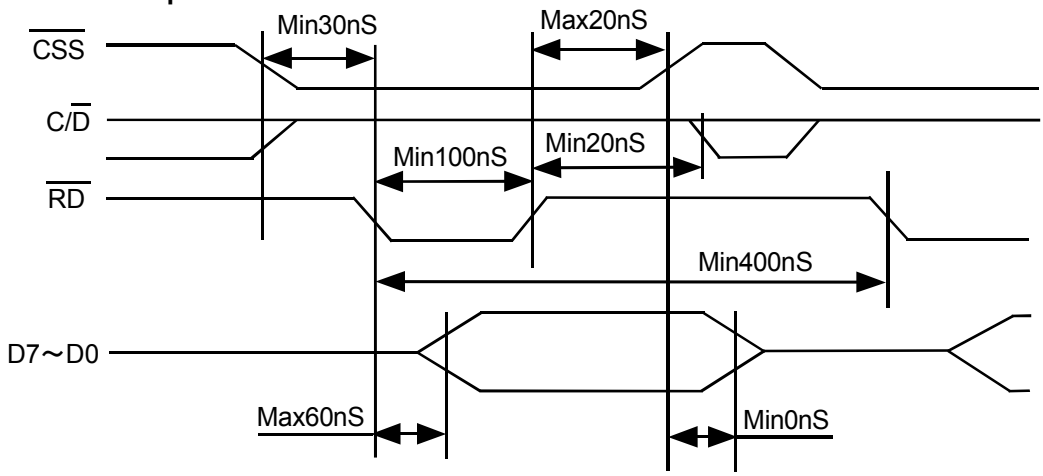
10. Interface

10.1 Parallel Interface (Parallel #1)

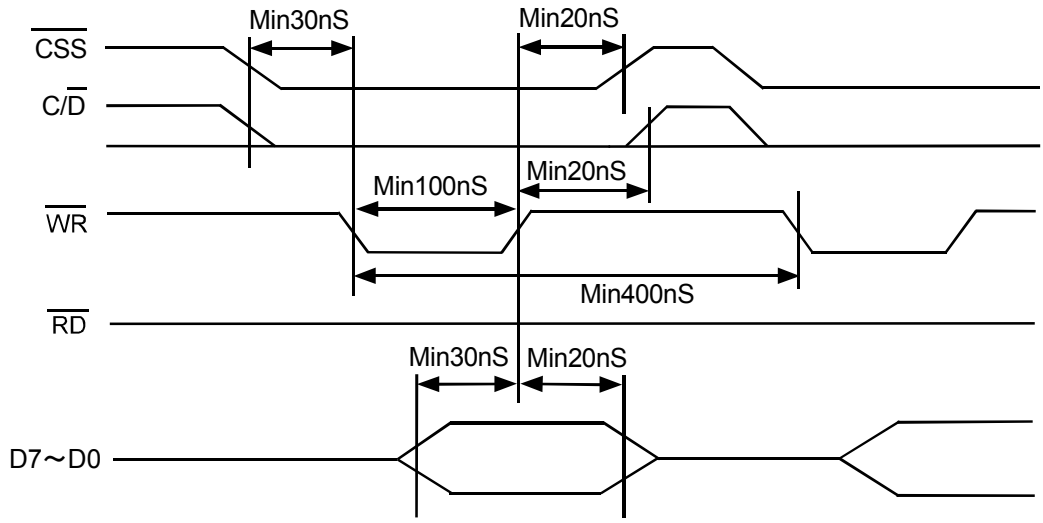
10.1.1 Command Write operation



10.1.2 Command Read operation

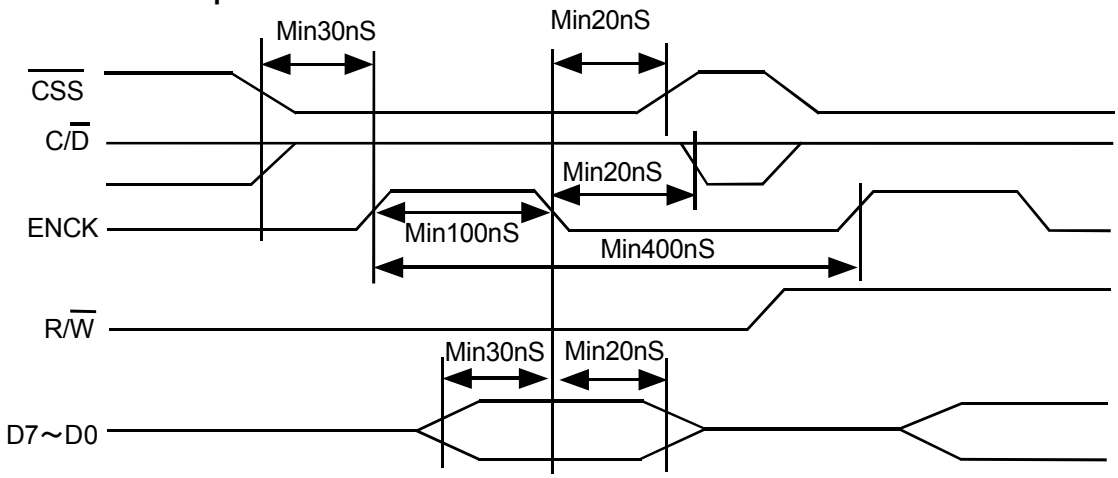


10.1.3 Data Write operation

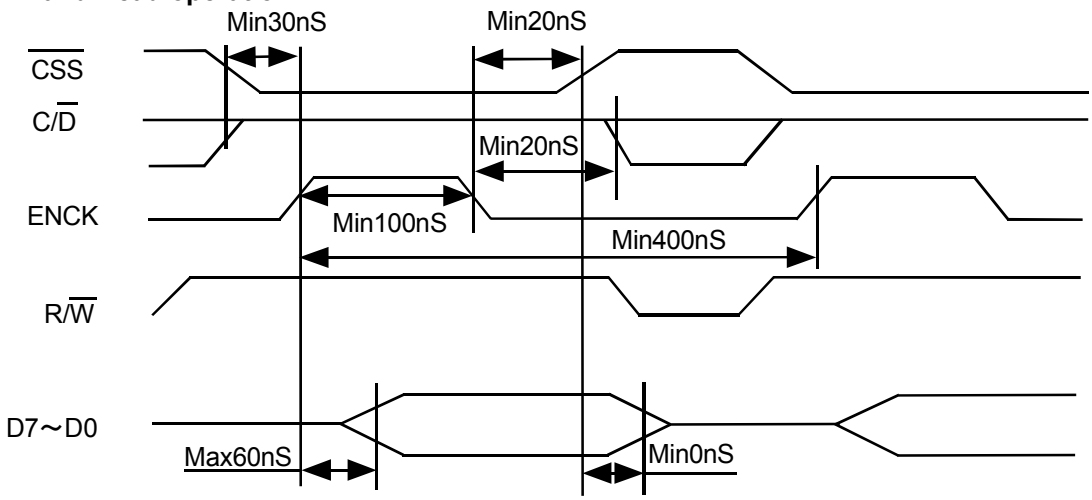


10.2 Parallel Interface(Parallel #2)

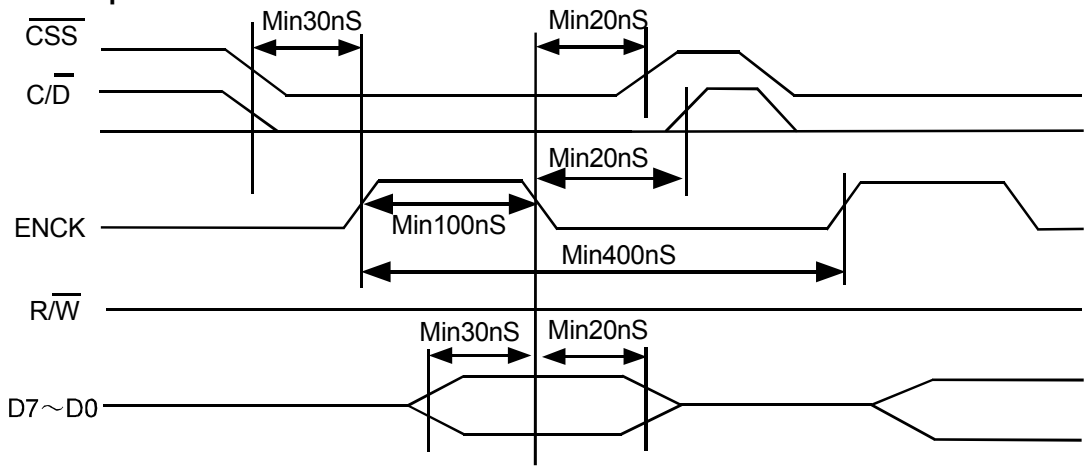
10.2.1 Command Write operation



10.2.2 Command Read operation

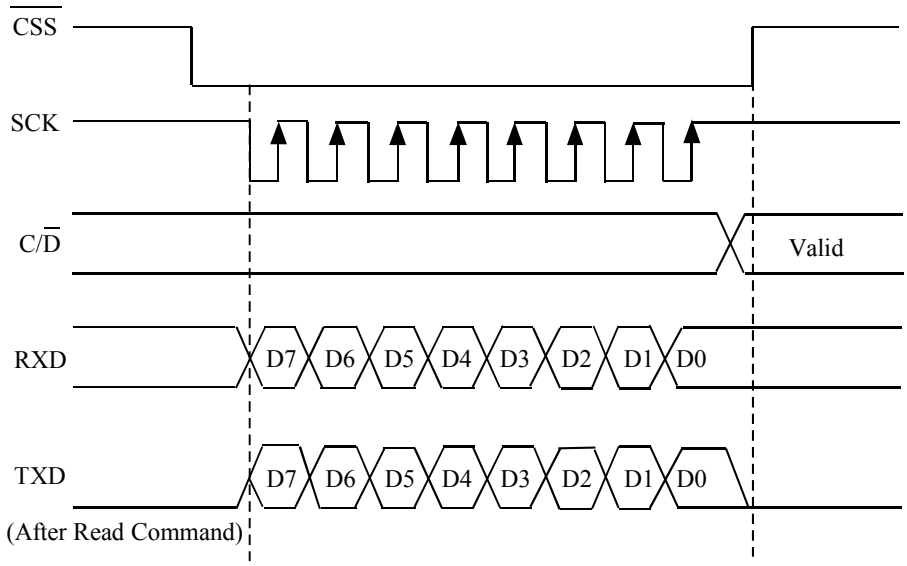


10.2.3 Data Write operation

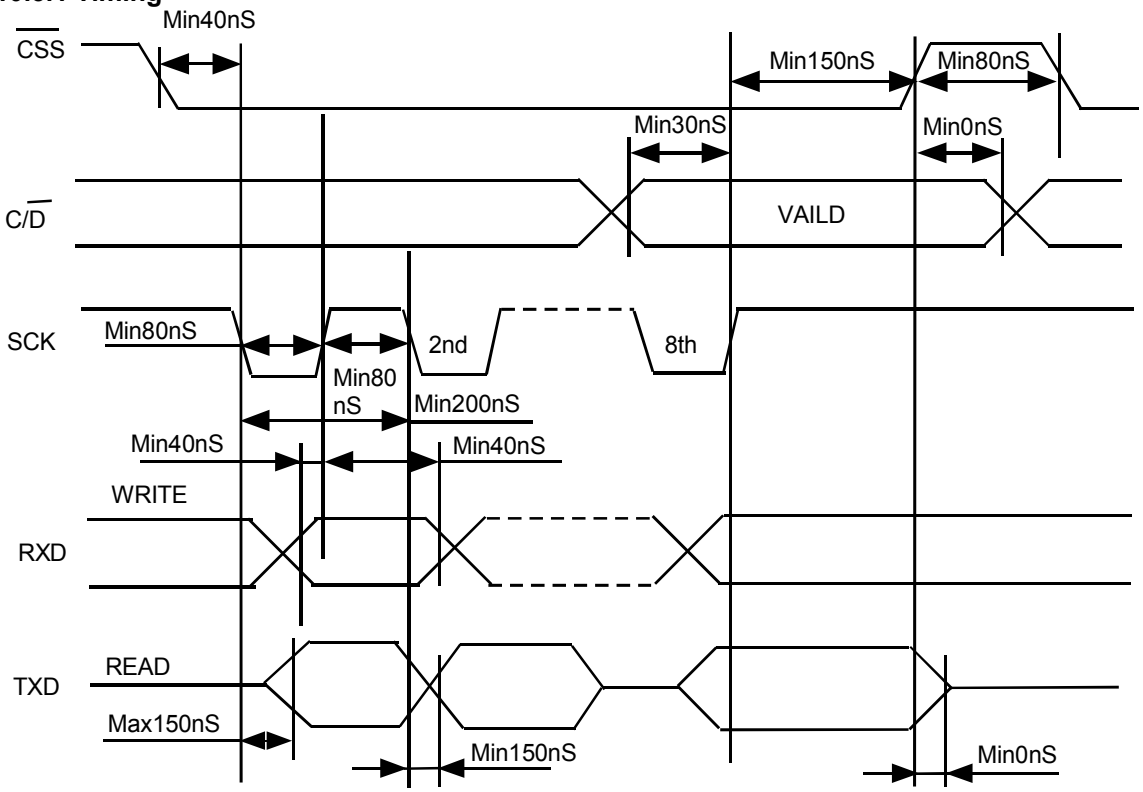


10.3 Serial Interface

To use the serial interface of this module, **(RXD,TXD and SCK)** will be activated by **CSS= "L"**.
The internal shift registers and counters will be reset by CSS= "H".
Serial data is transferred from MSB to LSB (D7->D0) on the rising edge of SCK. After the 8th clock edge, the data stream is converted to 8 bit parallel data.
Recognition of the RXD input as either data or command is determined by C/D on the 8th pulse SCK.



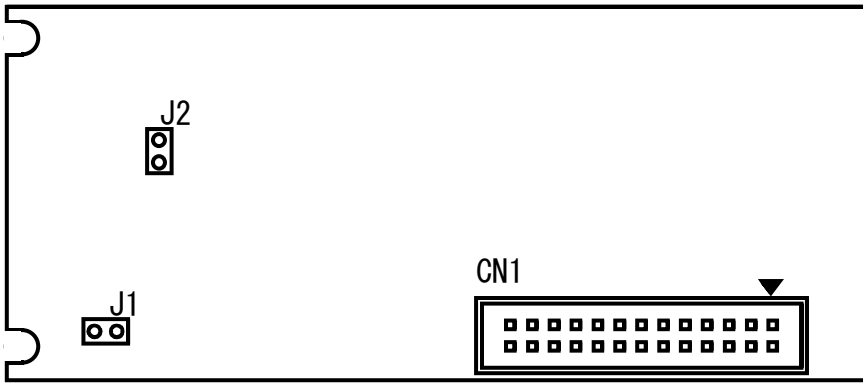
10.3.1 Timing



11. Jumper

11.1 Jumper Position

Component side of board



11.2 Jumper Setting (Must be done when power is **OFF**)

	J1	J2	Function
Interface	0	X	Serial Interface
	1	1	Parallel #1 Interface (Default)
	1	0	Parallel #2 Interface

1:Open 0:Short X: Open or Short

12. Pin Assignment *(See connector diagrams below)*

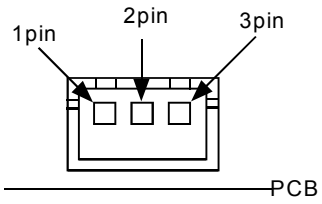
12.1 Signal Connection

Pin No.	Description		
	Parallel #1	Parallel #2	Serial
1	D7	D7	×
3	D6	D6	×
5	D5	D5	×
7	D4	D4	×
9	D3	D3	×
11	D2	D2	×
13	D1	D1	TXD
15	D0	D0	RXD
17	$\overline{WR}$	$\overline{R/W}$	×
19	$\overline{C/D}$	$\overline{C/D}$	$\overline{C/D}$
21	$\overline{RD}$	ENCK	SCK
23	$\overline{CSS}$	$\overline{CSS}$	$\overline{CSS}$
25	FRP	FRP	FRP

Pin No.	Description		
	Parallel #1	Parallel #2	Serial
2	GND	GND	GND
4	GND	GND	GND
6	GND	GND	GND
8	GND	GND	GND
10	GND	GND	GND
12	GND	GND	GND
14	GND	GND	GND
16	GND	GND	GND
18	GND	GND	GND
20	GND	GND	GND
22	GND	GND	GND
24	GND	GND	GND
26	$\overline{RESET}$	$\overline{RESET}$	$\overline{RESET}$

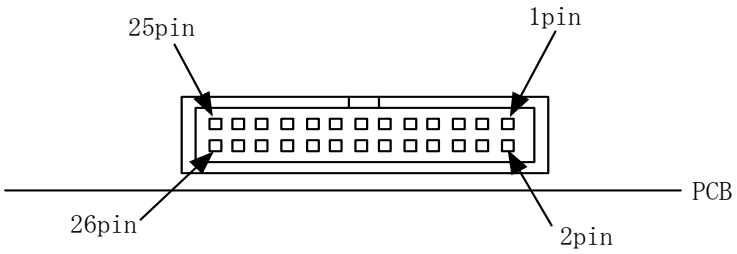
12.2 Power Connectors

Power Connector:
JST: B3B-XH-A or equivalent

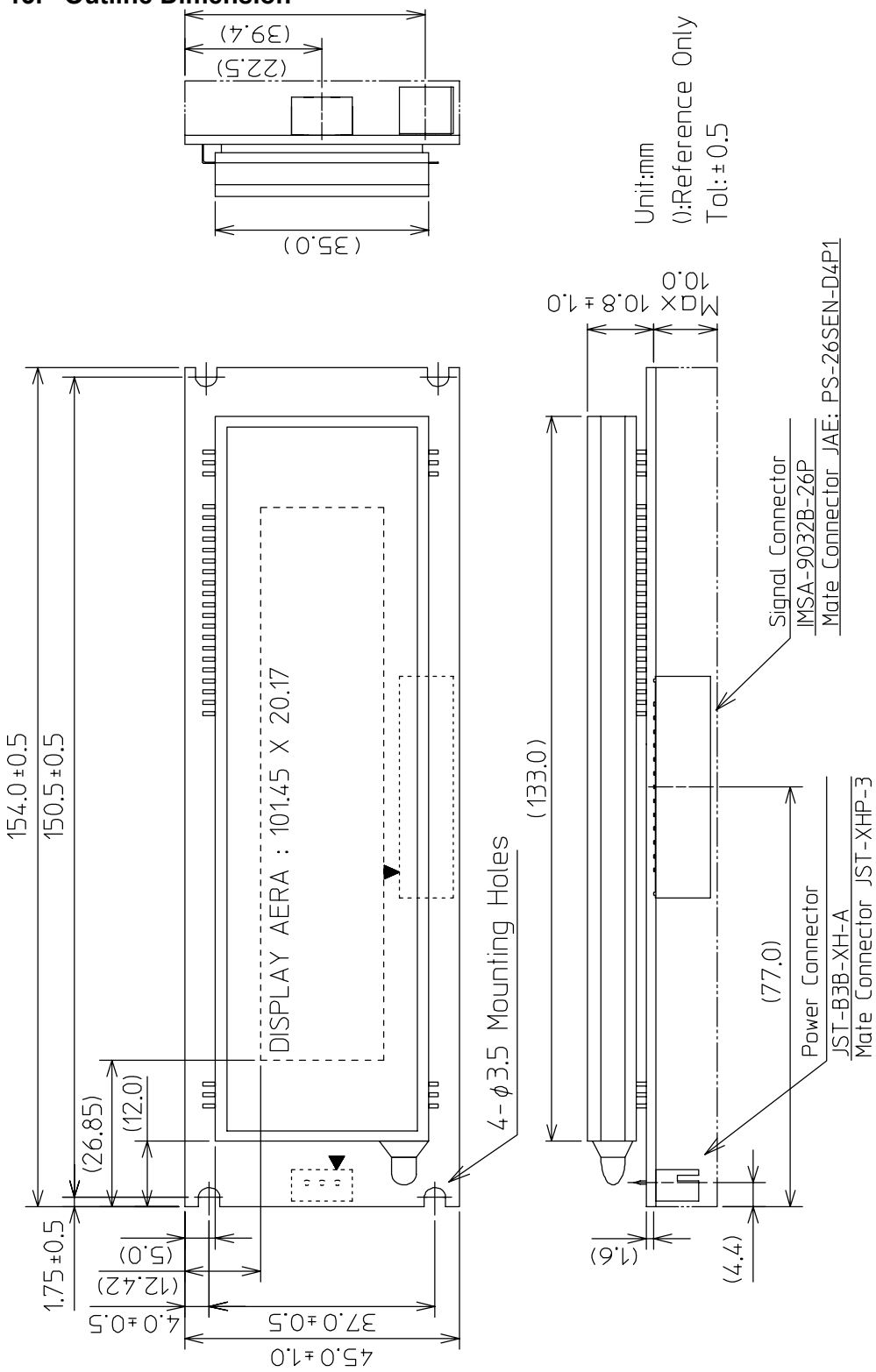


Pin No.	Description
1	Vcc
2	Test (Factory Only)
3	GND

Data Connector
IMSA: 9032B-26Por Equivalent



13. Outline Dimension



Notice for the Cautious Handling VFD Modules

Handling and Usage Precautions:
Please carefully follow the appropriate product application notes for proper usage, safety handling, and operation standards for maximum performance.

[VFD tubes are made of glass]

- Because the edges of the VFD glass-envelop are not smooth, it is necessary to handle carefully to avoid injuries to your hands
- Please avoid breaking the VFD glass-envelop to prevent injury from sharp glass particles.
- The tip of the exhaust pipe is fragile so avoid shock from impact.
- It is recommended to allow sufficient open space surrounding the exhaust pipe to avoid possible damage.
- Please design the PCB for the VFD-module within 0.3 mm warping tolerance to avoid any forces that may damage the display due to PCB distortion causing a breakdown of the electrical circuit leading to VFD failure.

[High voltage]

- Avoid touching conductive electrical parts, because the VFD-module uses high voltage exceeding 30～100 volts.
- Even when electric power is turned off, it may take more than one minute for the electrical current to discharge.

[Cable connection]

- Do not unplug the power and/or data cables of VFD-modules during operating condition because unrecoverable damage may result.
- Sending input signals to the VFD-module during a power off condition sometimes causes I/O port damage.
- It is recommended to use a 30 cm or shorter signal cable to prevent functional failures.

[Electrostatic charge]

- VFD-modules needs electrostatic free packaging and protection from electrostatic charges during handling and usage.

[Structure]

- During operation, VFD and VFD-modules generate heat. Please consider sufficient heat radiation dissipation using heat sink solutions.
- We prefer to use UL grade materials or components in conjunction with VFD-modules.
- Wrap and twist motion causes stress and may break VFDs & VFD modules. Please adhere to allowances within 0.3mm at the point of attachment.

[Power]

- Apply regulated power to the VFD-module within specified voltages to protect from failures.
- Because some VFD-modules may consume in rush current equal to twice the typical current at power-on timing, we recommend using a sufficient power capability and quick starting of the power regulator.
- VFD-module needs a specified voltage at the point of connection. Please use an adequate power cable to avoid a decrease in voltage. We also recommend inserting a power fuse for extra protection.

[Operating consideration]

- Illuminating phosphor will decrease in brightness during extended operation. If a fixed pattern illuminates for an extended period,(several hours), the phosphor efficiency will decrease compared to the non operating phosphor causing a non uniform brightness among pixels. Please consider programming the display patterns to use all phosphor segments evenly. Scrolling may be a consideration for a period of time to refresh the phosphor condition and improve even illumination to the pixels.
- We recommend using a signal cable 30cm or less to avoid some possible disturbances to the signal.

[Storage and operating environment]

- Please use VFD-modules under the recommended specified environmental conditions. Salty, sulfur and dusty environments may damage the VFD-module even during storage.

[Discard]

- Some VFDs contain a small amount of cadmium in the phosphor and lead in the solder. When discarding VFDs or VFD-modules, please adhere to governmental related laws or regulations.

[Others]

- Although the VFD-module is designed to be protected from electrical noise, please plan your circuitry to exclude as much noise as possible.
- Do not reconstruct or repair the VFD-module without our authorization. We cannot assure the quality or reliability of unauthorized reconstructed VFD-modules.

Notice:

・We do not authorize the use of any patents that may be inherent in these specifications.

・Neither whole nor partial copying of these specifications are permitted without our approval.
If necessary , please ask for assistance from our sales consultant.

・This product is not designed for military, aerospace, medical or other life-critical applications. If you choose to use this product for these applications, please ask us for prior consultation or we cannot take responsibility for problems that may occur.

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