

Noritake **itron**

Vacuum Fluorescent Display Module Specification

Model: GU256X32-800A

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Table of Contents

1. General Description	2
2. Absolute Maximum Ratings	2
3. Electrical Characteristics	2
4. Optical Specifications	2
5. Environmental Specifications	2
6. Description of Bus and Signals	3
6.1 Parallel Interface.....	3
6.2 Serial Interface.....	3
7. Block Diagram	3
8. Display Screen and Initialize Set	4
8.1 Graphic Display (GRAM).....	5
9. Function	7
9.1 Commands.....	7
9.2 Display On/Off (C/D= "1").....	8
9.3 Brightness Set (C/D= "1").....	8
9.4 Display Clear (C/D= "1") This command clears the GRAM	9
9.5 Display Area Set (C/D="1", only used for Initialize Set).....	10
9.6 GRAM Data Write position Address Set (Graphic Display) (C/D="1").....	11
9.6.1 GRAM Data Write Position X Address Set	11
9.6.2 GRAM Data Write Position Y Address Set.....	11
9.7 GRAM Display Start Position Address Set (C/D="1").....	11
9.7.1 Horizontal Shift.....	11
9.7.2 Vertical Shift.....	11
9.8 Address Mode Set (C/D="1")	12
9.9 Address Read (C/D="1")	12
9.10 Data Write to Graphic Display (GRAM) (C/D="0").....	13
9.11 Default Status at Reset.....	14
9.12 FRP (Frame Pulse).....	14
10. Interface	15
10.1 Parallel Interface (Parallel #1).....	15
10.1.1 Command Write operation.....	15
10.1.2 Command Read operation.....	15
10.1.3 Data Write operation	15
10.2 Parallel Interface(Parallel #2).....	16
10.2.1 Command Write operation.....	16
10.2.2 Command Read operation	16
10.2.3 Data Write operation.....	16
10.3 Serial Interface.....	17
10.3.1 Timing.....	17
11. Jumper	18
11.1 Jumper Position	18
11.2 Jumper Setting (Must be done when power is OFF)	18
12. Pin Assignment (See connector diagrams below)	19
12.1 Signal Connection	19
12.2 Connectors	19
13. Outline Dimension	20

1. General Description

- 1.1 Construction: A 256x32 dot BD-VFD single board display module consisting of an 8 bit micro-computer, and a DC/DC converter.
- 1.2 Features: Simultaneous display of graphic.
Flexible Display and Editing Functions.
Compact design due to the application of a BD-VFD tube.
- 1.3 Dimensions: See attached drawings

2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Input Voltage	VI	-0.5	—	Vcc +0.3	V	—
Power Supply Voltage	Vcc	0	—	6.5	VDC	—

3. Electrical Characteristics

Measurement Conditions: 25°C / Vcc=5.0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Input Voltage	"H"	VIH	4.0	—	—	VDC IIH= 2 μA
	"L"	VIL	—	—	1.0	
Logic Output Voltage	"H"	VOH	4.7	—	—	VDC IOH= - 300 μA
	"L"	VOL	—	—	0.3	
Reset Input Voltage	"H"	VRH	4.0	—	—	VDC IRH= 5 μA
	"L"	VRL	—	—	0.6	
Power Supply Voltage	Vcc	4.75	5.00	5.25	VDC	—
Power Supply Current	Icc	—	750	900	mA	VCC=+5V, All dots ON
		—	600	750		VCC=+5V, All dots OFF

Notes:

The rise time of **Vcc** should not exceed **100 ms**.
Icc may peak at power up may be more than twice the normal operating current

4. Optical Specifications

- Number of dots: 8192 (256x32)
- Display area: 166.25 mm x 20.65mm (X x Y)
- Dot size: 0.5 mm x 0.5 mm (X x Y)
- Dot pitch: 0.65 mm x 0.65 mm (X x Y)
- Luminance: 350cd/m² (Min.)
- Color of illumination: Green (Blue Green)

5. Environmental Specifications

- Operating temperature: -40 to +85°C
- Storage temperature: -40 to +85°C
- Storage humidity: 20 to 80 % R.H.(Non Condensation)
- Vibration: 10-55-10Hz, all amplitude 1mm, 30Min., X-Y-Z (Non operating)
- Shock: 539m/s² 10mS (Non operating)

6. Description of Bus and Signals

This module has serial and 2 types of parallel interface.

Type of interface can be selected by jumper settings. Refer to 11 on page # 18 for details

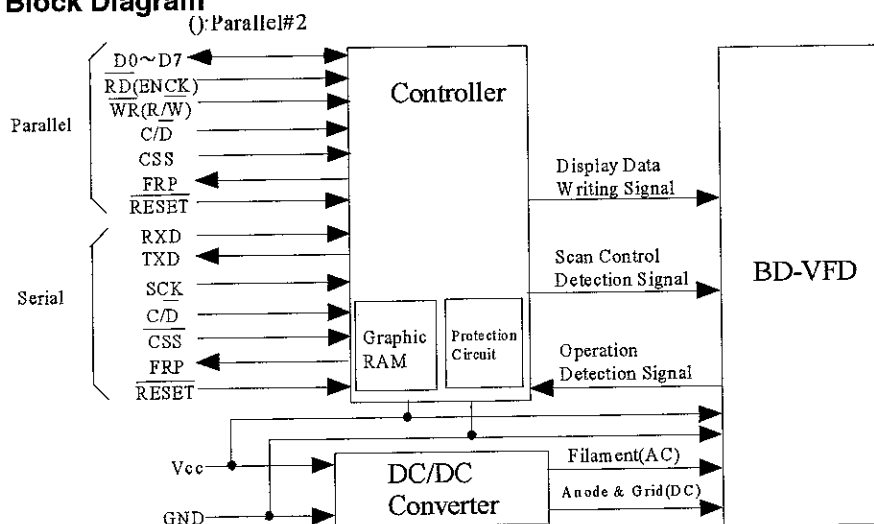
6.1 Parallel Interface

Data Line	Function
D0 ~ D7	Data Bus (Input / Output)
WR (R/W)	Parallel #1: Write Signal, Parallel #2: R/W (Input)
RD (ENCK)	Parallel #1: Read Signal, Parallel #2: ENCK (Input)
CSS	Chip Select (Input)
C/D	Command / Data Select Signal (Input) C/D = "1" ... Command C/D = "0" ... Data
FRP	Frame Pulse Signal (Output)
RESET	RESET="0" ... Reset (Input)
Vcc	Power Supply
GND	Ground

6.2 Serial Interface

Data Line	Function
RXD	Serial Input
TXD	Serial Output
SCK	Clock (Input)
CSS	Chip Select (Input)
C/D	Command / Data Select Signal (Input) C/D = "1" ... Command C/D = "0" ... Data
FRP	Frame Pulse Signal (Output)
RESET	RESET="0" ... Reset (Input) Active Low
Vcc	Power Supply
GND	Ground

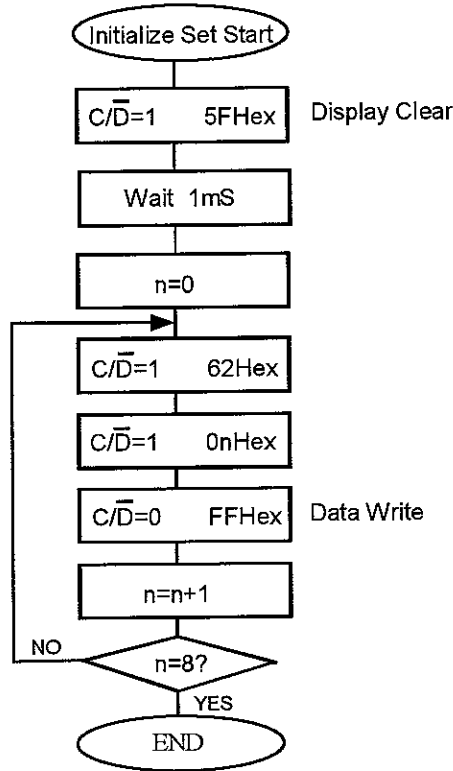
7. Block Diagram



8. Display Screen and Initialize Set

The Display screen consists of 8,192 dots arranged as 256 by 32 dots. It is divided into 64 display area blocks of 16 by 8 dots each. Each display area block can be assigned to GRAM (Graphic mode) or DDRAM (Character mode) by the Display Area Set command. (9.5 Page #10)

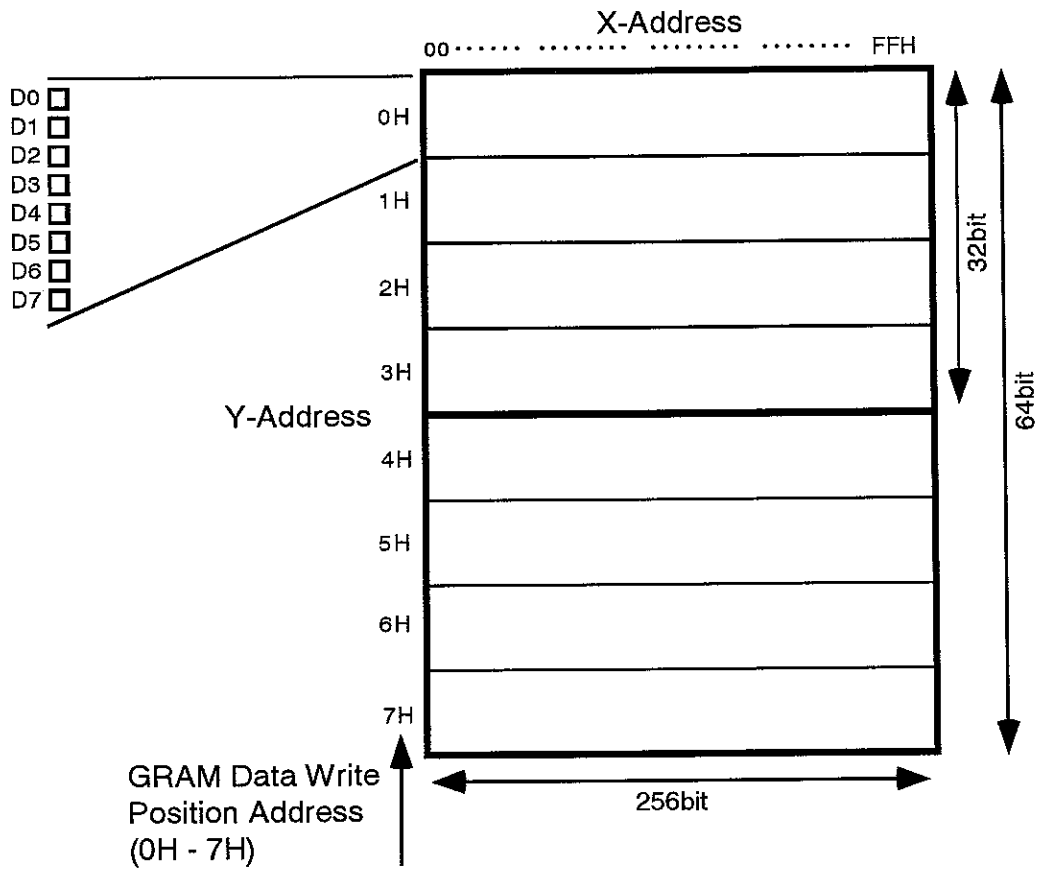
But, this is the version which has no Font ROM. Therefore, DDRAM is not available, all of display area block must be assigned to GRAM as the initialize setting, and this must be done when the module is powered up and also every time the reset is applied, because all display area blocks are set to DDRAM area as default setting. Initialize sequence is as follows;



8.1 Graphic Display (GRAM)

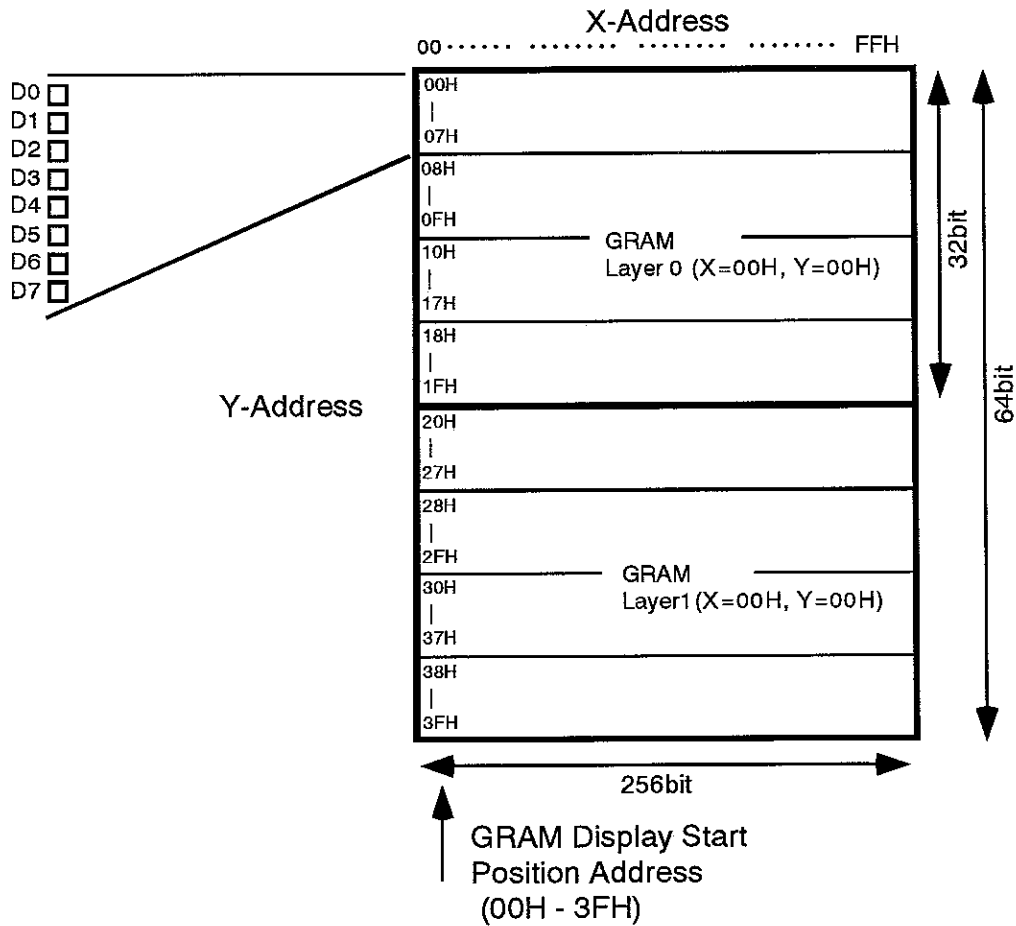
GRAM consists of 16,384 bits arranged in 256 by 64 bit blocks with access is structured as 8 bits of vertical data. The detail of GRAM is as follows:

GRAM Data Write Position Address



8.1 Cont'd

GRAM Display Start Position Address



This module has 2 layers - Layer 0 and Layer 1. Each layer in this display consists of 256 by 32 dots. Display merging using these 2 layers can be done with the Display ON/OFF command. Refer to 9.2 on page # 8 for details.

Layer 0 has an area of 256x32 dots that starts from top left point defined by the GRAM Start Position Address. The area of Layer 1 is the next 256x32 dots.

When the value of the GRAM Start Position Address X overflow = FFH, the next position goes to 00H. When the value of the GRAM Start Position Address Y overflow = 3FH, the next position goes to 00H.

For example:

If the GRAM Start Position Address is set as X=02H, Y=08H, the area of Layer0 is as follows;

X=02H,03H,04H... FFH,00H,01H
Y=08H,09H.....26H, 27H

In this case, the area of Layer1 is as follows;

X=02H,03H,04H.... FFH,00H,01H
Y=28H,29H06H,07H

9. Function
9.1 Commands

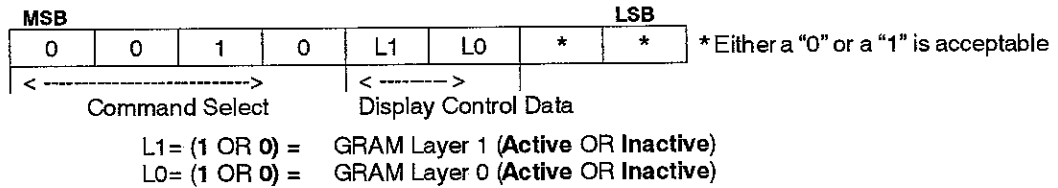
Command	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Comments	
Display ON/OFF	1	0	0	1	0	L1	L0	*	*	1st Byte	Display ON/OFF Control, 2 Byte Command
		0	GS	0	GRV	AND	EXOR	*	*	2nd Byte	
Brightness Set	1	0	1	0	0	BW3	BW2	BW1	BW0	1 Byte	1 Byte Command
Display Clear	1	0	1	0	1	G1C	G0C	1	HM	1 Byte	1 Byte Command
Display Area SET (Initialize)	1	0	1	1	0	0	0	1	0	1st Byte	Display Area is assigned 3 Byte Command
		0	0	0	0	0	(A2 - A0)			2nd Byte	
	0	1	1	1	1	1	1	1	1	3rd Byte	
Data Write Position Address Set	1	0	1	1	0	0	1	0	*	1st Byte	Graphic Display X-Address Set, 2 Byte Command
		GRAM X-Address (GXA7~GXA0)								2nd Byte	
Data Write Position Address Set	1	0	1	1	0	0	0	0	*	1st Byte	Graphic Address Y-Address Set, 2-Byte Command
		*	*	*	*	0	GXA2	GXA1	GXA0	2nd Byte	
Display Start Position Address Set	1	0	1	1	1	*	*	*	*	1st Byte	Graphic Display Horizontal Shift, 2-Byte Command
		XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	2nd Byte	
Display Start Position Address Set	1	1	0	1	1	UD	S1	S0	*	1 Byte	Graphic Display Vertical Shift, 1 Byte Command
Address Mode Set	1	1	0	0	0	*	IGX	IGY	*	1 Byte	Address Increment, 1 Byte Command
Address Read	1	1	1	0	1	0	1	*	*	1st Byte	Graphic Display (GRAM) Horizontal And Vertical Display Start Address, 3 Byte Command
		*	VG6	VG5	VG4	VG3	VG2	VG1	VG0	2nd Byte	
		HG7	HG6	HG5	HG4	HG3	HG2	HG1	HG0	3rd Byte	
Data Write	0	WRITE DATA									Writes Data Graphic Data is 1 Byte

* Either a "0" or a "1" is acceptable

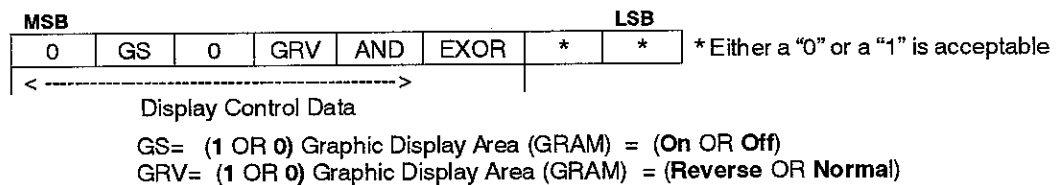
9.2 Display On/Off (C/D= "1")

The GRAM Layer is selected with the 1st Byte of data. DDRAM (On/Off), GRAM (On/Off), DDRAM (reverse or normal modes), GRAM (reverse or normal modes) and display merge are selected by the 2nd Byte. Reverse mode toggles the representation of green in the foreground and black in the background to the exact opposite - green to black and black to the foreground. This is similar to the concept of reverse video.

1st Byte:



2nd Byte:



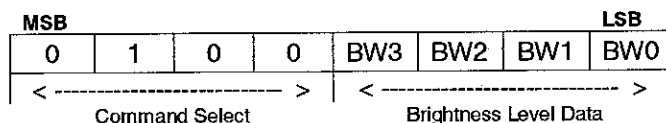
DS="0", GS="0": Stand-by mode

1st Byte		2nd Byte		Action
L1	L0	AND	EXOR	
*	*	1	*	AND Display of Layer 1 & 0
*	*	0	1	EXOR Display of Layer 1 & 0
1	1	0	0	OR Display of Layer 1 & 0
1	0	0	0	Only Layer1 selected for display
0	1	0	0	Only Layer0 selected for display
0	0	0	0	Graphic Display Off

* Either a "0" or a "1" is acceptable

9.3 Brightness Set (C/D= "1")

The Brightness level of the display screen can be scaled by the following four bit control. Please note that the brightness is consistent across the illuminated pixels. There is no scaling of individual pixels. The display self-initializes to 100% brightness.



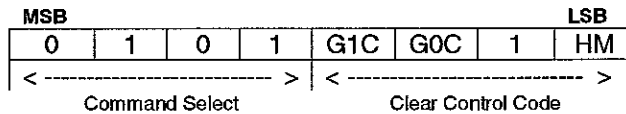
9.3 Cont'd

Brightness levels are set by the following:

BW3	BW2	BW1	BW0	Brightness Level
0	0	0	0	100%(Light)
0	0	0	1	94%
0	0	1	0	87%
0	0	1	1	81%
0	1	0	0	75%
0	1	0	1	69%
0	1	1	0	62%
0	1	1	1	56%
1	0	0	0	50%
1	0	0	1	44%
1	0	1	0	37%
1	0	1	1	31%
1	1	0	0	25%
1	1	0	1	19%
1	1	1	0	12%
1	1	1	1	6%(Dark)

9.4 Display Clear (C/D= "1") This command clears the GRAM

This command should always be applied at power on or reset. In the period of 1mS following the issue of this command, the module requires internal processing and does not accept any commands.



To clear the GRAM area, G1C or G0C bit must be asserted. By asserting HM bit, both data write position address and display start position address which selected by G1C, G0C, also be reset.

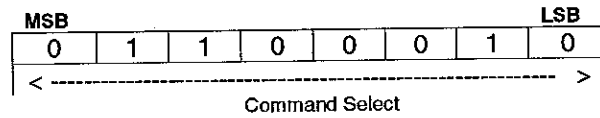
HM = (1 or 0) equals (Initialize data write position address and display start position address or Not initialize)

- G1C= (1 or 0) equals (GRAM area 1 is cleared or GRAM area 1 not cleared)
- G0C= (1 or 0) equals (GRAM area 0 cleared or GRAM area 0 not cleared)
- GRAM area 1: X= 00H-FFH, Y=0H – 3H (Display data write position address)
- GRAM area 2: X= 00H-FFH, Y=4H – 7H (Display data write position address)

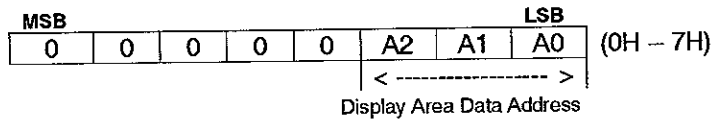
9.5 Display Area Set ($\overline{C/D}="1"$, only used for Initialize Set)

This command sets the display area block as Graphic Display (GRAM) or Character display (DDRAM). But, this is version which has no Font ROM Therefore, DDRAM is not available, all of display area block must be assigned to GRAM as the initialize setting, and this must be done when the module is powered up and also every time the reset is applied. Setup is performed by 3-byte command

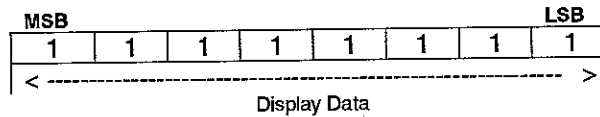
1st Byte: ($\overline{C/D}="1"$) Command Select



2nd Byte: ($\overline{C/D}="1"$) Display Area Data Address Select

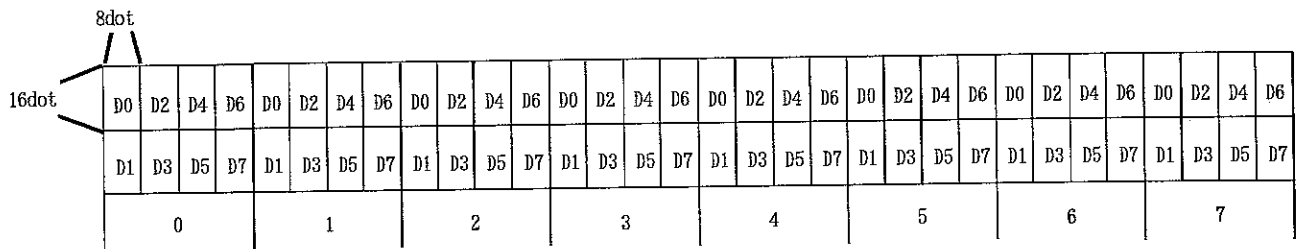


3rd Byte: ($\overline{C/D}="0"$) Display Area Block Select



D0 to D7 = "1": Graphic Display (GRAM)
D0 to D7 = "0": Character Display (DDRAM, **Not available**)

Display area block is assigned as follows on a screen.



Display Area Data Address (0 ~ 7H)

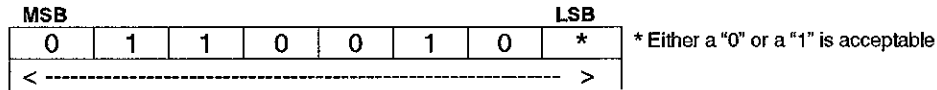
9.6 GRAM Data Write position Address Set (Graphic Display) ($\overline{C/D}$ ="1")

This command specifies both X & Y data write position address.

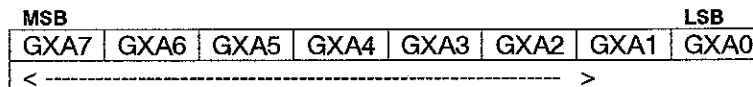
9.6.1 GRAM Data Write Position X Address Set

Data write position X address of GRAM expressed with 8 bits (00HexFFHex) is specified.
Refer to 8.1 Graphic Display (GRAM) on Page #5.

1st Byte: Command Select



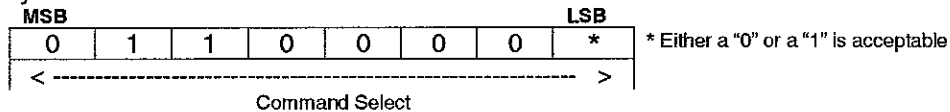
2nd Byte: GRAM Data Write Position X Address



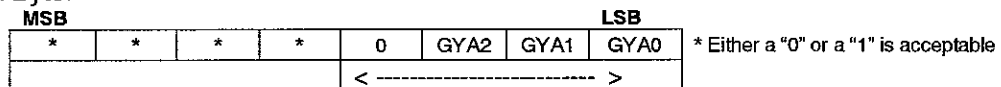
9.6.2 GRAM Data Write Position Y Address Set

Data write position Y address of GRAM expressed with 4 bits (0Hex7Hex) is specified.

1st Byte:



2nd Byte:

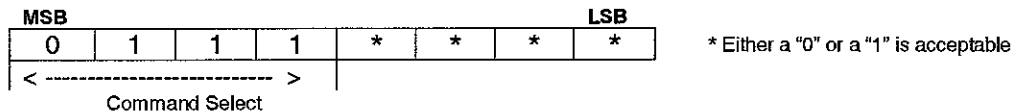


9.7 GRAM Display Start Position Address Set ($\overline{C/D}$ ="1")

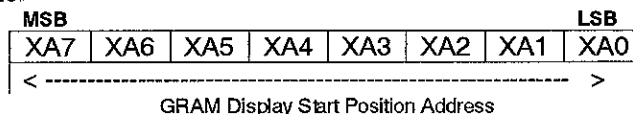
9.7.1 Horizontal Shift

This command specifies the address that a display pattern can be positioned to by **8 bits (00Hex to FFHex)**. This is equivalent to an offset in the X-axis.

1st Byte:

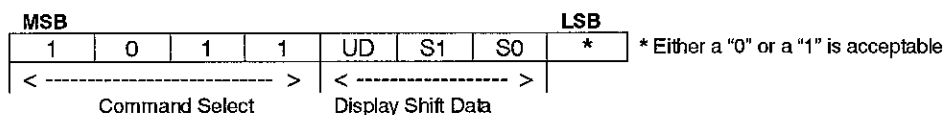


2nd Byte:



9.7.2 Vertical Shift

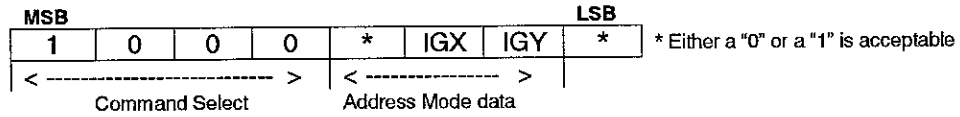
This is equivalent to an offset Y-axis.



UD= "1": Display scrolled up.
 UD= "0": Display scrolled down.
 S1= "0", S0= "1": Display shift by 8 dots.
 S1= "1", S0= "0": Display shift by 1 dot.
 S1= "1", S0= "1": Display shift by 2 dots.

9.8 Address Mode Set ($\overline{C/D}="1"$)

This command specifies the GRAM data write position address auto increment mode.

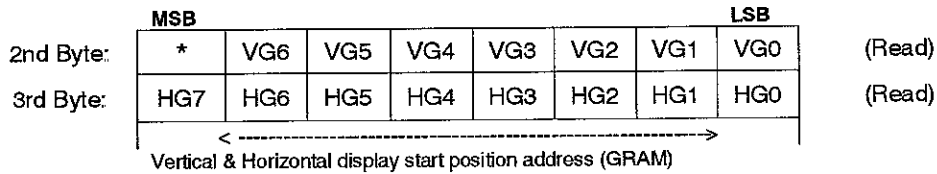
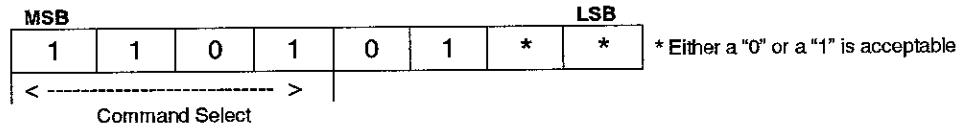


IGX = "1" : X-Address +1 (increment) when writing to GRAM. (It not affect to Y-Address.)
 IGX = "0" : GRAM X address fixed mode
 IGY = "1" : Y-Address +1 (increment) when writing to GRAM. (It not affect to X-Address)
 IGY = "0" : GRAM Y address fixed mode.

9.9 Address Read ($\overline{C/D}="1"$)

This command reads both vertical and horizontal display start position addresses of GRAM (Refer to sect. 8 - Display Screen and Initialize set on Page # 4). On the parallel interface, the data bus outputs the address until \overline{CSS} goes high after the \overline{READY} signal goes active (Parallel #1: $\overline{RD}=\text{LOW}$, Parallel #2: $\overline{R/W}=\text{HIGH}$). The Data bus becomes an input when other. On the serial interface, TXD outputs the data from SCK rising after command is issued until the \overline{CSS} goes high. Refer to 10 Interface on Page #15.

1st Byte:



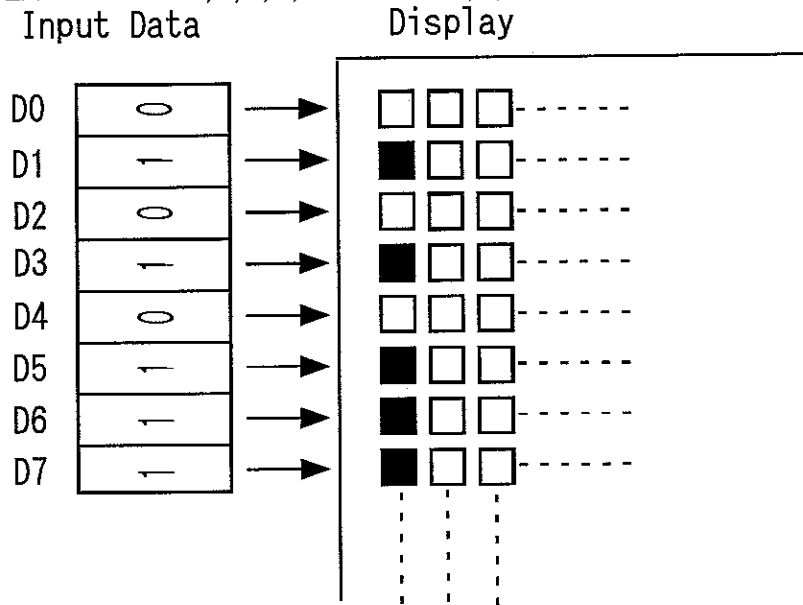
VG0 to VG6: Vertical display start position address
 HG0 to HG7: Horizontal display start position address

9.10 Data Write to Graphic Display (GRAM) ($\overline{C/D} = "0"$)

Can be written into GRAM by setting GRAM X or Y data write position address

Example:

Writing "EA Hex" sets "D1, 3, 5, 6, 7 = 1" and "D0, 2, 4 = 0".



■ : Display ON

9.11 Default Status at Reset

When the reset is applied, the display self-initializes into the following status:

GRAM Layer:	Layer (0)
Display ON/OFF:	Display (Off)
Display Area:	All DDRAM (Character display area)

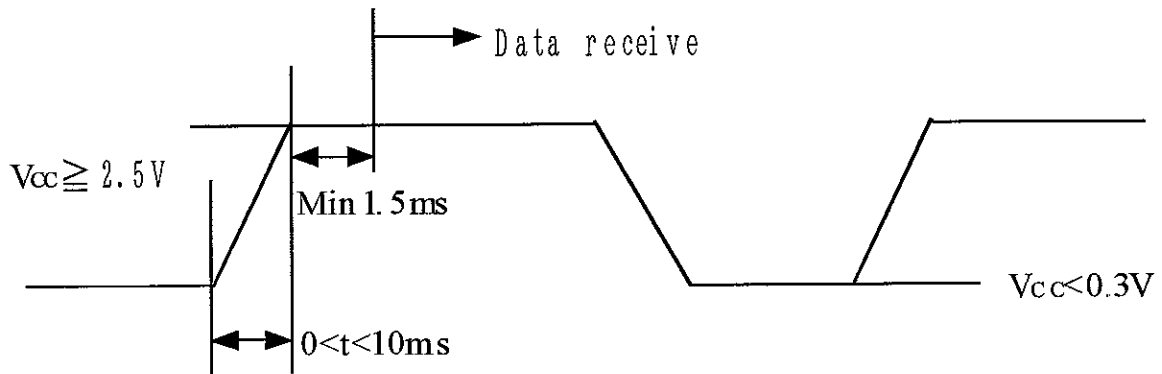
All of display area block must be assigned to GRAM again as the initialize setting after reset is applied because DDRAM is not available.

GRAM X-address:	Fixed mode
GRAM Y-address:	Fixed mode
Brightness Level:	100% Brightness

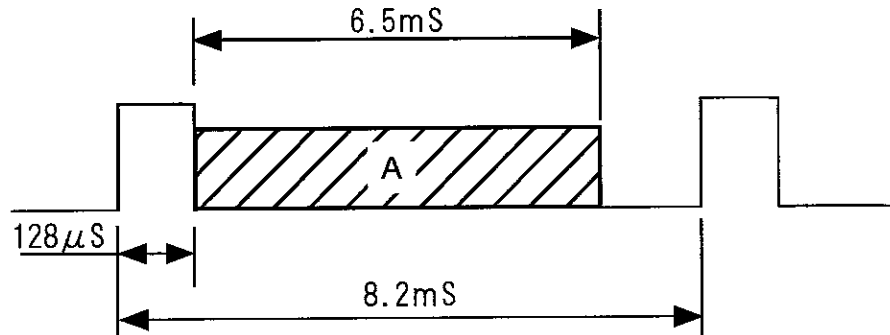
The following precautions should be observed at power on, and after a reset:

External Reset: After V_{cc} reaches 2.5V, the Reset level is "Low" for more than 1.5mS.

Power-Up: The following sequence occurs:



9.12 FRP (Frame Pulse)

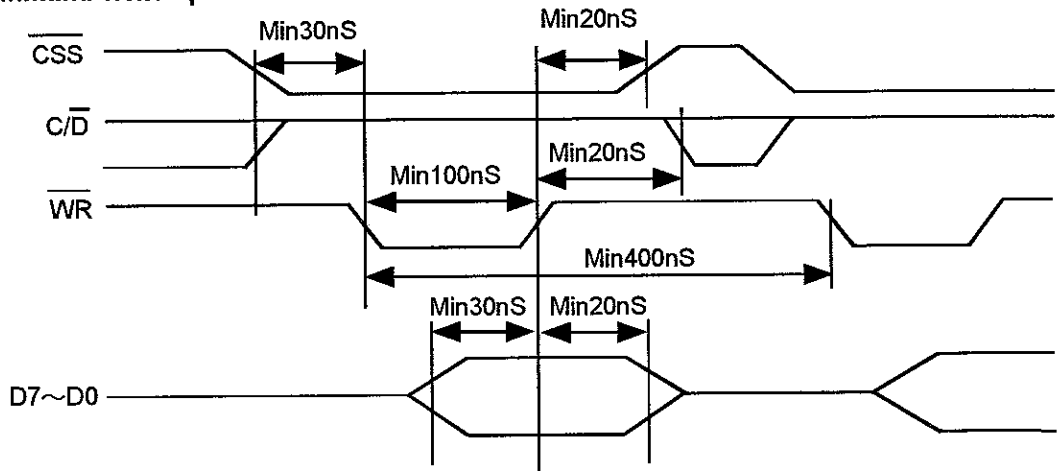


An FRP signal is triggered each time the display is refreshed by the module from its own memory. Smooth scrolling can be achieved by synchronizing the change of display start address with that of the FRP signal from the module. The area marked as "A" is optimal for writing commands.

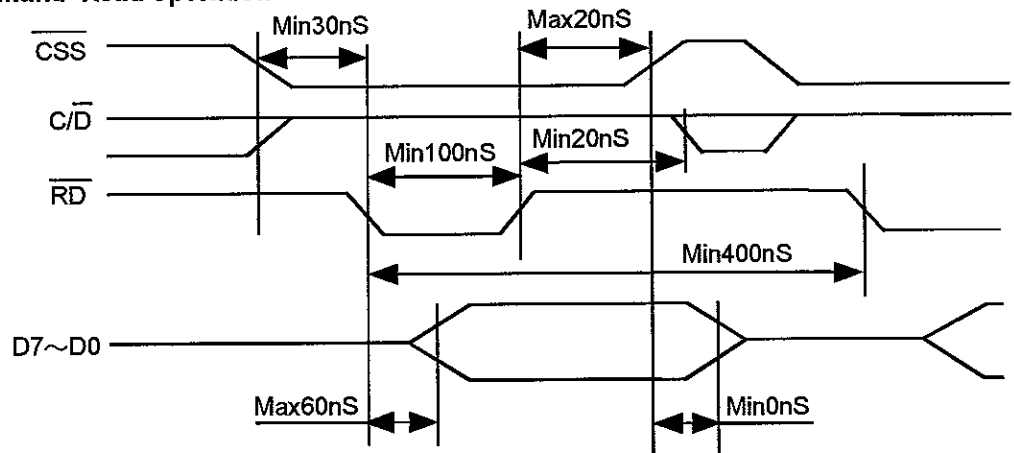
10. Interface

10.1 Parallel Interface (Parallel #1)

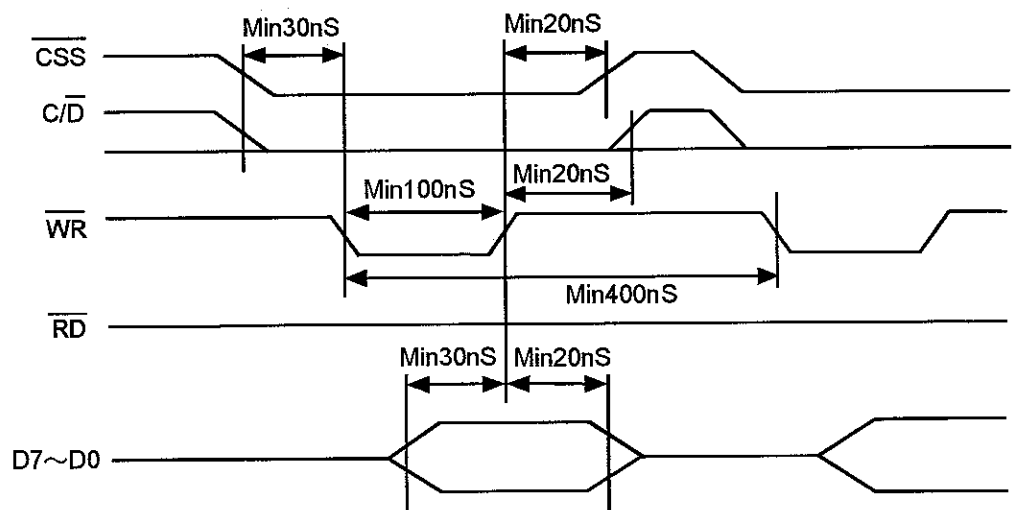
10.1.1 Command Write operation



10.1.2 Command Read operation

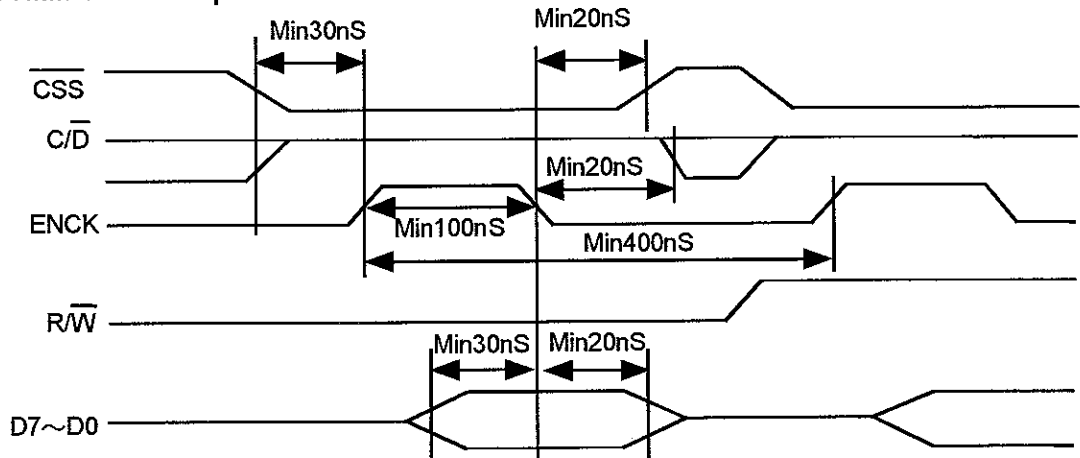


10.1.3 Data Write operation

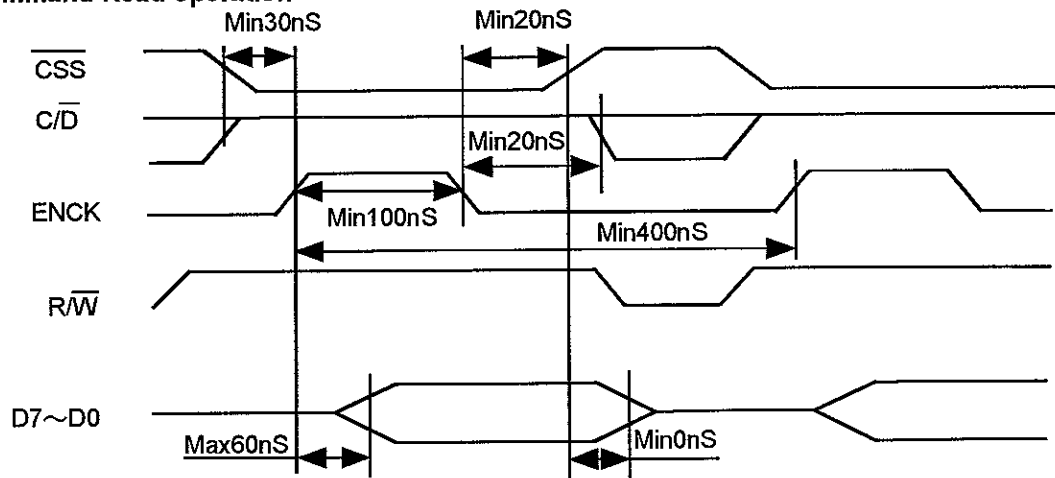


10.2 Parallel Interface(Parallel #2)

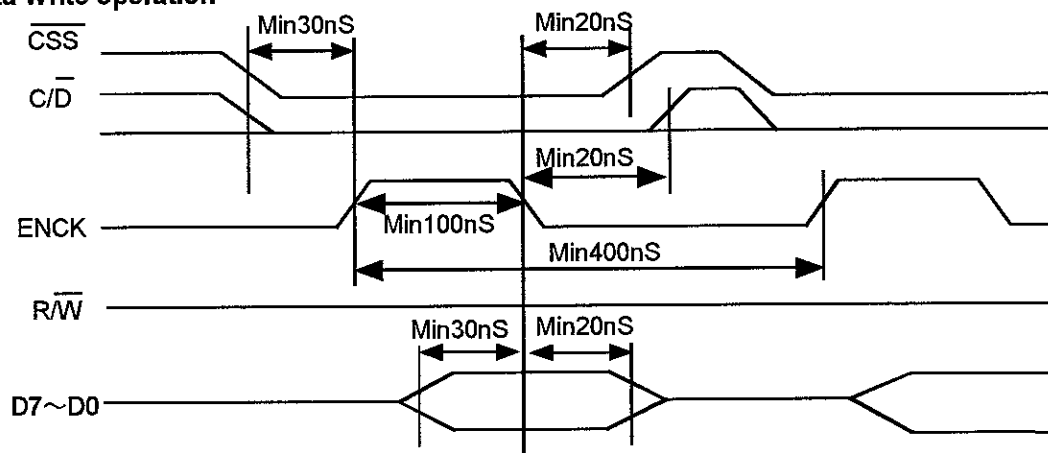
10.2.1 Command Write operation



10.2.2 Command Read operation

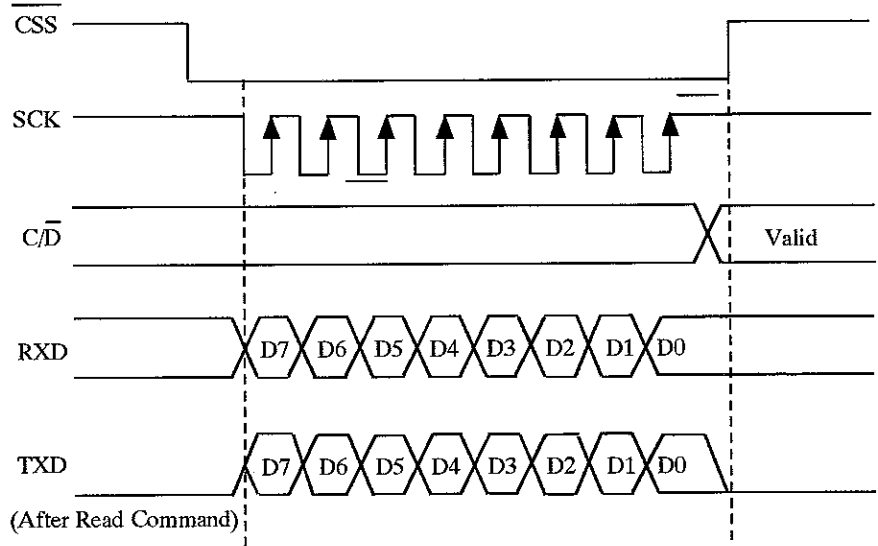


10.2.3 Data Write operation

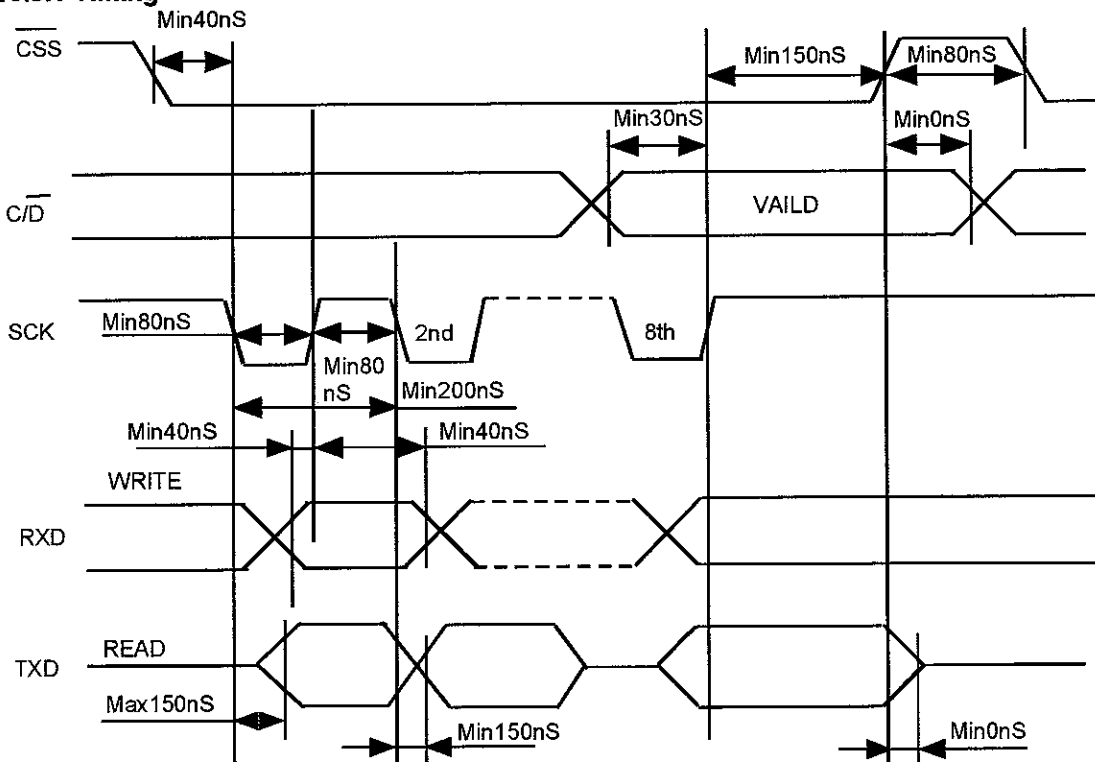


10.3 Serial Interface

To use the serial interface of this module, (RXD, TXD and SCK) will be activated by CSS= "L". The internal shift registers and counters will be reset by CSS= "H". Serial data is transferred from MSB to LSB (D7->D0) on the rising edge of SCK. After the 8th clock edge, the data stream is converted to 8 bit parallel data. Recognition of the RXD input as either data or command is determined by C/D on the 8th pulse SCK.



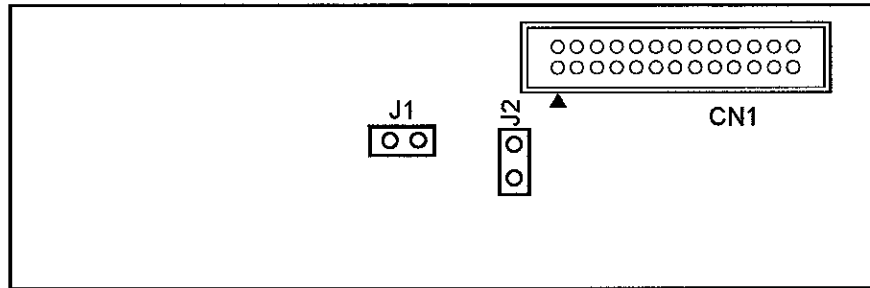
10.3.1 Timing



11. Jumper

11.1 Jumper Position

Component side of board



11.2 Jumper Setting (Must be done when power is OFF)

	J1	J2	Function
Interface	0	X	Serial Interface
	1	1	Parallel #1 Interface (Default)
	1	0	Parallel #2 Interface

1:Open

0:Short

X: Open or Short

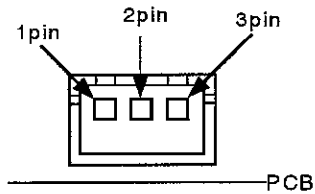
12. Pin Assignment *(See connector diagrams below)*

12.1 Signal Connection

Pin No.	Description		
	Parallel #1	Parallel #2	Serial
1	D7	D7	X
3	D6	D6	X
5	D5	D5	X
7	D4	D4	X
9	D3	D3	X
11	D2	D2	X
13	D1	D1	TXD
15	D0	D0	RXD
17	\overline{WR}	$\overline{R/W}$	X
19	$\overline{C/D}$	$\overline{C/D}$	$\overline{C/D}$
21	\overline{RD}	ENCK	SCK
23	\overline{CSS}	\overline{CSS}	\overline{CSS}
25	FRP	FRP	FRP

Pin No.	Description		
	Parallel #1	Parallel #2	Serial
2	GND	GND	GND
4	GND	GND	GND
6	GND	GND	GND
8	GND	GND	GND
10	GND	GND	GND
12	GND	GND	GND
14	GND	GND	GND
16	GND	GND	GND
18	GND	GND	GND
20	GND	GND	GND
22	GND	GND	GND
24	GND	GND	GND
26	\overline{RESET}	\overline{RESET}	\overline{RESET}

12.2 Connectors



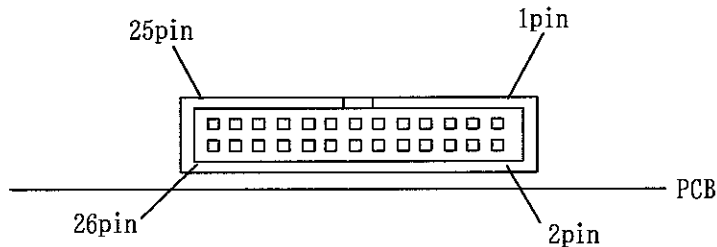
Power Connector:

JST: B3B-XH-A or equivalent

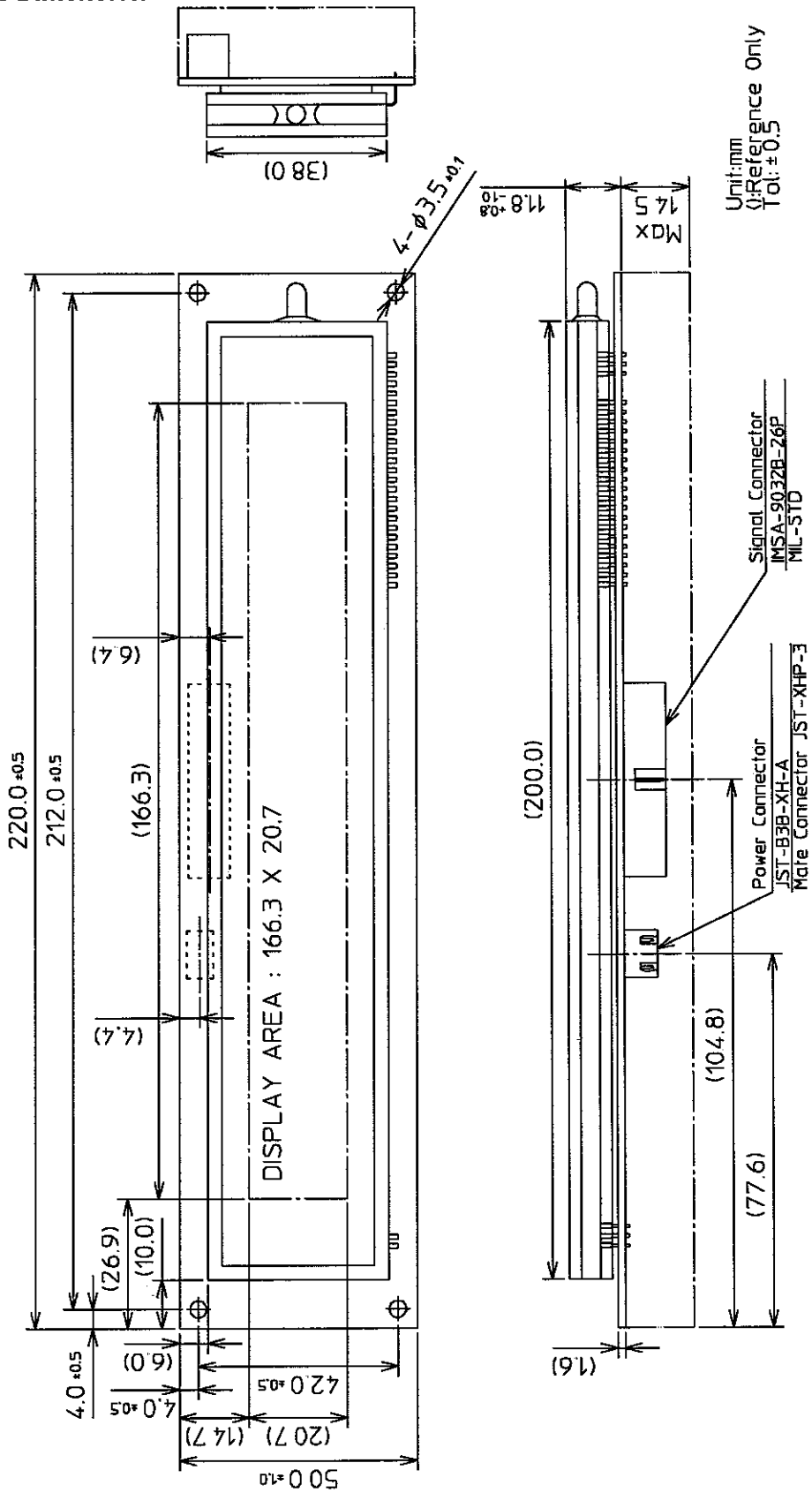
Pin No.	Description
1	Vcc
2	Test (Factory Only)
3	GND

Data Connector

IMSA: 9032B-26P or Equivalent



13. Outline Dimension



Important Precautions

- All VFD Modules contain MOS-LSI's ICs. Anti-Static handling is required.
- A VF Display is made with Soda-Lime glass. Heavy shock loads exceeding 55G, thermal shock greater than 10°C/minute, or a direct blow to the glass surface - especially to the EXHAUST PIPE; may CRACK the glass.
- Do not apply excessive pressure or torque to the display. When the factory builds the system frame, a slight gap between the display glass face and the front panel is necessary to avoid a contact failure of the lead pins of the display. Excessive pressure or torque will make the glass **CRACK** around the lead pins of the display.
- Neither the **DATA CONNECTOR** nor the **POWER CONNECTOR** should be connected or disconnected while power is applied. As is often the case with most subsystems, caution should be exercised in selectively disconnecting power to a computer-based system. The module receives high logic on its strobe lines as random signals to all data ports. Removal of the primary power with logic signals applied may damage input circuitry.
- Stress exceeding the specification listed under the Absolute Maximum Ratings may cause PERMANENT DAMAGE of the modules.
- The +5 Vdc power line must be regulated completely since all control logic depends on this line. Do not apply a slow start power supply. Provide sufficient output current to avoid INRUSH CURRENT loading the power supply or stagger the power up of system devices.
- *The Data cable length between the module and the host system is recommended to be **less than 300 mm** to eliminate noise.
- Do not place the module on a conductive surface (metal or ESD conductive) immediately after power off. Large filter capacitors on the module store energy and require more than 1 min. of discharging time to avoid a short circuit condition.
- When power is not applied for more than 2 months, several hours of operation under the test mode may help the stability of the brightness of the VFD.
- A fixed (static) message displayed longer than 5 hours continuously may cause phosphor burn-in. Some methods of avoiding this include: a sleep mode and "wake-up" event or periodically shifting the display pattern or periodically reversing the mode of green/black.
- The module contains a high voltage power source (70 Vdc). Handle with caution when power is applied.