Noritake itron

VACUUM FLUORESCENT DISPLAY MODULE SPECIFICATION

MODEL GU256X32-820

SPECIFICATION NO.	: DS-755-0001-01
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1. General Description

1.1 Construction : A single board display module consisting of a 256x32 dot BD-VFD, an 8 bit micro-computer, character generator and a DC/DC converter.

1.2 Features : Graphic and Character (8x16,16x16 font) mode available.
(Please refer to the KANJI Character cord table " DS-782-0000-00")
Flexible Display Editing Functions
Compact and slim Design using BD-VFD
Wide Range Temperature

1.3 Outline dimension : See attached drawings.

2. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Input Voltage	VI	-0.5	—	Vcc+0.3	V	—
Power Supply Voltage	Vcc	0	—	6.5	VDC	—

3. Electrical Characteristics

Measuring Conditions : TA (Ambient temperature) = 25°C, Vcc=5.0V

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Logic Input Voltage	"H"	VIH	4.0	—	—	VDC	IIH= 2 μ A
	"L"	VIL	—	—	1.0		IIL= - 600 μ A
Logic Output Voltage	"H"	VOH	4.7	—	—	VDC	IOH= - 300 μ A
	"L"	VOL	—	—	0.3		IOL= 300 μ A
Reset Input Voltage	"H"	VRH	4.0	—	—	VDC	IRH= 5 μ A
	"L"	VRL	—	—	0.6	VDC	IRL= - 600 μ A
Power Supply Voltage		Vcc	4.75	5.00	5.25	VDC	—
Power Supply Current		Icc	—	0.75	0.90	A	VCC=+5V, All dots ON
			—	0.60	0.75		VCC=+5V, All dots OFF

Note:
The rise time of **Vcc** should not exceed **100 ms**.
Icc may peak at more than twice the operating current upon power up (Inrush current)

4. Optical Specifications

Number of dots : 8192 (256x32)
Display area : 166.25 mm x 20.65mm (X x Y)
Dot size : 0.5 mm x 0.5 mm (X x Y)
Dot pitch : 0.65 mm x 0.65 mm (X x Y)
Luminance : 350cd/m^2 (Min.)
Color of illumination : Green (Blue Green)

5. Environmental Specifications

Operating temperature : -40 to +85°C
Storage temperature : -40 to +85°C
Storage humidity : 20 to 80 % R.H(Non Condensation)
Vibration : 10-55-10Hz, all amplitude 1mm, 30Min., X-Y-Z (Non operating)
Shock : 539m/s^2 10mS (Non operating)

6. Description of Bus and Signals

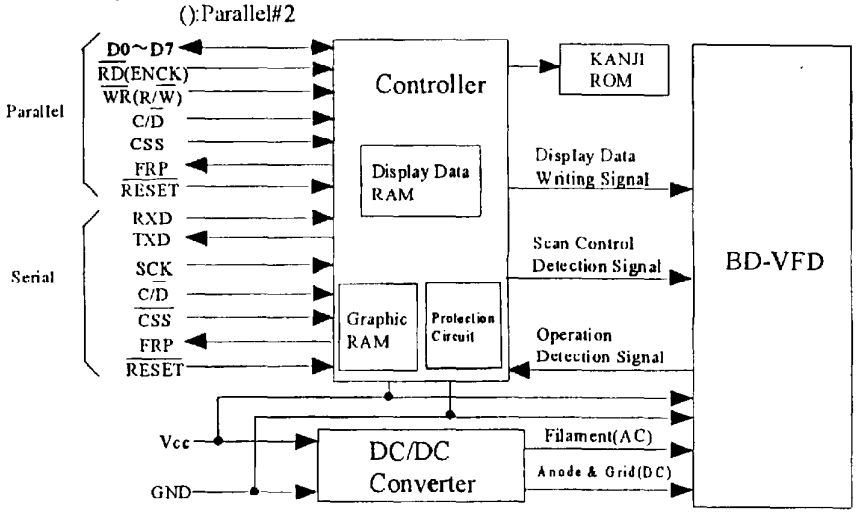
6.1 Parallel Interface

Data Line	Function
D0~D7	Data Bus (Input / Output)
WR(R/W)	Parallel #1:Write Signal, Parallel #2:R/W (Input)
RD(ENCK)	Parallel #1:Read Signal, Parallel #2:ENCK (Input)
CSS	Chip Select (Input)
C/D	Command / Data Select Signal (Input) C/D = "1" ··· Command C/D = "0" ··· Data
FRP	Frame Pulse Signal (Output)
RESET	RESET="0"··· Reset (Input)
Vcc	Input Voltage
GND	Ground

6.2 Serial Interface

Data Line	Function
RXD	Serial Input
TXD	Serial Output
SCK	Clock (Input)
CSS	Chip Select (Input)
C/D	Command / Data Select Signal (Input) $C/\overline{D}$ = "1" ··· Command $C/\overline{D}$ = "0" ··· Data
FRP	Frame Pulse Signal (Output)
$\overline{RESET}$	$\overline{RESET}$="0"··· Reset (Input)
Vcc	Input Voltage
GND	Ground

7. Block Diagram

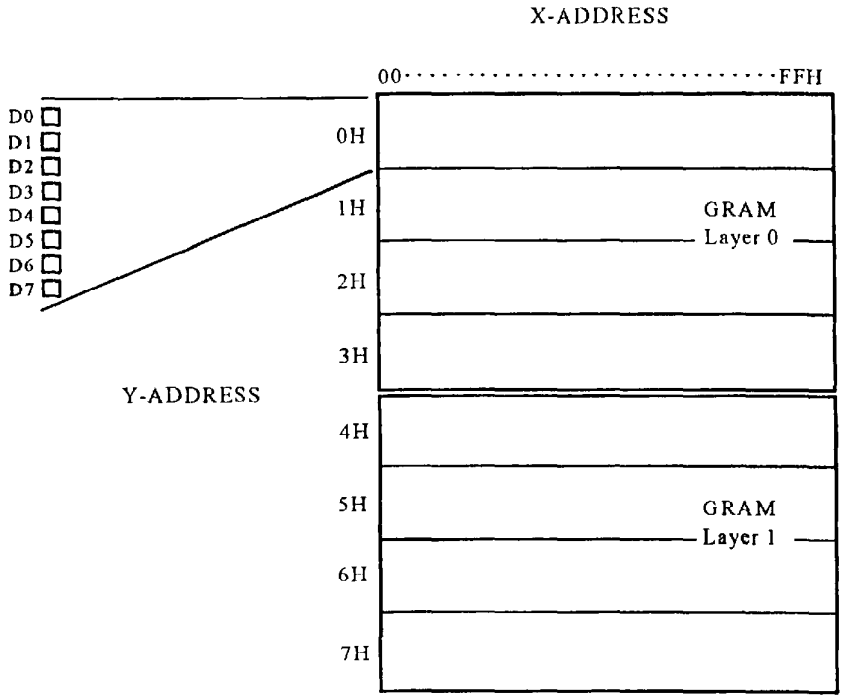


8. Display Screen

8.1 Graphic Display (GRAM)

The Graphics RAM will be referred to throughout as GRAM. This is composed of 16384 bits arranged as (256 x 32 bits) x 2, and the access is structured as 8 bits vertical data. When selected serial interface, RXD is Serial Input and TXD is Serial Output.

The relationship between the GRAM address and the graphic location is as follows:

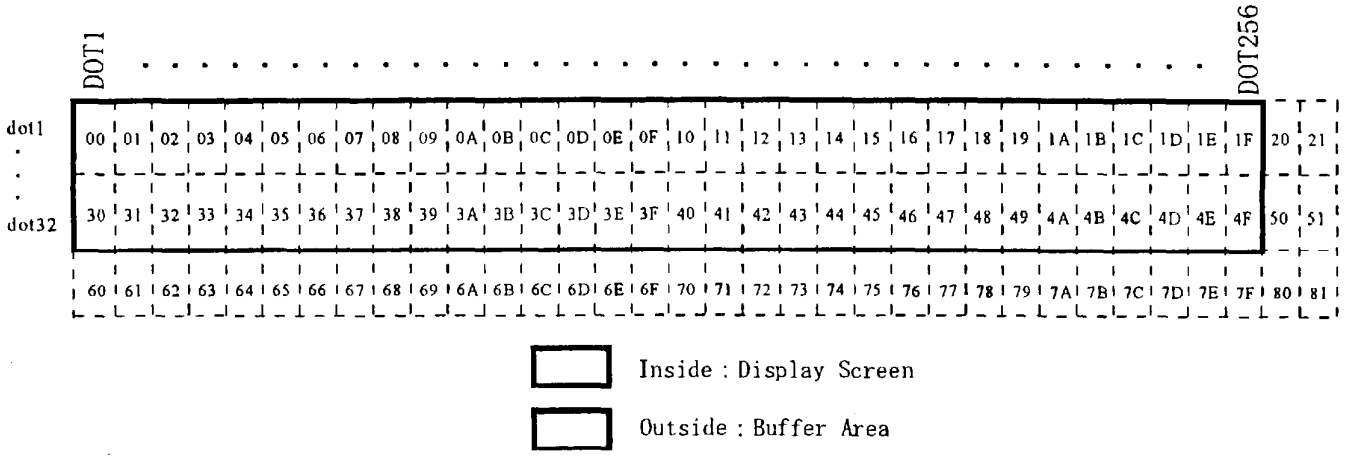


8.2 Character Display (DDRAM)

Character display consists of 16x16 dots or 8x16 dots at 17 characters x 3 lines.

When 8 bits data is sent twice, a charaeter code can be written in a memory.

The relationship between the memory address and display location as follows:



9. Function

9.1 Command

This command set is as follows:

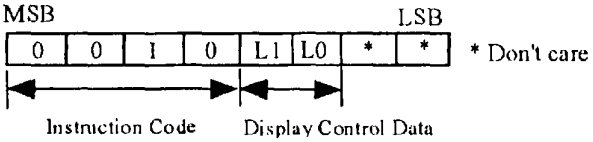
Command	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Comments	
Display ON/OFF	1	0	0	1	0	L1	L0	*	*	1st BYTE	Display ON/OFF Control, 2BYTE Command
		DS	GS	DRV	GRV	AND	EXOR	*	*	2nd BYTE	
Brightness Set	1	0	1	0	0	BW3	BW2	BW1	BW0	1BYTE	1BYTE Command
Display Clear	1	0	1	0	1	G1C	G0C	DC	HM	1BYTE	1BYTE Command
Display Area SET	1	0	1	1	0	*	*	1	*	1st BYTE	Display Area is assigned 3BYTE Command
		*	*	*	*	*	(A2~A0)			2nd BYTE	
	0	D7	D6	D5	D4	D3	D2	D1	D0	3rd BYTE	
Address SET	1	0	1	1	0	1	*	0	*	1st BYTE	Character Display Address Set, 2BYTE Command
		DDRAM Address (DDA7~DDA0)								2nd BYTE	
	1	0	1	1	0	0	1	0	*	1st BYTE	Graphic Display X-Address Set, 2BYTE Command
		GRAM X-Address (GXA7~GXA0)								2nd BYTE	
	1	0	1	1	0	0	0	0	*	1st BYTE	Graphic Address Y-Address Set, 2BYTE Command
		*	*	*	*	GYA3	GYA2	GYA1	GYA0	2nd BYTE	
GRAM Display Position Start Set	1	0	1	1	1	*	*	*	*	1st BYTE	Graphic Display Horizontal Shift, 2BYTE Command
		XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	2nd BYTE	
	1	1	0	1	1	UD	S1	S0	*	1BYTE	Graphic Display Vertical Shift, 1BYTE Command
DDRAM Display Position Start Set	1	1	0	1	0	*	*	*	0	1st BYTE	Character Display Horizontal Shift, 2BYTE Command
		AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	2nd BYTE	
	1	1	0	0	1	UD	S1	S0	*	1BYTE	Character Display Vertical Shift, 1BYTE Command
Address Mode Set	1	1	0	0	0	*	IGX	IGY	*	1BYTE	Address Increment, 1BYTE Command
Address Read	1	1	1	0	1	1	0	*	*	1st BYTE	Character Display (DDRAM) Horizontal And Vertical Display Start Address, 3BYTE Command
		VD6	VD5	VD4	VD3	VD2	VD1	VD0	HD8	2nd BYTE	
		HD7	HD6	HD5	HD4	HD3	HD2	HD1	HD0	3rd BYTE	
	1	1	1	0	1	0	1	*	*	1st BYTE	Graphic Display(GRAM) Horizontal And Vertical Display Start Address, 3BYTE Command
		*	VG6	VG5	VG4	VG3	VG2	VG1	VG0	2nd BYTE	
		HG7	HG6	HG5	HG4	HG3	HG2	HG1	HG0	3rd BYTE	
ROM Data Transfer Set	1	1	1	1	0	*	*	*	*	1st BYTE	Copy character in the external KANJI ROM, 3BYTE Command
		AD19	AD18	AD17	AD16	AD15	AD14	AD13	AD12	2nd BYTE	
		*	AD10	AD9	AD8	AD7	AD6	AD5	AD4	3rd BYTE	
Data Write	0	WRITE DATA									Writes Data to the Address Character Data is 2BYTE, Graphic Data is 1BYTE

*Don't Care

9.2 DISPLAY ON/OFF (C/$\overline{D}$= "1")

The GRAM Layer is selected with the 1st byte of data. Two modes; display (**ON / OFF**) and also (**reverse or normal modes**) are selected by the 2nd byte. Reverse mode toggles the representation of green in the foreground and black in the background to the exact opposite - green to back and black to the foreground. This is similar to the concept of reverse video.

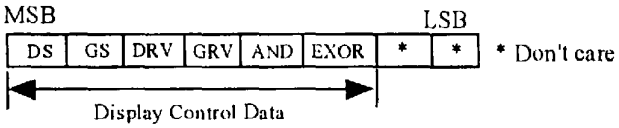
1st Byte:



Specify the layer of GRAM with the **1st BYTE**. Specify **(ON/OFF)** with the 2nd BYTE.

L1= **(1 OR 0)** = GRAM Layer 1 **(Active OR Inactive)**
L0= **(1 OR 0)** = GRAM Layer 0 **(Active OR Inactive)**

2nd Byte:



DS= **(1 OR 0)** Character Display Area = **(On OR Off)**
GS= **(1 OR 0)** Graphic Display Area = **(On OR Off)**
DRV= **(1 OR 0)** Character Display Area = **(Reverse OR Normal)**
GRV= **(1 OR 0)** Graphic Display Area = **(Reverse OR Normal)**

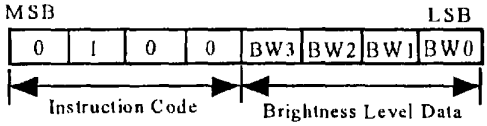
GS= "0": Stand-by mode

1st Byte		2nd Byte		Action
L1	L0	AND	EXOR	
*	*	1	*	AND Display of Layer 1& 0
*	*	0	1	EXOR Display of Layer 1& 0
1	1	0	0	OR Display of Layer 1& 0
1	0	0	0	Only Layer1 selected for display
0	1	0	0	Only Layer0 selected for display
0	0	0	0	Graphic Display Off

* Don't care

9.3 Brightness Control (C/$\overline{D}$= "1")

The Brightness level of the display screen can be scaled by the following four bit control. Please note that the brightness is consistent across the illuminated pixels. There is no scaling of individual pixels. The display self-initializes to 100% brightness.



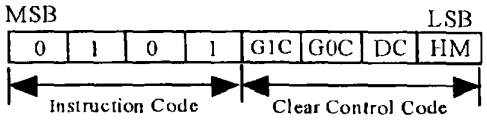
Brightness levels are as follows:

BW3	BW2	BW1	BW0	Brightness Level
0	0	0	0	100%(Light)
0	0	0	1	94%
0	0	1	0	87%
0	0	1	1	81%
0	1	0	0	75%
0	1	0	1	69%
0	1	1	0	62%
0	1	1	1	56%
1	0	0	0	50%
1	0	0	1	44%
1	0	1	0	37%
1	0	1	1	31%
1	1	0	0	25%
1	1	0	1	19%
1	1	1	0	12%
1	1	1	1	6%(Dark)

9.4 Display Clear (C/$\overline{D}$= "1")

This command clears a layer of the GRAM.

This command should always be applied at power on or reset. In the period of **1mS** following the issue of this command, the module requires internal processing and **does not accept any commands.**



To clear the GRAM Layer, G1C or G0C bit must be asserted. By asserting HM bit, both data write position address and display start position address also be reset. (The X address of GRAM is initialized as "HM=0".)

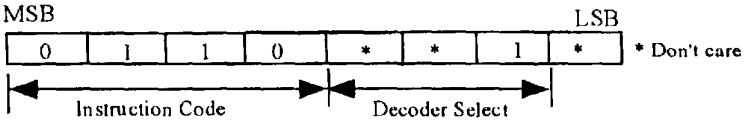
HM= (1 or 0) equals **(initialize data write position and display start position or initialize X address of data write position).**

G1C= (1 or 0) equals **(GRAM Layer 1 cleared or GRAM Layer 1 not cleared)**
G0C= (1 or 0) equals **(GRAM Layer 0 cleared or GRAM Layer 0 not cleared)**
DC= (1 or 0) equals **(DDRAM cleared or DDRAM not cleared)**
Example to clear both layers: **0101 1111**

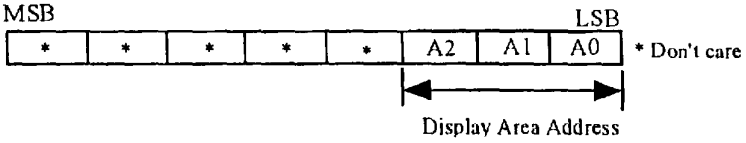
9.5 Display Area Set (C/$\overline{D}$="1")

This command sets display area as Graphic Display or Character display.
Setup is performed by 3 byte command.
1st byte of a Decoder Select and Display Area Data Address to set it as the 2nd byte are specified. 3rd byte of data to display on D0-D7 which corresponded all over the following figure is inputted.

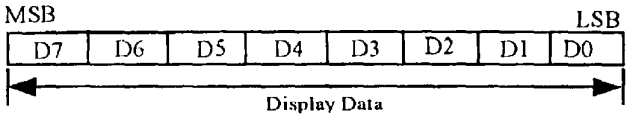
1st Byte: (C/$\overline{D}$="1")



2nd Byte: (C/$\overline{D}$="1")

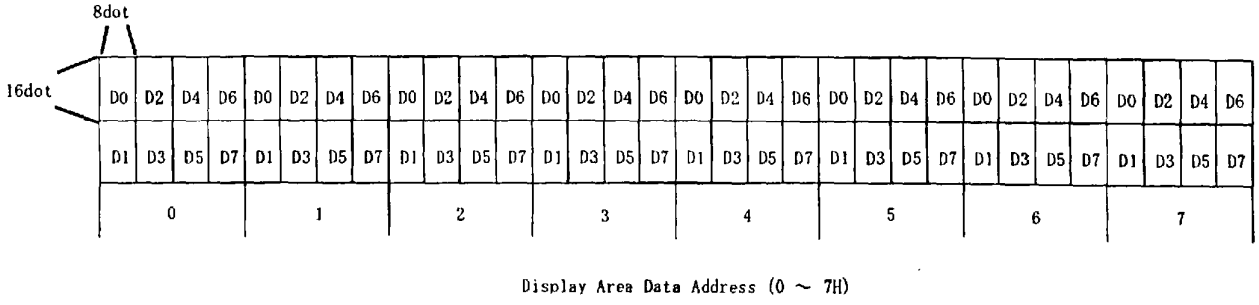


3rd Byte: (C/$\overline{D}$="0")



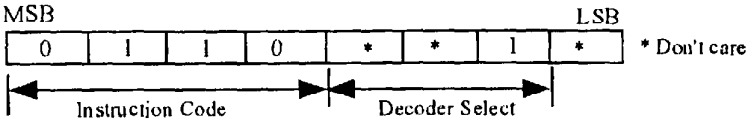
D0 to D7 = "1" : Graphic Display (GRAM)
D0 to D7 = "0" : Character Display (DDRAM)

Display area is assigned as follows on a screen.

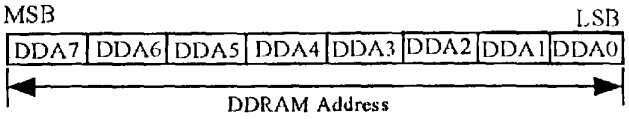


9.6 DDRAM Address (Character Display) (C/$\overline{D}$="1")

1st Byte:



2nd Byte:



The address of DDRAM expressed with 8 bits (00Hex-91Hex) of DDA0-A7 is specified, and a KANJI code is inputted after the 3rd byte. Not to set addresses other than a sphere.
Right end cannot write a 16x16 dots font in the place which is vacant only as for 8x16 dots.
Refer to 8.2 Character Display (DDRAM).

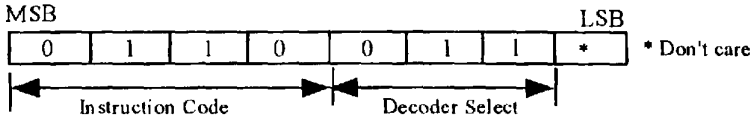
9.7 GRAM Address Set (Graphic Display) (C/$\overline{D}$="1")

GRAM Address Set is specified both of X & Y Address.

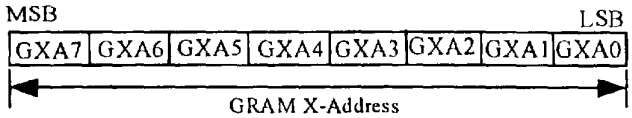
9.7.1 GRAM Write X Address Set

X address of GRAM expressed with 8 bits (00Hex-7FHex) is specified.
Refer to 8.1 Graphic Display (GRAM).

1st Byte:



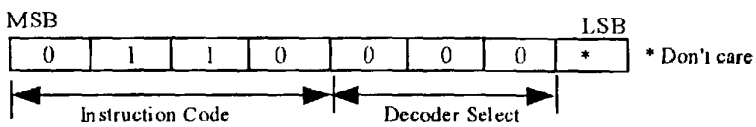
2nd Byte:



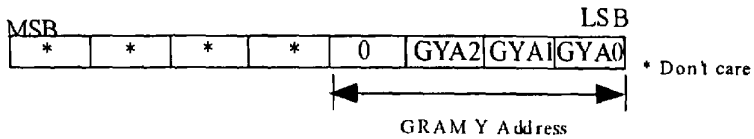
9.7.2 GRAM Write Y Address Set

Y address of GRAM expressed with 4 bits (0Hez-FHex) is specified.

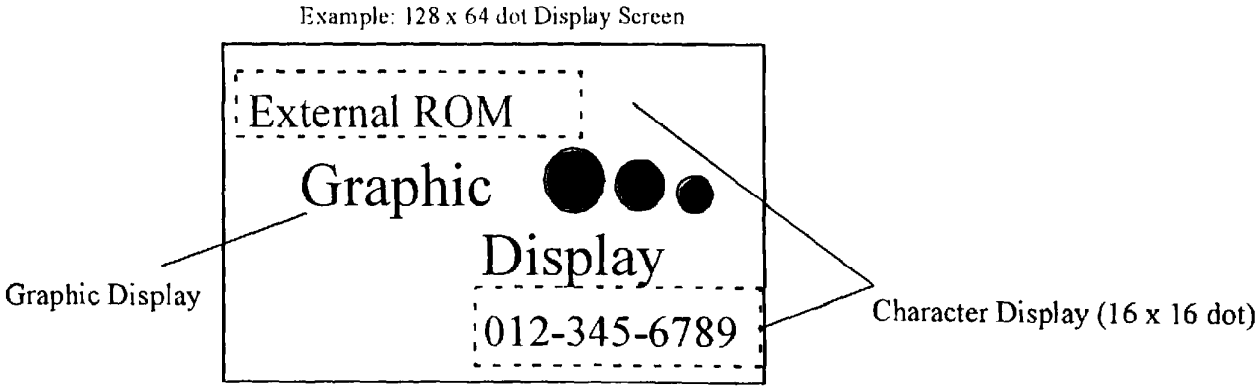
1st Byte:



2nd Byte



The example of mixture of the Graphic Display (GRAM) by the display area set and a character display (DDRAM) is shown in the following figure.
When switch display area, please perform from an Address Set command again.
(DDRAM to GRAM, GRAM to DDRAM)

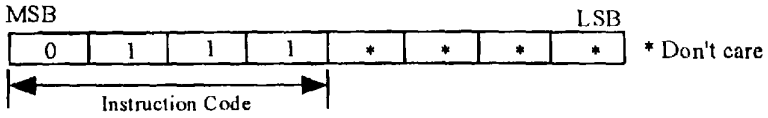


9.8 GRAM Graphic Display Position Start Set (C/$\overline{D}$="1")

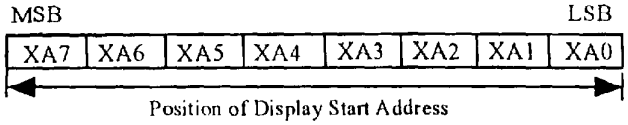
9.8.1 Horizontal Shift

This command specifies the address that a display pattern can be positioned to by **8 bits(00Hex to 7FHex)**. DDRAM display area is not influenced.
This is equivalent to an offset in the X axis.

1st Byte:

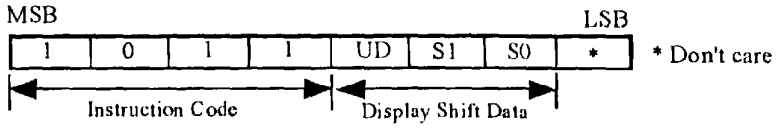


2nd Byte:



(b)Vertical Shift

This is equivalent to an offset Y axis.

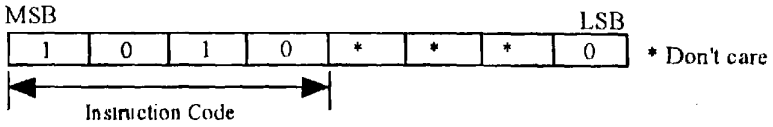


UD= "1": Display scrolled up.
UD= "0": Display scrolled down.
S1= "0", S0= "1": Display shift by 8 dots.
S1= "1", S0= "0": Display shift by 1 dots.
S1= "1", S0= "1": Display shift by 2 dots.

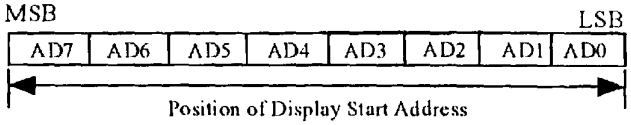
9.9 DDRAM Character Display Position Start Set (C/$\overline{D}$="1")

9.9.1 Horizontal Shift

1st Byte:



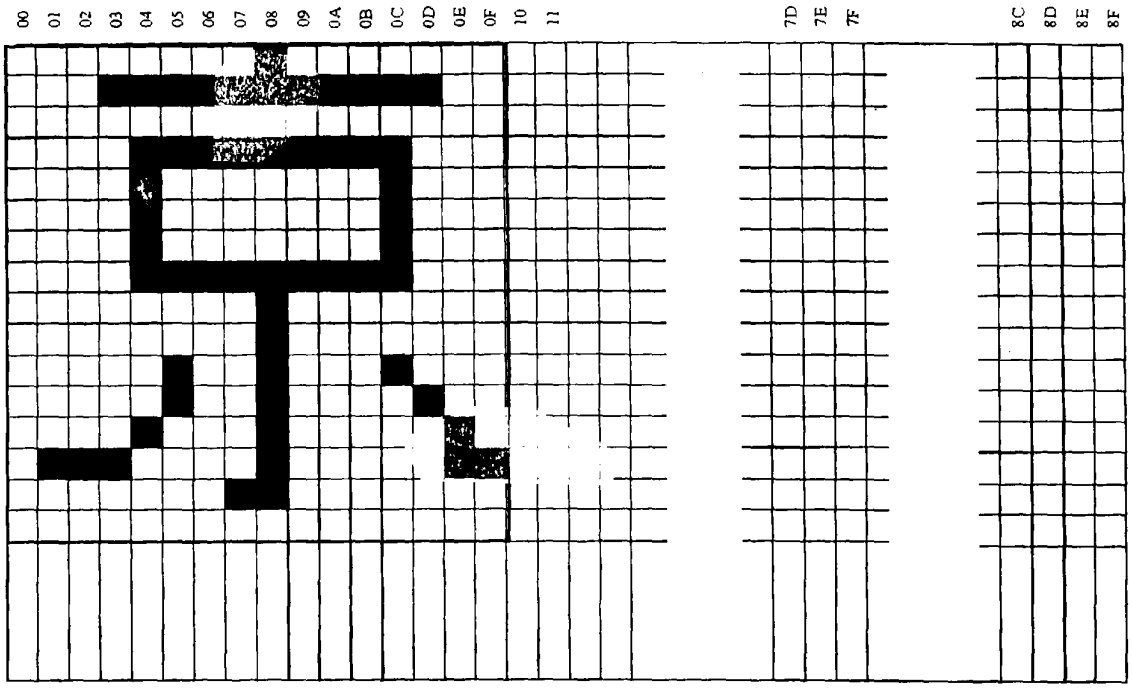
2nd Byte:



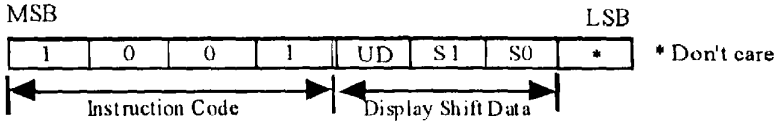
This command specifies the address that a display pattern can be positioned to by **8 bits(00Hex to 7FHex)**. GRAM display area is not influenced.

Display start address is expressed as follows.
A screen scrolls by setting a display start address with 00H and 01H one by one, and shifting in the transverse direction.

Display Start Address



9.9.2 Vertical Shift (C/$\overline{D}$="1")

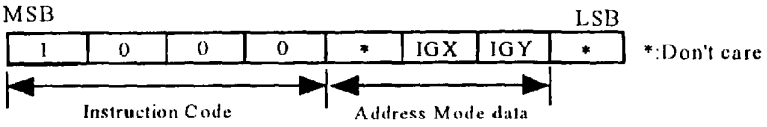


Y axis display shift of DDRAM display area is controlled.

UD= "1": Display scrolled up.
UD= "0": Display scrolled down.
S1= "0", S0= "1": Display shift by 8 dots.
S1= "1", S0= "0": Display shift by 1 dot.
S1= "1", S0= "1": Display shift by 2 dots.

9.10 Address Mode Set (C/$\overline{D}$="1")

When writing to *GRAM*, the address automatically jumps to the next available location.



IGX = "1" : X-Address +1(increment) when writing to GRAM.
IGX = "0" : GRAM X address fixed mode.
IGY = "1" : Y-Address +1(increment) when writing to GRAM.
IGY = "0" : GRAM Y address fixed mode.

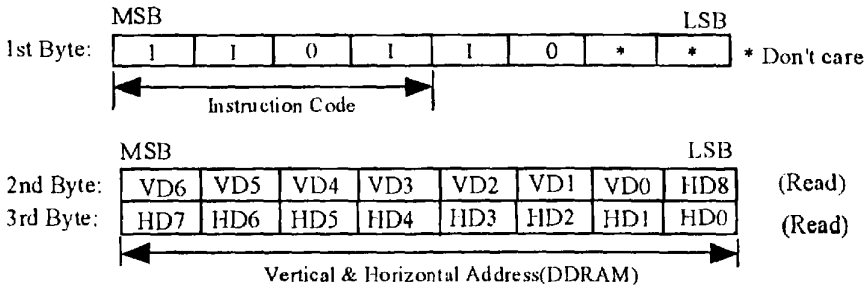
9.11 Address Read (C/$\overline{D}$="1")

This command will cause the vertical and horizontal display start address of DDRAM or GRAM to be read.

On the parallel interface, the data bus outputs the address until $\overline{CSS}$ goes high after the enable signal goes active. Data bus becomes an input when other.

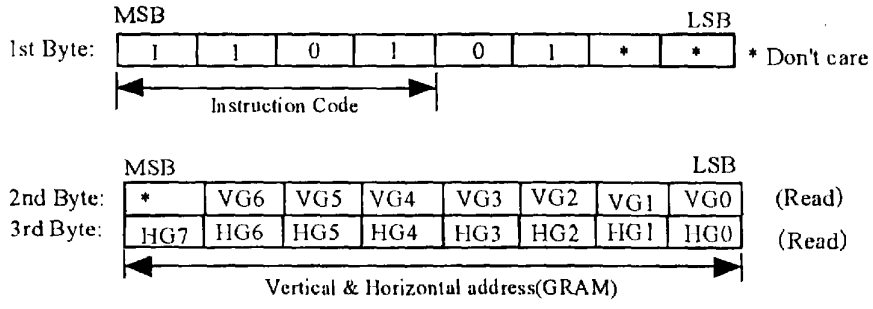
On the serial interface, TXD outputs the data from SCK rising after command is issued till $\overline{CSS}$ goes high.

9.11.1 Vertical and Horizontal display start address of character display(DDRAM)



VD0 to VD6: Vertical display start address
HD0 to HD8: Horizontal display start address

9.11.2 Vertical and Horizontal display start address of graphic display(GRAM)



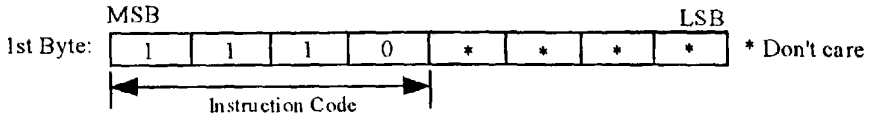
VG0 to VG6: Vertical display start address
HG0 to HG8: Horizontal display start address

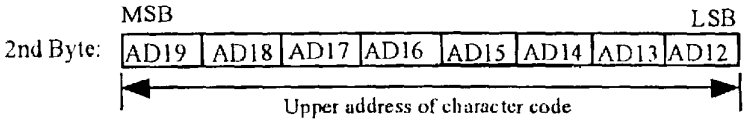
9.12 ROM Transfer (C/$\overline{D}$="1")

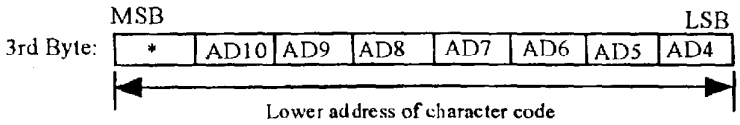
This command will copy the character in the external ROM as specified by the 2byte address, to GRAM location specified during the address set command for GRAM.
As transfer starts when RAM access completes, it is necessary to wait two 400uS.
Also, it is not necessary to have distinction of 16x16 dots and 8x16 dots.

Example: GRAM address after ROM transfer

In the case of GRAM X="00000000", GRAM Y="0001", Transfer 8x16 dots font, address will be X="00001000", Y="0001".
Transfer 16 x 16 dots font, will be X="00010000", Y="0001".







9.13 Data Write (C/$\overline{D}$="0")

9.13.1 Write to Character Display(DDRAM)

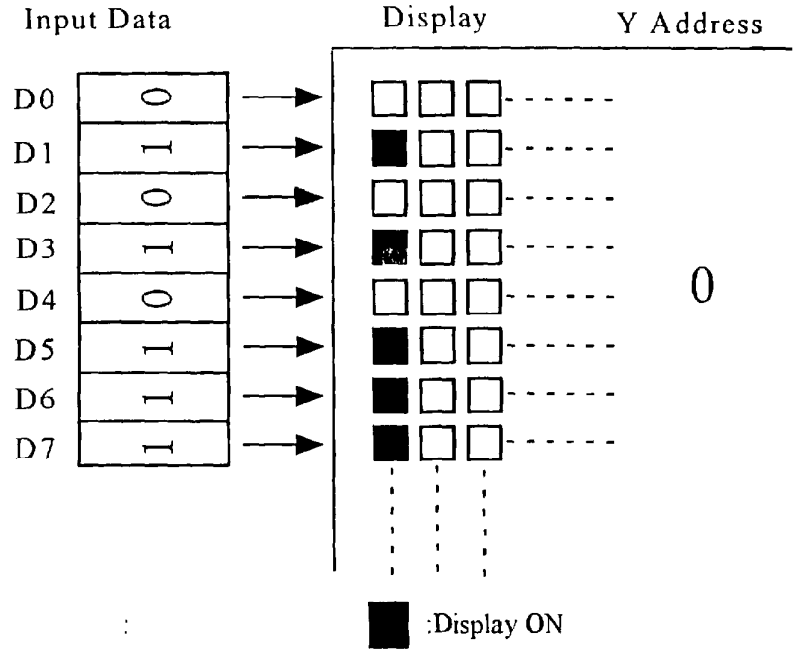
Can write on DDRAM by setting DDRAM address.
Complete an address with 2 byte writing.
1st byte is Upper address of character code and 2nd byte is lower address of character code.
For example, "23Hex" is sent to the 1st byte and "41Hex" is sent to the 2nd byte to display "A."
At this time, the 2nd byte is surely continuously sent with the 1st byte.
8x16 dots font is performed similarly.
Moreover, since a 8x16 dots font has 8 dots and 16 dots of 16x16 dos font in a transverse direction and a character is packed and displayed when a 16x16 dots font and a 8x16 dots font are intermingled, it is cautious of the number of characters.
Refer to KANJI ROM TABLE.

9.13.2 Write to Graphic Display(GRAM)

Can be written into GRAM by setting GRAM X or Y address.

Example:

Writing "EA Hex" sets "D1, 3, 5, 6, 7 =1" and "D0, 2, 4 =0" at "Y address =0".

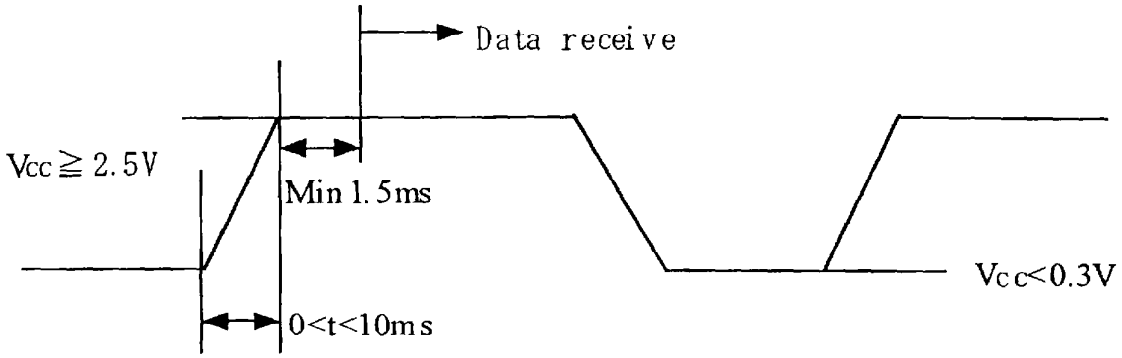


9.14 Default Status at Reset

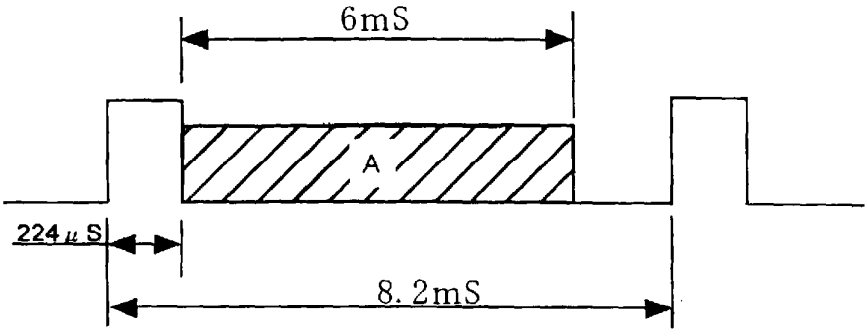
When the reset is applied, the display self-initializes into the following status:

GRAM Layer	:	**Layer (0)**
Display ON/OFF	:	**Display (Off)**
Display Area	:	**(Undefined)**
Address	:	**(Undefined)**
Address Mode	:	**GRAM X-address (fixed mode)**
		GRAM Y-address (fixed mode)
Brightness Level	:	**Brightness (100%)**

The following precautions should be observed at power on and after a reset:
External Reset : After Vcc reaches 2.5V, the Reset level is "Low" for more than 1.5mS.
Power-Up : The following sequence occurs:



9.15 FRP



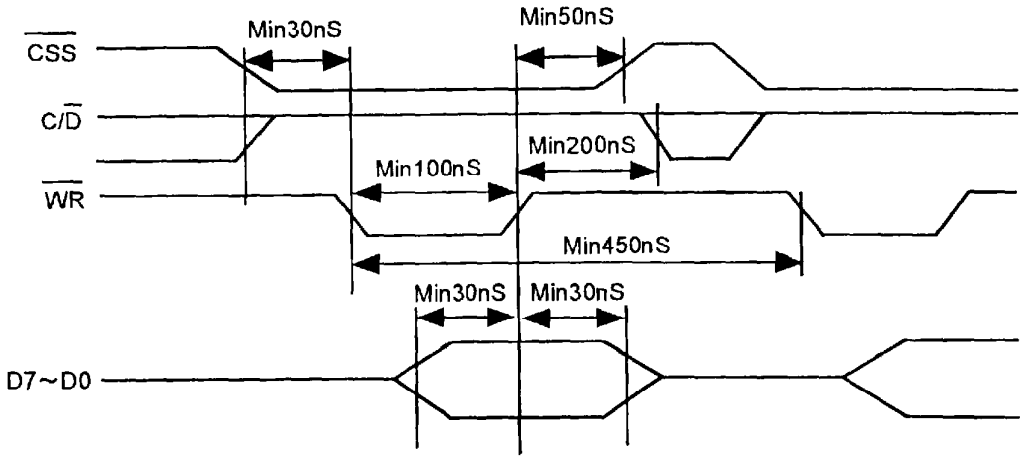
The FRP signal is triggered each time the display is refreshed by the module from its own memory.
Smooth scrolling can be achieved by synchronizing the change of display start address with of FRP signal from module. The region marked as "A" is optimal for writing commands.

10. Interface

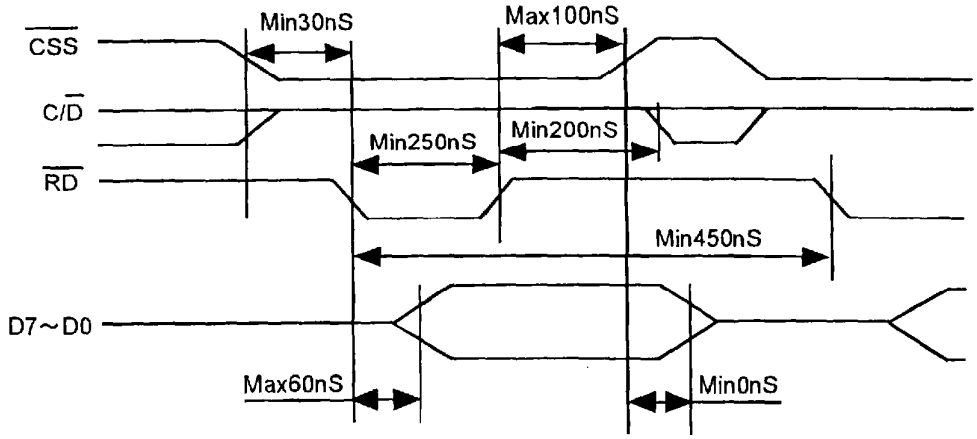
Condition:Ta=25°C,Vcc=5.0V

10.1 Parallel Interface(Parallel #1)

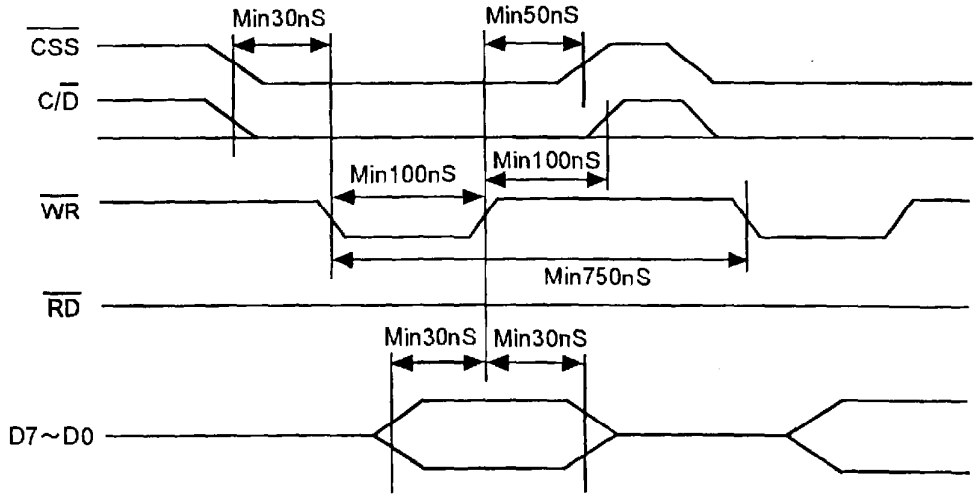
10.1.1 Command Write operation



10.1.2 Command Read operation

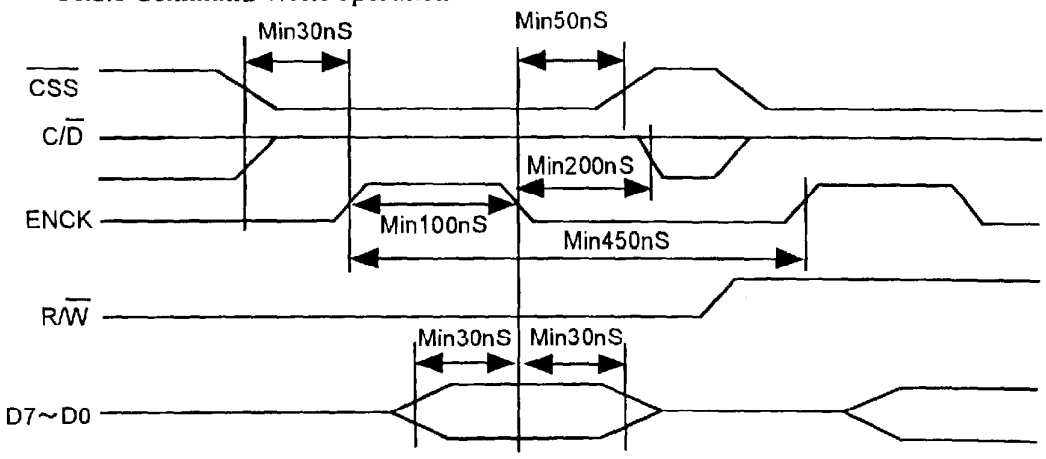


10.1.3 Data Write operation

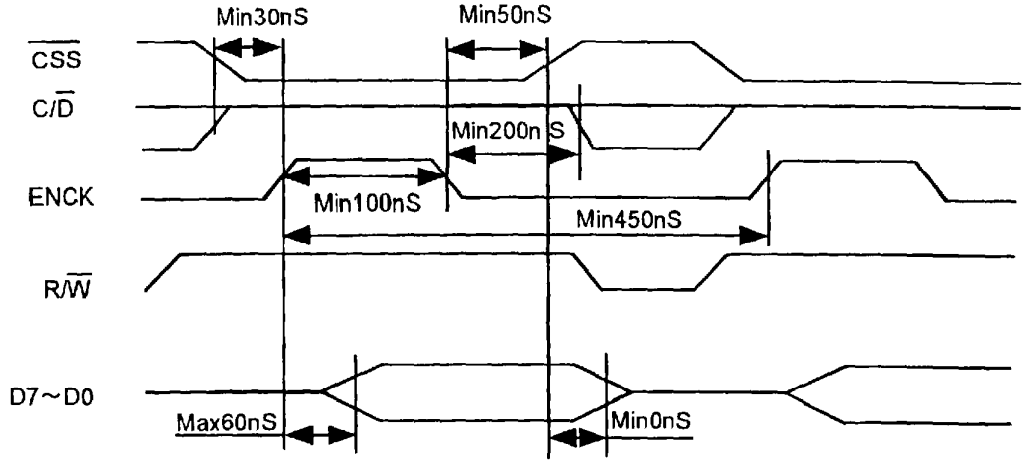


10.2 Parallel Interface(Parallel #2)

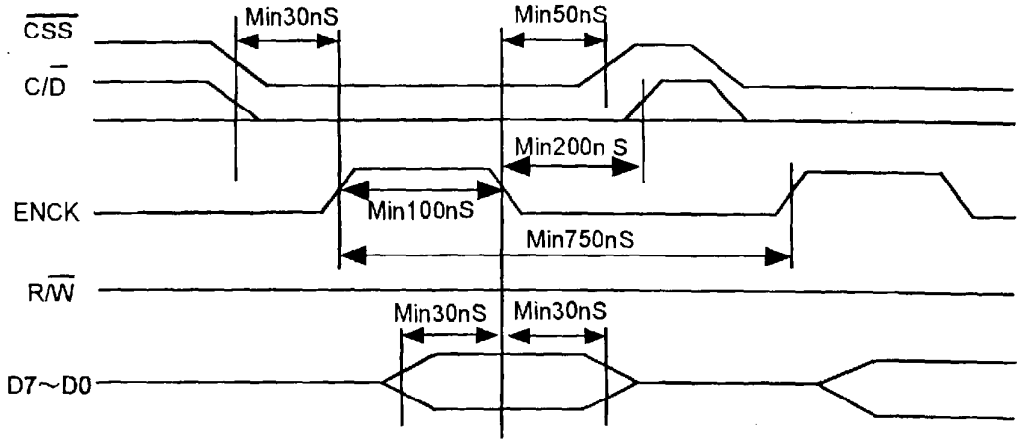
10.2.1 Command Write operation



10.2.2 Command Read operation

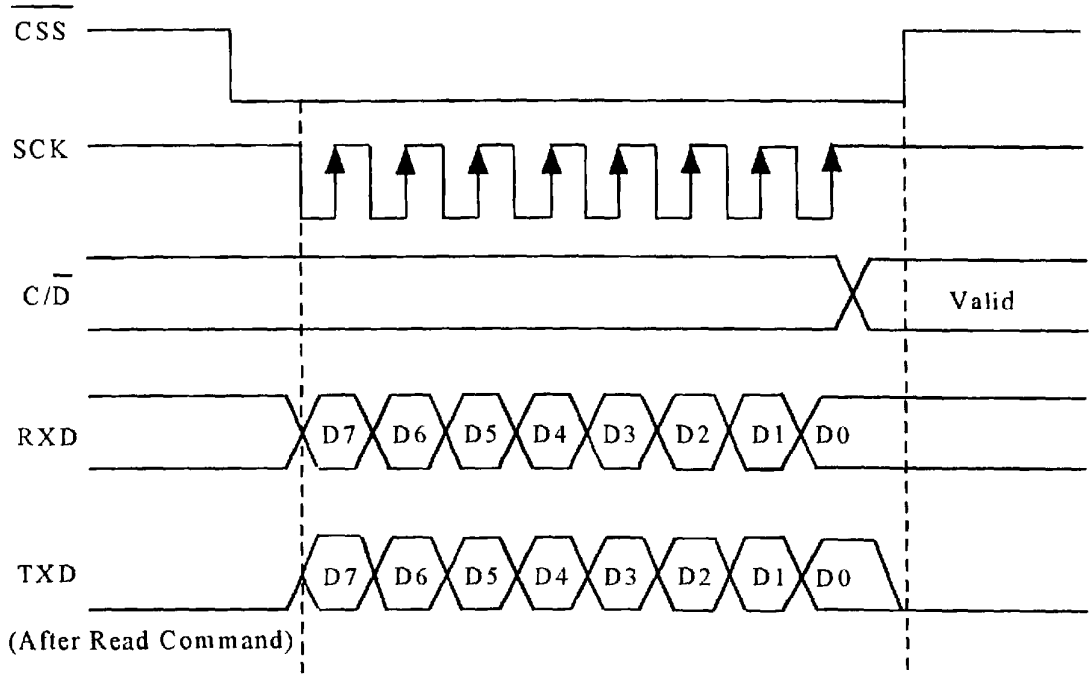


10.2.3 Data Write operation

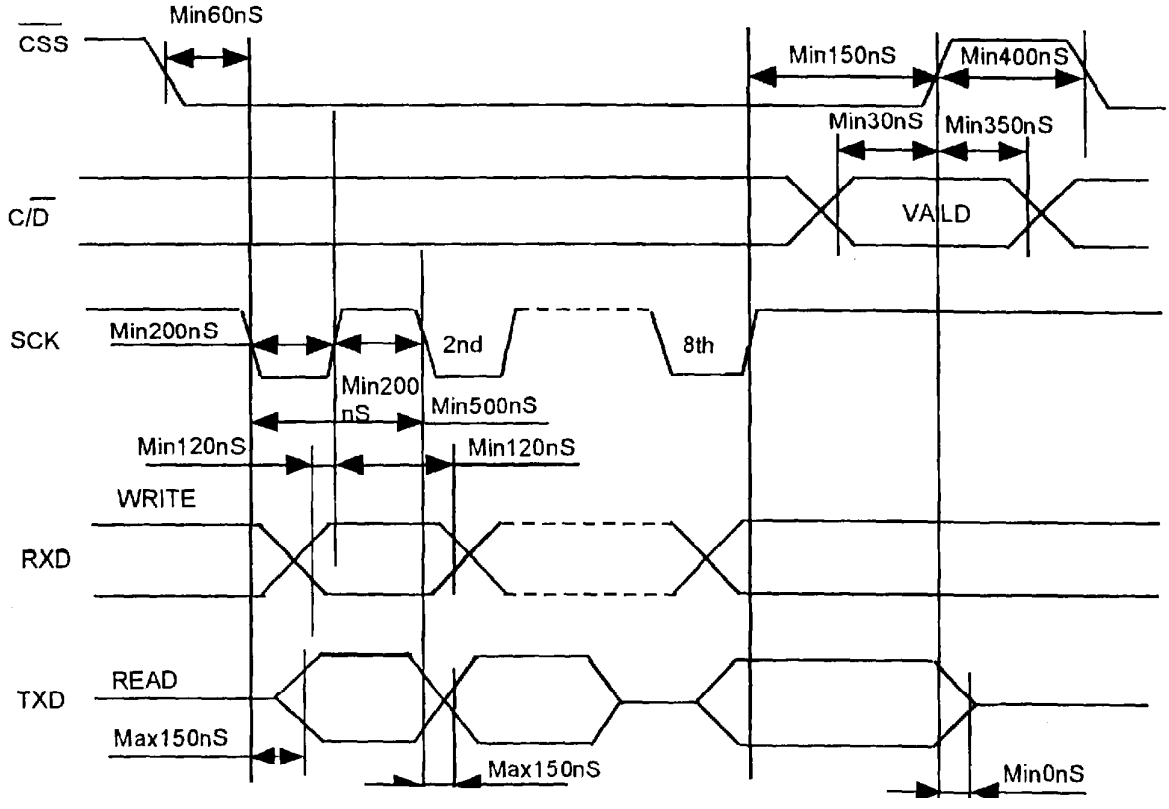


10.3 Serial Interface

To use the serial interface of this module, **(RXD,TXD and SCK)** will be activated by $\overline{CSS}$= "L". The internal shift registers and counters will be reset by $\overline{CSS}$= "H". Serial data is transferred from MSB to LSB (D7->D0) on the rising edge of SCK. After the 8th clock edge, the data stream is converted to 8 bit parallel data. The recognition of RXD input as data or command is determined by the C/$\overline{D}$ on the 8th clock of SCK.



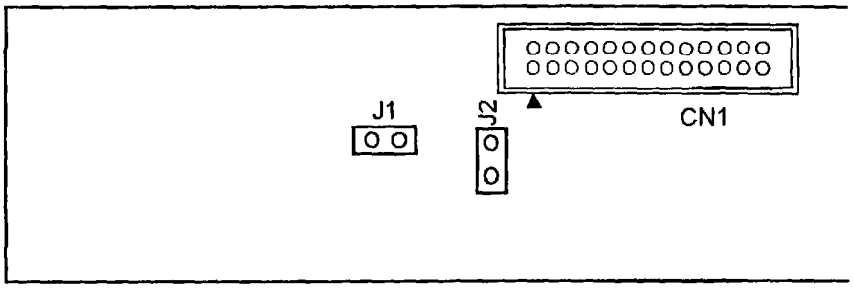
10.3.1 Timing



11. Jumper

11.1 Jumper Position

Parts side



11.2 Jumper Setting

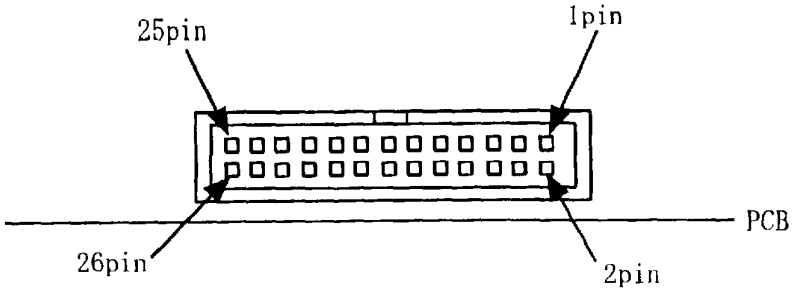
	J1	J2	Function
Interface	×	0	Serial Interface
	1	1	Parallel #1 Interface (Default)
	0	1	Parallel #2 Interface

1:Open 0:Short ×:Don't care

12. Pin Assignment

12.1 Signal Connector

IRISO:IMSA-9032B-26P or equivalent



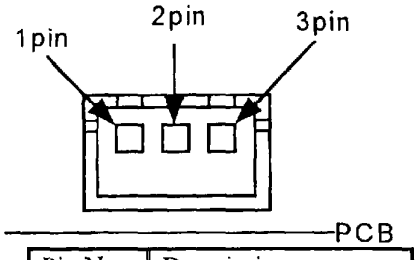
Pin No.	Description		
	Parallel #1	Parallel #2	Serial
1	D7	D7	×
3	D6	D6	×
5	D5	D5	×
7	D4	D4	×
9	D3	D3	×
11	D2	D2	×
13	D1	D1	TXD
15	D0	D0	RXD
17	WR	R/W	×
19	C/D	C/D	C/D
21	RD	ENCK	SCK
23	CSS	CSS	CSS
25	FRP	FRP	FRP

Pin No.	Description		
	Parallel #1	Parallel #2	Serial
2	GND	GND	GND
4	GND	GND	GND
6	GND	GND	GND
8	GND	GND	GND
10	GND	GND	GND
12	GND	GND	GND
14	GND	GND	GND
16	GND	GND	GND
18	GND	GND	GND
20	GND	GND	GND
22	GND	GND	GND
24	GND	GND	GND
26	RESET	RESET	RESET

×:Don't use

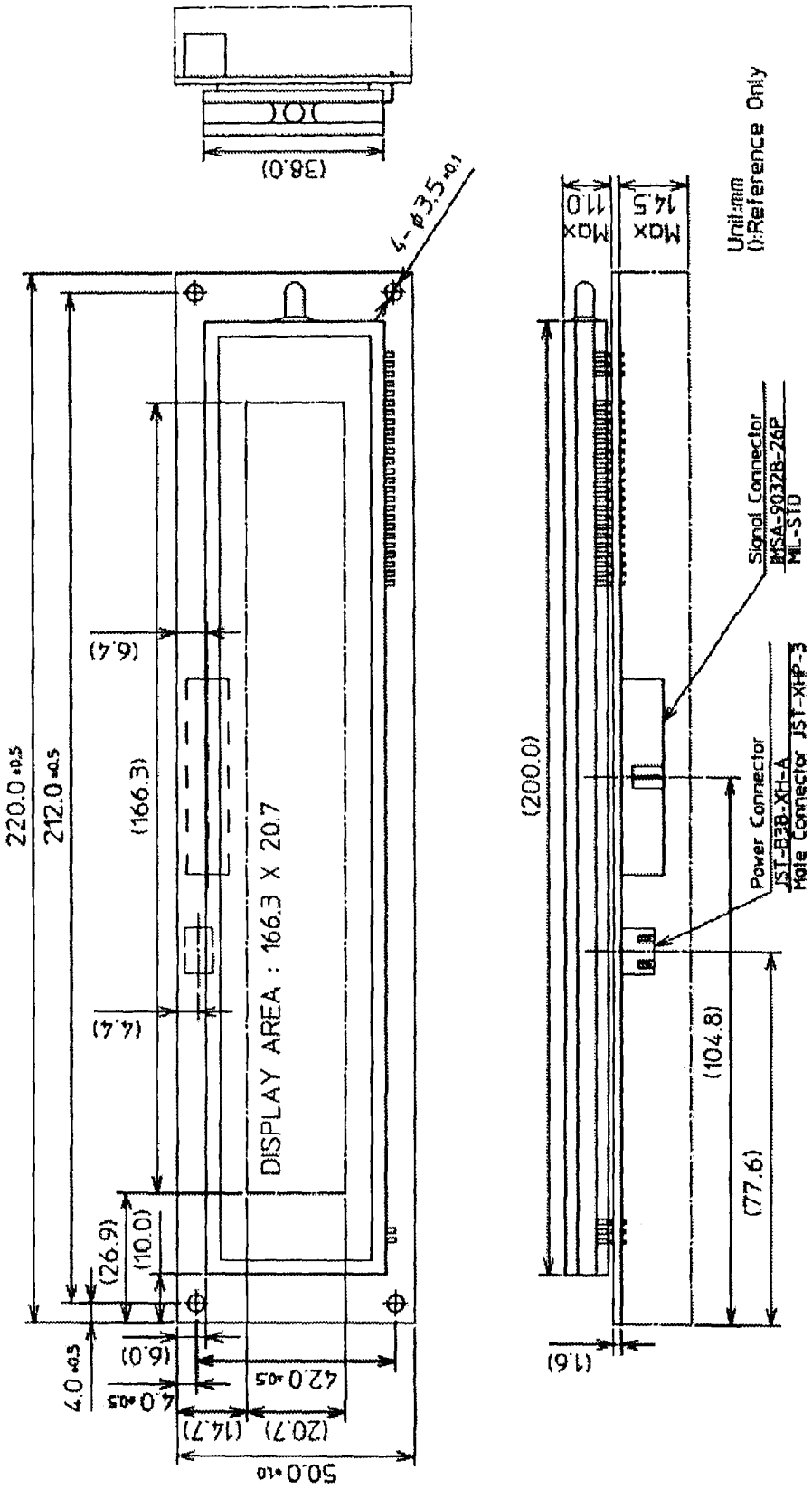
12.2 Power Connector

JST:B3B-XH-A or equivalent



Pin No.	Description
1	Vcc
2	Test(Factory Only)
3	GND

13. Outline Dimension



IMPORTANT PRECAUTIONS

*All VFD Modules contain MOS-LSIs ICs. Anti-Static handling is always required.

*The V.F.Display consists of Soda Lime glass. Heavy shock exceeding 55G, thermal shock greater than 10°C/minute, a direct blow to the glass surface - especially to the EXHAUST PIPE; may CRACK the glass.

*Do not apply excessive pressure or torque to the display. When the factory builds the system frame, a slight gap between the display glass face and the front panel is necessary to avoid a contact failure of the lead pins of the display. Excessive pressure or torque will make the glass CRACK around the lead pins of the display.

*Neither the DATA CONNECTOR nor the POWER CONNECTOR should be connected or disconnected while power is applied. As is often the case with most subsystems, caution should be exercised in selectively disconnecting power to a computer based system. The module receives high logic on its strobe lines as random signals to all data ports. Removal of the primary power with logic signals applied may damage input circuitry.

*Stress exceeding the specification listed under the Absolute Maximum Ratings may cause PERMANENT DAMAGE of the modules.

*The +5 VDC power line must be regulated completely since all control logic depends on this line. Do not apply a slow start power supply. Provide sufficient output current to avoid INRUSH CURRENT loading the power supply or stagger the power up of system devices.

*The Data cable length between the module and the host system is recommended to be **less than 300 mm** to eliminate noise.

*Do not place the module on a conductive surface(metal or ESD conductive) immediately after power off. Large filter capacitors on the module store energy and require more than 1 min. of discharging time to avoid a short circuit condition.

* When power is not applied for more than 2 months, several hours of operation under the test mode may help the stability of the brightness of the VFD

*A fixed (static) message displayed longer than 5 hours continuously may cause phosphor burn-in. Some methods of avoiding this include: a sleep mode and "wake-up" event or periodically shifting the display pattern or periodically reversing the mode of green/black.

*The module contains a high voltage power source (70VDC). Handle with caution when power is applied.