GV7700

HD-VLC™ Transmitter

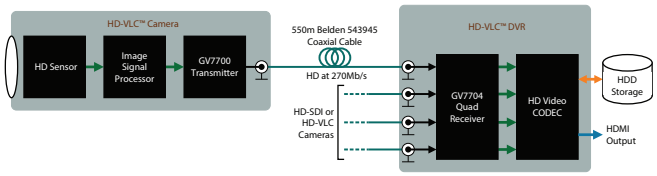
Key Features

- Serial digital video transmitter for HD and 3G video surveillance and HDcctv applications
- Quad rate operation: 270Mb/s, 540Mb/s, 1.485Gb/s, and 2.97Gb/s
- Supports HDcctv 1.0, HD-SDI (ST 292), 3G-SDI (ST 424), and SD-SDI (ST 259)[1]
- Integrated High Definition Visually Lossless CODEC (HD-VLC™) for extended cable reach:
  - HD over 550m of Belden 543945 CCTV coax at 270Mb/s
  - Full HD over 300m of Belden 543945 CCTV coax at 540Mb/s
  - HD over 150m of Cat-5e/6 UTP cable at 270Mb/s
- Configurable 50/75Ω cable driver output, for both coaxial and twisted pair cable transmission
- Integrated audio embedder with support for up to 4 channels of I^2S serial digital audio at 32kHz, 44.1kHz and 48kHz sample rates
- Downstream ancillary data insertion
- Supports both 720p and 1080p HD formats:
  - Full HD: 1080p50/59.94/60fps
  - HD: 1080p25/29.97/30fps
  - HD: 720p25/29.97/30/50/59.94/60fps
- Support for both 8/10-bit and 16/20-bit BT.1120 compliant video interfaces, with embedded TRS or external HVF timing
- 4-wire Gennum Serial Peripheral Interface (GSPI 2.0) for external host command and control
- Dedicated JTAG test interface
- 1.8V core power supply and 1.8V or 3.3V digital I/O supply
- Small-footprint 84-pin dual-row QFN (7mm x 7mm)
- Low power operation, typically 180mW
- Wide operating temperature range: -20°C to + 85°C
- Pb-free and RoHS compliant

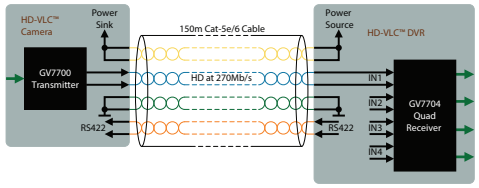
Applications

- HD/3G security cameras
- Industrial cameras
- HD-SDI, 3G-SDI, and HDcctv peripherals
- Media converters
- Video multiplexers

Coaxial Cable Application



UTP Cable Application



Description

The GV7700 is a serial digital video transmitter for High Definition component video. With integrated cable driving technology, the GV7700 is capable of transmitting compressed video at 270Mb/s or 540Mb/s, or uncompressed video at 1.485Gb/s or 2.97Gb/s, over 75Ω coaxial cable, or differentially over 100Ω twisted pair cable.

The GV7700 integrates the High Definition Visually Lossless CODEC (HD-VLC™) technology, which has been developed specifically to reduce the transmission data rate of HD video over both coaxial and unshielded twisted pair (UTP) cable. This is achieved by encoding the HD video, normally transmitted at a serial data rate of 1.485Gb/s, to the same rate as Standard Definition (SD) video, at 270Mb/s serial data rate.

At 270Mb/s, the effect of cable loss is greatly reduced, resulting in much longer cable transmission. For 75Ω coaxial cable, HD-VLC allows a 1.485Gb/s HD signal to be transmitted up to 3x the normal reach. In typical video over coaxial installations, when paired with Semtech's GV7704 HD-VLC receiver, cable distances over 550m are possible.

Similarly, a 2.97Gb/s 3G signal can be transmitted at 540Mb/s using HD-VLC.

The GV7700 can also be configured to transmit HD and 3G video over UTP cable, such as Cat-5e and Cat-6 cable, when HD-VLC encoded at 270Mb/s and 540Mb/s, respectively.

The device supports both 8-bit and 10-bit per pixel YCbCr 4:2:2 BT.1120 component digital video. A configurable 20-bit or 10-bit wide parallel digital video input bus is provided, with associated pixel clock and timing signal inputs. The GV7700 supports direct interfacing of HD video formats conforming to ITU-R BT.709 and BT.1120-6 for 1125-line formats, and SMPTE ST 296 for 750-line formats.

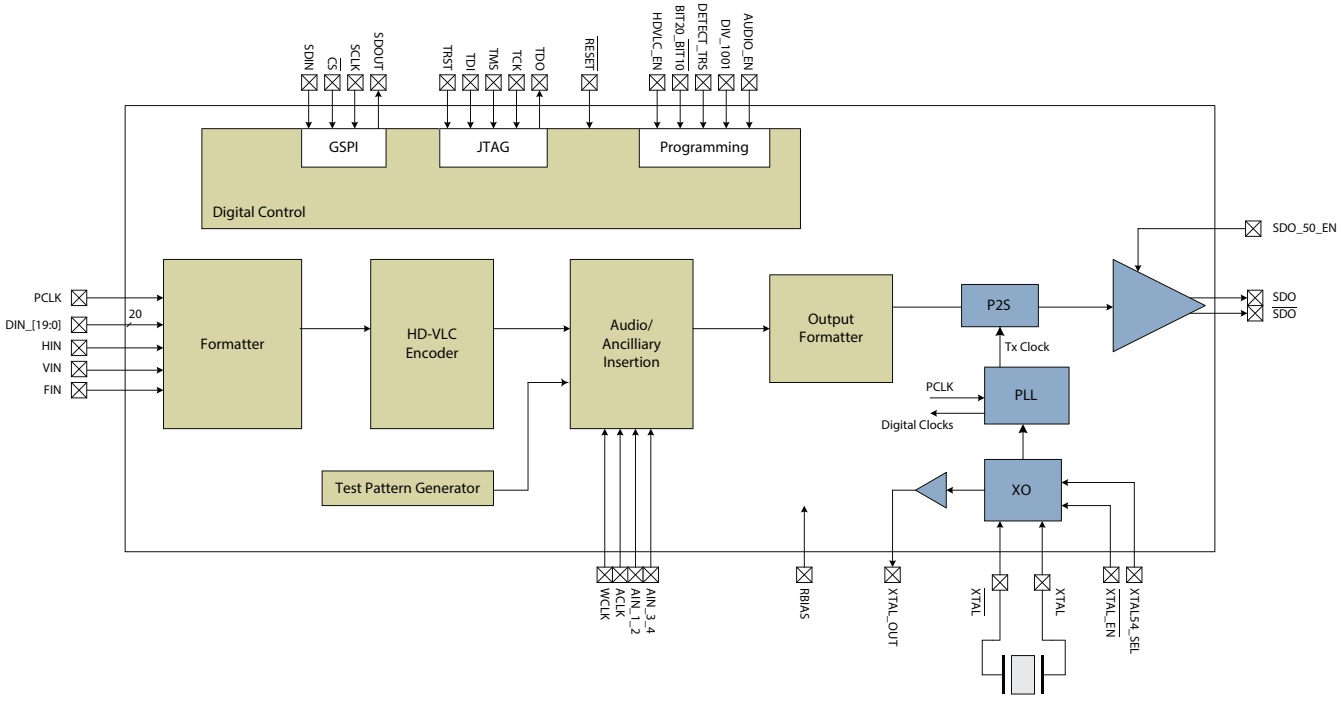
The GV7700 features an audio embedding core, which supports up to 4 channels of I^2S serial digital audio within the ancillary data space of the video data stream. The audio embedding core supports 32kHz, 44.1kHz, and 48kHz sample rates.

The GV7700 supports the insertion of ancillary data into the horizontal blanking of the video data stream. User data can be programmed via the GSPI, allowing downstream communication from the video source to sink device. The ancillary data packing format is compliant with HDcctv 2.0 communications protocol.

Packaged in a space-saving 84-pin dual-row QFN, the GV7700 is ideal for single PCB security cameras, where high-density component placement is required. Typically requiring only 180mW of power, the device does not require any special heat sinking or air flow, reducing the over-cost of HD security camera designs.

[1] *Frame structure with encoded HD only. Does not support SD/D1 video.*

Functional Block Diagram



GV7700 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Description
8	029991	—	March 2016	Addition of Figure 3-3: XTAL_N, XTAL_P, XTAL_EN. Updates to values in Table 4-6: Cable Reach for Various Cable Types (In Meters).
7	029012	—	December 2015	Updated values in Table 2-3: AC Electrical Characteristics.
6	028866	—	December 2015	Updated to Final Data Sheet from Preliminary Data Sheet.
5	027517	—	September 2015	Removed Proprietary and Confidential from footer. Updated Table 1-1, Table 2-3, Section 4.4, Section 4.11, Section 4.14, Figure 4-18, and Figure 6-1. Added Figure 6-2.
4	027026	—	July 2015	Updated cable reach values. Updated Table 2-2 and Table 2-3.
3	025836	—	May 2015	Updated to Preliminary Data Sheet from Draft Data Sheet
2	025126	—	April 2015	Updated GV7700 Functional Block Diagram, Figure 1-1, Figure 6-1. Updated Table 2-2 and Table 2-3. Various updates throughout document.
1	024223	—	February 2015	Updated Table 1-1, Table 2-2, Section 4.1
0	020611	—	August 2014	New Document

Contents

1. Pin Out

1.1 GV7700 Pin Assignment

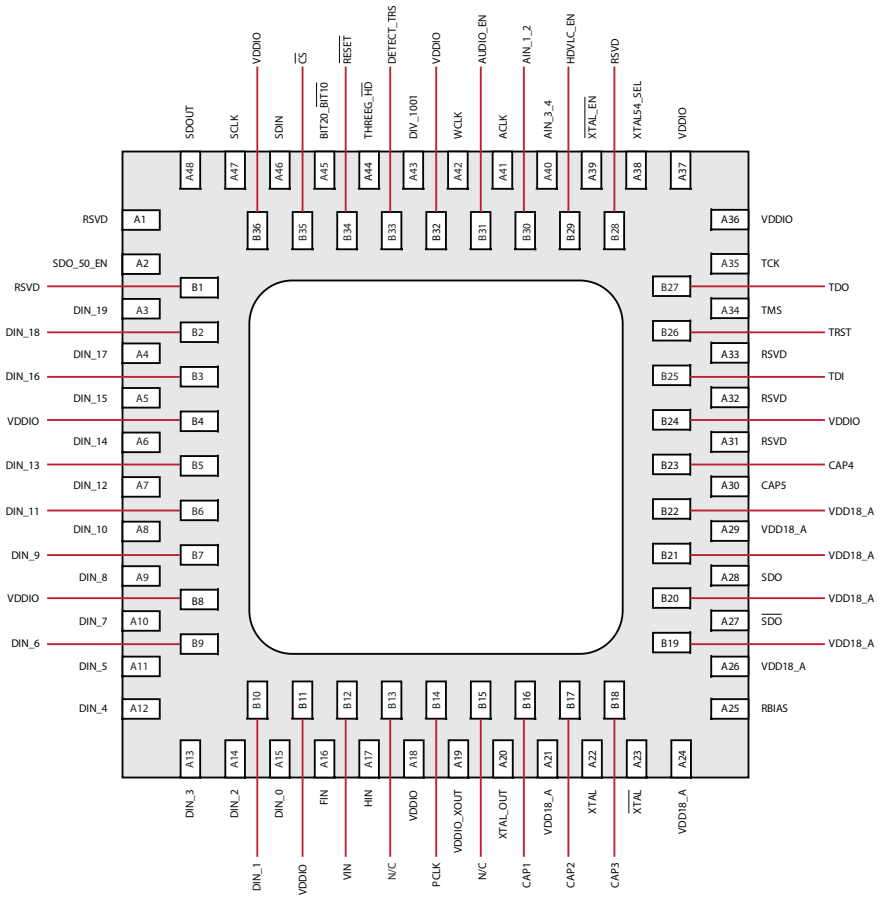


Figure 1-1: GV7700 Pin Out

1.2 Pin Descriptions

Table 1-1: GV7700 Pin Descriptions

Pin Number	Name	Type	Description
A1	RSVD	—	Connect to ground.
A2	SDO_50_EN	Input	HIGH = device outputs a 100Ω differential signal. LOW = device outputs a 75Ω single-ended output signal, with both complementary outputs ON by default. Each output can be manually disabled via GSPI. Schmitt Trigger Input with Pull-Down.
B1	RSVD	—	Connect to ground.
A3, B2, A4, B3, A5, A6, B5, A7, B6, A8	DIN_[19:10]	Input	Parallel data bus inputs [19:10]. If BIT20_$\overline{\text{BIT10}}$ = HIGH, the input data format must be word aligned, demultiplexed Luma and Chroma data. DIN_[19:10] are the input pins for Luma data. If BIT20_$\overline{\text{BIT10}}$ = LOW, the multiplexed Luma and Chroma data is presented on these pins.
B7, A9, A10, B9, A11 A12, A13, A14, B10, A15	DIN_[9:0]	Input	Parallel data bus inputs [9:0]. If BIT20_$\overline{\text{BIT10}}$ = HIGH, the input data format must be word aligned, demultiplexed Luma and Chroma data. DIN_[9:0] are the input pins for Chroma data. If BIT20_$\overline{\text{BIT10}}$ = LOW, these pins are unused and should be tied to ground.
B4, B8, B11, A18, B24, A36, A37, B32, B36	VDDIO	Power	Connect to 1.8V or 3.3V.
A16	FIN	Input	Field identification. Used in interlaced mode.
B12	VIN	Input	Vertical blanking.
A17	HIN	Input	Horizontal blanking.
B13	N/C	—	Do not connect.
B14	PCLK	Input	148.5MHz/74.25MHz input clock representing the time allocated to one 10 or 20-bit pixel.
A19	VDDIO_XOUT	Power	Connect to 1.8V or 3.3V[1].
B15	N/C	—	Do not connect.
A20	XTAL_OUT	Analog Output	Output capable of driving ISP clock input.
A21, A24, A26, B19, B20, B21, A29, B22	VDD18_A	Power	Connect to 1.8V.
B16	CAP1	Analog Input/Output	Must connect to external decoupling filter. Refer to Figure 6-1: GV7700 Typical Application Circuit.

Table 1-1: GV7700 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
B17	CAP2	Analog Input/Output	Must connect to external decoupling filter. Refer to Figure 6-1: GV7700 Typical Application Circuit.
A22	XTAL	Analog Input/Output	Pin to external 27MHz or 54MHz crystal. When not using a crystal reference ($\overline{\text{XTAL\_EN}}$ = HIGH), connect XTAL to ground.
B18	CAP3	Analog Input/Output	Must connect to external decoupling filter. Refer to Figure 6-1: GV7700 Typical Application Circuit.
A23	$\overline{\text{XTAL}}$	Analog Input/Output	Pin to external 27MHz or 54MHz crystal. When not using a crystal reference ($\overline{\text{XTAL\_EN}}$ = HIGH), $\overline{\text{XTAL}}$ can be left floating.
A25	RBIAS	Analog Input/Output	External 11kΩ resistor for bias reference. Connect the resistor to ground.
A27, A28	$\overline{\text{SDO}}$, SDO	Analog High-Speed Output	Serial differential output signal. Single-ended operation at data rates of 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s, 540Mb/s, or 270Mb/s.
B23	CAP4	Analog Input/Output	Must connect to external decoupling filter. Refer to Figure 6-1: GV7700 Typical Application Circuit.
A30	CAP5	Analog Input/Output	Must connect to external decoupling filter. Refer to Figure 6-1: GV7700 Typical Application Circuit.
A31	RSVD	—	Connect to ground.
A32	RSVD	—	This pin must be set HIGH.
B25	TDI	Input	Dedicated JTAG pin – Test data input. This pin is used to shift JTAG test data into the device. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin may be left floating.
A33	RSVD	—	Connect to ground.
B26	TRST	Input	Dedicated JTAG pin – Test Reset. When set LOW, the JTAG logic will be reset. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin must be pulled LOW.
A34	TMS	Input	Dedicated JTAG pin – Test Mode Select. This pin is used to control the operation of the JTAG test. Schmitt Trigger Input with Pull-Up. If JTAG is not used this pin may be left floating.
B27	TDO	Output	Dedicated JTAG pin – Test data output. This pin is used to shift results from the device.

Table 1-1: GV7700 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
A35	TCK	Input	Dedicated JTAG pin – Serial data clock signal. This pin is the JTAG clock. Schmitt Trigger Input. If JTAG is not used this pin must be pulled LOW.
A38	XTAL54_SEL	Input	HIGH = for use with a 54MHz crystal. LOW = for use with a 27MHz crystal (default). Schmitt Trigger Input with Pull-Down.
B28	RSVD	—	Connect to ground
A39	$\overline{\text{XTAL\_EN}}$	Input	HIGH = when using the PCLK input as a frequency reference. LOW = when using an external XTAL as a frequency reference. Schmitt Trigger Input with Pull-Down.
B29	HDVLC_EN	Input	HIGH = Enables HD-VLC compression for extended cable reach. LOW = Disables HD-VLC compression.
A40	AIN_3_4	Input	I^2S Serial Audio Input; Channels 3 and 4. Schmitt Trigger Input.
B30	AIN_1_2	Input	I^2S Serial Audio Input; Channels 1 and 2. Schmitt Trigger Input.
A41	ACLK	Input	Serial Audio Input bit clock. Serial bit clock for audio data from pins AIN_1_2 and AIN_3_4. Schmitt Trigger Input.
B31	AUDIO_EN	Input	HIGH = Enables the device to support the insertion of 4 audio channels. LOW = Disables device audio support.
A42	WCLK	Input	Serial Audio Left/Right Clock. Word rate clock for the audio data from pins AIN_1_2 and AIN_3_4. Supports sampling frequencies of 32KHz, 44.1kHz, and 48kHz. Schmitt Trigger Input.
A43	DIV_1001	Input	HIGH = Enable device support for when the incoming frame rate is 60/1.001 or 30/1.001 frames per second. LOW = When the incoming frame rate is 60, 50, 30, or 25 frames per second.
A44	THREEG_$\overline{\text{HD}}$	Input	HIGH = 3G video input. LOW = HD video input.
B33	DETECT_TRS	Input	Control Signal Input. Used to select external HVF timing mode or TRS extraction timing mode. LOW = the device extracts all internal timing from the supplied H:V:F. HIGH = the device extracts all internal timing from TRS signals embedded in the supplied video stream.

Table 1-1: GV7700 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
B34	$\overline{\text{RESET}}$	Input	Digital active-low reset input. Used to reset the internal operating conditions to default settings. Minimum reset duration of 10ms. See Section 4.14. Device configuration pins should be set prior to device reset. Schmitt Trigger Input.
A45	BIT20_$\overline{\text{BIT10}}$	Input	HIGH = Selects 20-bit wide input interface. LOW = Selects 10-bit wide input interface.
B35	$\overline{\text{CS}}$	Input	Chip select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. Active-low input.
A46	SDIN	Input	Serial data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port.
A47	SCLK	Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port.
A48	SDOUT	Output	Serial data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port.
—	Center Pad	Power	Common analog and digital ground connection, and main thermal path for device.

Notes:

1. Serial output jitter increases by 10ps at 3.3V.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage, Digital I/O (VDDIO)	-0.5V to +3.6V
Supply Voltage, Analog (VDD18_A)	-0.5V to +2.5V
DC Input Voltage, V_{IN} (except I/O pins)	-0.5V to (VDDIO + 0.5V)
DC Output Voltage, V_{OUT} (except I/O pins)	-0.5V to (VDDIO + 0.5V)
Input ESD Voltage (HBM)	2.5kV
Input ESD Voltage (CDM)	1kV
Storage Temperature Range (T_S)	-50°C to 125°C
Operating Temperature Range (T_A)	-40°C to 85°C
Solder Reflow Temperature (4s)	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC and DC Electrical Characteristics is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

VDD18_A = 1.8V±5% and TA = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, Digital I/O	VDDIO	1.8V mode	1.71	1.8	1.89	V	—
		3.3V mode	3.13	3.3	3.47	V	—
Supply Voltage, Analog	VDD18_A		1.71	1.8	1.89	V	—
Supply Current, Digital I/O	I_{DDIO}	1.8V mode	—	0.25	0.5	mA	—
		3.3V mode	—	3.5	4.75	mA	—
Supply Current, Analog	I_{DD18_A}		—	100	115	mA	1

Table 2-2: DC Electrical Characteristics (Continued)

VDD18_A = 1.8V±5% and TA = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Total Power Consumption	P_{total}	HD mode	—	140	170	mW	2
		3G mode	—	160	180	mW	2
		270 mode	—	180	215	mW	2
		540 mode	—	240	275	mW	2
External RBIAS Resistor			10.89	11	11.1	kΩ	—
Power Supply Noise Mask		0Hz–1.5GHz	—	—	20	mV_{pp}	3
Digital Logic Input	V_{IL}	Input LOW	-0.3	—	0.63	V	—
	V_{IH}	Input HIGH	1.17	—	3.465	V	—
Digital Logic Output	V_{OL}	Output LOW	—	—	0.45	V	—
	V_{OH}	Output HIGH	1.35	—	—	V	—

Notes:

1. SD mode.
2. Max = 85°C, VDD18_A = 1.89V.
3. Using recommended power supply decoupling. See Figure 6-1: GV7700 Typical Application Circuit.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VDD18_A = 1.8V±5% and TA = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Input Conditions							
Input PCLK clock frequency		10-bit mode	—	148.5	—	MHz	1
		20-bit mode	—	74.25	—	MHz	1, 3
PCLK Duty Cycle	DC_{PCLK}		40	—	60	%	—
Input Data Setup Time	t_{SU}		1.2	—	—	ns	—
Input Data Hold Time	t_{HOLD}		0.8	—	—	ns	—
Output Driver							
Impedance		75Ω single-ended	66	75	84	Ω	—
		100Ω differential	88	100	112	Ω	—

Table 2-3: AC Electrical Characteristics (Continued)

VDD18_A = 1.8V±5% and TA = -20°C to +85°C unless otherwise stated

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Return loss		1MHz - 5MHz	—	—	17.9	dB	—
		5MHz - 1.485GHz	—	—	6.7	dB	—
		1.485GHz - 2.25GHz	—	—	4	dB	—
Amplitude		75Ω single-ended	0.36	0.8	0.9	V_{pp}	—
		100Ω differential	0.36	0.8	0.9	V_{ppd}	—
Rise/Fall Time		100Ω differential 20% - 80%	—	85	95	ps	—
		75Ω single-ended 20% - 80%	—	102	150	ps	—
Rise/Fall Time Mismatch		20% - 80%	—	—	50	ps	—
Overshoot			—	—	10	%	—
Output Total Jitter		Data rate = 270Mb/s	—	0.021	—	UI_{pp}	2
		Data rate = 540Mb/s	—	0.04	—	UI_{pp}	2
		Data rate = 1.485Gb/s	—	0.115	—	UI_{pp}	2
		Data rate = 2.97Gb/s	—	0.2	—	UI_{pp}	2
De-emphasis		Post-Cursor	0	1	—	dB	—
Crystal Oscillator							
External Crystal Reference Frequency			—	27 or 54	—	MHz	—
Load Capacitance			8	—	9	pF	—
Start-up time			—	100	—	ms	—
Accuracy			—	±20	±100	ppm	—
GSPI Digital Control							
GSPI Read/Write Clock Frequency			—	—	40	MHz	—
Reset Time			10	—	—	ms	—
Register Access Time			—	—	300	ns	—

Notes:

1. If DIV_1001 = HIGH, divide the listed PCLK frequency by 1.001.
2. Jitter performance is only guaranteed when using a crystal (27/54MHz) as the clock reference for the device. Jitter performance is not guaranteed when using the PCLK clock generated by the ISP as the reference for the device.
3. In 3G 20-bit mode, the PCLK is 148.5MHz.

3. Input/Output Circuits

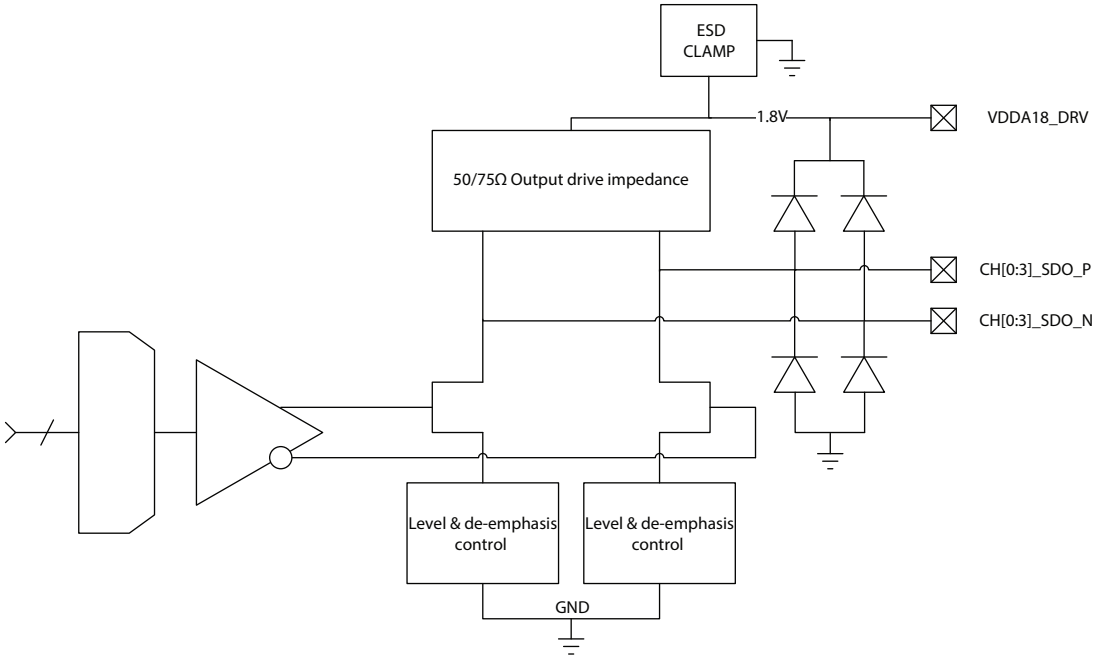


Figure 3-1: Serial Output Driver

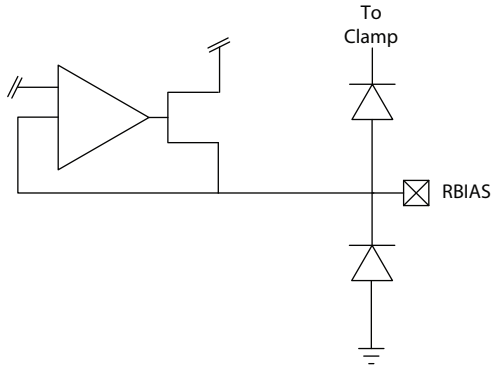


Figure 3-2: RBIAS

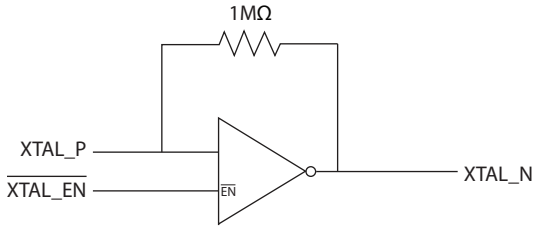


Figure 3-3: XTAL_N, XTAL_P, $\overline{\text{XTAL\_EN}}$

4. Detailed Description

4.1 Functional Overview

The GV7700 is a low cost, dual-rate HDcctv transmitter with integrated HD-VLC encoding. With integrated cable driving technology, the GV7700 is capable of transmitting compressed video at 270Mb/s or 540Mb/s, or uncompressed video at 1.485Gb/s or 2.97Gb/s, over 75Ω coaxial cable. Compressed signals can also be transmitted differentially over 100Ω twisted pair cable.

The High Definition Visually Lossless CODEC (HD-VLC™) technology is integrated in order to reduce the transmission data rate of HD video over both coaxial and unshielded twisted pair (UTP) cable. This is achieved by encoding the HD-SDI video, normally transmitted at a serial data rate of 1.485Gb/s, to the same rate as Standard Definition (SD-SDI) video, at 270Mb/s serial data rate. This provides extended cable reach for HD video up to 550m over Belden 543945 CCTV coax or 150m over Cat-5e/6 UTP cable. Similarly, 3G-SDI normally transmitted at 2.97Gb/s can be encoded down to 540Mb/s.

The GV7700 features an audio embedding core, which supports up to 4 channels of I^2S serial digital audio within the ancillary data space of the video data stream. The audio embedding core supports 32kHz, 44.1kHz, and 48kHz sample rates.

The device allows for both 8-bit and 10-bit per pixel YCbCr 4:2:2 BT.1120 component digital video. A configurable 20-bit wide parallel digital video input bus is provided, with associated pixel clock and H/V/F timing signal inputs.

The GV7700 supports the insertion of ancillary data into the horizontal blanking of the video data stream. User data can be programmed via the GSPI, allowing downstream communication from the video source to sink device. The ancillary data packing format is compliant with HDcctv 2.0 communications protocol.

The device includes a 4-wire Gennum Serial Peripheral Interface (GSPI 2.0) for external host command and control. All read or write access to the GV7700 is initiated and terminated by the application host processor. The host interface is provided to allow optional configuration of some of the functions and operating modes of the GV7700.

It is recommended to use the integrated low-noise crystal oscillator and an external crystal as the primary reference clock for the GV7700. This configuration will yield the optimal jitter performance. Degraded performance will likely occur when using a PCLK input from the ISP which typically has much more jitter. A derived clock must be used as the clock reference by the Image Signal Processing (ISP) IC to avoid any frequency mismatch. In this case, connect the GV7700's XTAL_OUT pin to the ISP's reference frequency input. Crystal values of 27MHz or 54MHz may be used, depending on the ISP requirement. XTAL54_SEL must be HIGH when using a 54MHz crystal and LOW when using a 27MHz crystal.

Jitter performance is only guaranteed when using a crystal (27/54MHz) as the clock reference for the device. Jitter performance is not guaranteed when using the PCLK clock generated by the ISP as the reference for the device.

4.2 Parallel Video Data Inputs DIN_[19:0]

Data signal inputs enter the device on the rising edge of PCLK, as shown in Figure 4-1.

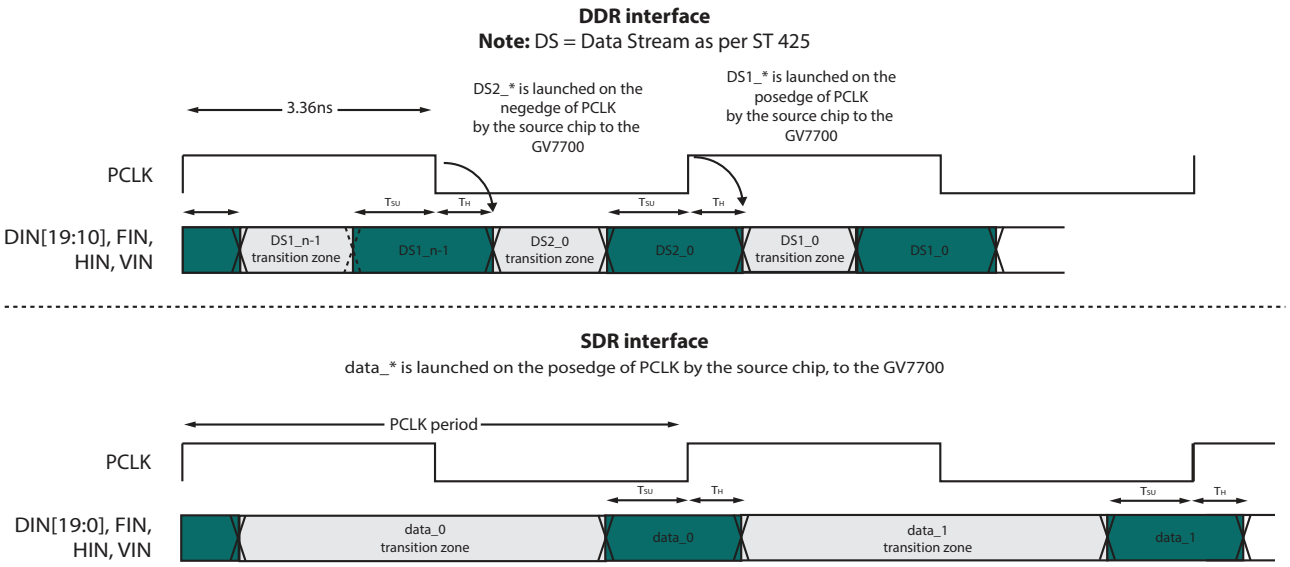


Figure 4-1: GV7700 Video Interface Timing Diagram

Table 4-1: GV7700 Parallel Input AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input data set-up time	T_{SU}	50% levels; 1.8V operation	1.2	—	—	ns
Input data hold time	T_H		0.8	—	—	ns

The GV7700 is a high performance serial digital video and audio transmitter. Source series termination resistors should be used to minimize reflections on the parallel video data inputs, PCLK, audio inputs, and H, V, F timing input signals. This will ensure that signals are received correctly by the GV7700. Resistors must be placed at the signal source away from the GV7700 inputs.

4.2.1 Parallel Input In Video Mode

Data must be presented to the input bus in either multiplexed or demultiplexed form, depending on the setting of the BIT20_$\overline{\text{BIT10}}$ pin.

When operating in 20-bit mode (BIT20_$\overline{\text{BIT10}}$ = HIGH), the input data format must be word aligned, demultiplexed Luma and Chroma data. The Luma (Y) data must be presented on the DIN[19:10] pins, and the Chroma (Cb/Cr) data must be presented on the DIN[9:0] pins.

When operating in 10-bit mode (BIT20_$\overline{\text{BIT10}}$ = LOW), the input data format must be word aligned, multiplexed Luma and Chroma data. In this mode, the data must be presented on the DIN[19:10] pins. The DIN[9:0] inputs are ignored and should be tied to ground.

When operating in 10-bit mode (BIT20_BIT10 = LOW) with 3G video (THREEG_$\overline{HD}$ = HIGH), the PCLK input is DDR 148.5MHz.

4.2.1.1 High Definition Video Input Formats

ITU-R BT.1120 describes the serial and parallel format for 1080-line interlaced and progressive digital video. The field/frame blanking period (V), the line blanking period (H), and the field identification (F), are embedded as digital timing codes (TRS) within the video. Data is transmitted over two 10-bit buses, one for Luma (Y') and one for colour difference ($C'_BC'_R$), operating at a clock rate of 74.25MHz or 74.25/1.001MHz.

The following figures show horizontal and vertical timing for 1080-line interlaced systems.

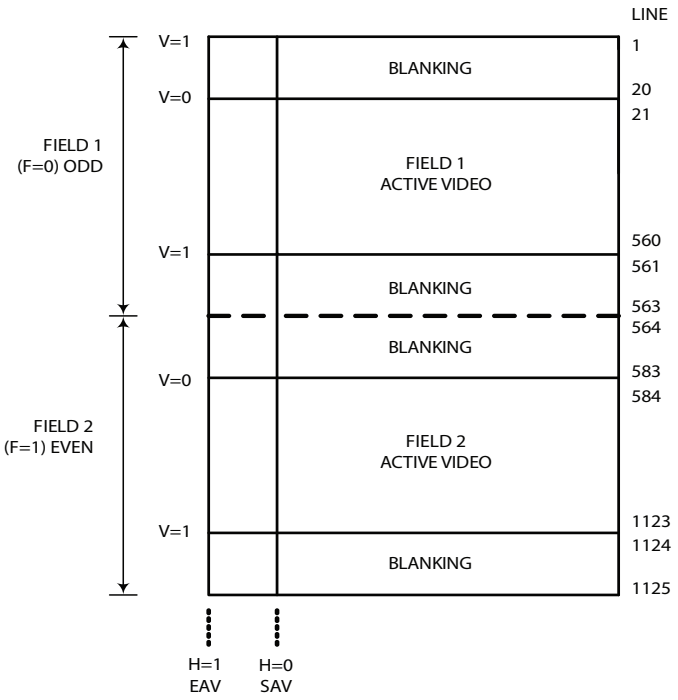


Figure 4-2: Field Timing Relationship for 1080-line Interlaced Systems

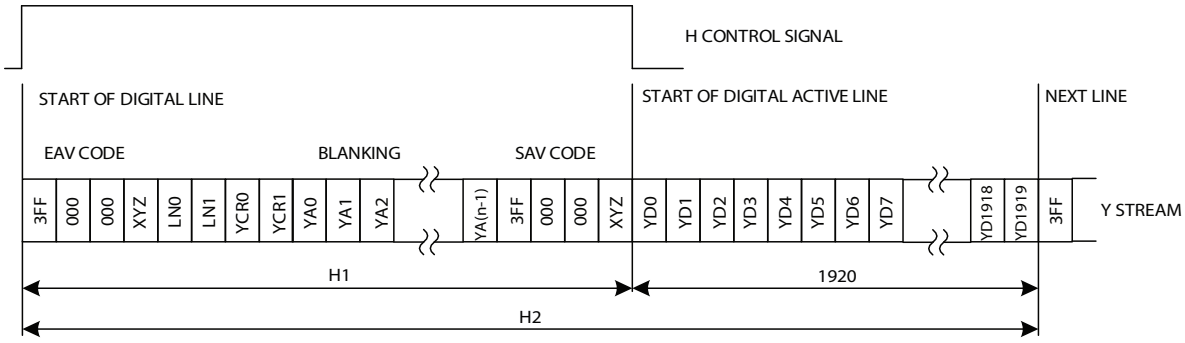


Figure 4-3: Luma Stream Over One Video Line - 1080i

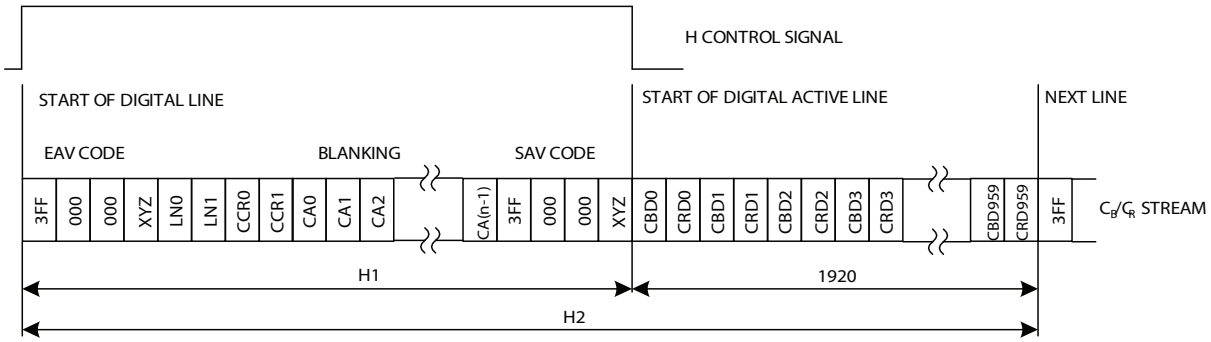


Figure 4-4: Chroma Stream Over One Video Line - 1080i

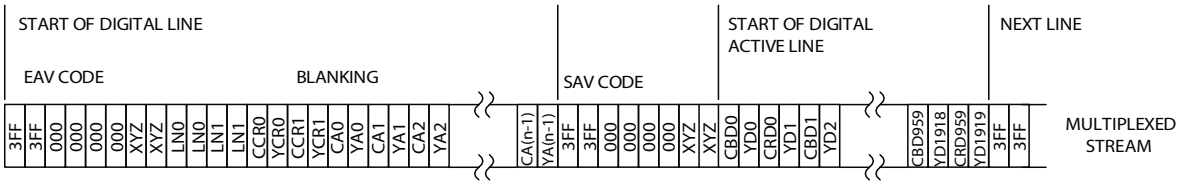


Figure 4-5: Multiplexed Luma and Chroma Over One Video Line - 1080i

Table 4-2: 1080-line Interlaced Horizontal Timing

Interlaced	60Hz or 60/1.001Hz	50Hz
H1	280	720
H2	2200	2640

4.2.1.2 High Definition 1080p Input Formats

ITU-R BT.1120 also includes progressive scan formats with 1080 active lines, with $Y'C'_BC'_R$ 4:2:2 sampling at pixel rates of 74.25MHz or 74.25/1.001MHz. The following diagrams show horizontal and vertical timing for 1080-line progressive systems.

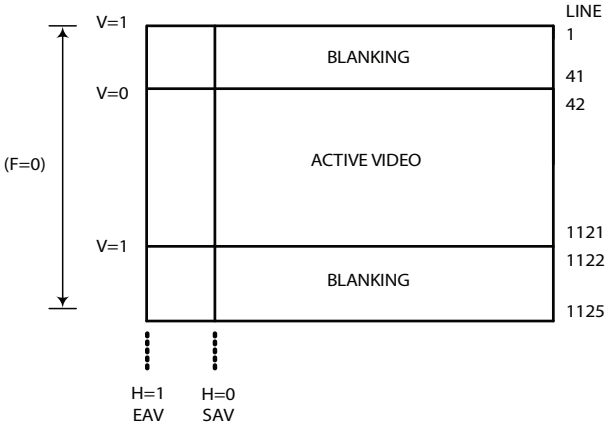


Figure 4-6: Frame Timing Relationship For 1080-line Progressive Systems

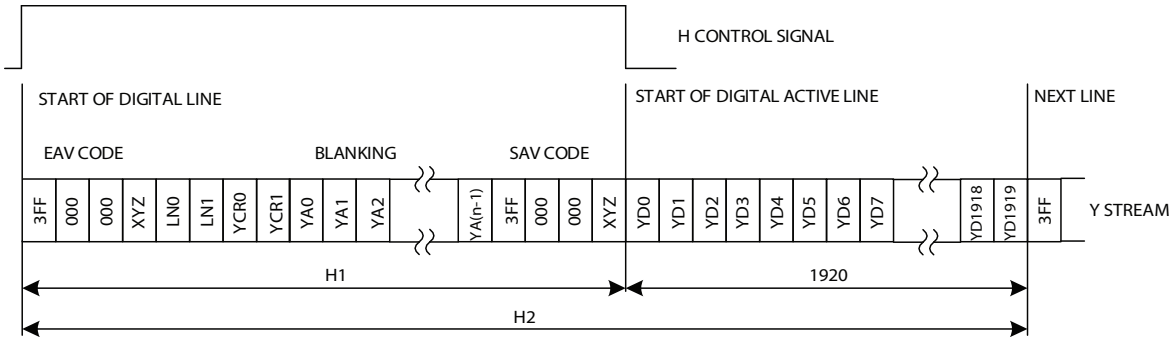


Figure 4-7: Luma Stream Over One Video Line - 1080p

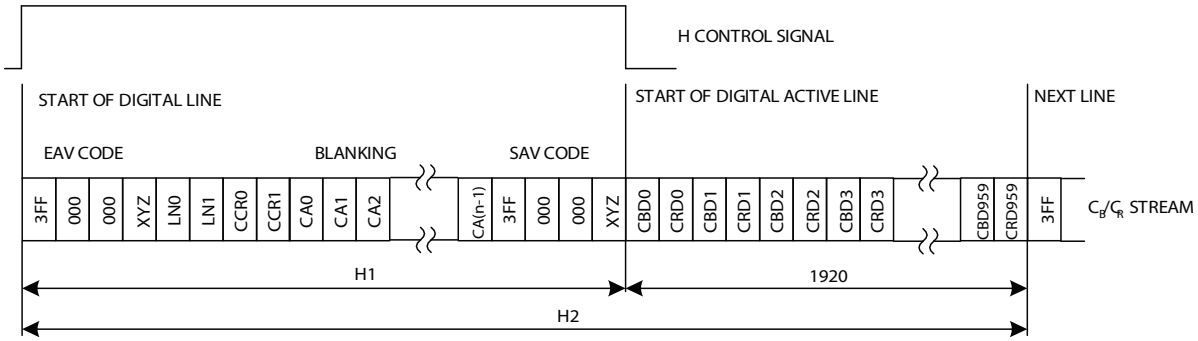


Figure 4-8: Chroma Stream Over One Video Line - 1080p

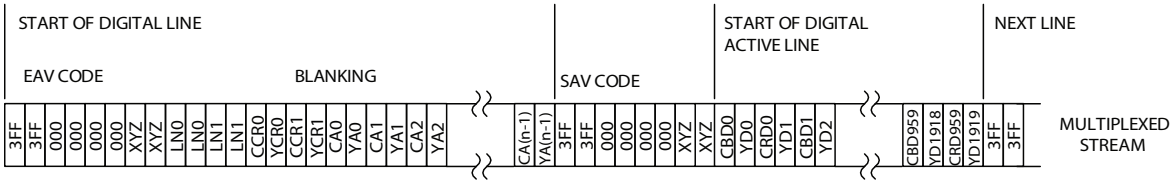


Figure 4-9: Multiplexed Luma and Chroma Over One Video Line - 1080p

Table 4-3: 1080-line Progressive Horizontal Timing

Progressive	30Hz, 30/1.001Hz, 60Hz, 60/1.001Hz	25Hz or 50Hz	24Hz or 24/1.001Hz
H1	280	720	830
H2	2200	2640	2750

4.2.1.3 High Definition 720p Input Formats

The Society of Motion Picture and Television Engineers (SMPTE) defines the standard for progressive scan 720-line HD image formats. SMPTE ST 296-2001 specifies the representation for 720p digital $Y'C'_BC'_R$ 4:2:2 signals at pixel rates of 74.25MHz or 74.25/1.001MHz.

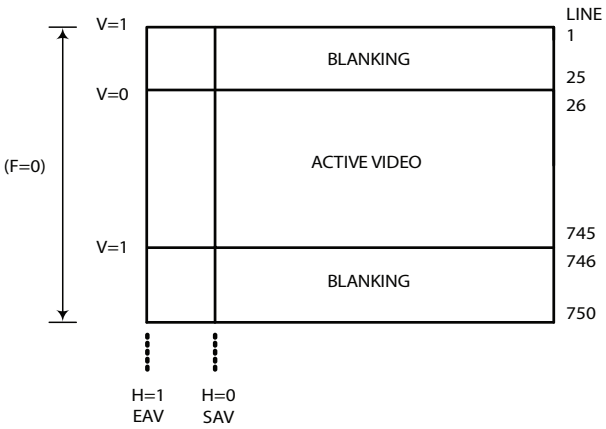


Figure 4-10: 720p Digital Vertical Timing

The frame rate determines the horizontal timing, which is shown in Table 4-4.

Table 4-4: 720p Horizontal Timing

Frame Rate	H = 1 Sample Number	H = 0 Sample Number	Total Samples Per Line
25	1280	0	3960
30 or 30/1.001	1280	0	3300
50	1280	0	1980
60 or 60/1.001	1280	0	1650

4.2.1.4 3G-SDI 1080p Input Formats

The Society of Motion Picture and Television Engineers (SMPTE) defines the standard for 3G-SDI image formats in ST 425. The GV7700 supports 1080p50/60 Y'C'$_B$C'$_R$ 4:2:2 8/10-bit.

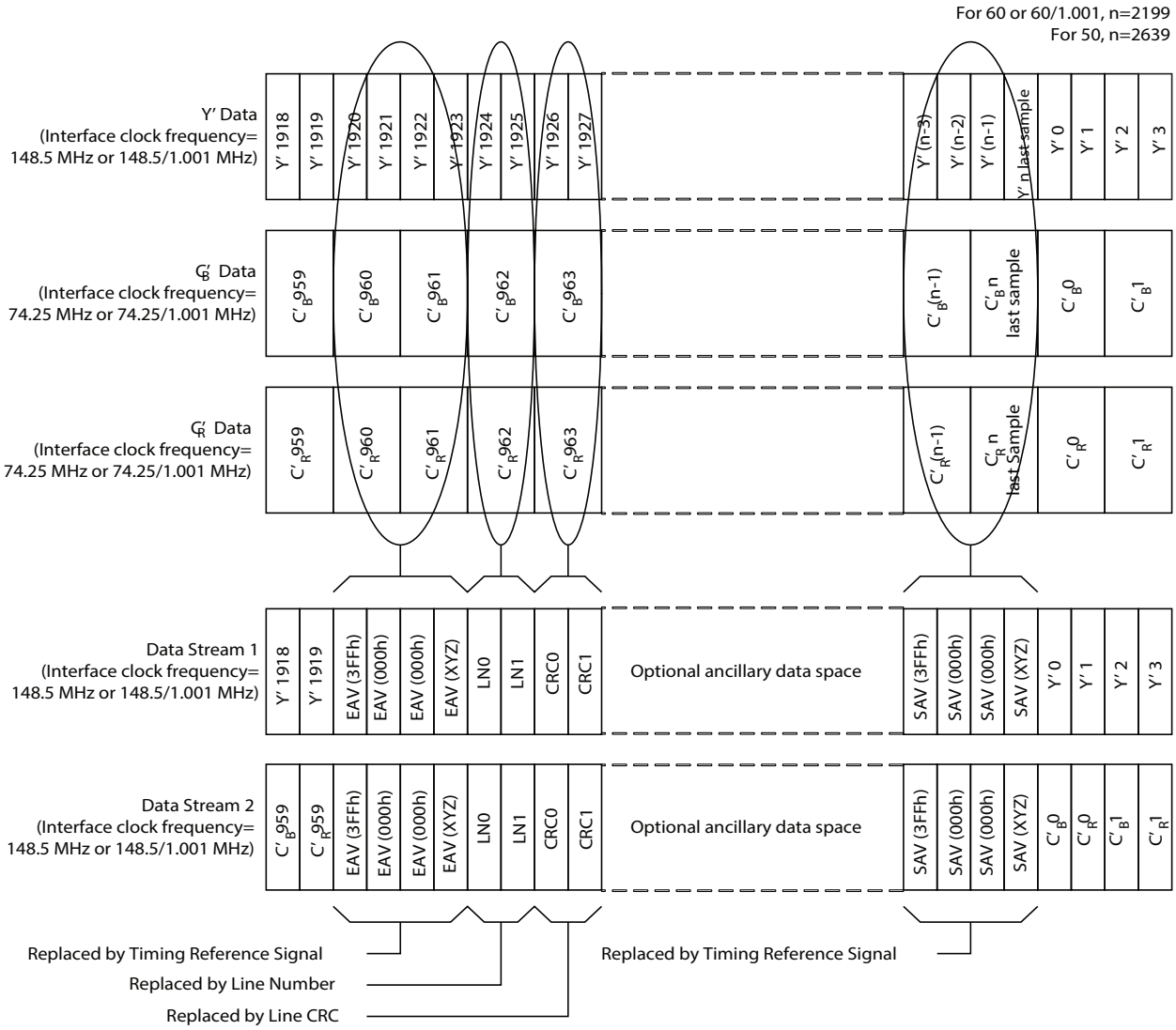


Figure 4-11: 20-bit Mapping Structure for 1920 x 1080 50/60Hz Progressive 4:2:2 (Y'C'BC'R) 8/10-bit Signals

Table 4-5: 1080p Y′C′$_B$C′$_R$ 4:2:0 & 4:2:2 10-bit Bit Structure Mapping

Data Stream	Bit Number									
	9	8	7	6	5	4	3	2	1	0
DS1	Y′[9:0]									
DS2	C′$_B$C′$_R$[9:0]									

Note: For 8-bit systems, the data should be justified to the most significant bit (Y′9 and C′$_B$C′$_R$9), with the two least significant bits (Y′[1:0] and C′$_B$C′$_R$[1:0]) set to zero.

4.3 Video Processing

The GV7700 is designed to carry out data scrambling according to ITU-R BT.1120, and to carry out NRZ to NRZI encoding prior to presentation to the parallel to serial converter.

4.3.1 H:V:F Timing

The GV7700 can automatically detect the video standard and generate all internal timing signals. The total line length, active line length, total number of lines per field/frame and total active lines per field/frame are calculated for the received parallel video.

When DETECT_TRS is LOW, the video standard and timing signals are based on the externally supplied horizontal blanking, vertical blanking, and field identification signals. These signals go to the HIN, VIN, and FIN pins respectively. When DETECT_TRS is HIGH, the video standard timing signals are extracted from the embedded TRS ID words in the parallel input data. Both 8-bit and 10-bit TRS code words are identified by the device.

The GV7700 determines the video standard by timing the horizontal and vertical reference information supplied at the HIN, VIN, and FIN input pins, or contained in the TRS ID words of the received video data. Therefore, full synchronization to the received video standard requires at least one complete video frame.

Once synchronization has been achieved, the GV7700 continues to monitor the received TRS timing or the supplied H, V, and F timing information to maintain synchronization. The GV7700 loses all timing information immediately following loss of H, V, and F.

The timing of these signals is shown in Figure 4-12 to Figure 4-13 below.

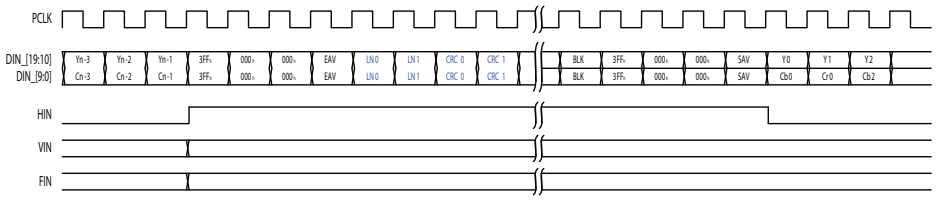


Figure 4-12: H:V:F Input Timing — HD 20-bit Input Mode

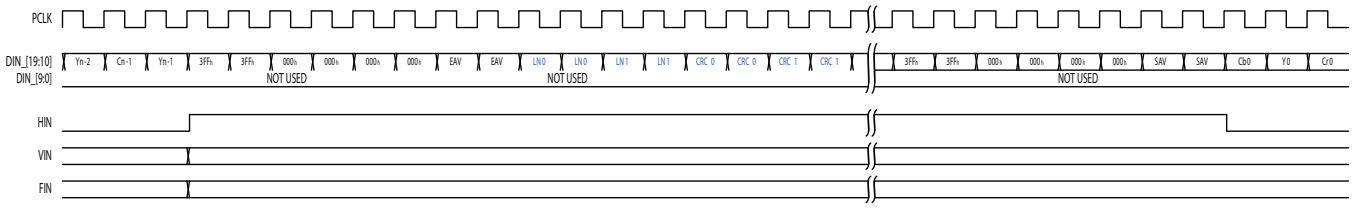


Figure 4-13: H:V:F Input Timing — HD 10-bit Input Mode

4.4 HD-VLC™ Encoder

The GV7700 integrates the High Definition Visually Lossless CODEC (HD-VLC) encoder for extended reach video transmission. When used in conjunction with the GV7704 HD-VLC Quad Receiver, HD video transmission can be extended significantly over existing HD serial digital video systems. HD-VLC is based on a simple visually lossless implementation of the Dirac compression tool kit. The visually lossless encoder is used to reduce the video bandwidth, using a very low latency mode, from a transmission rate of 1.485Gb/s (HD-SDI) to 270Mb/s (SD-SDI).

At a data rate of 270Mb/s, the serial digital encoded HD video can be transmitted over longer runs of coaxial cable. Table 4-6 below shows a comparison of cable distances between HD video transmission at 1.485Gb/s and HD-VLC encoded at 270Mb/s for various common coaxial cable types.

Table 4-6: Cable Reach for Various Cable Types (In Meters)

Cable Type	HD-VLC: 270Mb/s (m)	HD-VLC: 540Mb/s (m)	HD-SDI: 1.485Gb/s (m)	3G-SDI: 2.97Gb/s (m)
Belden 1694A / Canare L-4.5CHD	710	400	230	80
Belden 543945	550	300	150	50
KW-Link SYV 75-5	500	275	140	50
Canare L-3C2V	300	160	95	30
KW-Link SYV 75-3	300	160	80	30

Note: These values apply for new, properly terminated cables. Actual performance may vary.

Note: Longer cable reach performance at both 3G and 540M is possible; up to 100m at 3G and 400m at 540M can be achieved using Belden 543945. However, GV7704 lock times can increase significantly at these cable ranges, and may exceed the lock time requirements of the intended application.

After transmission over the coaxial cable, the 270Mb/s serial data is recovered using the GV7704 HD-VLC Quad Receiver and the data decoded back to the native HD format. The encoding and decoding process has a total latency of 12-14 HD lines, which makes the CODEC ideal for low latency real-time applications. Table 4-7 below shows the total encode/decode latency through the GV7700 and the GV7704.

Table 4-7: Encode and Decode Total Latency (GV7700 + GV7704)

Video Format	Delay (µs)	Delay (HD/3G Lines)
1080p25	422.2	11.9
1080p29.97	368.8	12.4
1080p30	368.4	12.4
720p25	635.1	11.9
720p29.97	546.6	12.2
720p30	546.6	12.2
720p50	368.6	13.8
720p59.94	324.2	14.5
720p60	324.2	14.5
1080p60	184.2	12.4
1080p59.94	184.4	12.4
1080p50	211.1	11.9

The HD-VLC encoder can be enabled by setting the HDVLC_EN input pin HIGH. When this pin is set HIGH, the GV7700 will output HD encoded video at 270Mb/s and 3G encoded video at 540Mb/s. Configuration pins should be set prior to device reset. The 270Mb/s data stream uses the same timing and frame structure as Standard Definition SDI (SD-SDI), and can be monitored using standard SD-SDI test equipment to check signal integrity. However, the data contained within the active picture area of the SD-SDI stream contains only encoded HD packets. The HD video content can only be viewed after the HD-VLC decoding process.

When the GV7700 is HD-VLC encoding video formats at “true” 30 or 60 frames per second, the 270Mb/s (540Mb/s) serial data output will actually operate at 270x1.001Mb/s (540x1.001Mb/s). This multiplication factor is to account for the fractional increase in the original HD video frame rate. For all other HD frame rates, the GV7700 serial data output will be exactly 270Mb/s (540Mb/s).

4.5 Stream ID Packet Insertion

The GV7700 will always insert Stream ID packets immediately after the CRC1 word of the Y channel if the chip is in Reclocker mode (HDVLC_EN = 0) or immediately after the CRC1 word of the YCbCr multiplexed data if the chip is in HD-VLC compression mode (HDVLC_EN = 1).

The chip will insert the Stream ID packet on the following lines shown in Table 4-8 below.

Table 4-8: Stream ID Line Insertion for Video Standards

Input Video Standard	HDVLC_EN	Output Video Standard	Line Number for Insertion
720p25	0	720p25	8
	1	625i50	7, 320
720p29.97	0	720p29.97	8
	1	525i59.94	11, 274
720p30	0	720p30	8
	1	525i60	11, 274
720p50	0	720p50	8
	1	625i25	7, 320
720p59.94	0	720p59.94	8
	1	525i29.97	11, 274
720p60	0	720p60	8
	1	525i30	11, 274
1080p25	0	1080p25	8
	1	625i25	7, 320
1080p29.97	0	1080p29.97	8
	1	525i29.97	11, 274
1080p30	0	1080p30	8
	1	525i30	11, 274
1080i50	0	1080i50	8, 570
	1	625i25	7, 320
1080i59.94	0	1080i59.94	8, 570
	1	525i29.97	11, 274
1080p60	0	1080p60	8
	1	525i69	11, 274

Table 4-8: Stream ID Line Insertion for Video Standards (Continued)

Input Video Standard	HDVLC_EN	Output Video Standard	Line Number for Insertion
1080p59.94	0	1080p59.94	8
	1	525i59.94	11, 274
1080p50	0	1080p50	8
	1	625i50	7, 320

4.6 Audio Embedding

The GV7700 includes an Audio Multiplexer, which is enabled by setting the AUDIO_EN pin HIGH. The device will embed audio in both HD and HD-VLC encoding modes.

The GV7700 can embed up to four channels of serial digital audio at an audio sampling rate of 32kHz, 44.1kHz, or 48kHz.

4.6.1 Serial Audio Data Inputs

The GV7700 supports the insertion of up to 4 channels of embedded audio, in one audio group according to SMPTE ST 299. When in HD-VLC mode (HDVLC_EN = 1), the audio data packets will be inserted in the YCbCr multiplexed data. When HD-VLC encoding is disabled (HDVLC_EN = 0), the audio data packets will be inserted in the C channel of the HD signal as per SMPTE ST 299.

The four audio channels must be input as 2-channel pairs, timed to a serial bit clock (ACLK) at a frequency of 64*f_S, and a word clock (WCLK) at a frequency of f_S, where f_S can be 32kHz, 44.1kHz, or 48kHz. The serial audio input format must conform to I^2S.

The serial audio input signals and WCLK input signals enter the device on the rising edge of ACLK as shown in Figure 4-14.

The audio sampling frequency can be programmed from the host interface by writing to the AUDIO_SAMPLING_FREQ bits in register 109. See Table 4-9 below.

Table 4-9: Audio Sampling Frequency Selection

AUDIO_SAMPLING_FREQ	Input Audio Sampling Rate
00	48kHz
01	44.1kHz
10	32kHz

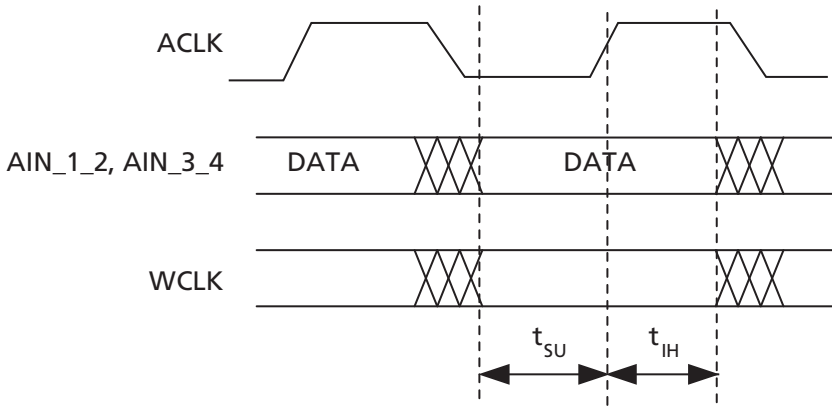


Figure 4-14: ACLK to Audio Data and WCLK Signal Input Timing

Table 4-10: GV7700 Serial Audio Data Inputs - AC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input data set-up time	t_{SU}	50% levels; 1.8V operation	1.3	—	—	ns
Input data hold time	t_{IH}		45	—	—	ns

4.6.2 Serial I²S Audio Data Format

The GV7700 supports the I²S serial audio data format, as shown in Figure 4-15 below.

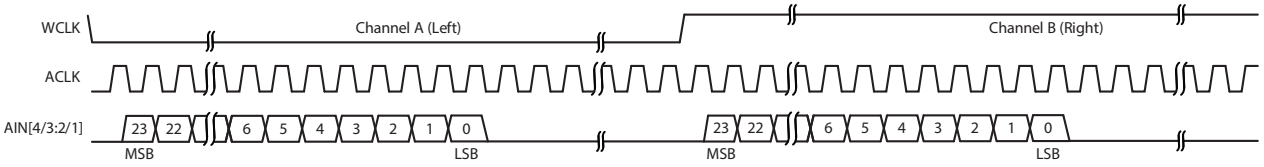


Figure 4-15: I²S Audio Input Format

4.6.3 Audio Mute

The GV7700 can mute either pair of input audio channels using 2 host interface control bits. The bits can mute channels 1 & 2 or channels 3 & 4. Channels 1 & 2 can be muted by asserting the MUTE_1_2 bit in the AUD_INS_CTRL_REG register. Channels 3 & 4 can be muted by asserting the MUTE_3_4 bit in the AUD_INS_CTRL_REG register. See Table 4-11.

By default, the 4 channels will not be muted.

Table 4-11: Audio Mute Controls

Address	Parameter	Description
$486F_h$ [1:1]	MUTE_3_4	HIGH = Channels 3 & 4 are muted LOW = Channels 3 & 4 are not muted
$486F_h$ [0:0]	MUTE_1_2	HIGH = Channels 1 & 2 are muted LOW = Channels 1 & 2 are not muted

4.6.4 ECC Error Detection and Correction

For audio embedding in HD video formats, the packeted audio sample data is protected from bit errors using error correction codes (ECC). The error correction codes are carried in the same packet as the audio sample data for error detection and correction in the GV7704 receiver. The GV7700 uses BCH(31,25) code for ECC.

The GV7700 automatically generates the error detection and correction fields in the audio data packets.

4.7 Ancillary Data Insertion

The horizontal blanking region of a digital video signal may be used to carry ancillary data packets. The vertical blanking region is used by the HD-VLC encoder which inserts compression coefficients which cannot be overwritten. The payload of the ancillary data packet can be used to carry user-defined or proprietary data, which can be sent between an Aviia transmitter and receiver.

The ancillary data packet is formatted according to the Figure 4-16 below. The packet must always begin with the Ancillary Data Flag (ADF), defined as the following 10-bit word sequence: 000_h, $3FF_h$, $3FF_h$.
The next data word is the 8-bit Data ID (DID), used to define the contents of the packet. For example, a unique DID can be used to denote alarm data, with another DID to denote status data. The 8-bit DID is written to the ANC_INS_DID bits of the ANC_INS_DID_REG register.

After the DID insertion, there are two possible options, as shown in Figure 4-16.

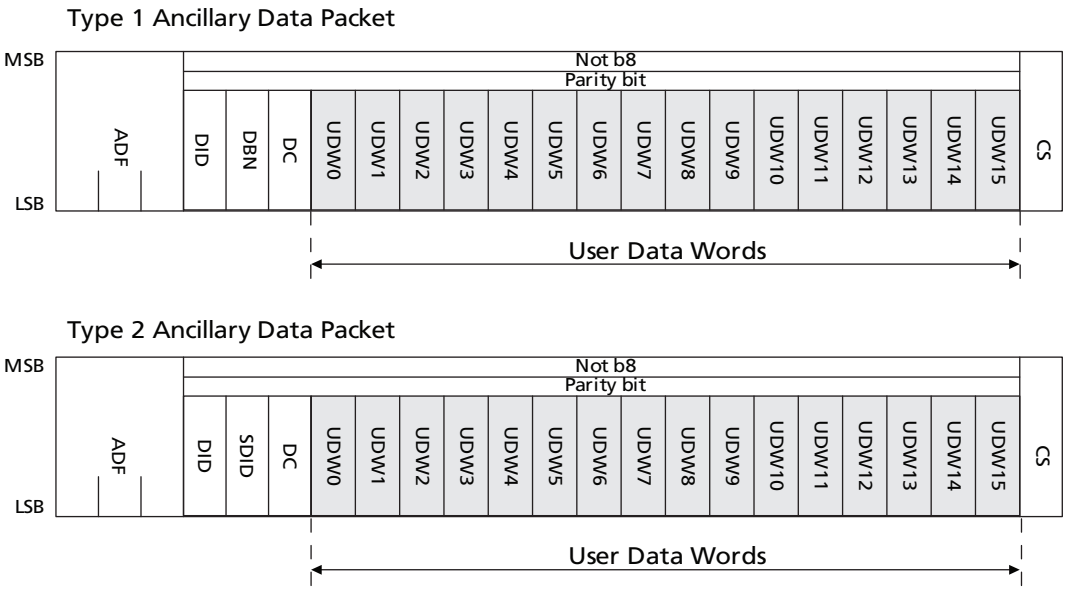


Figure 4-16: Ancillary Data Packets

A Type 1 packet defines an 8-bit Data Block Number (DBN) sequence, used to distinguish successive packets with the same DID. The DBN simply increments with each packet of the same DID, between 0 and 15.

For a Type 2 packet, an 8-bit Secondary Data ID (SDID) word is defined, which can be used to denote variants of payloads with the same DID. For example, packets with a DID to denote error data may distinguish different error types using unique SDID's. The SDID or DBN word is written to the ANC_INS_SDID bits of the ANC_INS_SDID_REG register.

After the DBN or SDID, the next data word is the 8-bit Data Count (DC). This word must be set to the number of user data words (UDW) that follow the DC, and must not exceed 16 (maximum payload size). The Data Count (DC) word is written to the ANC_INS_DC bits of the ANC_INS_DC_REG register. The valid range for this word is 00000001_b to 00010000_b.

The final word of the ancillary data packet is the 9-bit Checksum (CS). The CS value must be equal to the nine least significant bits of the sum of the nine least significant bits of the DID, the DBN or the SDID, the DC and all user data words (UDW) in the packet. The CS value is automatically calculated by the GV7700, so no user configuration is required.

For HD video formats, the GV7700 only inserts ancillary data packets in the Luma channel.

Data words may be inserted on any line in the horizontal blanking region by writing the line number to the two bit slices ANC_INS_LINE_NUMBER_10_8 and ANC_INS_LINE_NUMBER_7_0.

The three most significant bits of the line number (bits 10:8) are written to ANC_INS_LINE_NUMBER_10_8, and the remaining eight bits (bits 7:0) are written to ANC_INS_LINE_NUMBER_7_0. An example is illustrated in Table 4-12 below.

Table 4-12: Examples of Ancillary Data Insertion Line Number Selection

ANC_INS_LINE_ NUMBER_10_8	ANC_INS_LINE_NUMBER_7_0	Horizontal Line Number Insertion
000	00000001	1
100	01100101	1125

Up to 23 Data Words may be inserted per frame with all Data Words — including the ancillary packet ADF, DID, SDID/DBN, DC, and CSUM words — being provided by the user via host interface configuration.

User configuration of the ancillary data insertion function includes the following information:

- Line Number for Insertion — any line in the Horizontal blanking region may be programmed for ancillary data insertion
- Total number of words to insert — includes all data words for all ancillary packets to be inserted on each line
- Ancillary data — up to 23 user data words may be inserted
- Operating Mode — two modes of operation can be selected:
  - Continuous Mode (ANC_INS_SELECT = 0) — the data packet will be inserted continuously each time the current line number equals the line number specified through the ANC_INS_LINE_NUMBER_10_8 and ANC_INS_LINE_NUMBER_7:0 bits in the host interface.
  - One-time Mode (ANC_INS_SELECT = 1) — the data packet will be inserted once, and then it will not be inserted again until the host resets the ANC_INS_ENABLE signal LOW, and then sets it HIGH.

4.8 Additional Processing Functions

4.8.1 Test Pattern Generation

The GV7700 supports test pattern generation through CSR configuration. Two types of patterns are supported:

- Flat-field pattern (a single programmable colour for the whole active picture)
- Pathological pattern

Test pattern generation is enabled via the INSERT_TEST_PAT_ENABLE bit of the TPG_CTRL_REG register. When this bit is HIGH, test patterns are inserted into the active picture region of the incoming video data.

The type of test pattern is determined by the PATTERN_SEL bit of the TPG_CTRL_REG register, shown in Table 4-13 below.

Table 4-13: Test Pattern Type Selection

PATTERN_SEL	Output Test Pattern
0	Pathological
1	Flat-field

The following is an example of how to program a Flat-field Red test pattern (PATTERN_SEL = 1). The pixel setting registers, and the required values to write to the registers, are shown in Table 4-14 below.

Note that when HD-VLC encoding is enabled, the pixel registers are programmed with the same values as when HD-VLC encoding is disabled.

Table 4-14: Flat-Field Red Test Pattern

Parameter	Bit Value	Pixel Value	Channel Outputs (HDVLC_EN = 0)	Channel Outputs (HDVLC_EN = 1)
PIXEL0_Y0_9_8	0_d	$0FC_h$	**Y Channel:** $0FC_h - 0FC_h - 0FC_h - 0FC_h - 0FC_h - 0FC_h - 0FC_h - 0FC_h$...	**YCbCr Channel:** $198_h - 0FC_h - 3C0_h - 0FC_h - 198_h - 0FC_h - 3C0_h - 0FC_h$ ...
PIXEL0_Y0_7_0	252_d			
PIXEL0_Y1_9_8	0_d	$0FC_h$		
PIXEL0_Y1_7_0	252_d			
PIXEL0_CB0_9_8	1_d	198_h	**C Channel:** $198_h - 3C0_h - 198_h - 3C0_h - 198_h - 3C0_h - 198_h - 3C0_h$...	
PIXEL0_CB0_7_0	152_d			
PIXEL0_CR0_9_8	3_d	$3C0_h$		
PIXEL0_CR0_7_0	192_d			

Note: All "PIXEL1" registers, from register address $48A0_h$ to $48A7_h$, are not required for programming Flat-field test patterns. They may all be set to "0000_h"

In order to generate a pathological test pattern as per SMPTE recommended practice RP 198, the GV7700 should be configured as shown in Table 4-15 below.

Table 4-15: Pathological Test Pattern (SMPTE RP 198 Recommended)

Parameter	Bit Value	Pixel Value	Channel Outputs
Equalizer Test Signal			
PIXEL0_Y0_9_8	1_d	198_h	**Y Channel:** 198_h – 198_h – 198_h – 198_h – 198_h – 198_h – 198_h...
PIXEL0_Y0_7_0	152_d		
PIXEL0_Y1_9_8	1_d	198_h	
PIXEL0_Y1_7_0	152_d		
PIXEL0_CB0_9_8	3_d	300_h	**C Channel:** 300_h – 300_h – 300_h – 300_h – 300_h – 300_h – 300_h – 300_h ...
PIXEL0_CB0_7_0	0_d		
PIXEL0_CR0_9_8	3_d	300_h	
PIXEL0_CR0_7_0	0_d		
PLL Test Signal (See Note 1)			
PIXEL1_Y0_9_8	1_d	110_h	**Y Channel:** 110_h – 110_h – 110_h – 110_h – 110_h – 110_h – 110_h – 110_h...
PIXEL1_Y0_7_0	16_d		
PIXEL1_Y1_9_8	1_d	110_h	
PIXEL1_Y1_7_0	16_d		
PIXEL1_CB0_9_8	2_d	200_h	**C Channel:** 200_h – 200_h – 200_h – 200_h – 200_h – 200_h – 200_h – 200_h ...
PIXEL1_CB0_7_0	0_d		
PIXEL1_CR0_9_8	2_d	200_h	
PIXEL1_CR0_7_0	0_d		

Note:

1. Transition from the equalizer test signal to the PLL test signal occurs according to Table 4-16 below.

The line that the pathological test signal will transition on is dependent on the output video format. The transition point should be consistent from frame to frame, and from field to field if the video is interlaced. See Table 4-16 below on how to program the transitional line number.

Table 4-16: Pathological Test Signal Transition Line

Video Format	PATHO_PLL_LINE_F1	PATHO_PLL_LINE_F2
1080i50	384_d	973_d
1080i59.94	288_d	851_d
1080p25	697_d	N/A

Table 4-16: Pathological Test Signal Transition Line (Continued)

Video Format	PATHO_PLL_LINE_F1	PATHO_PLL_LINE_F2
1080p30/29.97	579_d	N/A
720p (All frame rates)	383_d	N/A

4.8.2 TRS Generation and Insertion

The GV7700 is capable of generating and inserting TRS codes.

TRS word generation and insertion are performed in accordance with the timing parameters generated by the timing circuits, which are locked to the externally provided H:V:F signals, or the TRS signals embedded in the input data stream.

10-bit TRS code words are inserted at all times.

4.8.3 HD Line Number Calculation and Insertion

The GV7700 is capable of line number generation and insertion, in accordance with the relevant HD video standard, as determined by the automatic video standard detector.

The GV7700 generates and inserts line numbers into both the Y and C channels of the data stream when HDVLC_EN = 0, and generates and inserts line numbers in the YCbCr multiplexed stream when HDVLC_EN = 1.

4.8.4 Line Based CRC Generation and Insertion

The GV7700 generates and inserts line based CRC words into both the Y and C channels of the data stream when HDVLC_EN = 0, and generates and inserts line based CRC words in the YCbCr multiplexed stream when HDVLC_EN = 1.

4.8.5 Illegal Code Re-Mapping

The GV7700 detects and corrects illegal code words within the active picture area.

All codes within the active picture (outside the horizontal and vertical blanking periods), between the values of $3FC_h$ and $3FF_h$ are re-mapped to $3FB_h$. All codes within the active picture area between the values of 000_h and 003_h are remapped to 004_h.

8-bit TRS code words and ancillary data preambles are also re-mapped to 10-bit values.

4.9 Parallel to Serial Conversion

The parallel data output of the internal data processing blocks is fed to the parallel to serial converter.

Note: The internal data path bus width is independent of the parallel data bus input bus width, which is controlled by the setting of the BIT20_$\overline{\text{BIT10}}$ pin.

4.10 PLL

Internal division ratios for the PCLK are determined by the setting of the HDVLC_EN pin, the BIT20_$\overline{\text{BIT10}}$ pin and the DIV_1001 pin as shown in Table 4-17:

Table 4-17: PCLK and Serial Digital Clock Rates

External Pin Setting				Supplied PCLK Rate	Serial Digital Output Rate	Notes
THREEG_$\overline{\text{HD}}$	HDVLC_EN	BIT20_$\overline{\text{BIT10}}$	DIV_1001			
LOW	HIGH	HIGH	LOW	74.25MHz	270Mb/s	1
LOW	HIGH	HIGH	HIGH	74.25/1.001MHz	270Mb/s	—
LOW	HIGH	LOW	LOW	148.5MHz	270Mb/s	1
LOW	HIGH	LOW	HIGH	148.5/1.001MHz	270Mb/s	—
LOW	LOW	HIGH	LOW	74.25MHz	1.485Gb/s	—
LOW	LOW	HIGH	HIGH	74.25/1.001MHz	1.485/1.001Gb/s	—
LOW	LOW	LOW	LOW	148.5MHz	1.485Gb/s	—
LOW	LOW	LOW	HIGH	148.5/1.001MHz	1.485/1.001Gb/s	—
HIGH	HIGH	HIGH	LOW	148.5MHz	540Mb/s	1
HIGH	HIGH	HIGH	HIGH	148.5/1.001MHz	540Mb/s	—
HIGH	HIGH	LOW	LOW	148.5MHz	540Mb/s	1, 2
HIGH	HIGH	LOW	HIGH	148.5/1.001MHz	540Mb/s	2
HIGH	LOW	HIGH	LOW	148.5MHz	2.97Gb/s	—
HIGH	LOW	HIGH	HIGH	148.5/1.001MHz	2.97/1.001Gb/s	—
HIGH	LOW	LOW	LOW	148.5MHz	2.97Gb/s	2
HIGH	LOW	LOW	HIGH	148.5/1.001MHz	2.97/1.001Gb/s	2

Note:

1. For 720p30, 720p60, and 1080p30, the serial output rate when HD-VLC encoding is enabled will be 270x1.001Mb/s. For 1080p60, the encoded output rate will be 540x1.001Mb/s.
2. For 3G 10-bit mode the clock is DDR

As well as generating the serial digital output clock signals, the PLL is also responsible for generating all internal clock signals required by the device.

4.10.1 Frequency Reference

The frequency reference for the GV7700 PLL can either be the PCLK input or an external crystal.

While using an external XTAL as the frequency reference, set the input pin $\overline{\text{XTAL\_EN}}$ low. Two pins, XTAL and $\overline{\text{XTAL}}$, are provided to connect to the external crystal.

The use of a 27MHz or 54MHz crystal is supported, depending on the front-end ISP chip reference clock frequency. XTAL54_SEL is an input pin which is set low when the default 27MHz crystal is used. The pin has an on-chip pull-down. When set HIGH, a 54MHz crystal can be used.

XTAL_OUT is designed to drive the front-end ISP crystal input pin. VDDIO_XOUT pin is the power supply for this buffer, which can be powered from 1.8V or 3.3V, depending on the ISP requirement.

While using the PCLK as the frequency reference, set the input pin $\overline{\text{XTAL\_EN}}$ HIGH, connect the XTAL pin to ground, and leave $\overline{\text{XTAL}}$ pin floating.

Figure 4-17 shows a block diagram with the PCLK, crystal connection and XTAL_OUT back to ISP chip.

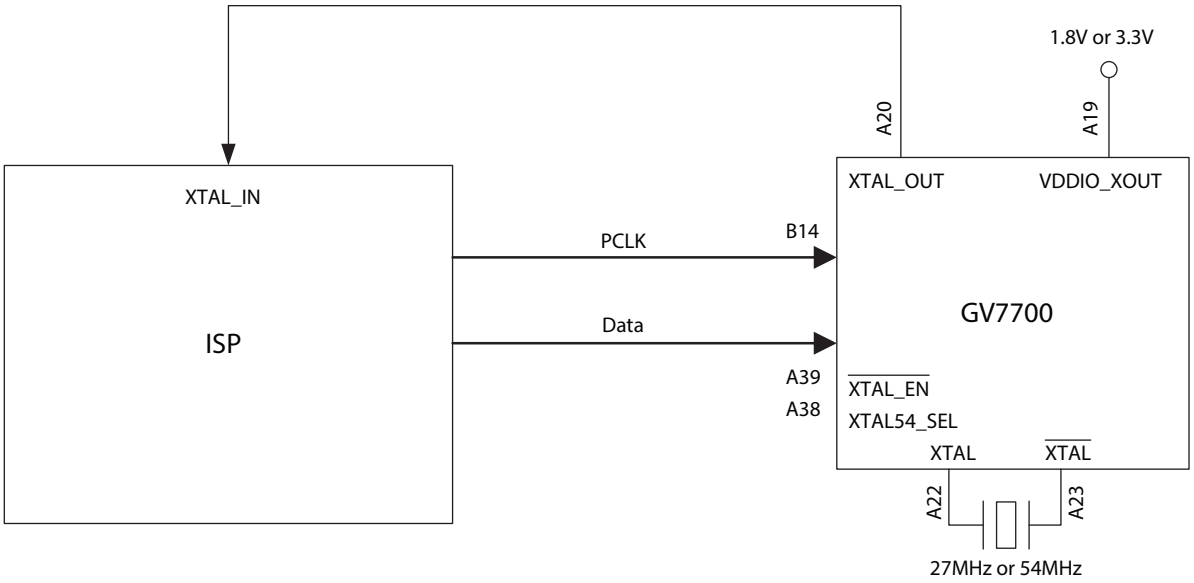


Figure 4-17: External Crystal Frequency Reference Connection

4.11 Serial Data Output

The GV7700 has a single, low-impedance current mode differential output driver, capable of driving at least 800mV into a 75Ω single-ended load.

The SDO and $\overline{\text{SDO}}$ pins of the device provide the serial data output.

Compliance with all requirements defined in Section 4.11.1 through Section 4.11.2 is guaranteed when measured across a 75Ω terminated load at the output of 1m of Belden 543945A cable, including the effects of the BNC and coaxial cable connection, except where otherwise stated.

Figure 4-18 illustrates this requirement.

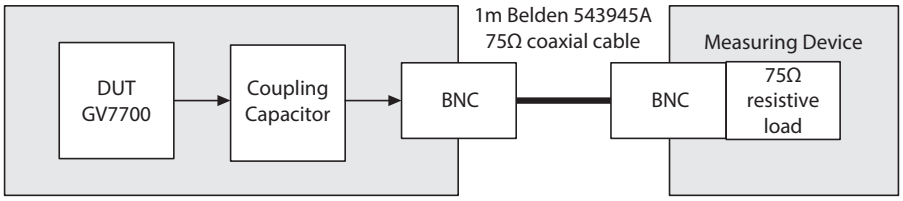


Figure 4-18: BNC and Coaxial Cable Connection

4.11.1 Output Signal Interface Levels

The Serial Data Output signals (SDO and $\overline{\text{SDO}}$ pins), of the device meet the amplitude requirements as defined in ITU-R BT.656 and BT.1120 for an unbalanced generator (single-ended).

These requirements are met across all ambient temperature and power supply operating conditions described in 2. Electrical Characteristics.

4.11.2 Serial Data Output Signal

When the SDO_50_EN pin is set HIGH, the device outputs a 100Ω differential signal

When the SDO_50_EN pin is LOW, the serial data output signals of the device become 75Ω single-ended outputs, with both complementary outputs ON by default.

4.12 GSPI Host Interface

The GV7700 is controlled via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (SDIN pin), serial data output signal (SDOUT pin), an active-low chip select ($\overline{\text{CS}}$ pin) and a burst clock (SCLK pin).

The GV7700 is a slave device, so the SCLK, SDIN, and $\overline{\text{CS}}$ signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

4.12.1 $\overline{\text{CS}}$ Pin

The Chip Select pin ($\overline{\text{CS}}$) is an active-low signal provided by the host processor to the GV7700.

The HIGH-to-LOW transition of this pin marks the start of serial communication to the GV7700.

The LOW-to-HIGH transition of this pin marks the end of serial communication to the GV7700.

4.12.2 SDIN Pin

The SDIN pin is the GSPI serial data input pin of the GV7700.

The 16-bit Command and Data Words from the host processor are shifted into the device on the rising edge of SCLK when the $\overline{CS}$ pin is LOW.

4.12.3 SDOUT Pin

The SDOUT pin is the GSPI serial data output of the GV7700.

All data transfers out of the GV7700 to the host processor occur from this pin.

By default at power up or after system reset, the SDOUT pin provides a non-clocked path directly from the SDIN pin, regardless of the $\overline{CS}$ pin state, except during the GSPI Data Word portion for read operations to the device.

For read operations, the SDOUT pin is used to output data read from an internal Configuration and Status Register (CSR) when $\overline{CS}$ is LOW. Data is shifted out of the device on the falling edge of SCLK, so that it can be read by the host processor on the subsequent SCLK rising edge.

4.12.4 SCLK Pin

The SCLK pin is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GV7700 SDIN pin on the rising edge of SCLK. Serial data is clocked out of the device from the SDOUT pin on the falling edge of SCLK (read operation). SCLK is ignored when $\overline{CS}$ is HIGH.

4.12.5 Command Word Description

All GSPI accesses are a minimum of 48 bits in length (a 16-bit Command Word, a 16-bit Extended Address field, and a 16-bit Data Word) and the start of each access is indicated by the HIGH-to-LOW transition of the chip select ($\overline{CS}$) pin of the GV7700.

The format of the Command Word and Data Words are shown in Figure 4-19.

Data received immediately following this HIGH-to-LOW transition will be interpreted as a new Command Word.

4.12.5.1 R/$\overline{W}$ bit - B15 Command Word

This bit indicates a read or write operation.

When R/$\overline{W}$ is set to 1, a read operation is indicated, and data is read from the register specified by the ADDRESS field of the Command Word.

When R/$\overline{W}$ is set to 0, a write operation is indicated, and data is written to the register specified by the ADDRESS field of the Command Word.

4.12.5.2 BROADCAST ALL - B14 Command Word

This bit must always be set to 0.

4.12.5.3 EMEM - B13 Command Word

This bit must always be set to 1.

4.12.5.4 AUTOINC - B12 Command Word

When AUTOINC is set to 1, Auto-Increment read or write access is enabled.

In Auto-Increment Mode, the device automatically increments the register address for each contiguous read or write access, starting from the address defined in the ADDRESS field of the Command Word.

The internal address is incremented for each 16-bit read or write access until a LOW-to-HIGH transition on the $\overline{CS}$ pin is detected.

When AUTOINC is set to 0, single read or write access is required.

4.12.5.5 UNIT ADDRESS - B11:B5 Command Word

The 7 bits of the UNIT ADDRESS field of the Command Word should always be set to 0.

4.12.5.6 ADDRESS - B4:B0 Command Word, B15:B0 Extended Address

The Address Word consists of bits [4:0] of the Command Word, plus another 16 bits [15:0] from the Extended Address Word. The total Command and Data Word format, including the Extended Address, is shown in Figure 4-19 below.

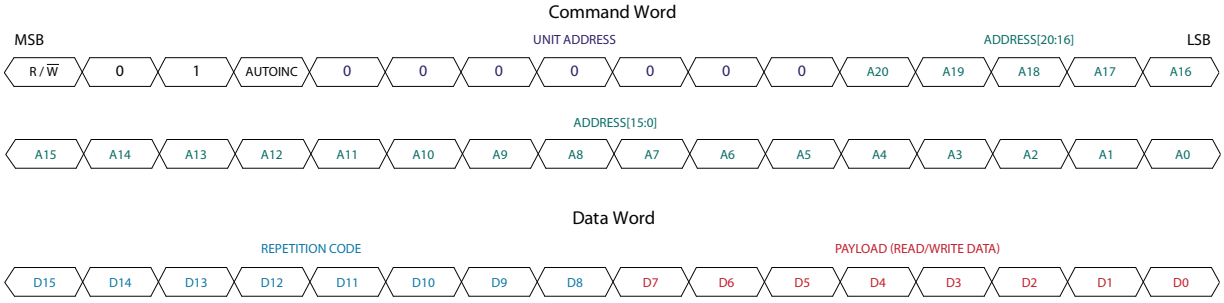


Figure 4-19: Command and Data Word Format

4.12.6 Data Word Description

The Data Word portion of the GSPI access consists of an 8-bit repetition code, followed by an 8-bit Read or Write access Payload. All registers in the GV7700 are 8 bits long, however since GSPI write commands are required to be 16 bits long, the Data Word will have the same byte repeated. For example, to write FC_h to a register within the CSR, the 16-bit Data Word of the GSPI Command should be $FCFC_h$.

4.12.7 GSPI Transaction Timing

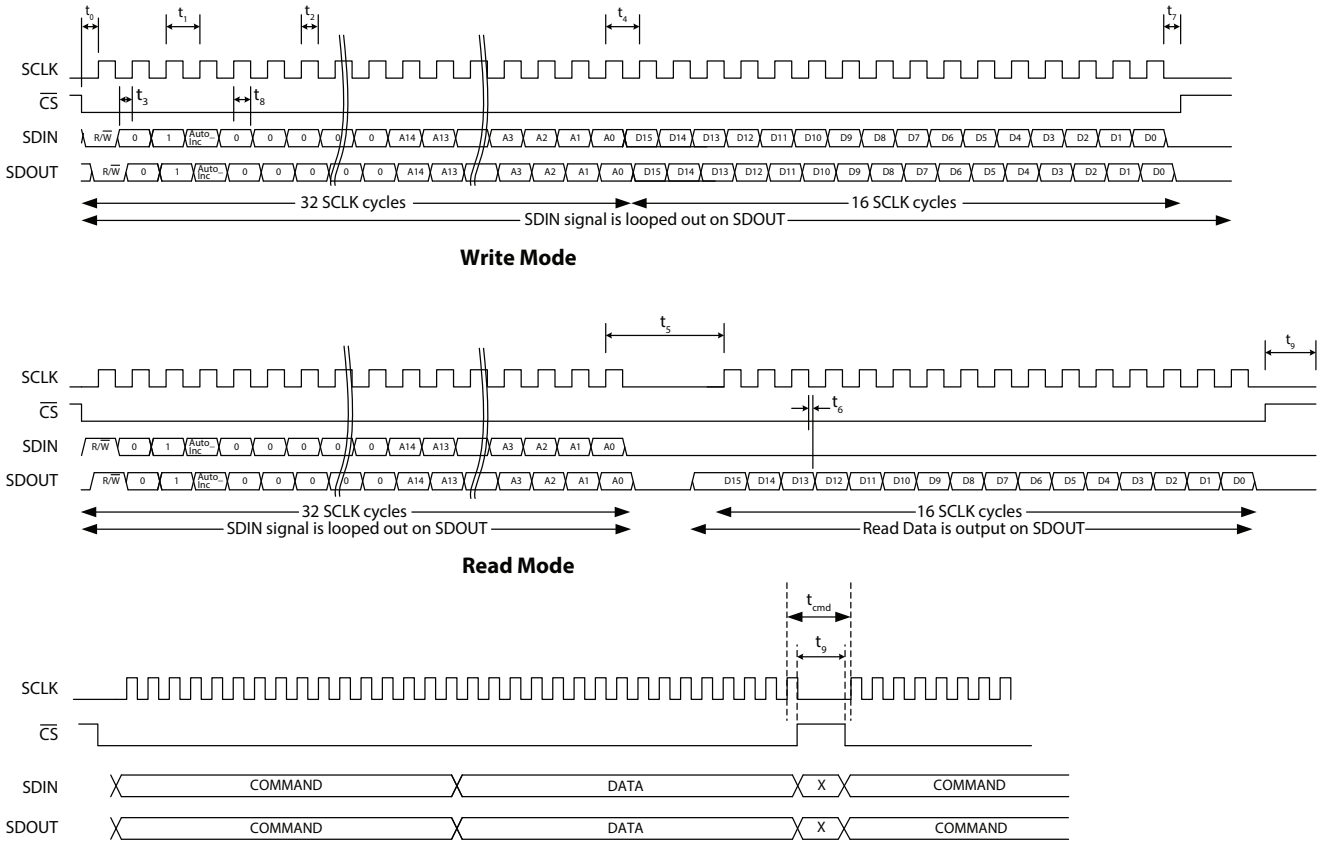


Figure 4-20: GSPI External Interface Timing

Table 4-18: GSPI Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
$\overline{CS}$ low before SCLK rising edge	t_0	2.0	—	—	ns
SCLK frequency		—	—	45	MHz
SCLK period	t_1	22.2	—	—	ns
SCLK duty cycle	t_2	40	50	60	%
Input data setup time	t_3	2.7	—	—	ns
SCLK idle time -write	t_4	41.7	—	—	ns
SCLK idle time - read	t_5	161.0	—	—	ns
Inter-command delay time	t_{cmd}	162.0	—	—	ns
SDOUT after SCLK falling edge	t_6	—	—	7.5	ns

Table 4-18: GSPI Timing Parameters (Continued)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{CS}$ high after final SCLK falling edge	t_7	0.0	—	—	ns
Input data hold time	t_8	1.0	—	—	ns
$\overline{CS}$ high time	t_9	57.0	—	—	ns
SDIN to SDOUT combinational delay		—	—	5.0	ns

4.12.8 Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-21 and Figure 4-22.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 48-bits long, consisting of a Command Word, an Extended Address, and a single Data Word. The read or write cycle begins with a high-to-low transition of the $\overline{CS}$ pin. The read or write access is terminated by a low-to-high transition of the $\overline{CS}$ pin.

The maximum interface clock frequency (SCLK) is 45MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of 4 SCLK clock cycles.

For read access, the time from the last bit of the Command Word to the start of the data output, as defined by t_5, corresponds to no less than 4 SCLK clock cycles at 45MHz.

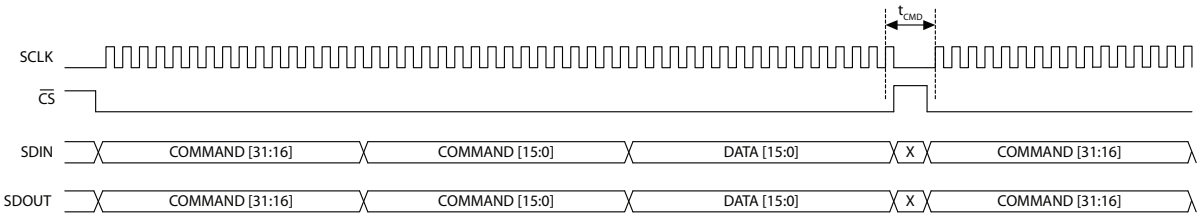


Figure 4-21: GSPI Write Timing – Single Write Access

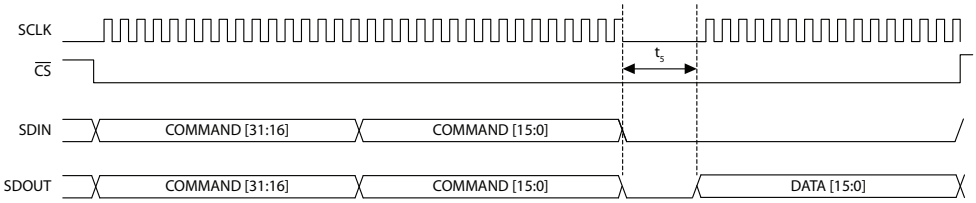


Figure 4-22: GSPI Read Timing – Single Read Access

4.12.9 Auto-increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in Figure 4-23 and Figure 4-24.

Auto-increment mode is enabled by the setting of the AUTOINC bit of the Command Word.

In this mode, multiple Data Words can be read from/written to the device using only one starting address. Each access is initiated by a HIGH-to-LOW transition of the $\overline{CS}$ pin, and consists of a Command Word and one or more Data Words. The internal address is automatically incremented after the first read or write Data Word, and continues to increment until the read or write access is terminated by a LOW-to-HIGH transition of the $\overline{CS}$ pin.

The maximum interface clock frequency (SCLK) is 45MHz and the inter-command delay time indicated in the diagram as t_{cmd}, is a minimum of 4 SCLK clock cycles.

For read access, the time from the last bit of the first Command Word to the start of the data output of the first Data Word as defined by t_5, will be no less than 4 SCLK cycles at 45MHz. All subsequent read data accesses will not be subject to this delay during an Auto-Increment read.

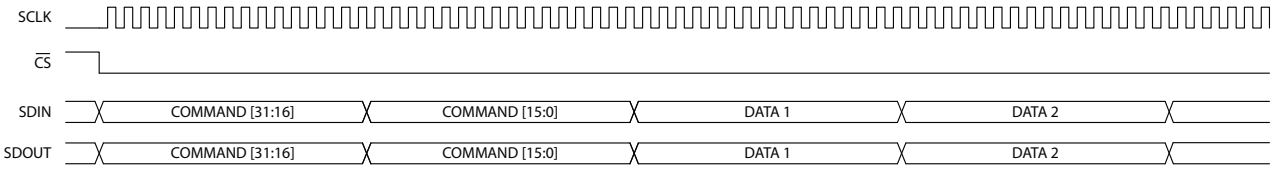


Figure 4-23: GSPI Write Timing – Auto-Increment

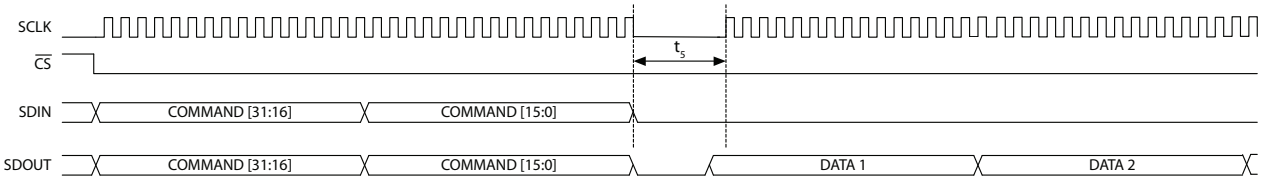


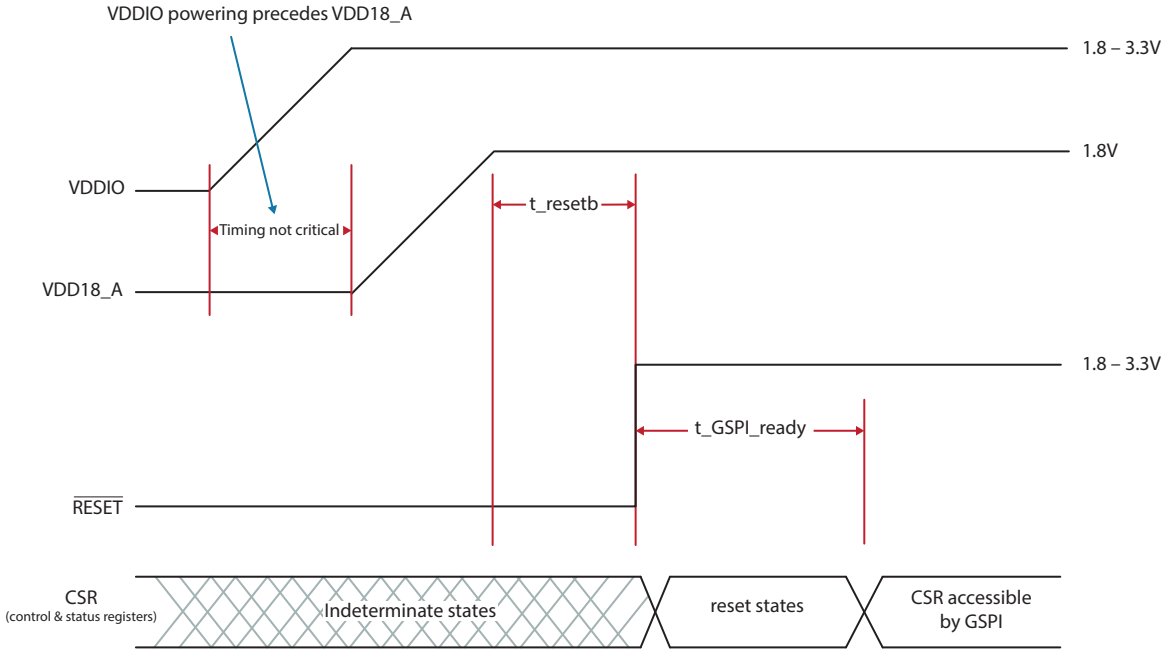
Figure 4-24: GSPI Read Timing – Auto-Increment

4.13 JTAG

The GV7700 provides an IEEE 1149.1-compliant JTAG TAP interface for boundary scan test and debug.

The GV7700 TAP interface consists of the TCK clock input, TRST, TDI, and TMS inputs, and the TDO output as defined in the standard. TMS and TDI inputs are clocked with respect to the rising edge of TCK and the TDO output with respect to the falling edge of TCK.

4.14 Power Supply and Reset Timing



T_resetb >= 10ms
T_GSPI_ready = 10µs

Figure 4-25: Power Supply and Reset Timing

Note: Configuration pins should be set prior to device reset.

5. Register Map

Table 5-1: GV7700 Register Descriptions

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$486D_h$	AUDIO_SAMPLING_FREQ_REG	AUDIO_SAMPLING_FREQ	1:0	RW	0	Audio Sampling Frequency. 00 = 48kHz audio samples 01 = 44.1kHz audio samples 10 = 32kHz audio samples
$486F_h$	AUD_INS_CTRL_REG	MUTE_1_2	0:0	RW	0	Audio Mute for channels 1 & 2. When HIGH, the device will insert audio samples with a value of 0 into channels 1 & 2.
		MUTE_3_4	1:1	RW	0	Audio Mute for channels 3 & 4. When HIGH, the device will insert audio samples with a value of 0 into channels 3 & 4.
4879_h	ANC_INS_MODES_REG	ANC_INS_ENABLE	0:0	RW	0	Enables Ancillary Data Insertion. 1 = Ancillary data insertion is enabled. 0 = No ancillary data is inserted.
		ANC_INS_SELECT	1:1	RW	0	Mode allowing continuous insertion of the packet or only once. 1= Packet inserted on current frame only 0 = Continuous insertion on every frame
		ANC_INS_REGION	2:2	RW	0	Selects insertion data region. 1 = VANC region (vertical blanking) 0 = HANC region (horizontal blanking)
		ANC_INS_ASAP	3:3	RW	0	When ANC_INS_SELECT is HIGH, this bit enables packet insertion on the next available line: 1 = Insert the packet in the next available line. Ignores the ANC_INS_LINE_NUMBER setting. 0 = Wait for the line number specified in ANC_INS_LINE_NUMBER to insert the packet.
		ANC_INS_STREAM_TYPE	4:4	RW	0	Selects Y/C component for insertion. For SD, it will always be 0. 1 = Puts a packet on C of HD, or puts a packet on DS2 of 3G Level-A (DS2 shows up on C). 0 = Puts a packet in YCbCr of SD, or puts a packet in Y of HD, or puts a packet in DS1 of 3G Level-A (DS1 shows up on Y).
$487A_h$	ANC_INS_LINE_NUMBER_10_8_REG	ANC_INS_LINE_NUMBER_10_8	2:0	RW	0	Defines line number for ANC data insertion. Bits 10 down to 8.
$487B_h$	ANC_INS_LINE_NUMBER_7_0_REG	ANC_INS_LINE_NUMBER_7_0	7:0	RW	0	Defines line number for ANC data insertion. Bits 7 down to 0.
$487C_h$	ANC_INS_NUMBER_OF_WORDS_REG	ANC_INS_NUMBER_OF_WORDS	4:0	RW	0	Defines number of ANC data words in the packet. Includes: 000-$3FF_h$-$3FF_h$-DID-SDID/DBN-DC-All UDWs-CS

Table 5-1: GV7700 Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
$487D_h$	ANC_INS_DID_REG	ANC_INS_DID	7:0	RW	0	DID field of the ancillary data packet to be inserted.
$487E_h$	ANC_INS_SDID_REG	ANC_INS_SDID	7:0	RW	0	SDID/DBN field of the ancillary data packet to be inserted.
$487F_h$	ANC_INS_DC_REG	ANC_INS_DC	7:0	RW	0	DC field of the ancillary data packet to be inserted.
4880_h	ANC_INS_UDW0_REG	ANC_INS_UDW0	7:0	RW	0	User Data Word 0 of the ancillary data packet to be inserted.
4881_h	ANC_INS_UDW1_REG	ANC_INS_UDW1	7:0	RW	0	User Data Word 1 of the ancillary data packet to be inserted.
4882_h	ANC_INS_UDW2_REG	ANC_INS_UDW2	7:0	RW	0	User Data Word 2 of the ancillary data packet to be inserted.
4883_h	ANC_INS_UDW3_REG	ANC_INS_UDW3	7:0	RW	0	User Data Word 3 of the ancillary data packet to be inserted.
4884_h	ANC_INS_UDW4_REG	ANC_INS_UDW4	7:0	RW	0	User Data Word 4 of the ancillary data packet to be inserted.
4885_h	ANC_INS_UDW5_REG	ANC_INS_UDW5	7:0	RW	0	User Data Word 5 of the ancillary data packet to be inserted.
4886_h	ANC_INS_UDW6_REG	ANC_INS_UDW6	7:0	RW	0	User Data Word 6 of the ancillary data packet to be inserted.
4887_h	ANC_INS_UDW7_REG	ANC_INS_UDW7	7:0	RW	0	User Data Word 7 of the ancillary data packet to be inserted.
4888_h	ANC_INS_UDW8_REG	ANC_INS_UDW8	7:0	RW	0	User Data Word 8 of the ancillary data packet to be inserted.
4889_h	ANC_INS_UDW9_REG	ANC_INS_UDW9	7:0	RW	0	User Data Word 9 of the ancillary data packet to be inserted.
$488A_h$	ANC_INS_UDW10_REG	ANC_INS_UDW10	7:0	RW	0	User Data Word 10 of the ancillary data packet to be inserted.
$488B_h$	ANC_INS_UDW11_REG	ANC_INS_UDW11	7:0	RW	0	User Data Word 11 of the ancillary data packet to be inserted.
$488C_h$	ANC_INS_UDW12_REG	ANC_INS_UDW12	7:0	RW	0	User Data Word 12 of the ancillary data packet to be inserted.
$488D_h$	ANC_INS_UDW13_REG	ANC_INS_UDW13	7:0	RW	0	User Data Word 13 of the ancillary data packet to be inserted.
$488E_h$	ANC_INS_UDW14_REG	ANC_INS_UDW14	7:0	RW	0	User Data Word 14 of the ancillary data packet to be inserted.
$488F_h$	ANC_INS_UDW15_REG	ANC_INS_UDW15	7:0	RW	0	User Data Word 15 of the ancillary data packet to be inserted.

Table 5-1: GV7700 Register Descriptions (Continued)

Address	Register Name	Parameter Name	Bit Slice	R/W	Reset Value	Description
4891_h	TPG_CTRL_REG	INSERT_TEST_PAT_ENABLE	0:0	RW	0	Enables the test pattern insertion on the active picture region of the incoming video data. 1 = Enables the insertion of the test patterns 0 = No insertion
		PATTERN_SEL	1:1	RW	0	Test Pattern Selection. 0 = Pathological test pattern 1 = Flat-field test pattern
4894_h	TPG_PATHO_PLL_LINE_F1_10_8_REG	PATHO_PLL_LINE_F1_10_8	2:0	RW	0	Starting line number for the Pathological PLL Testing when FIN = 0. Bits 10 down to 8.
4895_h	TPG_PATHO_PLL_LINE_F1_7_0_REG	PATHO_PLL_LINE_F1_7_0	7:0	RW	0	Starting line number for the Pathological PLL Testing when FIN = 0. Bits 7 down to 0.
4896_h	TPG_PATHO_PLL_LINE_F2_10_8_REG	PATHO_PLL_LINE_F2_10_8	2:0	RW	0	Starting line number for the Pathological PLL Testing when FIN = 1. Bits 10 down to 8.
4897_h	TPG_PATHO_PLL_LINE_F2_7_0_REG	PATHO_PLL_LINE_F2_7_0	7:0	RW	0	Starting line number for the Pathological PLL Testing when FIN = 1. Bits 7 down to 0.
4898_h	TPG_PIXEL0_CB0_9_8_REG	PIXEL0_CB0_9_8	1:0	RW	0	Pixel 0 setting register. Cb0. Bits 9 down to 8.
4899_h	TPG_PIXEL0_CB0_7_0_REG	PIXEL0_CB0_7_0	7:0	RW	0	Pixel 0 setting register. Cb0. Bits 7 down to 0.
$489A_h$	TPG_PIXEL0_Y0_9_8_REG	PIXEL0_Y0_9_8	1:0	RW	0	Pixel 0 setting register. Y0. Bits 9 down to 8.
$489B_h$	TPG_PIXEL0_Y0_7_0_REG	PIXEL0_Y0_7_0	7:0	RW	0	Pixel 0 setting register. Y0. Bits 7 down to 0.
$489C_h$	TPG_PIXEL0_CR0_9_8_REG	PIXEL0_CR0_9_8	1:0	RW	0	Pixel 0 setting register. Cr0. Bits 9 down to 8.
$489D_h$	TPG_PIXEL0_CR0_7_0_REG	PIXEL0_CR0_7_0	7:0	RW	0	Pixel 0 setting register. Cr0. Bits 7 down to 0.
$489E_h$	TPG_PIXEL0_Y1_9_8_REG	PIXEL0_Y1_9_8	1:0	RW	0	Pixel 0 setting register. Y1. Bits 9 down to 8.
$489F_h$	TPG_PIXEL0_Y1_7_0_REG	PIXEL0_Y1_7_0	7:0	RW	0	Pixel 0 setting register. Y1. Bits 7 down to 0.
$48A0_h$	TPG_PIXEL1_CB0_9_8_REG	PIXEL1_CB0_9_8	1:0	RW	0	Pixel 1 setting register. Cb0. Bits 9 down to 8.
$48A1_h$	TPG_PIXEL1_CB0_7_0_REG	PIXEL1_CB0_7_0	7:0	RW	0	Pixel 1 setting register. Cb0. Bits 7 down to 0.
$48A2_h$	TPG_PIXEL1_Y0_9_8_REG	PIXEL1_Y0_9_8	1:0	RW	0	Pixel 1 setting register. Y0. Bits 9 down to 8.
$48A3_h$	TPG_PIXEL1_Y0_7_0_REG	PIXEL1_Y0_7_0	7:0	RW	0	Pixel 1 setting register. Y0. Bits 7 down to 0.
$48A4_h$	TPG_PIXEL1_CR0_9_8_REG	PIXEL1_CR0_9_8	1:0	RW	0	Pixel 1 setting register. Cr0. Bits 9 down to 8.
$48A5_h$	TPG_PIXEL1_CR0_7_0_REG	PIXEL1_CR0_7_0	7:0	RW	0	Pixel 1 setting register. Cr0. Bits 7 down to 0.
$48A6_h$	TPG_PIXEL1_Y1_9_8_REG	PIXEL1_Y1_9_8	1:0	RW	0	Pixel 1 setting register. Y1. Bits 9 down to 8.
$48A7_h$	TPG_PIXEL1_Y1_7_0_REG	PIXEL1_Y1_7_0	7:0	RW	0	Pixel 1 setting register. Y1. Bits 7 down to 0.
$48A8_h$	CRC_INS_ENABLE_REG	CRC_INS_ENABLE	0:0	RW	0	When HIGH, enables the CRC insertion. When LOW, CRC insertion will not be done. Must be set HIGH when TPG mode enabled.

6. Typical Application Circuit

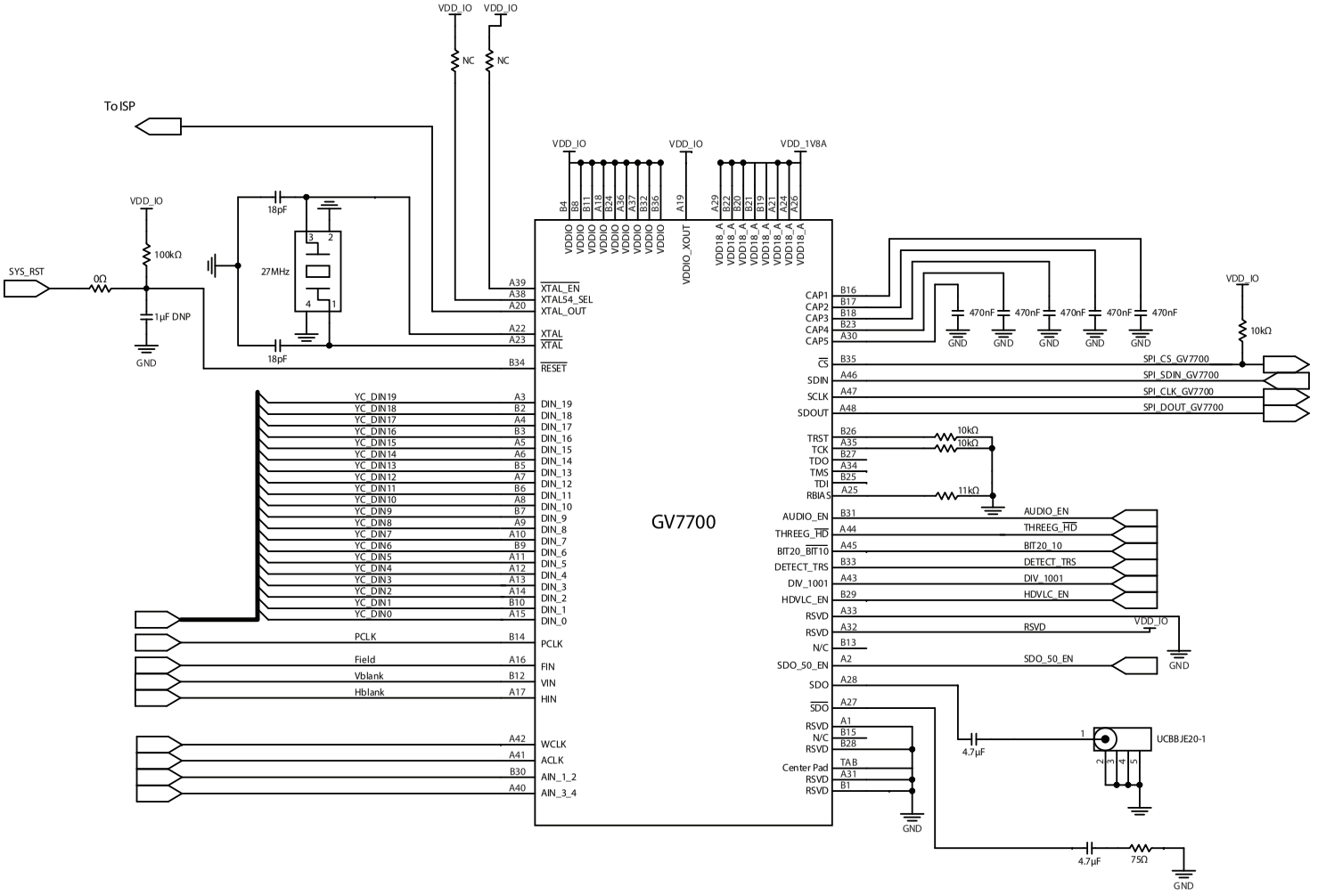


Figure 6-1: GV7700 Typical Application Circuit

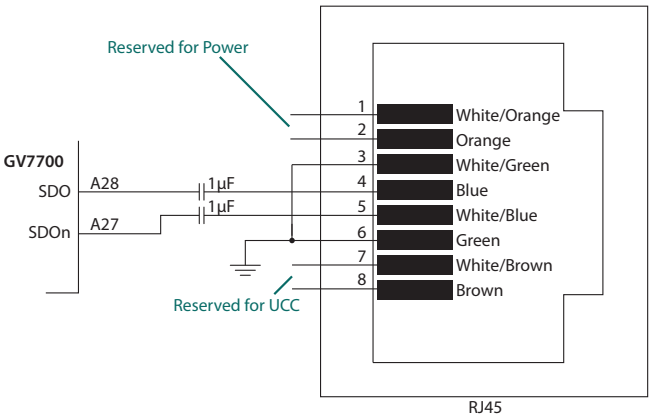


Figure 6-2: Alternative CATx Output Circuit

6.1 Power Supply Decoupling and Filtering

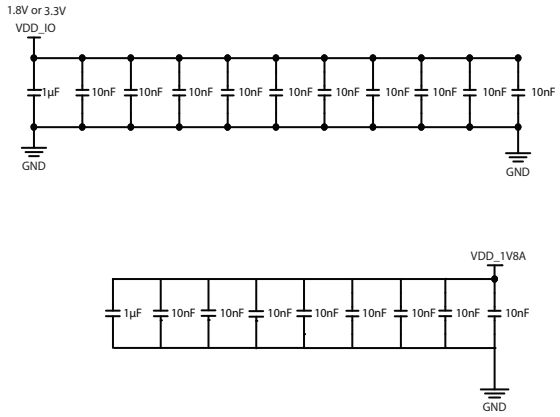
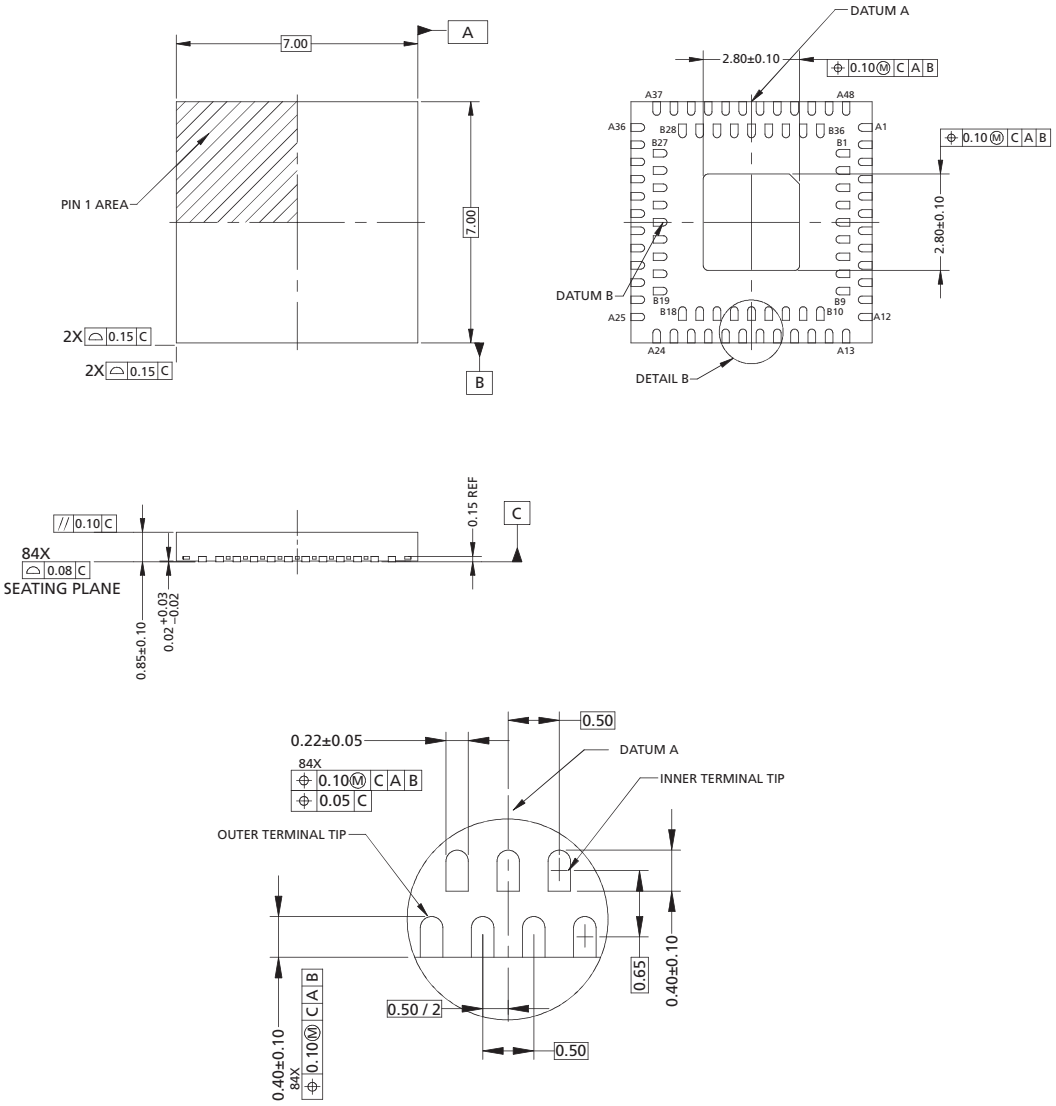


Figure 6-3: GV7700 Power Supply Decoupling and Filtering Schematic

7. Packaging Information

7.1 Package Dimensions



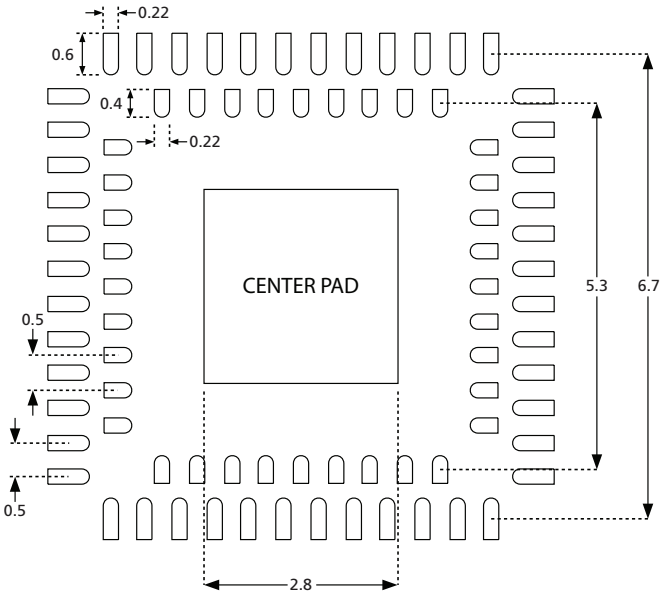
DETAIL B (SCALE 3:1)

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Figure 7-1: GV7700 Package Dimensions

7.2 Recommended PCB Footprint



Notes:
1. All dimensions in millimeters
2. All signal pads have a 0.11mm inner end radius

Figure 7-2: GV7700 PCB Footprint

7.3 Marking Diagram

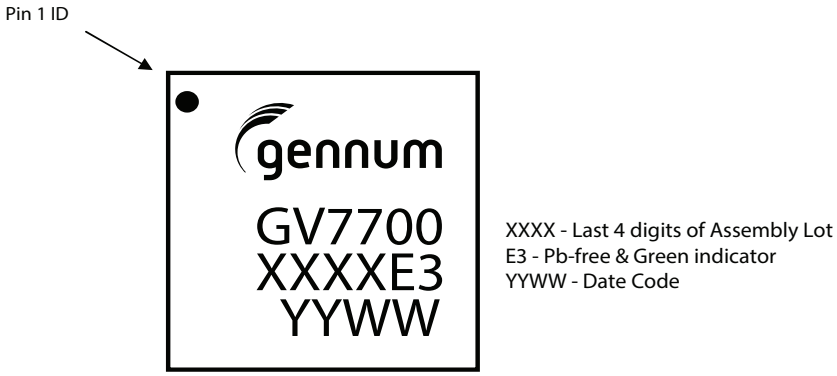


Figure 7-3: GV7700 Marking Diagram

7.4 Solder Reflow Profile

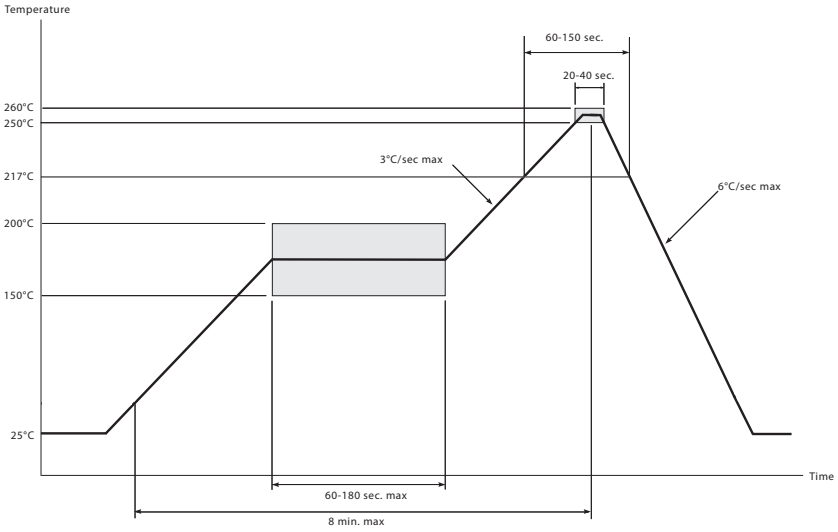


Figure 7-4: Maximum Pb-free Solder Reflow Profile

7.5 Packaging Data

Table 7-1: GV7700 Packaging Data

Parameter	Value
Package Type/Dimensions/Pad Pitch	Dual-row QFN: 84L 7mm x 7mm, 0.5mm pitch
Moisture Sensitivity Level (MSL)	3
Junction to Case Thermal Resistance, θ_{j-c}	28.8°C/W
Junction to Ambient Thermal Resistance (zero airflow), θ_{j-a}	42°C/W
Junction-to-Top of Package Characterization, ψ_{j-t}	1.0°C/W
Junction to Board Thermal Resistance, θ_{j-b}	13.6°C/W
Pb-free and RoHS Compliant	Yes

7.6 Ordering Information

Table 7-2: GV7700 Ordering Information

Part	Package
GV7700-INE3	84-pin dual-row QFN (260 pc/Tray)

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com