SEMTECH
GENNUM PRODUCTS

GV8500

Aviia™ Cable Driver

Features

- HDcctv 1.0, HD-SDI (ST 292), 3G-SDI (ST 424) and SD-SDI (ST 259) compliant
- Dual coaxial cable driving outputs with selectable slew rate
- 50Ω differential PECL input
- Pb-free and RoHS compliant
- Single 3.3V power supply operation
- Operating temperature range: 0°C to 70°C
- Small footprint (4mm x 4mm)

Applications

- Security and surveillance cameras
- Industrial and professional cameras
- Digital video recorders (DVR)
- Video mixers and switchers
- Camcorders
- Distribution amplifiers
- Repeaters

Description

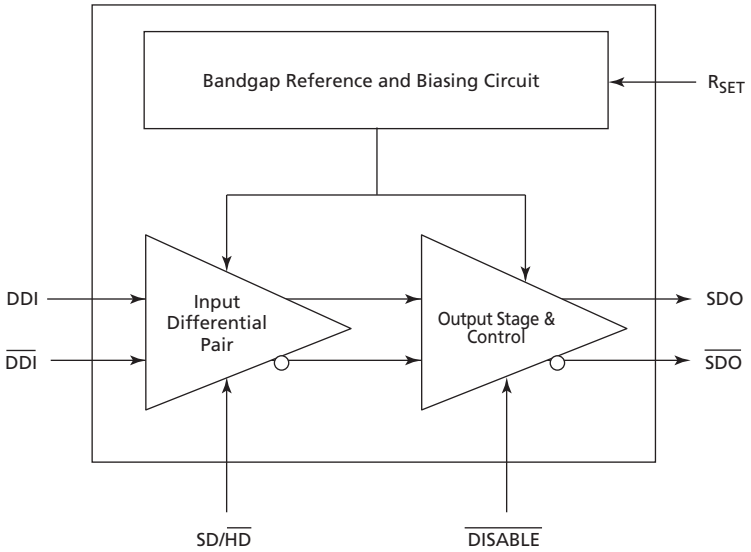
The GV8500 is a high-speed BiCMOS integrated circuit designed to drive one or two 75Ω coaxial cables.

The GV8500 can drive data rates up to 2.970Gb/s, and provides two selectable slew rates in order to achieve compliance to HDcctv 1.0, ST 292 at 1.485Gb/s, ST 424 at 2.970Gb/s, and ST 259 at 270Mb/s.

The GV8500 accepts a LVPECL level differential input that may be AC-coupled. External biasing resistors at the inputs are not required.

Power consumption is typically 168mW using a 3.3V power supply. The GV8500 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



Functional Block Diagram

Contents

1. Pin Out

1.1 Pin Assignment

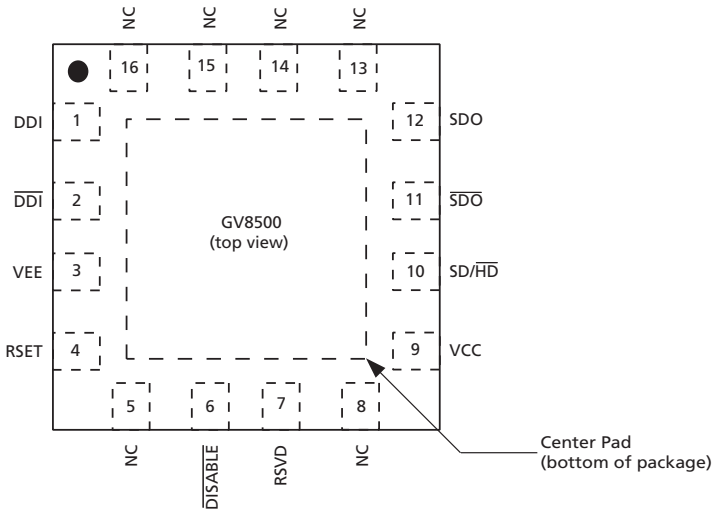


Figure 1-1: 16-Pin QFN

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description
1,2	DDI, $\overline{\text{DDI}}$	Analog	Input	Serial digital differential input.
3	V_{EE}	–	Power	Most negative power supply connection. Connect to GND.
4	R_{SET}	Analog	Input	External output amplitude control resistor.
5,8,13,14, 15,16	NC	–	–	No Connect. Not bonded internally.
7	RSVD	–	Reserved	Do not connect.
6	$\overline{\text{DISABLE}}$	Non Synchronous	Input	Serial output disable. When asserted LOW, the SDO/$\overline{\text{SDO}}$ output driver is powered off. SDO/$\overline{\text{SDO}}$ will float to V_{CC} through the pull-up resistor.
9	V_{CC}	–	Power	Most positive power supply connection. Connect to +3.3V.
10	SD/$\overline{\text{HD}}$	Non Synchronous	Input	Output slew rate control. When set HIGH, the output will meet ST 259 rise/fall time specifications (270Mb/s operation). When set LOW, the serial outputs will meet HDcctv 1.0/ST 292 (1.485Gb/s data rate) and ST 424 (2.970Gb/s data rate) rise/fall time specifications .
11,12	$\overline{\text{SDO}}$, SDO	Analog	Output	Serial digital differential output.
–	Center Pad	–	Power	Connect to most negative power supply plane following the recommendations in Recommended PCB Footprint on page 11.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to 3.6 V_{DC}
Input ESD Voltage	4kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Solder Reflow Temperature	260°C

NOTE: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristic sections is not implied.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

V_{CC} = 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CC}	–	3.135	3.3	3.465	V
Power Consumption	P_D	T_A = 25°C, SDO/$\overline{SDO}$ enabled	–	168	180	mW
		T_A = 25°C, SDO/$\overline{SDO}$ disabled	–	96	–	mW
Supply Current	I_s	T_A = 25°C, SDO/$\overline{SDO}$ enabled	–	51	–	mA
		T_A = 25°C, SDO/$\overline{SDO}$ disabled	–	29	–	mA
Output Voltage	V_{CMOUT}	Common mode	–	V_{CC} - V_{OUT}	–	V
Input Voltage	V_{CMIN}	Common mode	1.4 + ΔV_{DDI}/2	–	V_{CC} - ΔV_{DDI}/2	V
SD/$\overline{HD}$, $\overline{DISABLE}$ Input	V_{IH}	I_{IH} <= 10µA	2.0	–	–	V
	V_{IL}	I_{IL} <= 10µA	–	–	0.8	V

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

V_{CC} = 3.3V ±5%; T_A = 0°C to 70°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR_{SDO}	–	–	–	2.97	Gb/s	1
Additive Jitter	–	2.97Gb/s	–	22	–	ps_{p-p}	–
	–	1.485Gb/s	–	20	–	ps_{p-p}	–
	–	270Mb/s	–	16	–	ps_{p-p}	–
Rise/Fall Time	t_r, t_f	SD/$\overline{HD}$=0	–	–	135	ps	2
	t_r, t_f	SD/$\overline{HD}$=1	400	–	800	ps	2
Mismatch in rise/fall time	$\triangle t_r$, $\triangle t_f$	–	–	–	35	ps	–
Duty cycle distortion	–	SD/$\overline{HD}$=0, 2.97Gb/s	–	–	27	ps	3
	–	SD/$\overline{HD}$=0, 1.485Gb/s	–	–	30	ps	3
	–	SD/$\overline{HD}$=1, 270Mb/s	–	–	100	ps	3
Overshoot	–	SD/$\overline{HD}$=0	–	–	10	%	3
	–	SD/$\overline{HD}$=1	–	–	8	%	3
Output Return Loss	ORL	5MHz – 1.485GHz	15	20	–	dB	4
Output Voltage Swing	V_{OUT}	R_{SET} = 750Ω	750	800	850	mV_{p-p}	3
Input Voltage Swing	$\triangle V_{DDI}$	Differential	100	–	2200	mV_{p-p}	–

NOTES:

1. The input coupling capacitor must be set accordingly for lower data rates.
2. Rise/Fall time measured between 20% and 80%.
3. Single Ended into 75Ω external load.
4. ORL depends on board design. The GV8500 achieves this specification on Gennum's evaluation boards.

3. Input/Output Circuits

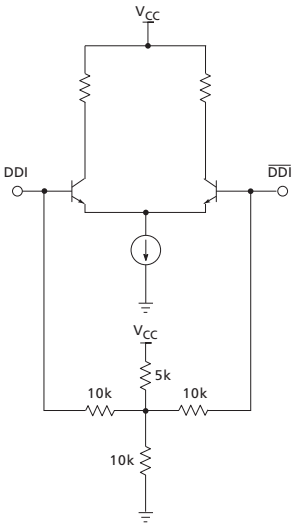


Figure 3-1: Differential Input Stage (DDI/$\overline{\text{DDI}}$)

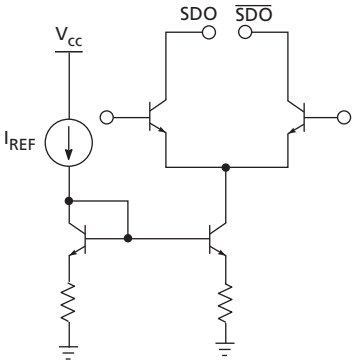


Figure 3-2: Differential Output Stage (SDO/$\overline{\text{SDO}}$)

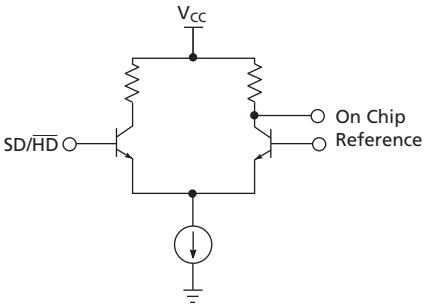


Figure 3-3: Slew Rate Select Input Stage

4. Detailed Description

4.1 Input Interfacing

DDI/$\overline{\text{DDI}}$ are high impedance differential inputs. The equivalent input circuit is shown in Figure 3-1.

Several conditions must be observed when interfacing to these inputs:

- The differential input signal amplitude must be between 100 and 2200mVpp
- The common mode voltage range must be as specified in the DC Electrical Characteristics on page 4
- For input trace lengths longer than approximately 1cm, the inputs should be terminated as shown in the Typical Application Circuit

The GV8500 inputs are self-biased, allowing for simple AC-coupling to the device. For serial digital video, a minimum capacitor value of 4.7µF should be used to allow coupling of pathological test signals. A tantalum capacitor is recommended.

SD/$\overline{\text{HD}}$ Input Pin

The GV8500 SDO rise and fall times can be set to comply with both HDcctv 1.0, ST 292, ST 424 and ST 259. At 270Mb/s (ST 259) or any data rate that requires longer rise and fall time characteristics, the SD/$\overline{\text{HD}}$ pin must be set HIGH by the application layer.

For HDcctv 1.0, ST 292 and ST 424 standards and signals which require faster rise and fall times, this pin should be set LOW.

4.2 Output Interfacing

The GV8500 outputs are current mode, and will drive typically 800mV into a 75Ω load. These outputs are protected from accidental static damage with internal ESD protection diodes.

In order for a DDI output circuit using the GV8500 to meet this specification, the output application circuit shown in the Typical Application Circuit on page 9 is recommended.

The value of L_{COMP} will vary depending on the PCB layout, with a typical value of 5.6nH. A 4.7µF capacitor is used for AC-coupling the output of the device. This value is chosen to ensure that pathological signals can be coupled without a significant DC component occurring. Please see Application Information on page 9 for more details.

4.2.1 Output Amplitude (RSET)

The output amplitude of the GV8500 can be adjusted by changing the value of the R_{SET} resistor as shown in Table 4-1. For an 800mV_{p-p} output with a nominal ±7% tolerance, a value of 750Ω is required. A ±1% SMT resistor should be used.

The R_{SET} resistor is part of the high-speed output circuit of the GV8500. The resistor should be placed as close as possible to the R_{SET} pin. In addition, the PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the R_{SET} resistor and the R_{SET} pin.

Table 4-1: R_{SET} vs. V_{OD}

R_{SET} R (Ω)	Output Swing (mVp-p)
995	608
824	734
750	800
680	884
573	1040

NOTE: For reliable operation of the GV8500 over the full temperature range, do not use an R_{SET} value below 573Ω.

4.2.2 Output Disable

The serial output disable ($\overline{\text{DISABLE}}$), disables power to the current mode serial digital output driver. When asserted LOW, the SDO/$\overline{\text{SDO}}$ output driver is powered off. SDO/$\overline{\text{SDO}}$ will float to V_{CC} through the pull-up resistor.

NOTE: If the $\overline{\text{DISABLE}}$ pin is left as a No Connect (NC), the SDO/$\overline{\text{SDO}}$ outputs are still active.

4.3 Output Return Loss Measurement

To perform a practical return loss measurement, it is necessary to force the GV8500 output to a DC high or low condition. The actual measured return loss will be based on the outputs being static at V_{CC} or V_{CC}-1.6V. Under normal operating conditions the outputs of the device swing between V_{CC}-0.4V and V_{CC}-1.2V.

5. Application Information

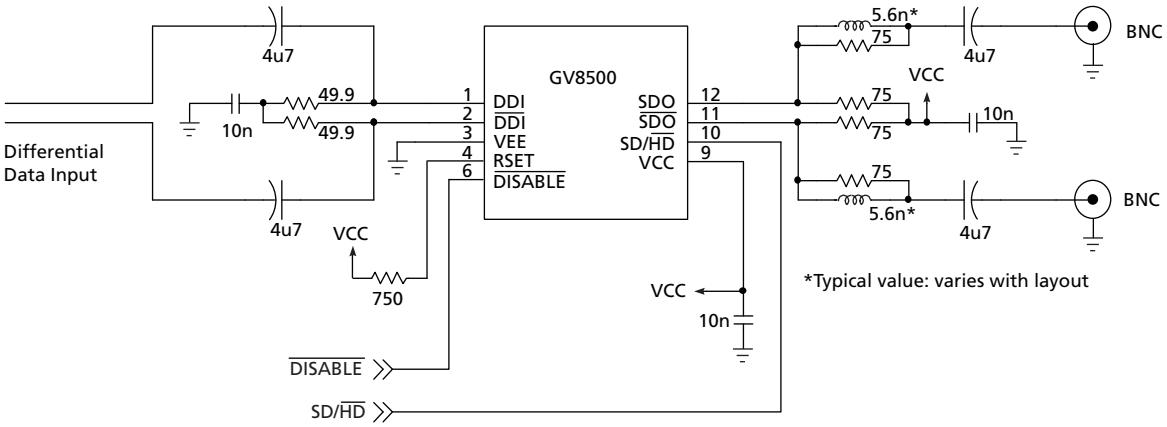
5.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDcctv.

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- The PCB trace width for 1.485Gb/s data rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance
- The PCB ground plane is removed under the GV8500 output components to minimize parasitic capacitance
- The PCB ground plane is removed under the GV8500 R_{SET} pin and resistor to minimize parasitic capacitance
- Input and output BNC connectors are surface mounted in-line to eliminate a transmission line stub caused by a BNC mounting via high-speed traces which are curved to minimize impedance variations due to change of PCB trace width

5.2 Typical Application Circuit

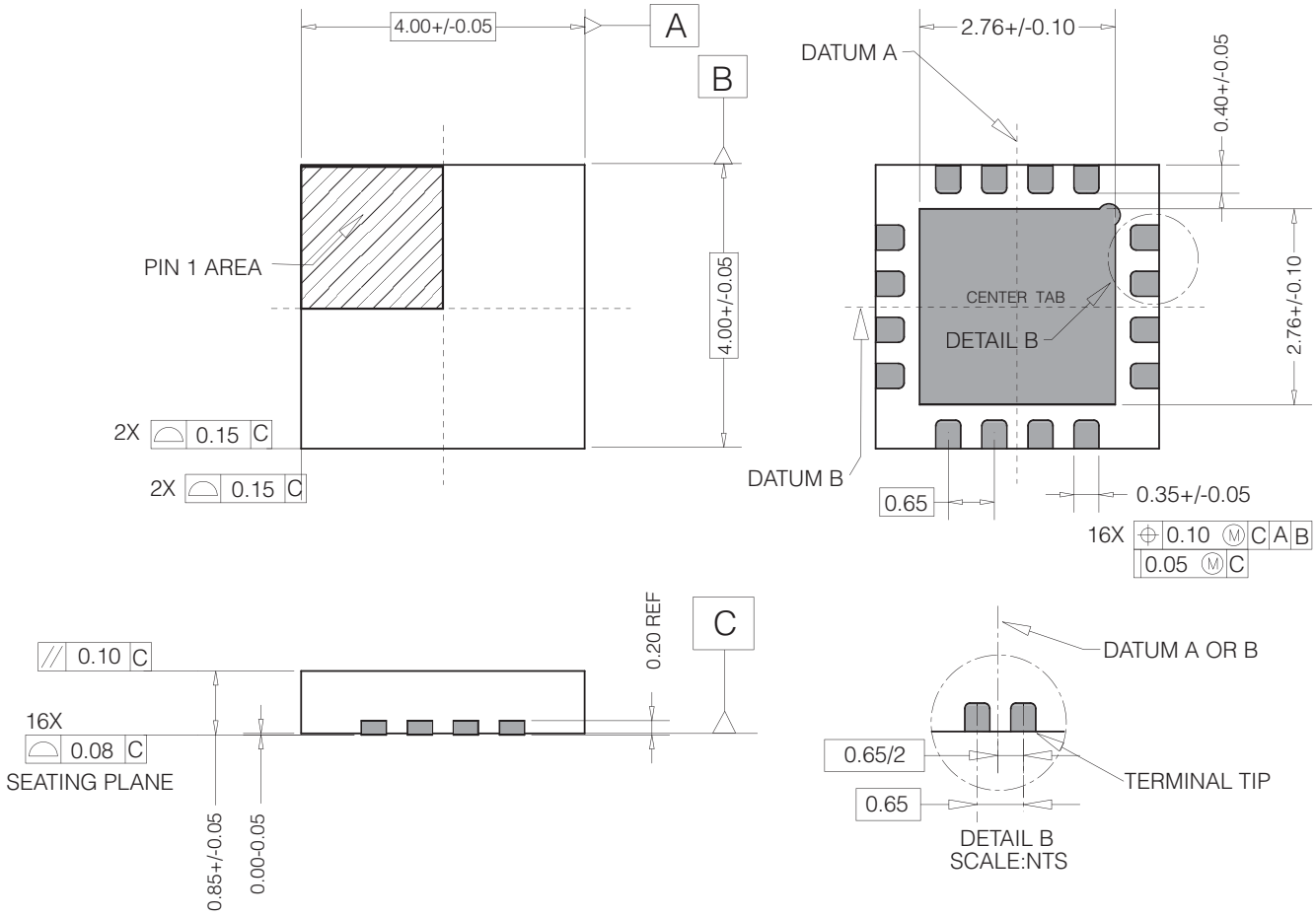


NOTE: All resistors in Ohms, capacitors in Farads, and inductors in Henrys, unless otherwise noted.

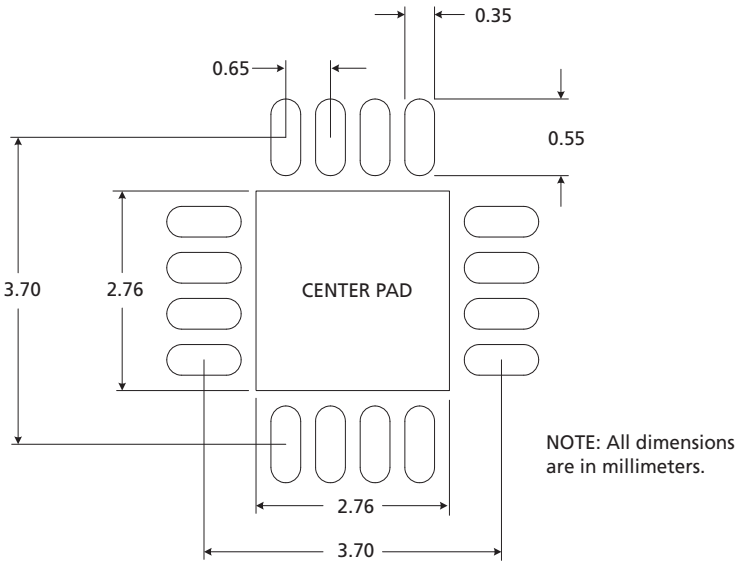
Figure 5-1: Typical Application Circuit

6. Package & Ordering Information

6.1 Package Dimensions



6.2 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane (VEE) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, Ψ	11.0°C/W
Pb-free and RoHS compliant	Yes

6.4 Solder Reflow Profiles

The GV8500 is available in a Pb-free package. Its is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 6-1.

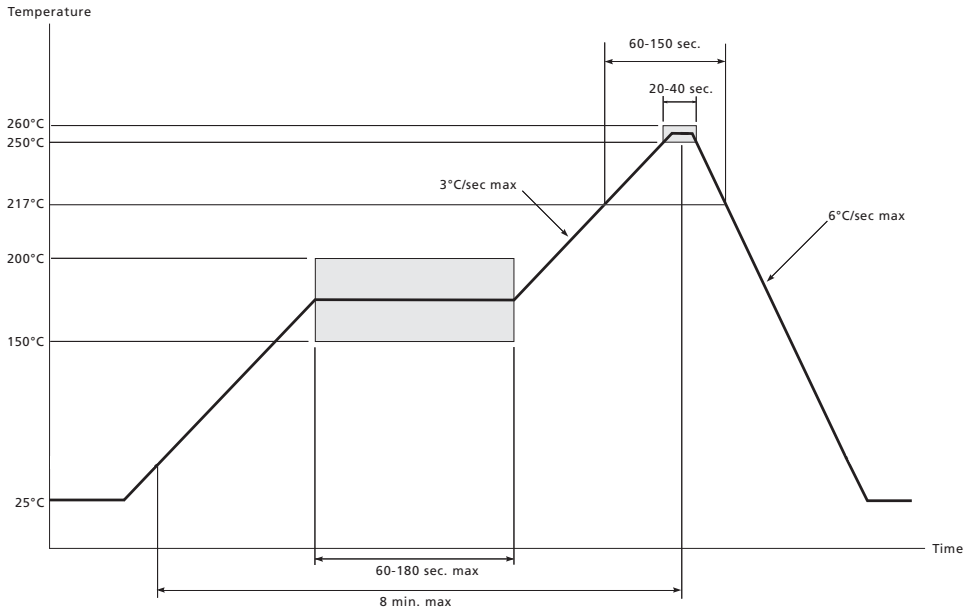
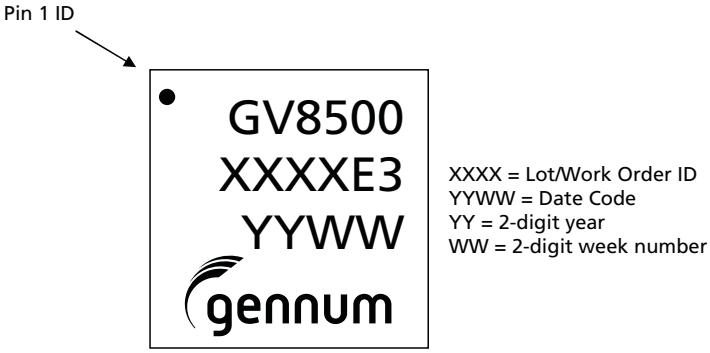


Figure 6-1: Maximum Pb-free Solder Reflow Profile (Preferred)

6.5 Marking Diagram



XXXX = Lot/Work Order ID
YYWW = Date Code
YY = 2-digit year
WW = 2-digit week number

6.6 Ordering Information

Part Number	Package	Temperature Range
GV8500-CNE3	16-pin QFN	0°C to 70°C

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
1	157936	–	April 2012	Added 3Gb/s functionality.
0	156703	–	July 2011	New document

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