Document No. QR-DE-02/C

汕頭超聲顯示器有限公司
SHANTOU GOWORLD DISPLAY CO., LTD.

SPECIFICATION FOR TFT MODULE

Part No.: GWMTF6619E

Customer: _____

Rev: E00

Issued Date: 2008-08-01

Approved by: _____

Signature: _____

Date: _____

Please sign the cover page of the spec for your approval and return it to us within a month after you receive the spec from Goworld Display. If we do not receive the signed spec even after one month later, we will consider that the spec was already accepted by your company.

Designed by: Engineering Dept.				QA Dept	Customer
Prepared		Checked	Approved	Approved	Approved
LCD	LCM				
	林铤	王彦涵	黄宏生		

Table of Contents

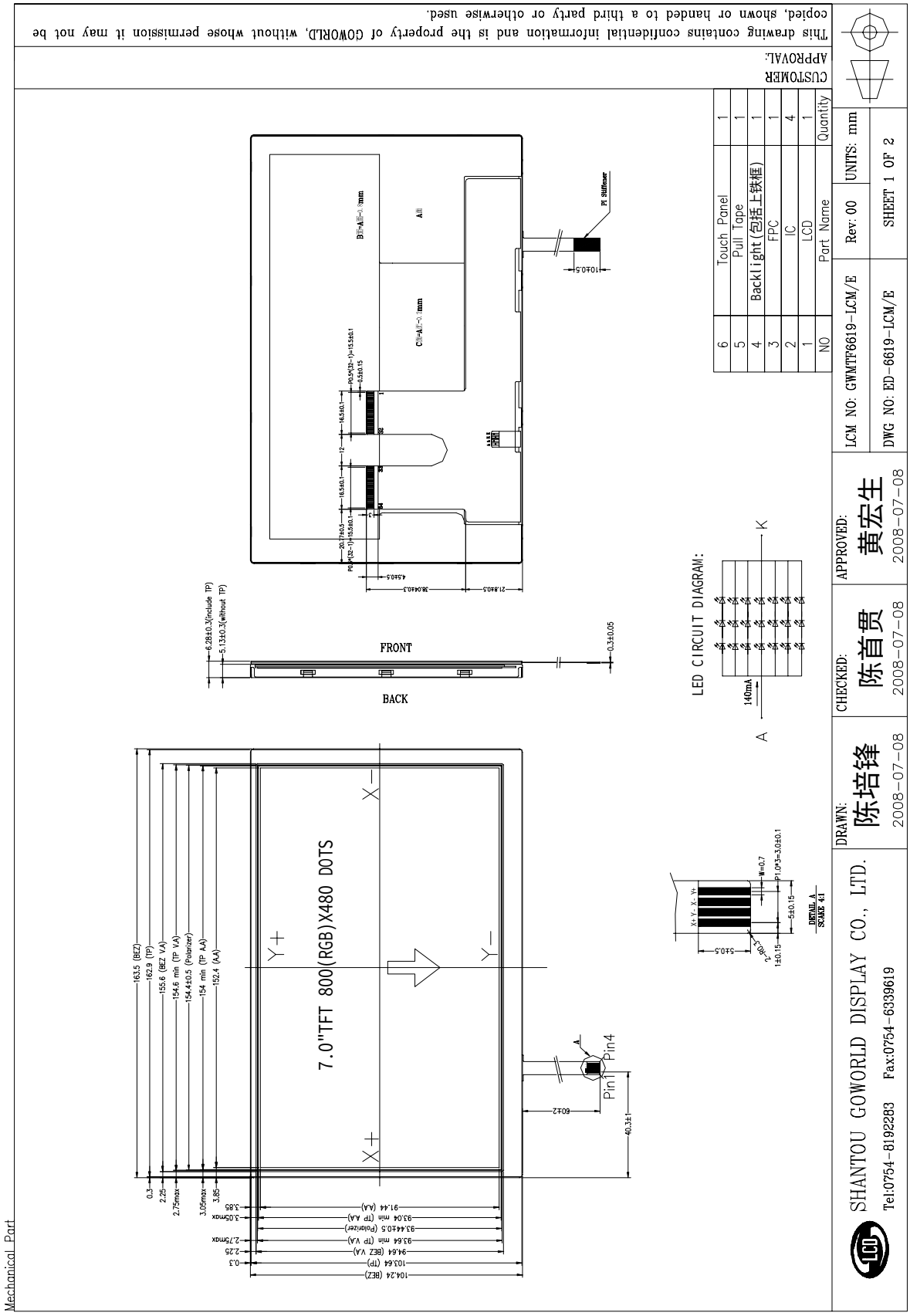
Revision History

Rev.	Comment	Date
A00	Original Version	2008-03-06
A01	Add cell gap and polarizer feature. Modify the function description of pins.	2008-03-14
B00	Modify the FPC, PCB and connectors.	2008-04-28
B01	Modify Viewing Angle range	2008-06-18
D00	Remove the PCB	2008-07-08
E00	Add the TP.	2008-08-01

1 General Specifications

Item	Standard Value	Unit
LCD Type	TFT, NORMALLY WHITE	/
Viewing Direction	12 O'CLOCK (Better Vision)	/
Color	262K	/
LCM Size	7"	inch
Module Dimension	163.5(W) ×104.24(H) ×6.28 (T)	mm
Active Area	152.4(W)X91.44(H)	mm
Pixel Format	800(RGB)X480	pixel
Pixel size	190.5X190.5	um
Cell gap	3.85	um
LCD Controller & Driver	Source:HX8232A x 3 Gate:HX8643A x 1	/
Interface Type	18 Bits RGB	/
Backlight Type	21-led (Parallel and serial)	/
Operation temperature range	-20~+70	°C
Storage temperature range	-30~+80	°C
TP Surface Feature	Anti-glare	/

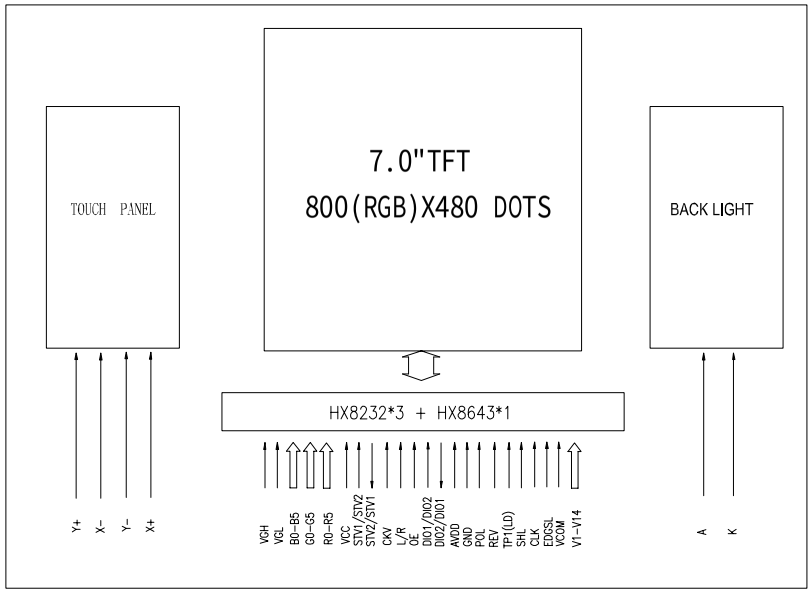
2 Mechanical Diagram



Add: 21 Xingye Road, Shantou, Guangdong Post Code: 515041
Tel: 86-754-8245666 FAX: 86-754-8256157

Electrical Part

Block Diagram:



Display type:TFT/Normal white
Display mode:Transmissive
Viewing direction: 12'clock
Driver IC:HX8232*3+HX8643*1
Interface type: 6-6-6bits RGB
(Digital power)VCC=3.3±0.3V
(Analog power)AVDD=6.5V~13.5V
Backlight: White LED
Iled=140mA Vled=9.9V±0.6V
Operating temprature: -20° C ~ +70° C
Storage temprature: -30° C ~ +80° C
All unmarked tolerance: ±0.3mm

PIN	SYMBOL
1	X+
2	Y-
3	X-
4	Y+

Pin Description:

PIN	Symbol	Description
1~2	K	**Power supply cathode input for backlight.**
3	NC	**NC**
4~5	A	**Power supply anode input for backlight.**
6	NC	**NC**
7	GND	**Ground.**
8	NC	**NC**
9	VGH	**Power supply for LCM drive output High.**
10	NC	**NC**
11	VGL	**Power supply for LCM drive output low.**
12	NC	**NC**
13	VCC	**Digital power supply**
14	STV1	When L/R=H, STV1 is used for start pulse input. When L/R=L, STV1 is used for start pulse output.
15	STV2	When L/R=H, STV2 is used for start pulse output. When L/R=L, STV2 is used for start pulse input.
16	CKV	This is the clock input for chip internal shift register. Data is shifted at each rising edge of this clock.
17	L/R	**Shift direction control pin.**
18	OE	**Output enable.**
19	DIO2	When SHL=H, DIO2 is used for start pulse output. When SHL=L, DIO2 is used for start pulse input.
20	AVDD	**Analog power supply.**
21	POL	**Polarity inverting input.**
22	REV	The REV signal controls data inversion internally to the driver. Display data is inverted when REV=H. Display data is not inverted when REV=L.
23	TP1(LD)	The contents of the data register are transferred to the latch circuit at the rising edge of LD. Then the gray scale voltage is output from the device at the falling edge of LD. For normal operation, it is required to input one LD per horizontal display line.
24~29	B5~B0	**DATA BUS**
30~43	V14~V1	**Correction reference voltage.**
44~49	G5~G0	**DATA BUS**
50~55	R5~R0	**DATA BUS**
56	SHL	**Shift direction control input.**
57	CLK	**The display data is stored to the internal data register at the rising edge of CLK.**
58	EDGSL	Define clock edge select input, default EDGSL=L. EDGSL=L:Latch data by rising edge of clock. EDGSL=H:Latch data by rising and falling edges of clock.
59	VCOM	**A supply voltage to the common electrode of TFT panel.**
60	DIO1	When SHL=H, DIO1 is used for start pulse input. When SHL=L, DIO1 is used for start pulse output.
61	NC	**NC**
62	NC	**NC**
63	NC	**NC**
64	NC	**NC**

E00:Add Touch Panel base on D00。
D00:remove PCB base on B00,modify backlight current 。
B00:修改FPC、PCB和连接器型号。
A03:修改模块工作温度。
A02:修改模块厚度和背光电流值，增加透明胶纸。
A01:修改模块厚度、连接器位置标注方式和背光灯数量。
A00: Original Edition
Revison History:

CUSTOMER APPROVAL:

SHANTOU GOWORLD DISPLAY CO., LTD.
Tel:0754-8192283 Fax:0754-6339619

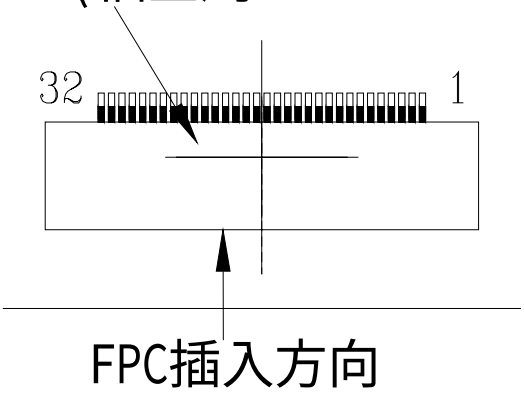
DRAWN:	CHECKED:	APPROVED:			
林鋌	王彦涵	黄宏生	LCM NO: GWMTF6619-LCM/E	Rev: 00	UNITS: mm
2008-07-08	2008-07-08	2008-07-08	DWG NO: ED-6619-LCM/E	SHEET 2 OF 2	

3 I/O Terminal

3.1 Pin Description

PIN	Symbol	Description
1~2	K	Power supply cathode input for backlight.
3	NC	NC
4~5	A	Power supply anode input for backlight.
6	NC	NC
7	GND	Ground.
8	NC	NC
9	VGH	Power supply for LCM drive output High.
10	NC	NC
11	VGL	Power supply for LCM drive output low.
12	NC	NC
13	VCC	Digital power supply
14	STV1	When L/R=H, STV1 is used for start pulse input. When L/R=L, STV1 is used for start pulse output.
15	STV2	When L/R=H, STV2 is used for start pulse output. When L/R=L, STV2 is used for start pulse input.
16	CKV	This is the clock input for chip internal shift register. Data is shifted at each rising edge of this clock.
17	L/R	Shift direction control pin.
18	OE	Output enable.
19	DIO2	When SHL=H, DIO2 is used for start pulse output. When SHL=L, DIO2 is used for start pulse input.
20	AVDD	Analog power supply.
21	POL	Polarity inverting input.
22	REV	The REV signal controls data inversion internally to the driver. Display data is inverted when REV=H. Display data is not inverted when REV=L.
23	TP1(LD)	The contents of the data register are transferred to the latch circuit at the rising edge of LD. Then the gray scale voltage is output from the device at the falling edge of LD. For normal operation, it is required to input one LD per horizontal display line.
24~29	B5~B0	DATA BUS
30~43	V14~V1	Correction reference voltage.
44~49	G5~G0	DATA BUS
50~55	R5~R0	DATA BUS
56	SHL	Shift direction control input.
57	CLK	The display data is stored to the internal data register at the rising edge of CLK.
58	EDGSL	Define clock edge select input, default EDGSL=L. EDGSL=L:Latch data by rising edge of clock. EDGSL=H:Latch data by rising and falling edges of clock.
59	VCOM	A supply voltage to the common electrode of TFT panel.
60	DIO1	When SHL=H, DIO1 is used for start pulse input. When SHL=L, DIO1 is used for start pulse output.
61	NC	NC
62	NC	NC
63	NC	NC
64	NC	NC

Connector(福金鹰：FPC PH0.5mm 32P下接翻盖 卧贴)



Note 1

Note 1:

Connector	Feature
FPC PH0.5mm 32P 下接翻盖 卧贴	Bottom Contact；Pitch:0.5mm；32pin

Note2

SHL=H: DIO1➔OUT1➔•••➔OUT804➔DIO2

SHL=L: DIO2➔OUT804➔•••➔OUT1➔DIO1

L/R =H: STV1➔OUT1➔OUT2➔ ••• ➔OUT480➔STV2

L/R =L: STV2➔OUT480➔ ••• ➔OUT2➔OUT1➔STV1

4 Electro-optical Specifications

4.1 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Digital supply voltage for LCD	VCC	-0.5	5	**V**
Analog supply voltage for LCD	AVDD	-0.5	13.5	**V**
Supply voltage	Vγ1~ Vγ7	0.4AVDD	AVDD + 0.3V	/
Supply voltage	Vγ8 ~ Vγ14	-0.3V	0.6AVDD	/
TFT Gate Operating Voltage	VGH	-0.3	+40	V
TFT Gate Operating Voltage	VGL	VGH-40	+0.3	V

4.2 Optical Characteristics

Ta = 25°C

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Lcm surface brightness		Ld			210		Cd/m2	
Viewing Angle range	**Horizontal**	3H	CR > =10		60		Deg.	
		9H			60		Deg.	Note 3
	Vertical	12H			45		Deg.	
		6H			60		Deg.	
Contrast ratio		CR	θ= 0°		400			Note 4
Luminous Uniformity		ΔL			85%		%	
White Chromaticity		x_w	θ= 0°		0.3070			Note5
		y_w			0.3362			
Reproduction of color	**Red**	x_R	θ= 0°		0.5838			
		y_R			0.3655			
	Green	x_G			0.3439			
		y_G			0.5449			
	Blue	x_B			0.1480			
		y_B			0.1173			

Note:

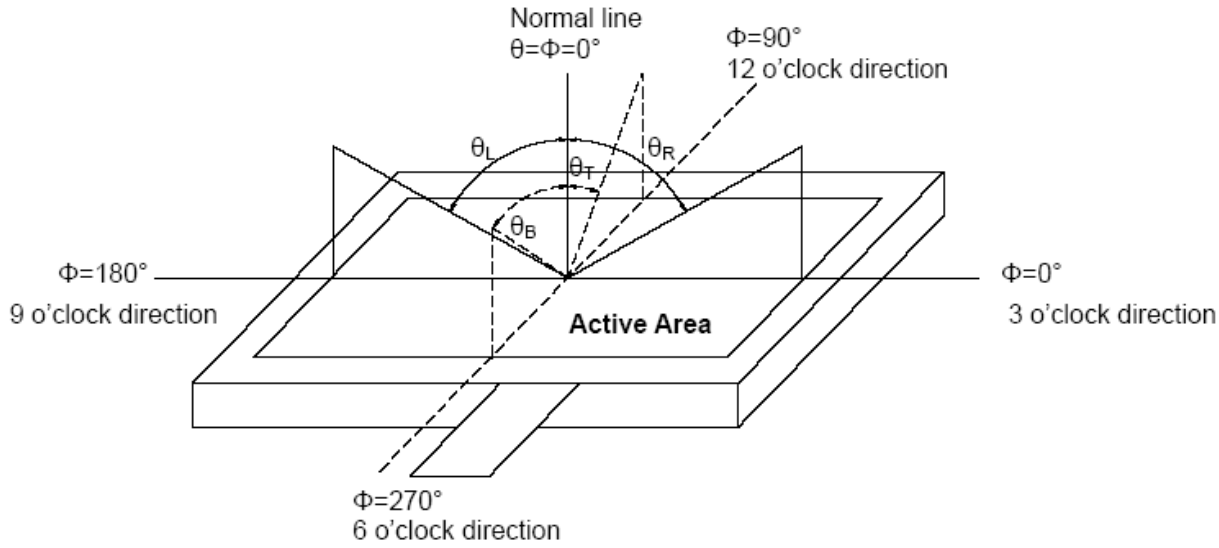
3、Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface .

4、Contrast measurements shall be made at viewing angle of θ= 0°and at the center of the LCD surface.Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. shown in Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

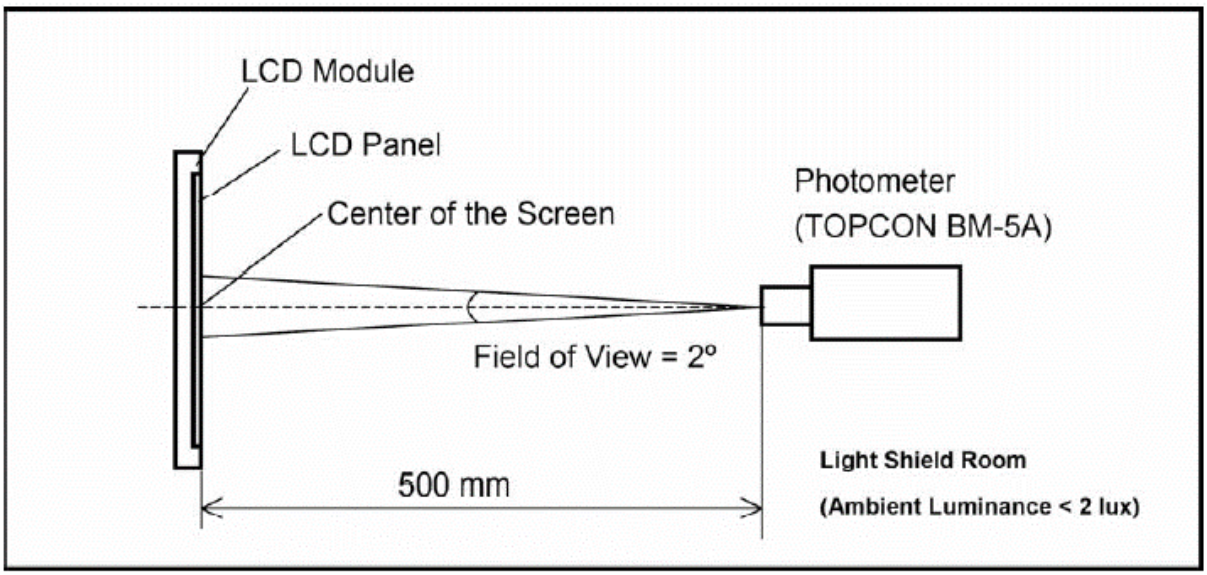
5、The color chromaticity coordinates specified in above Table shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the C/F. Measurement condition is C - light source & Halogen Lamp.

Note 3: Definition of Viewing Angle



Note 4: Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



4.3 Electrical Characteristics

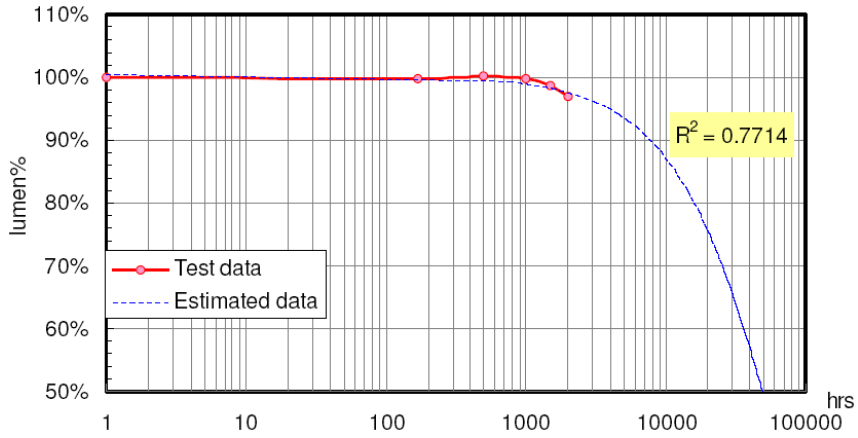
4.3.1 DC Electrical Characteristics

(VCC=2.7 to 3.6V,AVDD=6.5 to 13.5V, GND=0V,TA=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	Vcc	2.7	3.3	3.6	V	Digital power
Supply Voltage	AVDD	6.5	8.4	13.5	V	For the analog circuit power
Digital Operating Current For IC1	Icc		1.3	1.6	mA	FCLK=40MHZ, FLD=50KHZ, Vcc=3.3V in black pattern.
Analog Operating Current For IC1	Ioc		16	18	mA	FCLK=40MHZ, FLD=50KHZ, AVDD=8.4V,V1=8V,V14=0.4V In black pattern.
TFT Gate ON Voltage	VGH	7	16	20	V	
TFT Gate OFF Voltage	VGL	-15	-7	-5	V	
TFT Common Electrode Voltage	Vcom		+3.16		V	Note 6
Output Voltage for LED	Vf	9.3	9.9	10.5	V	
Output Current for LED	If		140		mA	20mA*7
LED life time	Hr1		50000		Hour	Note 7
TP Life Time	Hr2		1,000,000		t	250gf, 2t/s, R12.5mm Silicon rubber.

Note:

6. Vcom must be adjusted to optimize display quality : contrast ratio and etc.
7. LED life time (Hr) must be defined as the time in which it continues to operate under the follow graph:



LED Operating Life (25°C, 45%RH , 20mA)

Example of Correction Reference Voltage

Correction Reference Voltage	V1	9.93	V
	V2	9.44	V
	V3	7.92	V
	V4	7.38	V
	V5	7.00	V
	V6	6.35	V
	V7	6.07	V
	V8	4.02	V
	V9	3.73	V
	V10	3.09	V
	V11	2.72	V
	V12	2.18	V
	V13	0.64	V
	V14	0.14	V

4.3.2 AC Electrical Characteristics

(VCC=3.3V, AVDD=8.4V, GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK frequency	FCLK	-	40	47	MHZ	-
CLK pulse width	Tcw	6	-	-	ns	-
Data set-up time	Tsu	4	-	-	ns	D00~D55,REV and DIO1/2 to CLK
Data hold time	Thd	2	-	-	ns	D00~D55,REV and DIO1/2 to CLK
Propagation delay of DIO2/1	Tphl	6	10	15	ns	CL=25pF (Output)
Time that the last data to LD	Tld	1	-	-	Tcph	-
Pulse width of LD	Twld	2	-	-	Tcph	-
Time that LD to DIO1/2	Tlds	5	-	-	Tcph	-
POL set-up time	Tpsu	6	-	-	ns	POL to LD
POL hold time	Tphd	6	-	-	ns	POL to LD
Output stable time	Tst	-	-	12	us	10% or 90% target voltage, CL=60pF, R=2kΩ

(The measurement point for all of above signals is at 50% of input/output amplitude)

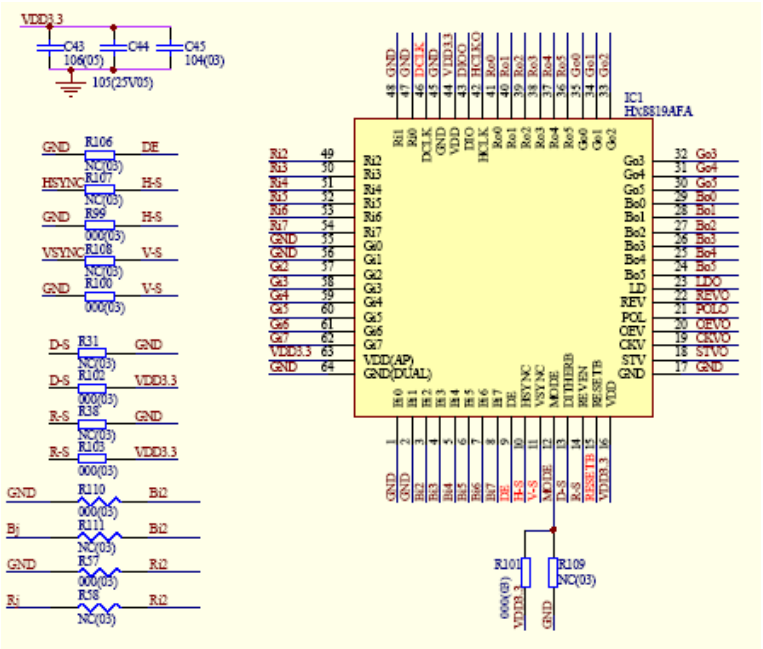
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CPV period	tCPV	5	-	-	us	-
CPV pulse width	tCPVH, tCPVL	2.5	-	-		50% duty cycle
Data setup time	tSU	0.7	-	-		-
Data hold time	tHD	0.7	-	-		-
CPV to output delay time	tPD1	-	-	1		CL=300pF
Start pulse output delay time	tPD2	-	-	0.8		CL=30pF

4.3.3 Power ON/OFF sequence

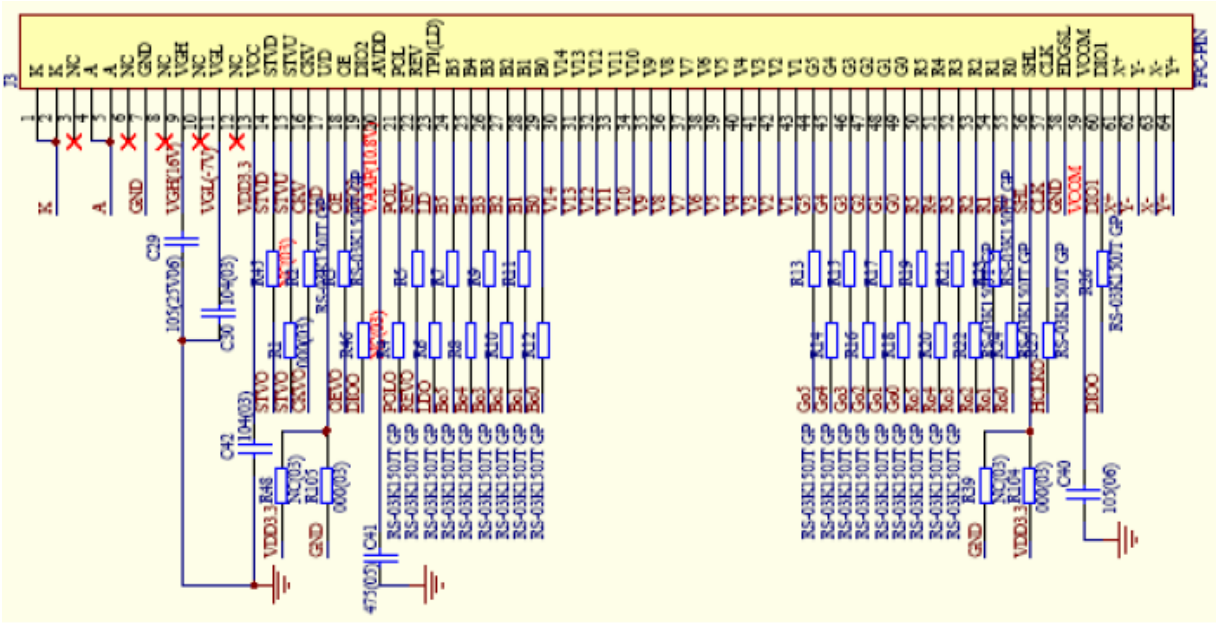
To prevent the device damage from latch up, the power ON/OFF sequence shown below must be followed.
When power on: VDD→VGL→VGH
When power off: VGH→VGL→VDD

4.3.4 HX8819AFA can be used for T-CON

Example of HX8819AFA(DE Mode):



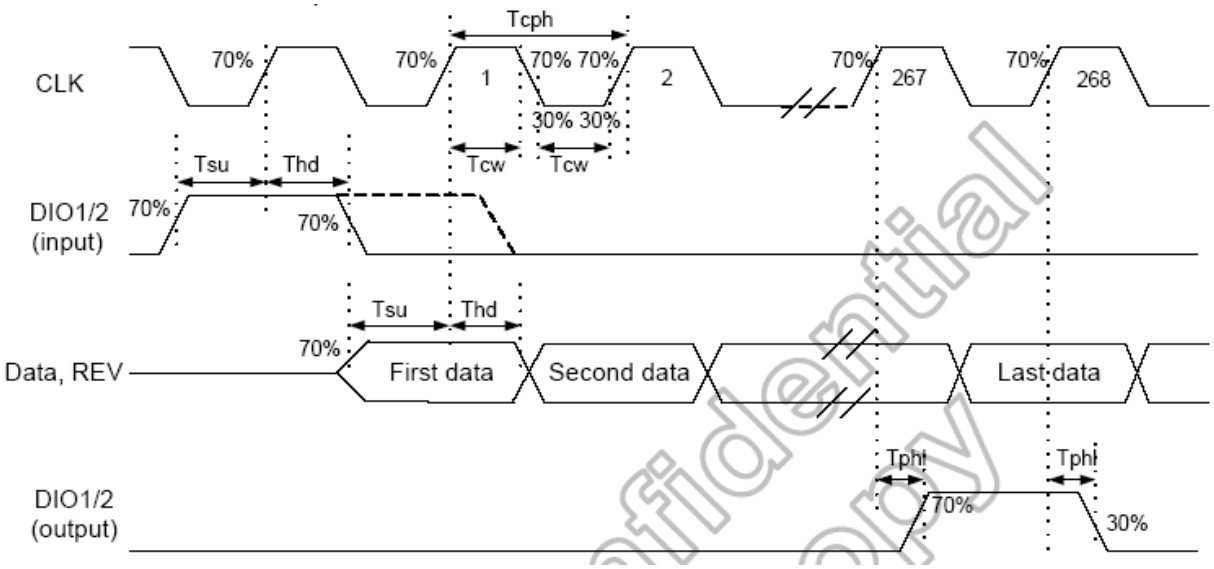
Example of FPC pin:



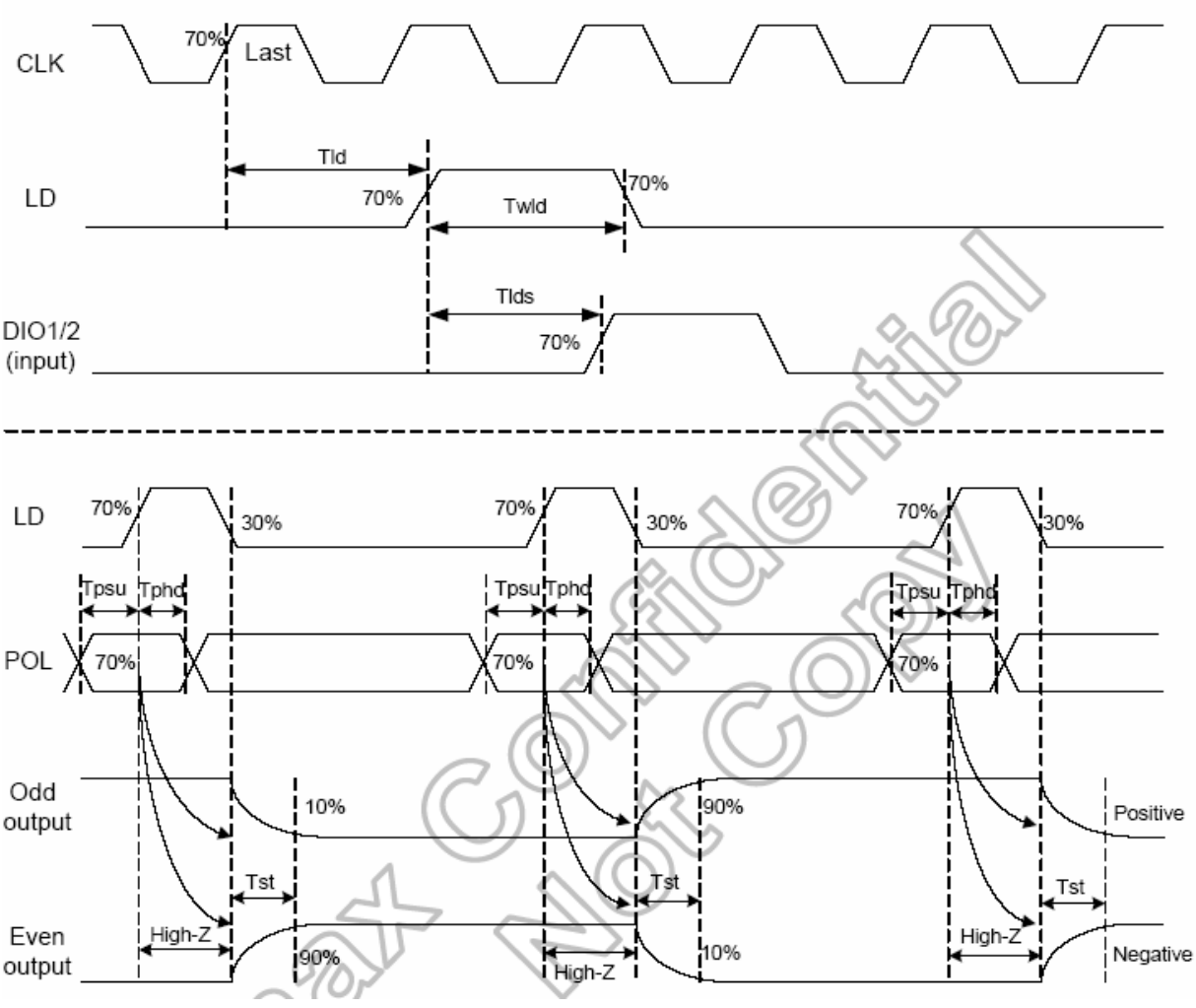
5 Waveform

5.1 Timing diagram 1

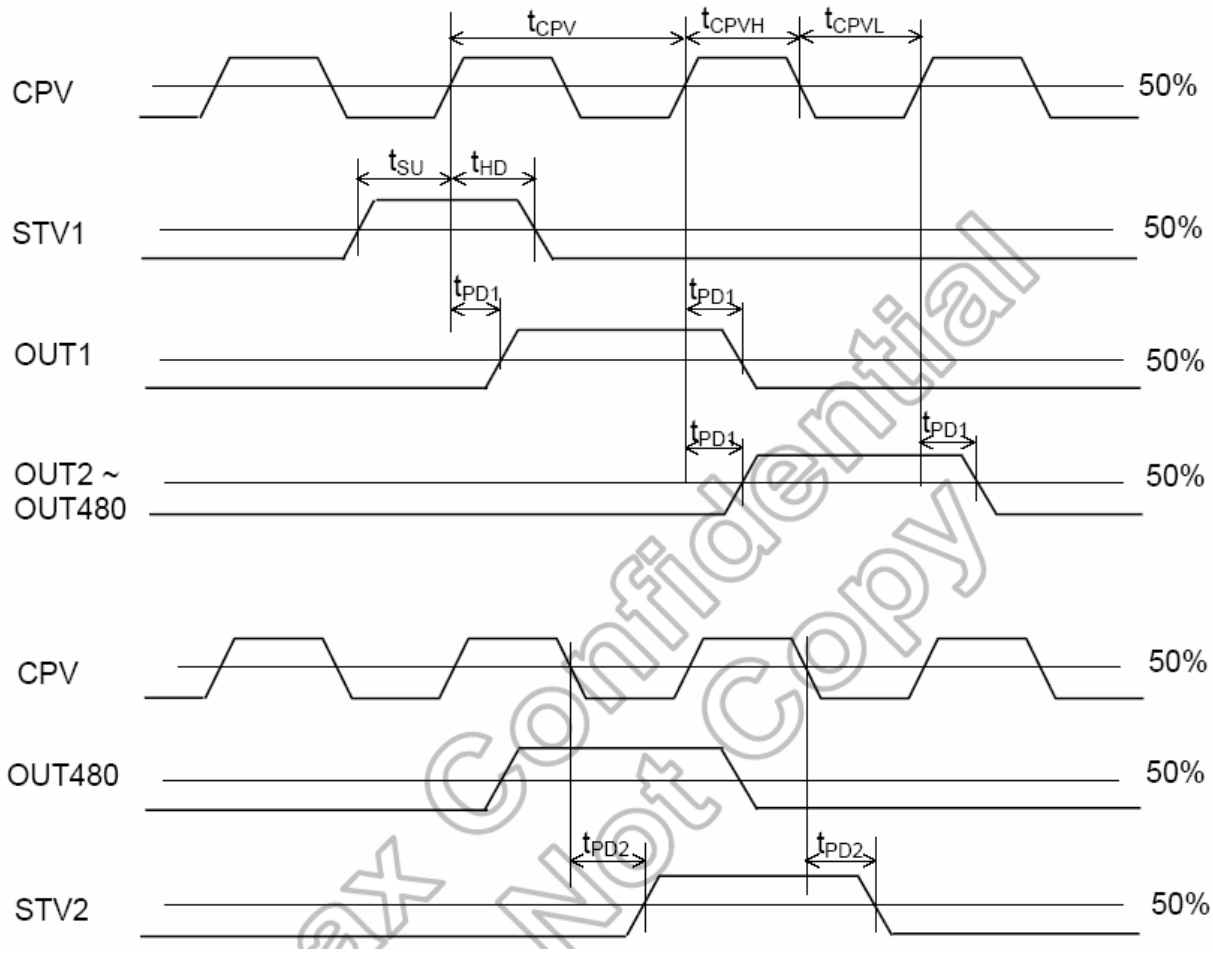
Example1(EDGSL=L):



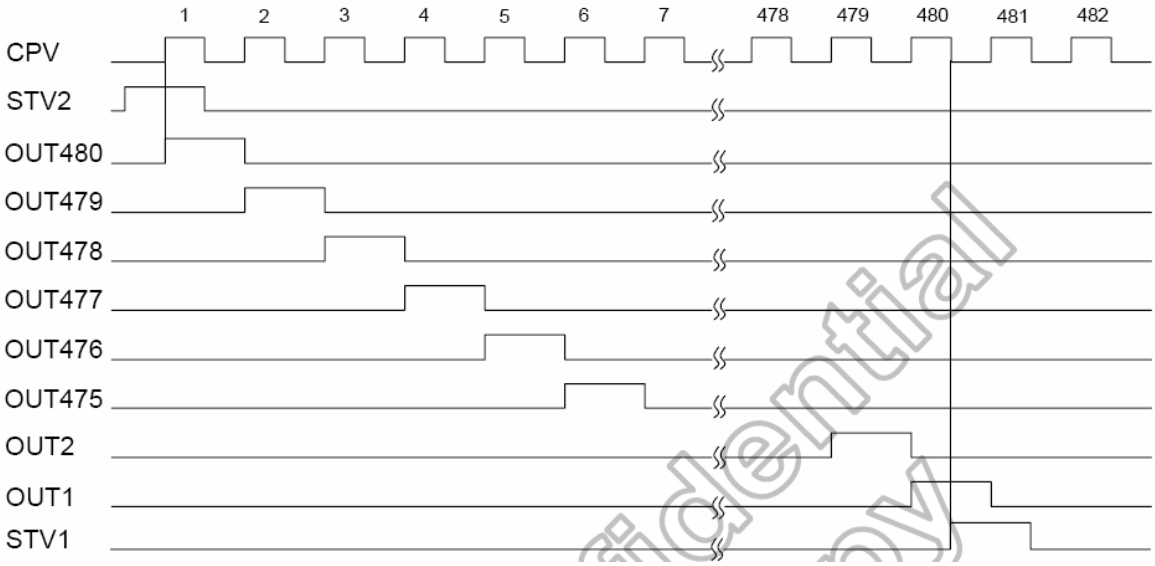
5.2 Timing diagram 2



5.3 Timing diagram 3



Example 2(L/R=L):



6 Reliability Test Items

NO.	Item	Test Conditions	Remark
1	High Temperature Storage	80±2℃/96H	Uncompleted Item
2	Low Temperature Storage	-30±2℃/96H	Uncompleted Item
3	High Temperature Operation	70±2℃/96H	Uncompleted Item
4	Low Temperature Operation	0±2℃/96H	Uncompleted Item

Note:

1、The test samples should be applied to only one test item.

2、Sample size for each test item is 5~10pcs.

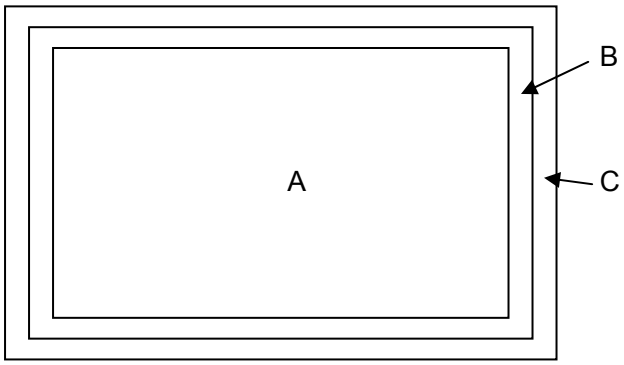
7 Quality Units

7.1 Inspection Condition

Light Source: Fluorescent light (Day-light Type) 20~40W

Distance: 30cm~50cm from inspector eyes to display surface. The viewing angle should be perpendicular to display surface.

7.2 Definition of Active Area, Viewing Area & Invisible Area



A: Active Area (A.A.)

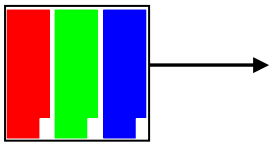
B: Viewing Area (V.A.)

C: Invisible Area (I.A.: After assembly by customer, this area is invisible. Cosmetic defect on this area must be ignored.)

7.3 Inspection Criteria

7.3.1 Definition of dot defect (Pixel defect)

7.3.1.1 Pixel and sub-pixel (Refer to below illustration)



A pixel = (R sub-pixel + G sub-pixel + B sub-pixel)

7.3.1.2 The definition of dot: The size of a defective dot over 1/2 sub-pixel should be regarded as one defective dot.

7.3.1.3 Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

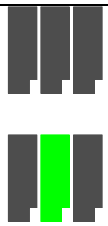
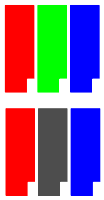
7.3.1.4 Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure R/G/B pattern.

7.3.1.5 Two dots adjacent (Refer to below illustration)

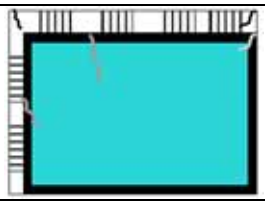
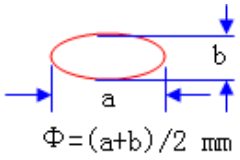
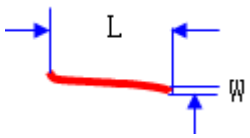
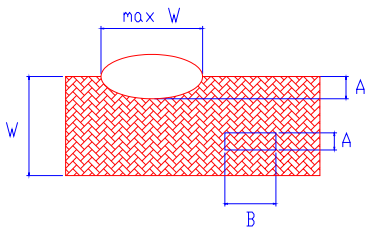
2 dot adjacent (Left-right) 2 dot adjacent (Top-down) 2 dot adjacent (Diagonal)

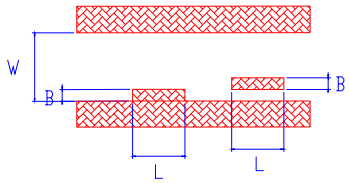
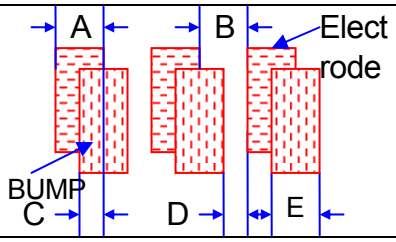
* In this section: black dot express defective dot; grey dot express normal dot.

7.3.2 Dot Defect (Bright Dot / Dark Dot)

Defect Description	Illustration	Judgment Criteria	Acceptable Defect Qty.		Class
			V.A. & A.A.	I.A.	
Bright Dot	OK black Pattern: All R/G/B Dark <u>Bright Green Dot:</u> R/G/B should be dark at black pattern, but G is bright. 	Bright R/G/B dot 2 dots adjacent	3 0	NA	Minor
Dark Dot	OK White pattern: All R/G/B Bright Dark Green Dot: R/G/B should be bright at white pattern, but G is dark. 	Dark R/G/B Dot 2 dots adjacent	5 1	NA	Minor
Remark	1. Total dot defect quantity should be equal or less than 5.				

7.3.3 Appearance inspection

Defect Description	Illustration	Judgment Criteria	Class
Glass crack		Not allowed	Minor
Circular type defect (Black spot / White spot)		Φ≤0.15mm, ignored 0.15mm<Φ≤0.50mm, N≤4 Φ>0.50mm, NG	Minor
Line type defect		W≤0.05mm & L≤0.3mm, Ignored 0.05mm<W≤0.10mm, 0.3mm<L≤2.0mm, N≤4 W>0.1mm or L>2.0mm, NG	Minor
FPC Defect: Pinhole, damage on circuit		A≤W/4 & B≤3W, ignored A>W/4 or B>3W, NG	Major

	W: Width		
FPC Defect: Etching defect (Protrude/Copper residue/burr)	 W: Distance btw two electrode	B≤W/4 & L≤3W, irremovable, ignored B>W/4 or L>3W, removable, NG	Major
FPC Defect: Crease/Impress	NA	Crease with an acute angle, NG Crease or impress with an obtuse angle, ignored	Minor
SMT: Component shifit		C≥E/2 & D≥B/2, ignored C<E/2 or D<B/2, NG	Minor

7.3.4 Function defect

Defect Description	Illustration	Judgment Criteria	Class
Line defect	Vertical lines Horizontal lines Cross lines etc	Not allowed	Major
Display defect	Abnormal display No display etc	Not allowed	Major

7.4 Precaution for using

(1) Recommended storage condition: 50-60%RH，25±5°C；

(2) TFT LCD is brittle. It may break when it is dropped or bumped on a hard surface. Please handle carefully.

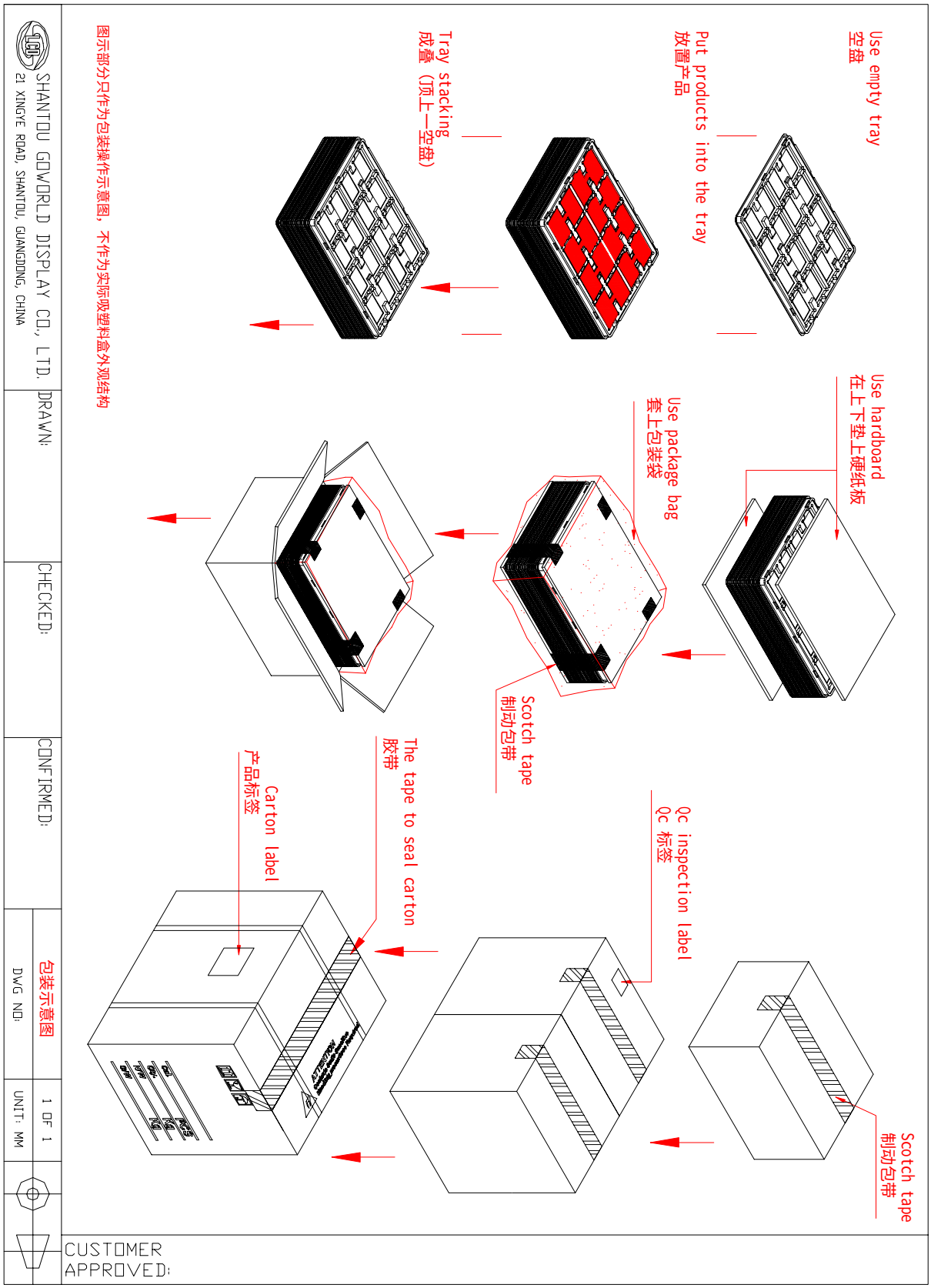
(3) Please don't clean polarizer by alcohol or acetone. Pure water is recommended.

(4) Please don't disassembly the module, it will invalidate the warranty agreements. Please use it within 6 months.

(5) This product is ESD sensitive. Please assure enough ESD protection whenever handling the product.

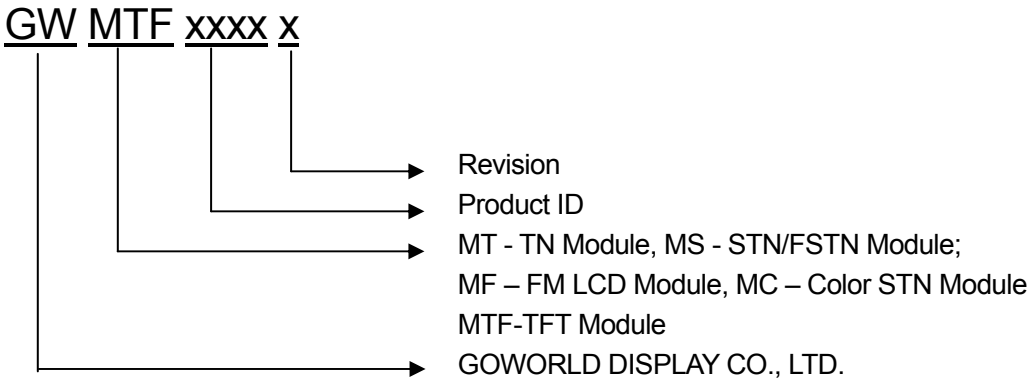
8.Others

8.1 Packaging



8.2 Classification

1) Part Number



2) Code-printing