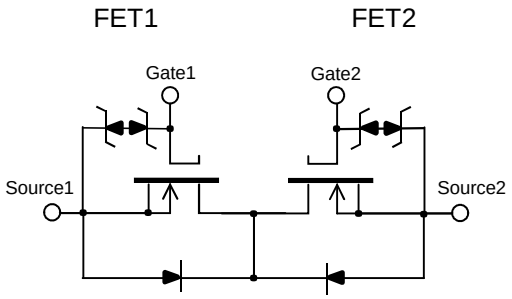
GWS2111
Dual 12V N-Channel Power MOSFET

Product Summary			
$V_{(BR)DSS}$	I_D=250uA	12.0 V	Min
$r_{DS(on)}$	V_{GS}=4.5V	34 mΩ	Typ

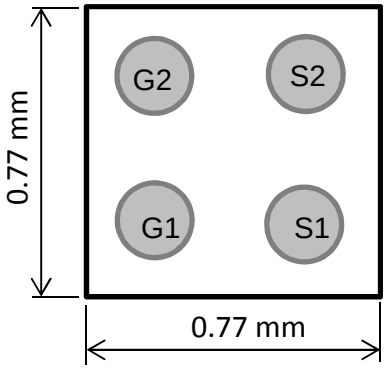
Features
- Low RDS (on) in a small footprint
- Ultra low gate charge and figure of merit
- Chip-scale 0.77 mm x 0.77 mm LGA package
- Low Thermal Resistance

Applications
- Li ion Battery Protection
- Portable Devices, Cell Phones, PDA
- Rated for short circuit and over current protection
- Integrated gate diodes provide ESD protection of 2500V HBM.

Equivalent Circuit



Description
The GWSXXXX is a Dual 12V, 34 mΩ, N-Channel Power Mosfet used for Li ion battery protection. It is offered in a chip-scale 0.77 mm X 0.77 mm LGA with a very low thickness profile of 0.20 mm. The device uses Great Wall Semiconductor's patented Lateral Power™ CMOS technology. It has extremely high power density, reducing the board size of Li Ion Battery power system. Designed for hand held devices with a high level of ESD protection.



Bottom View

Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

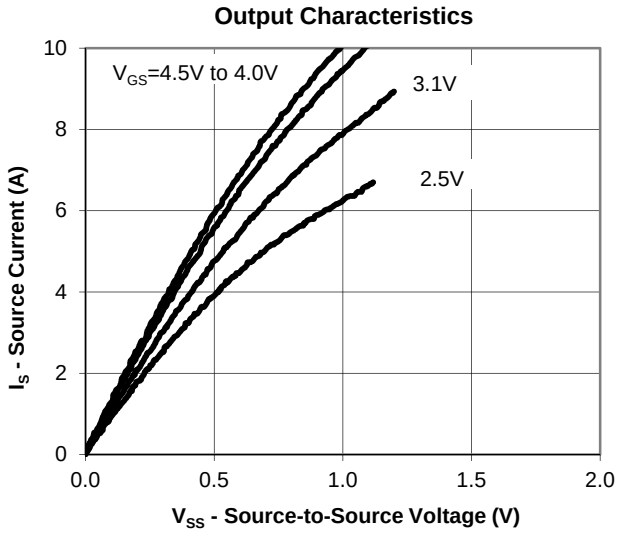
Parameter		Symbol	Steady State	Unit
Drain-Source Voltage		V_{DS}	12	V
Gate-Source Voltage		V_{GS}	± 8	
Drain Current[a]		I_D	1.0	A
Pulsed Drain Current		I_{DM}	10	
Maximum Power Dissipation[a]	T_A=25°C	P_D	1.0	W
	T_A=70°C		0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C

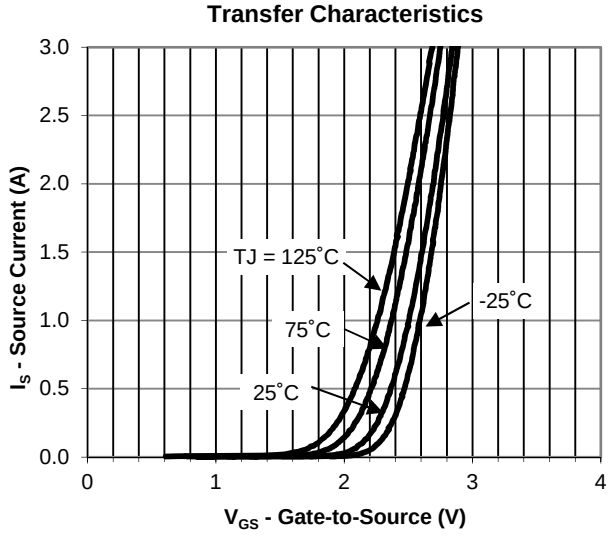
Thermal Resistance Ratings				
Parameter		**Symbol**	**Typ**	**Unit**
Junction-to-Ambient	Steady Sate	R_{thJA}	125	°C/W
Junction-to-Foot (Lead)	Steady Sate	R_{thJF}	16	

[a] Surface Mounted on FR4 Board.

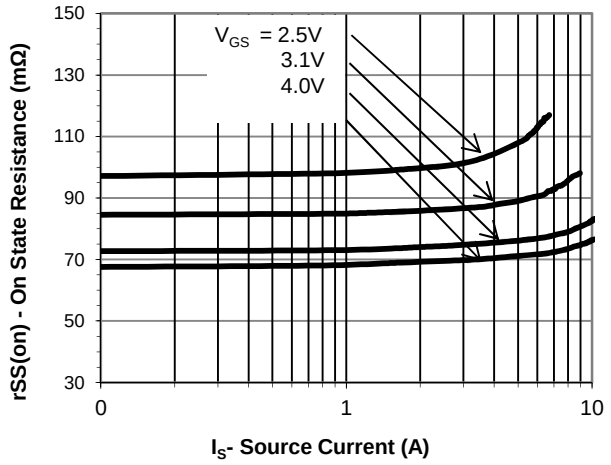
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	12			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0V, V_{DS} = 12V			1	uA
Gate Body Leakage	I_{GSS}	V_{DS} = 0V V_{GS} = ±8V			±10	uA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1mA	0.5	0.8	1.5	V
Drain-Source On-State Resistance[1] (per MOSFET)	$r_{DS(on)}$	V_{GS} = 4.5V, I_D = 0.5A	25	34	44	mΩ
		V_{GS} = 4.0V, I_D = 0.5A	27	36	49	
		V_{GS} = 3.1V, I_D = 0.5A	30	42	74	
		V_{GS} = 2.5V, I_D = 0.5A	43	50	114	
Source-Source On-State Resistance[1] (both MOSFETs in series)	$r_{SS(on)}$	V_{GS} = 4.5V, I_{SS} = 0.5A	50	68	88	
		V_{GS} = 4.0V, I_{SS} = 0.5A	53	72	97	
		V_{GS} = 3.1V, I_{SS} = 0.5A	59	84	148	
		V_{GS} = 2.5V, I_{SS} = 0.5A	86	100	228	
Source-Drain Diode Voltage	V_{SD}	V_{GS} = 0, I_S = 1A	0.5	0.8	1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 9.6V, I_D = 0.5A, V_{GS} = 4.0V		1.3		nC
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V, f = 1 MHz		150		pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			50		

Note: 1.Good Kelvin Measurement Required.

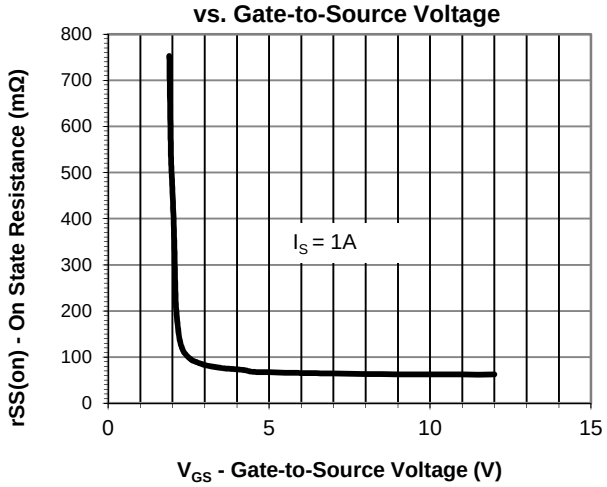




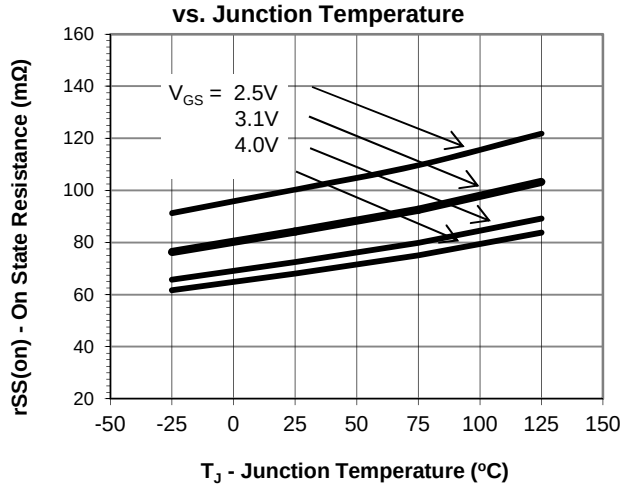
Source-Source On-State Resistance vs. Source Current



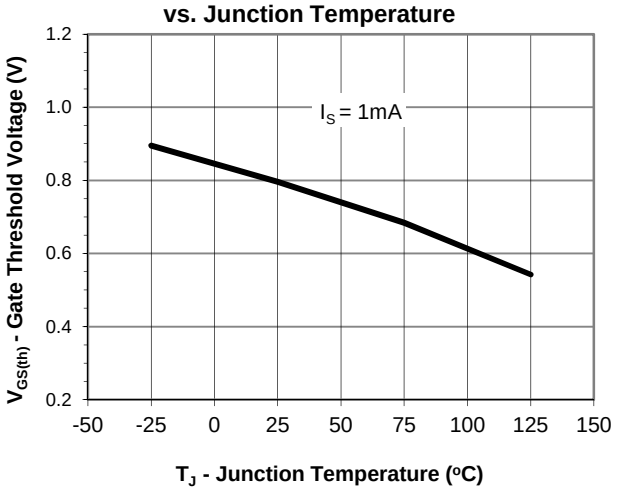
Source-Source On-State Resistance vs. Gate-to-Source Voltage



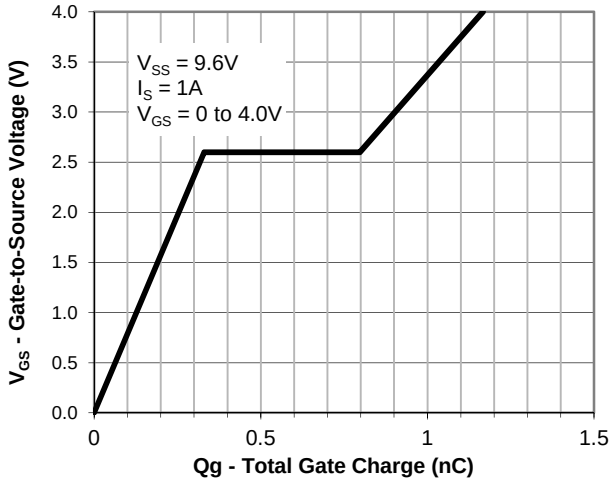
Source-Source On State Resistance vs. Junction Temperature



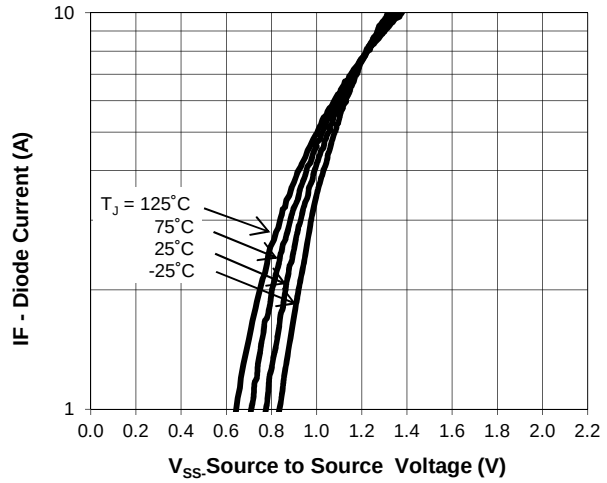
Gate Threshold Voltage vs. Junction Temperature



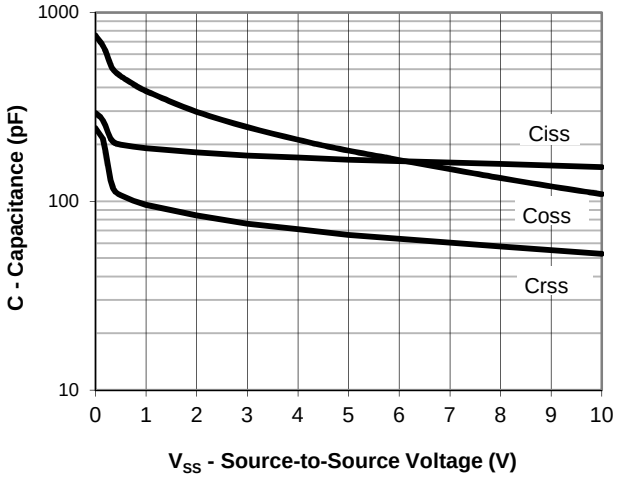
Gate Charge



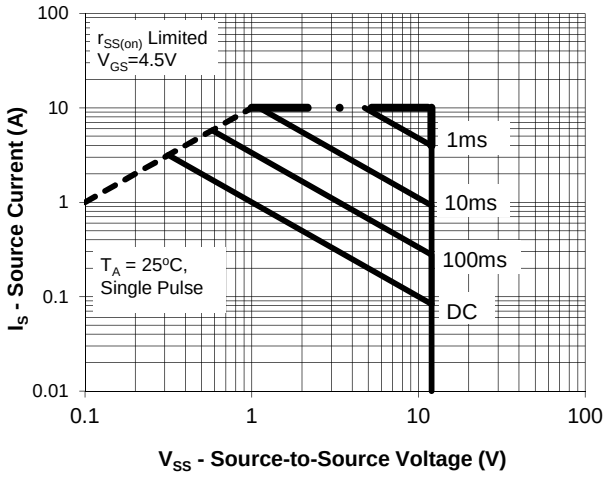
Source-Source Diode Forward Voltage



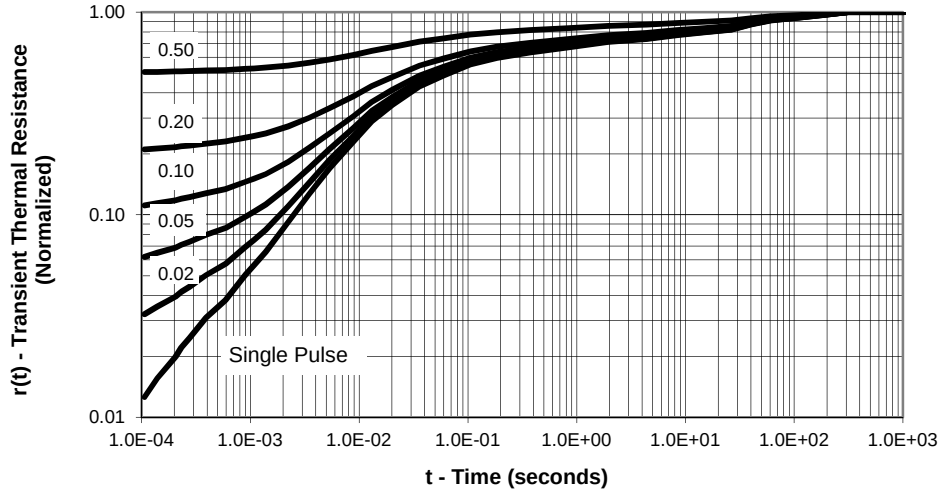
Capacitance



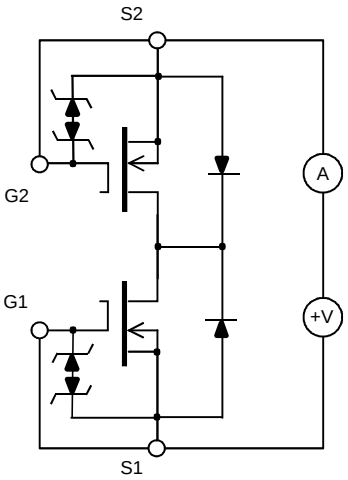
Maximum Rated Forward Biased Safe Operating Area



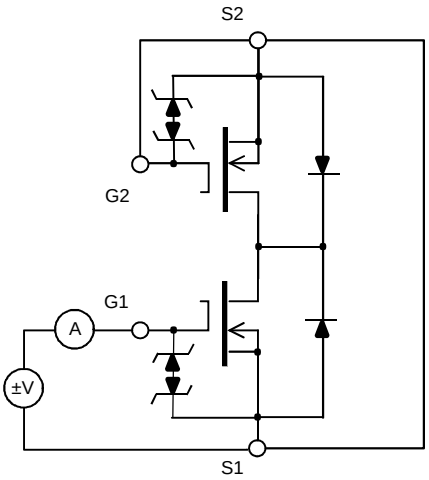
Transient Thermal Response, Junction-to-Ambient



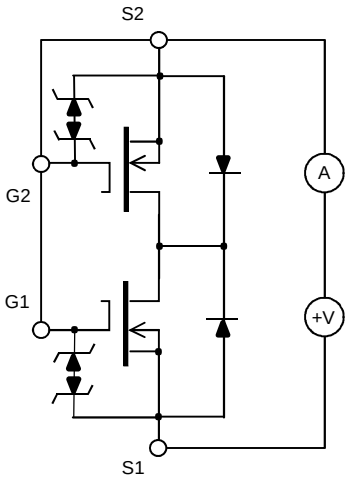
Test Circuit Examples for Measuring FET1 Key Parameters



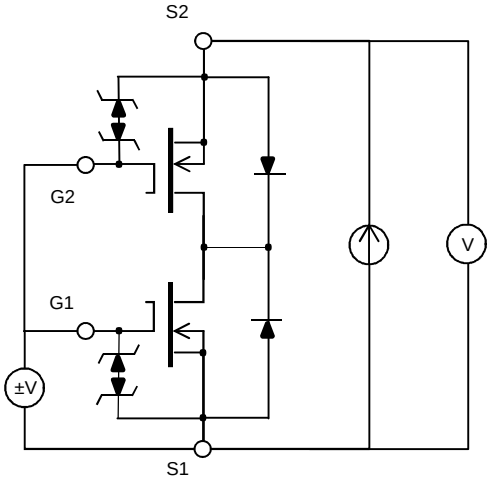
Test Circuit 1: I_{SSS}



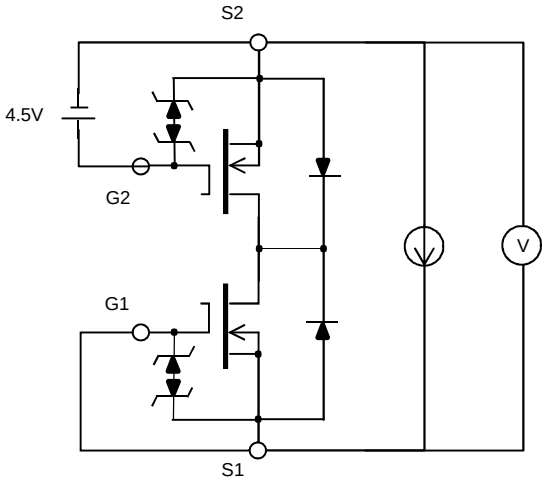
Test Circuit 2: I_{GSS}



Test Circuit 3: $V_{GS(th)}$

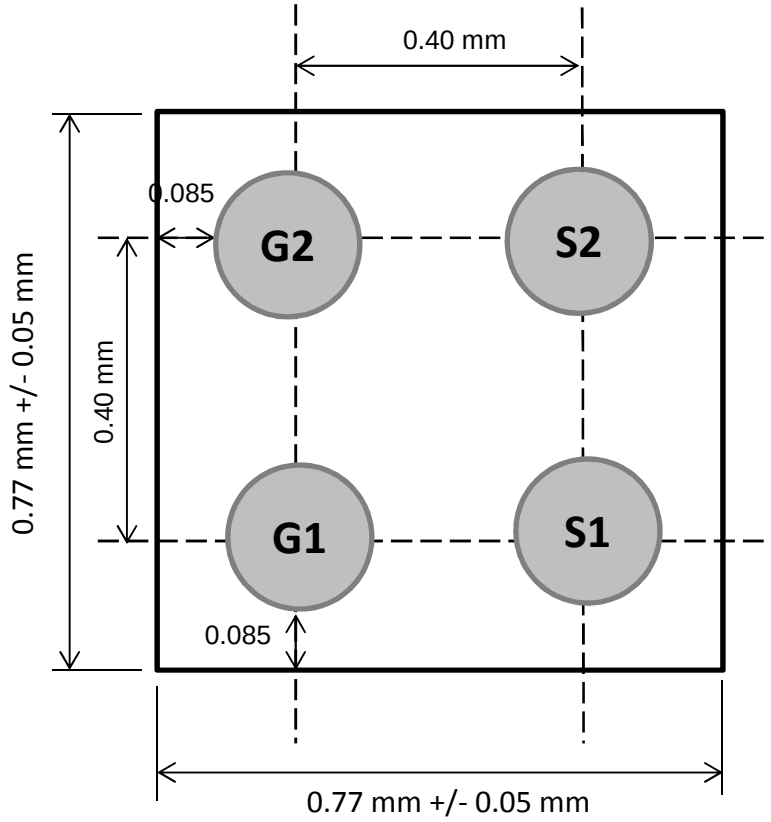


Test Circuit 4: $r_{SS(on)}$



Test Circuit 5: V_{FS-S}

Dimensional Outline and Pad Layout

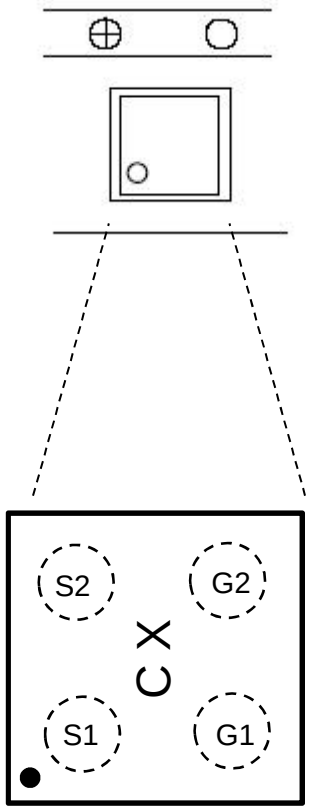


BOTTOM VIEW

Die Thickness = 0.20 mm ±0.015 mm
Gate Pads = 0.20 mm dia
Source Pad = 0.20 mm dia
Pad Pitch = 0.40 mm

Dimensions in mm

Tape and Reel Orientation



TOP VIEW

Backside Marking

C = GWS2111 Product Code

X = Date /Lot Traceability Code

● = Dot indicates location over S1 ball