GWS7301E – Dual 20V N-Channel Power MOSFET

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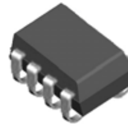
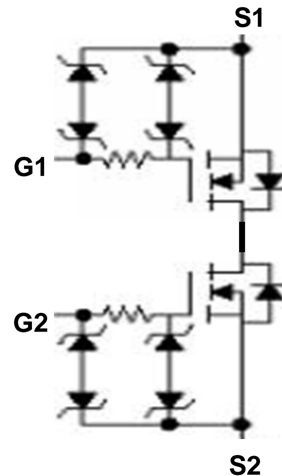
General Description

The GWS7301E is a dual low threshold gate protected MOFET designed for the small battery, cell phone, and PDA markets. Using ultra high density MOSFET process and space saving small outline J-lead package, performance normally found in a TSSOP8 footprint has been squeezed into the footprint of a TSOP6 package.

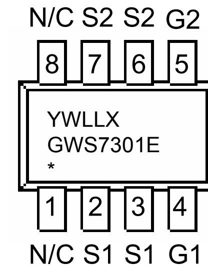




Features

- 6.5A, 20V $r_{DS(ON)}$ = 18mΩ typ. at 4.5 Volts
- 5.5A, 20V $r_{DS(ON)}$ = 25mΩ typ. at 2.5 Volts
- Excellent thermal characteristics.
- Rated for High Electrical Overstress Performance of 15A short circuit and over current.
- Integrated gate diodes provide Electro-Static Discharge (ESD) protection of 2500V HBM.

TSOPJW-8 Package



Maximum Ratings and Thermal Characteristics (T_A=25°C unless otherwise noted)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		V
Gate-Source Voltage		V_{GS}	± 12		
Drain Current[a]	T_A=25°C	I_D	5.7	4.6	A
	T_A=70°C		4.6	3.5	
Pulsed Drain Current		I_{DM}	30		
Maximum Power Dissipation[a]	T_A=25°C	P_D	1.3	0.83	W
	T_A=70°C		0.83	0.53	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

Thermal Resistance Ratings					
Parameter		Symbol	Typ	Max	Unit
Junction-to-Ambient	t ≤10 sec	R_{thJA}	81	96	°C/W
	Steady Sate		135	150	
Junction-to-Foot (Lead)	Steady Sate	R_{thJF}	70	85	

[a] Surface Mounted on FR4 Board.

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Electrical Characteristics (T_J = 25 °C unless otherwise noted)

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0V, V_{DS} = 20V			1	uA
Gate Body Leakage	I_{GSS}	V_{DS} = 0V V_{GS} = +/-12V			+/-10	uA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	0.5	0.6	1.5	V
Drain-Source On-State Resistance	$r_{DS(on)}$	V_{GS} = 4.5V, I_D = 6.5A	11	18	25	mΩ
		V_{GS} = 2.5V, I_D = 5.5A	15	25	35	
Source-Drain Diode Voltage	V_{SD}	V_{GS} = 0, I_D = 6.5A	0.8	1.0	1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 4.0A, V_{GS} = 5.0V		12		nC
Input Capacitance	C_{iss}	V_{DS} = 20V, V_{GS} = 0V, f = 1 MH_Z		870		pF
Output Capacitance	C_{oss}			320		
Reverse Transfer Capacitance	C_{rss}			240		

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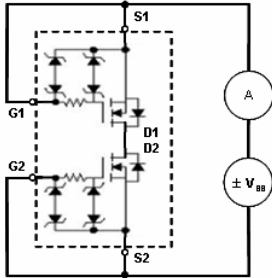
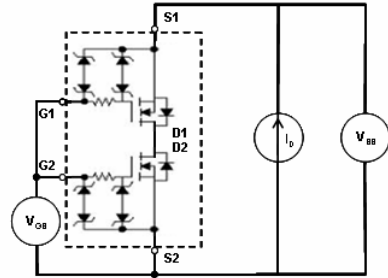
Test Circuit 1: I_{DSS}, Zero Gate Voltage Drain Current



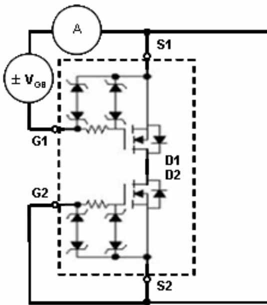
FET (1) I_{DSS}: VS2=VG2=20V, VS1=VG1=0V
FET (2) I_{DSS}: VS1=VG1=20V, VS2=VG2=0V

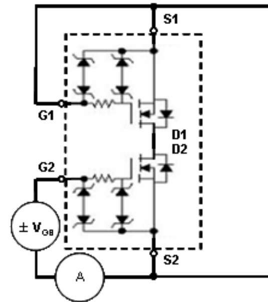
Test Circuit 2: $R_{DS(ON)}$, Drain-to-Source ON State Resistance



FET (1 or 2) $R_{DS(ON)} = (V_{SS} / I_D) / 2$

Test Circuit 3: I_{GSS}, Gate Body Leakage

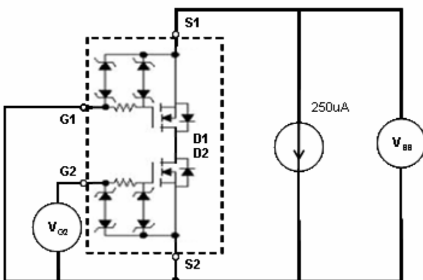


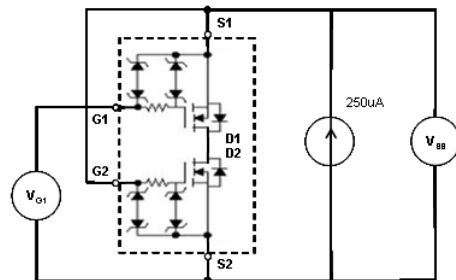


FET (1) I_{GSS}: V_{GS1}= ± 12V, V_{S1}=V_{S2}=V_{G2}=0V

FET (2) I_{GSS}: V_{GS2}= ± 12V, V_{S1}=V_{S2}=V_{G1}=0V

Test Circuit 4: $V_{GS(th)}$, Gate Body Leakage





FET (1) $V_{GS(th)1}$ **= Vss**
Where: V_{G1}=V_{S2}, V_{S1}=0V, V_{G2}=4.5V, I_{Ss}=250uA

FET (2) $V_{GS(th)2}$ **=** V_{SS}
Where: V_{G2}=V_{S2}, V_{S2}=0V, V_{G1}=4.5V, I_{SS}=250uA

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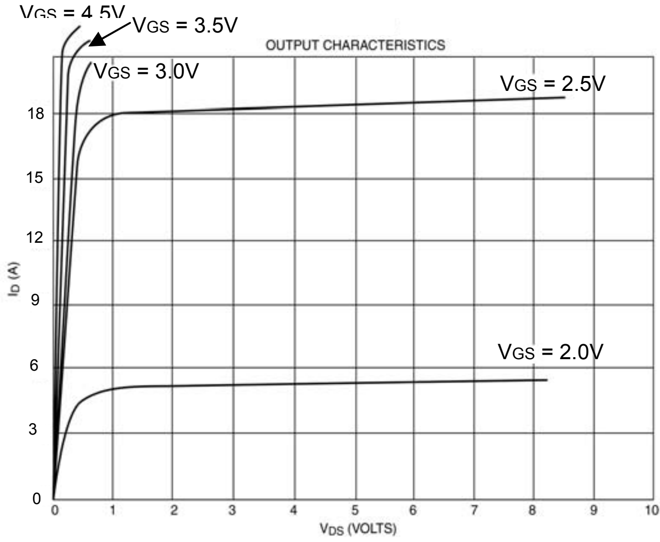

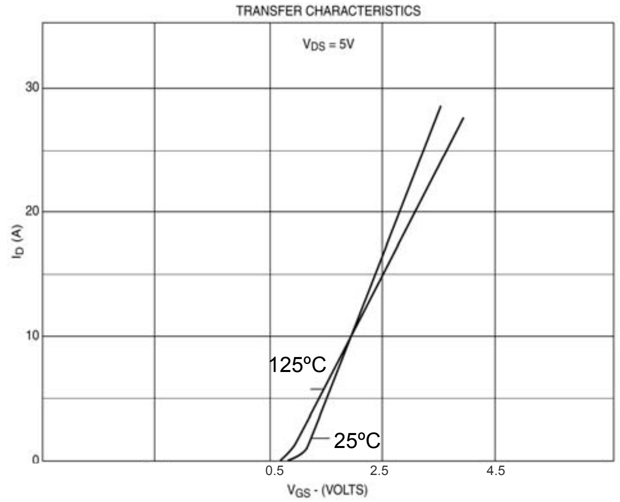

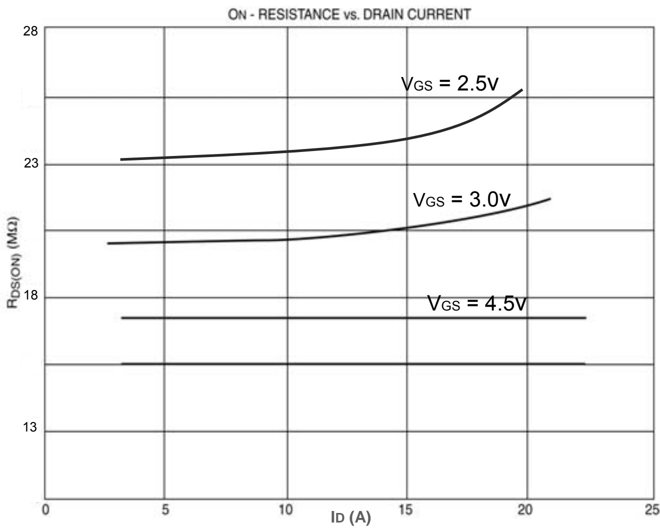

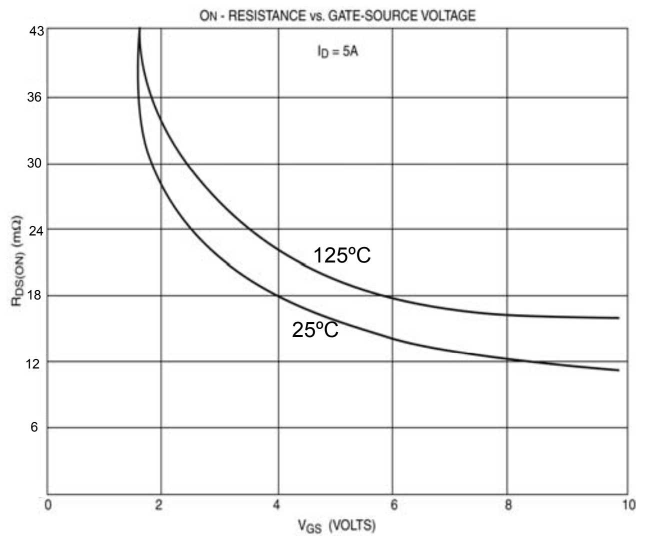

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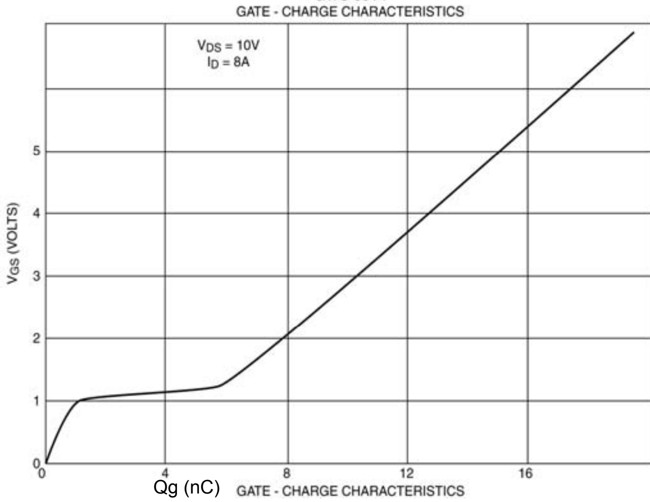

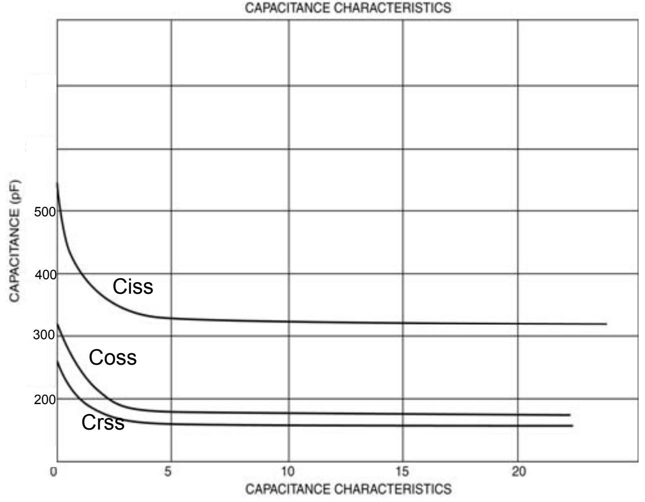

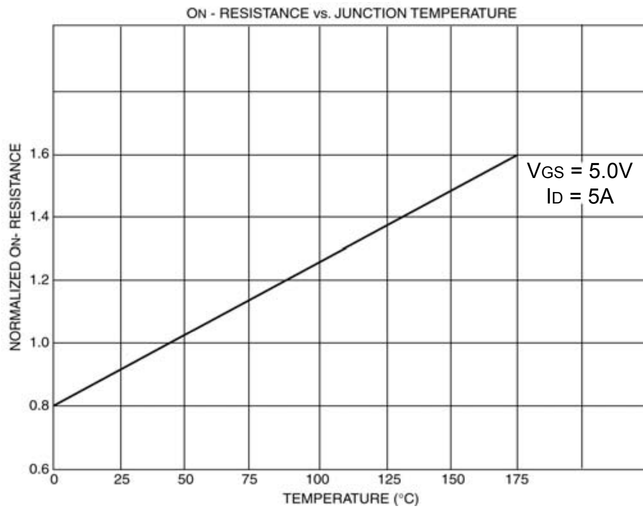

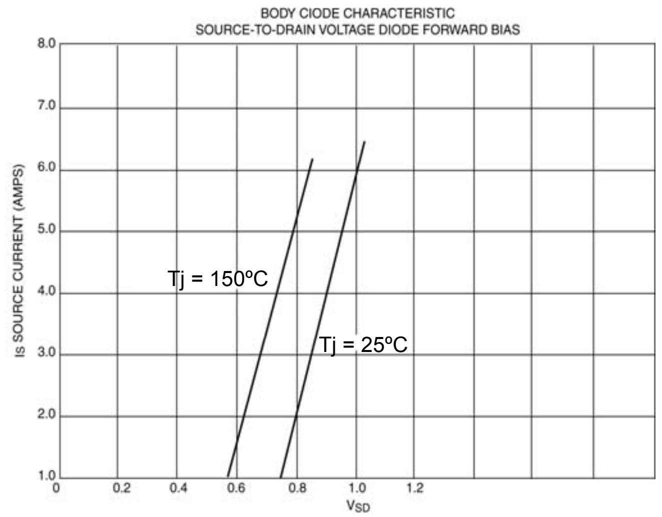

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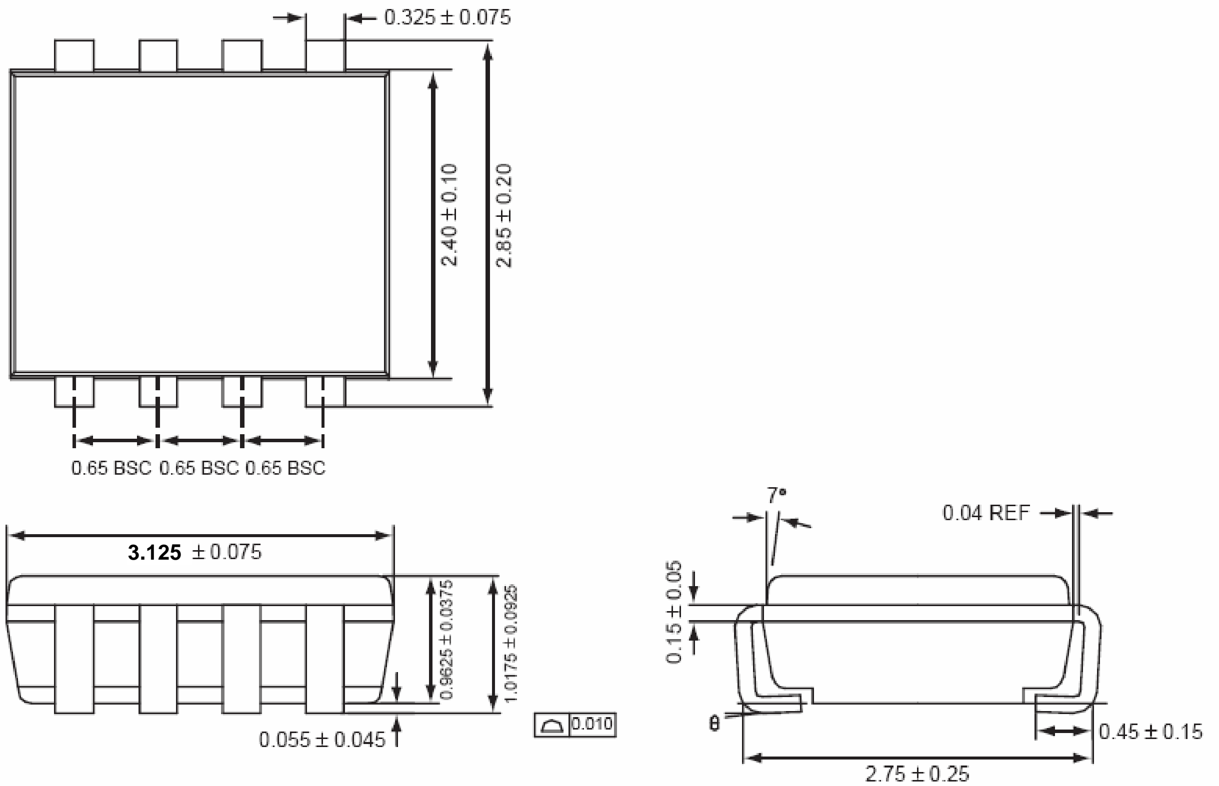
Ordering Information

Package	Marking	Part Number	
		Bulk	Tape and Reel
TSOPJW-8		N/A	GWS7301EITS-T1

Package Information



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