GX2431 1024-Bit 1-Wire EEPROM

Features

- Only one port is required for communication using 1-Wire interface
- Each device equipped with a global unique 64-bit serial number
- 1024 bits of EEPROM memory partitioned into four pages of 256 bits
- Individual memory pages can be permanently write protected or put in EPROM-emulation mode (write to 0)
- No external components required
- Powered by the data line with a range is 2.5V~5.5V
- Reads and writes over a wide voltage range from -55°C to +125°C
- ESD protection: HBM8000V MM800V
- Communicates to host with a single digital signal at 15.4kbps or 125kbps

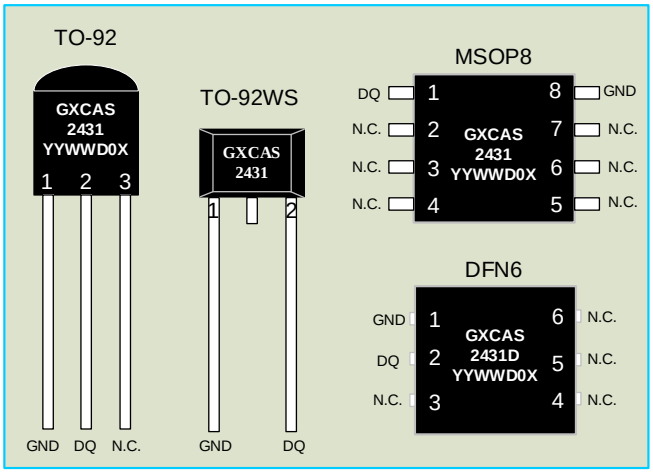
Applications

- Host accessory/PCB identification
- Medical sensor calibration data storage
- Analog sensor calibration
- Ink and toner print cartridge identification
- After-market management of consumables
- BMS product data storage

Description

The GX2431 is an EEPROM chip, which support 1 wire communication. The chip has a 64 bit ROM, which has a family code of 2D. The size of the EEPROM is 1024 bit, which contains 4 pages of 256 bit each. The EEPROM can be set to locked or EPROM mode separately.

Common Package Diagram



Package information

DEVICE	PACKAGE	SIZE（ mm³）
GX2431	TO92	4.6*4.6*3.6
GX2431WS	TO92S-2	4.0*3.15*1.52
GX2431D	DFN6	4.0*4.0*0.75
GX2431T	DFN6	4.0*4.0*0.75
GX2431P	MSOP8	3.0*3.0*1.0
GX2431G	SFN2	6.0*6.0*0.73
GX2431GA	SFN2	3.5*6.5*0.73
GX2431Q	QFN16	1.8*2.6*0.55
GX2431S	SFN2	5.0*3.5*0.4
GX2431DVS	DFN6	4.0*4.0*0.75
GX2431TVS	DFN6	4.0*4.0*0.75

Pin Description

PIN			NAME	DESCRIPTION
MOSP8	TO-92(WS)	DFN6		
2,3,4,5,6,7	-	3,4,5,6	N.C.	Empty pin or no connection required
-	3	-	N.C.	Grounded or floating
1	2	2	DQ	Data input and output pins, drain pins, external pull-up resistors required
8	1	1	GND	Ground

Revision History

DATE	REASON	PAGES
01/01/2017	first release	all
07/12/2017	Change the drive circuit	6
03/03/2018	Change the power voltage	1
10/06/2018	Change the inch of package	27
18/09/2018	Add the package of SP2 and change the inch of package	26 27
15/05/2019	Add the package of UT_QFN	27
10/09/2021	Add the list of package	1
01/09/2021	Add the package of SFN	27
07/25/2022	Change package	27
03/20/2023	Add ordering, Change Package	27, 24
05/09/2024	Updated the package and ordering information	26-31

Table of Contents

1 Description

The GX2431 is a 1-Wire chip which contains 1024 bits of EEPROM, and also 8 byte registers to control the mode of each page. The GX2431 has a unique 64-bit ROM address code written into the chip at the factory. The GX2431 uses the scratchpad for write and read the data, and the data is copied from the scratchpad into the EEPROM.

The GX2431 uses 1-Wire protocol and communicates through a 1-Wire port. When all devices are connected to the bus via a tri-state port or open-drain port, the control line needs to be connected to a weak pull-up resistor. In this bus system, the microprocessor (master device) relies on each device's unique 64-bit serial number to identify the devices on the bus and record the device address on the bus. Since each device has a unique serial number, the number of devices that can be connected to the bus is virtually unlimited. The 1-Wire protocol, including a detailed explanation of the commands and "timing" see the **1-Wire System** section.

The GX2431 operates without an external power supply. When the bus is in a high state, DQ is connected to a pull-up resistor to power the device through 1-Wire. At the same time, the bus signal in the high-level state charges the internal capacitor. When the bus is in the low-level state, the capacitor provides energy to the device. The way of providing energy is called "parasitic power supply".

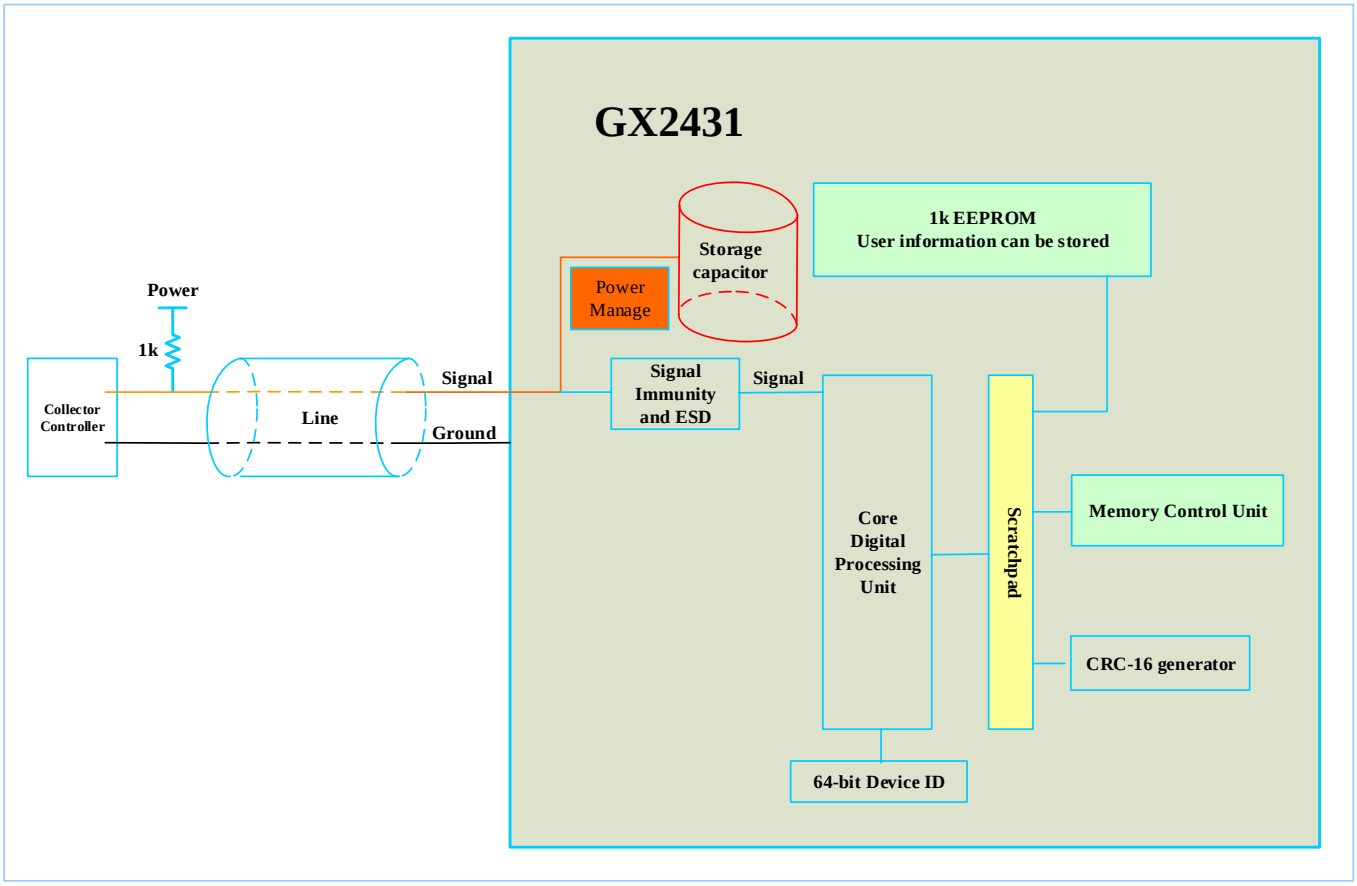


Figure 1. The GX2431 Block Diagram

The GX2431 block diagram is shown as in Figure 1. The chip contains a Power management block and a Storage capacitor to support parasitic powering. A 1k EEPROM is integrated together with the 1 wire interface. And the EEPROM is separated into 4 pages which help the user to control each page individually. Each page can be set to write protected or EPROM mode using the register. In order to improve the communication quality, the chip also incorporates a signal filter at the interface and improves the ESD level. A CRC-16 is integrated inside the chip to verify the read/write communication.

2 Power Supply

The GX2431 works in parasitic power mode. Parasitic power modes are useful in long-distance testing or space-constrained applications. The control loop for parasitic power is shown in Figure 2. When the bus is high, the control loop "steals" energy from the bus. Part of the "stealed" energy is stored in the parasitic power storage capacitor, which is released for use by the device when the bus is low.

In parasitic power mode, the 1-Wire and storage capacitor can supply enough current to the GX2431 to meet the specified timing and voltage (see the **DC and AC Characteristics** sections) in most operations. However, when the GX2431 is performing data transfer from the register to the EEPROM, the operating current can reach 0.5mA. This current may cause an unacceptable voltage drop across weak pull-up resistors connected to a 1-Wire, requiring more current than the storage capacitor can provide. To ensure that the GX2431 has enough power supply, when copying data to EEPROM, a strong pull-up must be provided for the single bus, which is realized by directly pulling the bus to the power supply by MOSFET. During the copy data timing (twr=9ms), it must always remain in a strong pull-up state. When the strong pull-up state is maintained, no other actions are allowed. In addition to this, the size of the pull-up resistor can also be limited within a predetermined range.

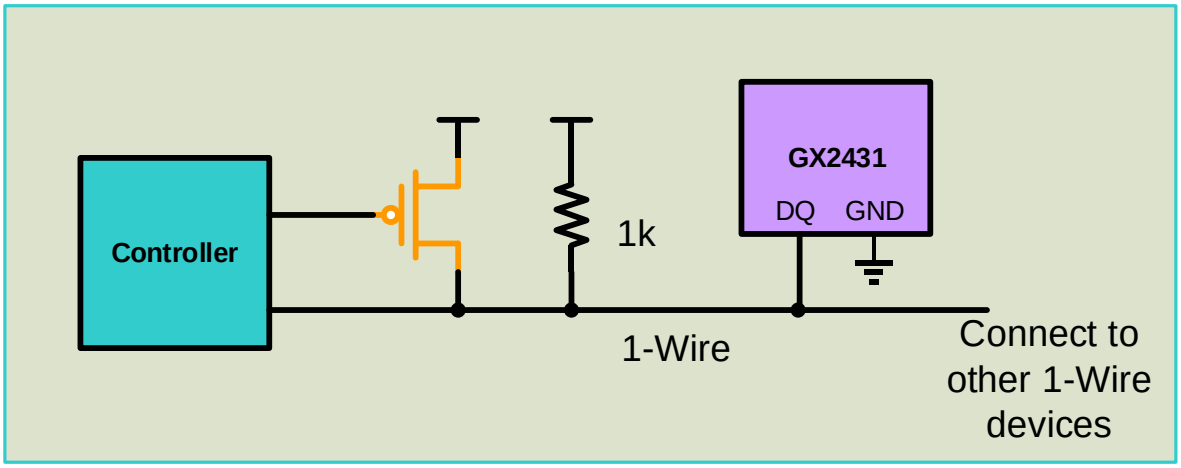


Figure 2. Parasitic Mode Replicated Data Circuit

3 64-Bit Lasered ROM

Each GX2431 has a globally unique 64 ROM, as shown in Figure 3. The first 8 bits are the family code: 2Dh. The next 48 bits are a unique serial number. The last 8 bits are the CRC encoding of the above 56 bits. See the **CRC Generator** section for a detailed explanation of CRC. 64-bit ROM and ROM operation allow the GX2431 to operate as a 1-Wire device and according to the 1-Wire protocol detailed in the **1-Wire System** section.

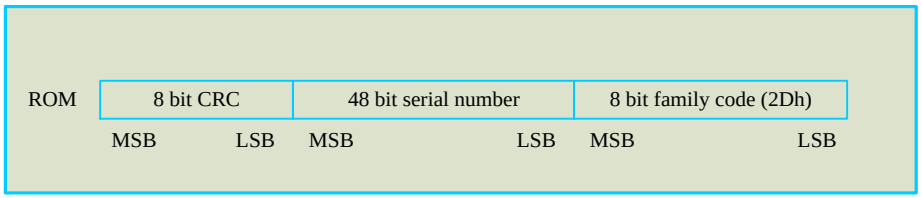


Figure 3. 64-Bit ROM

4 Memory

As shown in Table 1, are the data memory and registers structure. The GX2431 has 18 rows EEPROM, each row is 8 bytes, which are separated into 4 memory pages with 32 bytes each. By setting the corresponding protection byte register, each page can be individually set to normal, write-protected, or EPROM mode. The last two rows include protection registers and reserved bytes. The register line includes 4 protection control bytes, 1 copy protection byte, 1 factory preset byte, and 2 user/vendor ID bytes. The vendor ID can be programmable. The last row is useless.

The GX2431 also has a volatile scratchpad with 8-byte length. Writing data to the EEPROM array will use this scratchpad. The user should first write data to the scratchpad and using read scratchpad to verify the data, then copying it to the main memory array. User should write 8 bytes each time for data integrity. Or the data copied into the EERPOM without write maybe unknown.

If the page protection control register is set to 55h, then the data loaded into the scratchpad is the data in the EEPROM.

If the page protection control register is set to AAh, then the data loaded into the scratchpad is the logical and of the input data and the data in the EEPROM.

Otherwise, the data loaded into the scratchpad is the input data.

If user don’t want to copy the EEPROM, then the copy protection byte can be used. After programmed to 55/AAh, no copy will be allowed.

Once the protection byte is programmed to 55/AAh, then the protection byte itself is write protected.

Table 1. Memory Map

ADDRESS RANGE	TYPE	DESCRIPTION	PROTECTION CODES
0000h to 001Fh	R/(W)	Page 0	—
0020h to 003Fh	R/(W)	Page 1	—
0040h to 005Fh	R/(W)	Page 2	—
0060h to 007Fh	R/(W)	Page 3	—
0080h*	R/(W)	Protection Control Byte of Page 0	55h: Page 0 Write Protected; AAh: Page 0 EPROM Mode; 55h or AAh: 80h Write Protected
0081h*	R/(W)	Protection Control Byte of Page 1	55h: Page 1 Write Protected; AAh: Page 1 EPROM Mode; 55h or AAh: 81h Write Protected
0082h*	R/(W)	Protection Control Byte of Page 2	55h: Page 2 Write Protected; AAh: Page 2 EPROM Mode; 55h or AAh: 82h Write Protected
0083h*	R/(W)	Protection Control Byte of Page 3	55h: Page 3 Write Protected; AAh: Page 3 EPROM Mode; 55h or AAh: 83h Write Protected
0084h*	R/(W)	Copy Protection Byte	55h or AAh: Copy Protected 0080h:008Fh, and Any Write-Protected Pages
0085h	R	Factory Byte.	AAh: 85h, 86h, 87h Write Protected; 55h: 85h Write Protected;
0086h	R/(W)	User Byte ID	—
0087h*	R/(W)	User Byte ID	—
0088h to 008Fh	—	Reserved	—

*Note: Once programmed to 55 or AA, this address is read only. When programmed to other code, this address is not write protected, and have no function.

4.1 Address Registers and Transfer Status

The GX2431 uses 3 address registers: TA1, TA2, and E/S (see Figure 4) to access memory. TA1 and TA2 must are the target memory address where data is written or read. E/S is a read-only transfer status register contains flags. The E2:E0 bits of the ES load the T2:T0 bits input by the Write Scratchpad command, and increment by 1 byte for each input data byte. The fifth bit of the E/S register, which is called PF, means partial flag. If the data may encounter a loss due to voltage low or other situation, then this flag is set. The master must send the full 8 bytes of data. Bits 3, 4, and 6 is always 0. The highest bit of the E/S register, which is called AA, is grant flag. A successful write copy will clear this bit.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Target address TA1	T7	T6	T5	T4	T3	T2	T1	T0
Target address TA2	T15	T14	T13	T12	T11	T10	T9	T8
Communication status E/S	AA	0	PF	0	0	E2	E1	E0

Figure 4. The GX2431 Address Registers

4.2 Write Read and Copy

When writing data to the memory of GX2431, the scratchpad is used as an intermediate memory. First, the host sends the Write Scratchpad command and specifies the target memory address, and then sends the data to be written into the register, then the host will receive an inverse CRC16 checksum to verify the command, the address (the address actually sent) and the data until the end of the Write Scratchpad command sequence. After receiving the CRC check code, the host compares with its own calculation result to check if the communication is successful. Second, the host shall send a Read Scratchpad command to verify the data, after the command, the host will receive the target address TA1 and TA2, and the E/S register value first(these three register is used for the following Copy command), then the data. If there is anything wrong during the sequence, then the PF flag bit is set. The host should rewrite data to the registers. If the AA flag is set, the device reject the write command. If both flags are cleared. The host can send the Copy Scratchpad command. After the command, the host should send address registers, TA1, TA2 and E/S.

5 CRC Generator

5.1 CRC-8

The CRC8 is stored in memory as part of the 64-bit ROM. The CRC8 code is calculated from the first 56 bits of the ROM and is included in the important bytes of the ROM. The CRC is calculated from the data stored in the memory, so when the data in the memory changes, the value of CRC8 also changes.

CRC8 can perform data verification when the bus controller reads the GX2431. In order to verify that the data is read correctly, the bus controller must use the received data to calculate a CRC8 value and the value stored in the 64-bit ROM of the GX2431 (when reading the ROM) or the 8-bit CRC8 value calculated inside the GX2431 (when reading register 1) to compare. If the calculated CRC8 value matches the read CRC8 value, the data is transmitted error-free. The comparison of the CRC8 value and whether to proceed to the next step is entirely at the discretion of the bus controller. The calculation formula of CRC8 is as follows:

$$CRC8 = X^8 + X^5 + X^4 + 1$$

The 1-Wire CRC8 can be generated by a polynomial generator consisting of a shift register and XOR gate, as shown in Figure 5. This loop consists of a shift register and several XOR gates, each bit of the shift register is initialized to 0. Starting with the least significant bit in ROM or byte 0 of the register, the registers are shifted one at a time. The CRC8 value is stored in the shift register after the data in the 56-bit ROM has been transferred or the MSB of the 7th byte of the register has been shifted. Next, the value of CRC8 must be cyclically shifted in. At this point, if the calculated CRC8 is correct, the shift register will be reset to 0.

5.2 CRC-16

The CRC16 check code is used to quickly check the data transmitted when reading and writing the register. Unlike the 8-bit CRC8 check code, the 16-bit CRC16 check code is always transmitted in the form of the inverse code. By comparing the CRC16 check code read by the slave with the CRC16 check code calculated by the received data, the host decides whether to continue an operation or re-read the data part with an incorrect CRC16 code, as shown in Figure 5. The calculation formula of CRC16 is as follows:

$$CRC16 = X^{16} + X^{15} + X^2 + 1$$

In the Write Scratchpad command, the CRC16 generator is first cleared, then the command code, target addresses TA1 and TA2, and all data bytes sent by the host are shifted in. GX2431 only sends CRC check code when E2:E0 = 111b.

In the Read Scratchpad command, first clear the CRC16 generator, then shift in the command code, target addresses TA1 and TA2, E/S bytes, and register data sent by the GX2431. The GX2431 sends the CRC16 check code only when the register data is continuously read until the end.

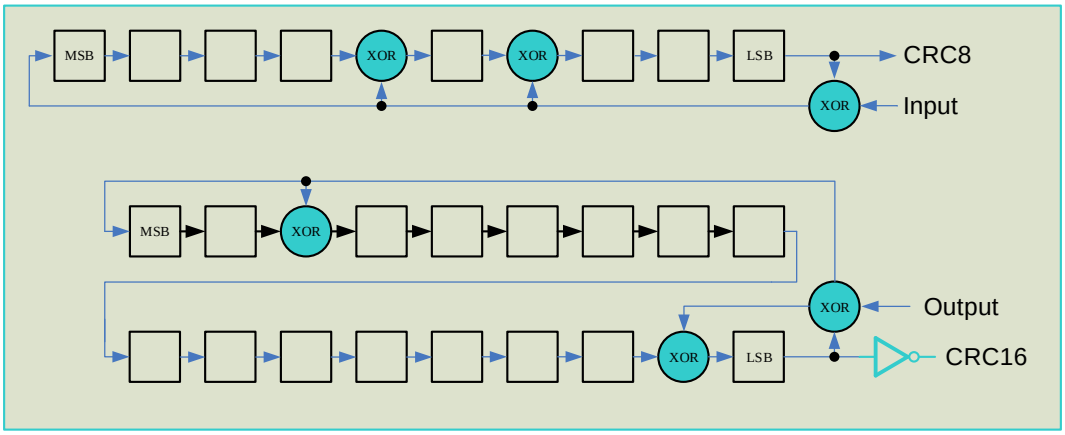


Figure 5. CRC Generator

6 1-Wire Bus System

1-Wire system is a system targeting less wiring or long distance communication. The system has one controller and many slave devices. The GX2431 is a slave device which only reacting with the controller and don't start a communication by itself. The system is referred as a "single-point" system when only one slave is attached to the bus; the system is referred as a "multi-point" system if there are multiple slaves attached to the bus.

All data and instruction transfers are carried over a single bus starting with the least significant bit. The discussion on the 1-Wire system is divided into three aspects: hardware structure, execution sequence and 1-Wire signal (signal type and timing). Finally, a single bus communication example is added.

6.1 Hardware Configuration

A 1-Wire system has only a signal line and a ground line (which a vdd line as optional), and the device (master or slave) on each bus must be an open-drain or tri-state output. Such a mechanism would allow every device on the bus that is not transmitting data to release the bus for use by other devices. The 1-Wire port (DQ pin) of GX2431 is open-drain type, and the internal equivalent circuit is shown in Figure 6.

The 1-Wire requires an external 1KΩ pull-up resistor; the 1-Wire idle state is high. After suspending a transfer due to some need, the bus must remain idle if the transfer is to be resumed. During recovery, if the 1-Wire is inactive (high), the bit-to-bit recovery time can be infinite. All devices on the bus will be reset if the bus stays low for over 480us.

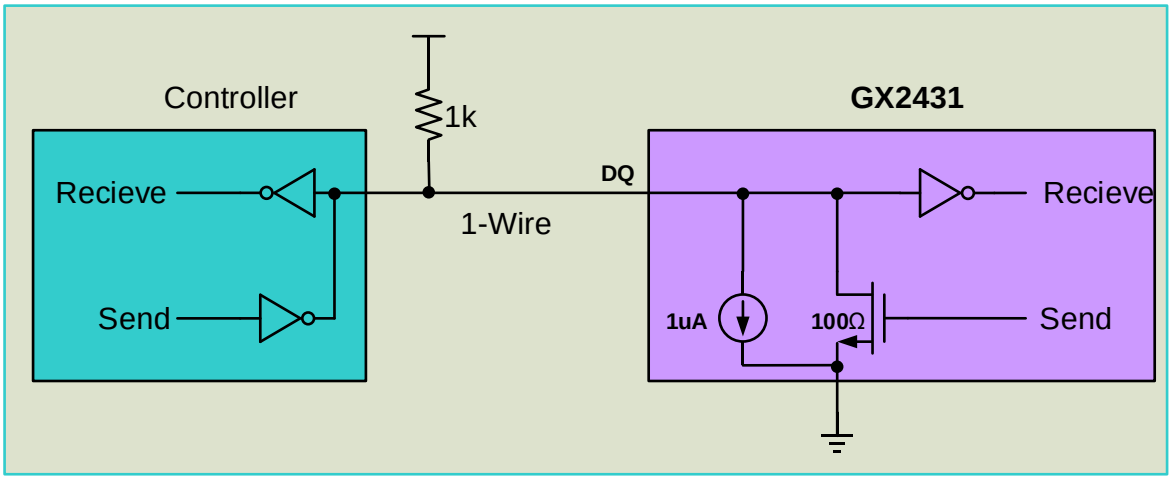


Figure 6. Hardware Configuration

6.2 Transaction Sequence

The protocol for accessing the GX2431 through the 1-Wire port is as follows:

Step1: Initialization

Step2: ROM Function Command

Step3: Memory Function Command

Each operation of the GX2431 must meet the above steps. If the steps are missing or the sequence is disordered, the device will not have a return value.

1) Initialization

A 1-Wire operation start from initialization, which begins with the master sending a reset pulse. When GX2431 receives the reset pulse, it will send a present pulse which tells the master that the GX2431 is ready to receive commands.

2) ROM Commands

Once the bus controller detects a presence pulse, it issues a ROM command, see Table 2. If there are multiple GX2431s on the bus, these instructions operate based on the unique 64-bit ROM serial code of the device, so that the bus controller selects the specific device to be operated. These commands can also make the bus controller identify how many and what type of devices are on the bus. There are 7 ROM instructions, all of which are 8 bits. The bus controller issues a ROM instruction before initiating a GX2431 function instruction. The ROM instruction operation diagram is shown in Figure 7.

Table 2. ROM Commands

ROM COMMAND	SEND COMMAND	FUNCTION	RETURN VALUE
Read ROM	0x33	(Single chip only)	64-bit ROM
Match ROM	0x55		None
Skip ROM	0xCC		None
Search ROM	0xF0	(Search for chips on bus)	
Continue ROM	0xA5		
(Accelerated) Skip ROM	0x3C		
(Accelerated) Match ROM	0x69		

Read ROM [33h]

This Read ROM command can only be used if there is a single slave on the bus, for if there are many slave on the bus, then the rom readed is a logical and of all the slave which results a wrong ROM. This controller can use this command to easily read the 64-bit serial code of the slave.

Match ROM [55h]

The Match ROM command is used to match a specific slave and then communicated with it. The master needs to send a 64-bit ROM after the Match ROM command for the slave to match. This command is mainly using for a multidrop situation, and can be used in single drop situation too.

Skip ROM [CCh]

The Skip ROM command is used mainly for single drop situation. When there is only one slave on the bus, the master can use this command to save time, which don’t need to send the 64 ROM bit. For multi drop situation, this command is not suggested to be used, for many slave may be operated in the same time.

Search ROM [F0h]

The Search ROM command is used for multi drop situation. When there are many slave on a bus, the search ROM command can be used, which will search the entire binary tree for all the slave on the bus, which search from the root bit to the least leaf bit.

Resume [A5h]

The resume ROM command is used for a high data transfer situation. When the master needs to communicate

with one specific slave for a long time, for example, the master needs to program all the pages of the salve, traditionally the master may need to send Match ROM command and 64 bit rom and function command, thanks to the Resume ROM command, the master only needs to send Resume ROM command (without the 64 bit ROM) and the function command, which saves a lot of time.

Overdrive-Skip ROM [3Ch]

The OverDrive Skip ROM command help the master to save time by sending the salve into OverDrive mode which speeds up the clock inside the chip. After this command, all the slave on the bus enter into OverDrive mode, and all the subsequent command need to follow the OverDriver protocol. A reset pulse of more than 480us will send all the slave back into normal mode.

Overdrive-Match ROM [69h]

The Overdrive-Match ROM command will send the slave which match the 64 bit ROM into OverDrive mode, which speeds up the clock inside the chip. This command is used for a specific slave chip. After this command, only the matched slave on the bus will enter into OverDriver mode, with all the other slave in normal speed. All the subsequent command for this chip need to follow the OverDriver protocol. A reset pulse of more than 480us will send all the slave back into normal mode.

3) Function Commands

After the bus controller uses ROM commands to identify the GX2431 it wishes to communicate with, the host can issue a GX2431 function command. These instructions allow the bus controller to read and write the registers of the GX2431 and perform memory operations. The functional instructions of GX2431 are detailed below, and are summarized in Table 3, and the flow is shown in Figure 8.

Table 3. Memory Function Commands

FUNCTION COMMAND	SEND	WRITE VALUE	RETURN VALUE	OTHER
Writ Scratchpad	0x0F	See **Operation Example** Sections 1 and 2 for details.		
Read Scratchpad	0xAA			
Copy Scratchpad	0x55			
Read Memory	0xF0			

Note 1: For GX2431 in parasitic power mode, during writing data to EEPROM, a strong pull-up must be given to the 1-Wire, and the bus cannot have other activities during this time.

Note 2: The bus controller can abort the data transfer at any time by issuing a reset signal.

Note 3: Writing to the register is done before the reset signal is asserted.

Write Scratchpad [0Fh]

The Write Scratchpad command is used for the master to send the data to slave's scratchpad which is to be copied into the EEPROM. The master must send exactly 8 bytes data to the scratchpad.

After the Write Scratchpad command, the master first send 2 bytes address TA, then 8 bytes data. The data is then written into the scratchpad. Then the master can read the CRC-16 which includes the function command, address TA, and all the data sent. For the CRC16, please refer to CRC-16 section. If the address is write protected, the data is not written into the scratchpad, while the data in the EEPROM is loaded into scratchpad. If the addresss is in EPROM mode, then a logical and of the input data and the data in EEPROM is loaded into scratchpad.

Read Scratchpad [AAh]

The Read Scratchpad command is used for the master to read back all the address TA and data, in order to verify data sent. After the command, the master first read back the TA address, then a ES status bytes which include the ending offset and data status, then the bytes in the scratchpad is read out, followed by the CRC.

Copy Scratchpad [55h]

The Copy Scratchpad command is used to program the data in the scratchpad into the EEPROM. The master first needs to write the data into scratchpad using Write Scratchpad command, then read data back to verify using the Read Scratchpad command which can obtain the ES byte, finally the master using the Copy Scratchpad command to copy the data into EEPROM. After the Copy Scratchpad command, the master needs to send the TA address and the ES byte read by the Read Scratchpad command, then wait for the slave to copy, after a while, if the program is succeed, then the master may read AA. If the target is write protected, then the copy will fail.

Read Memory [F0h]

The Read Memory command is used to read the EEPROM. This command don't need to use the scratchpad as an intermedia. The data is read out directly from the EEPROM to the interface. After the command, the master needs to send 2bytes TA address, then the master may read to EEPROM data out. If the address is target at illegal address, then FF is read out.

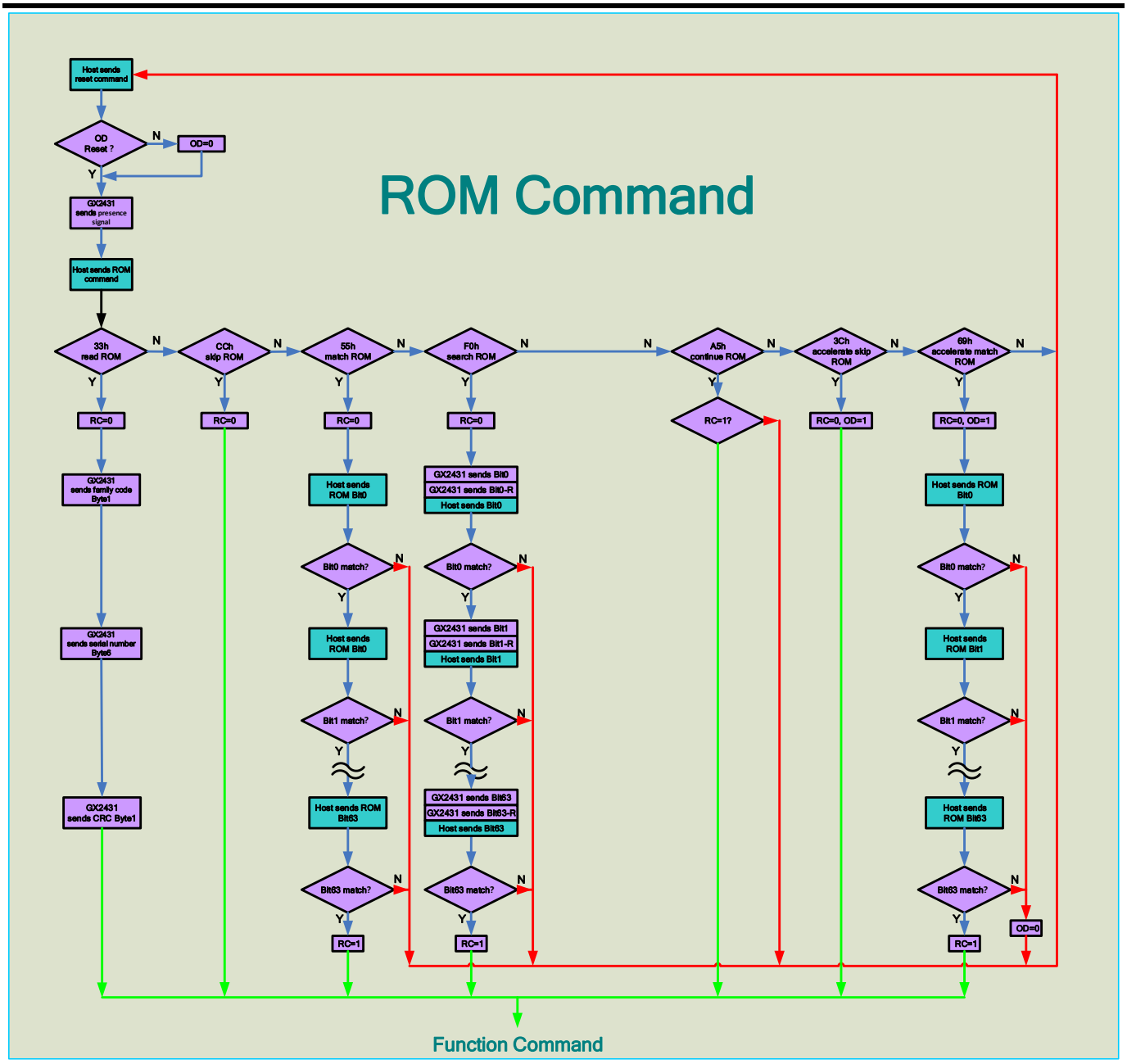


Figure 7. ROM Functions Flowchart

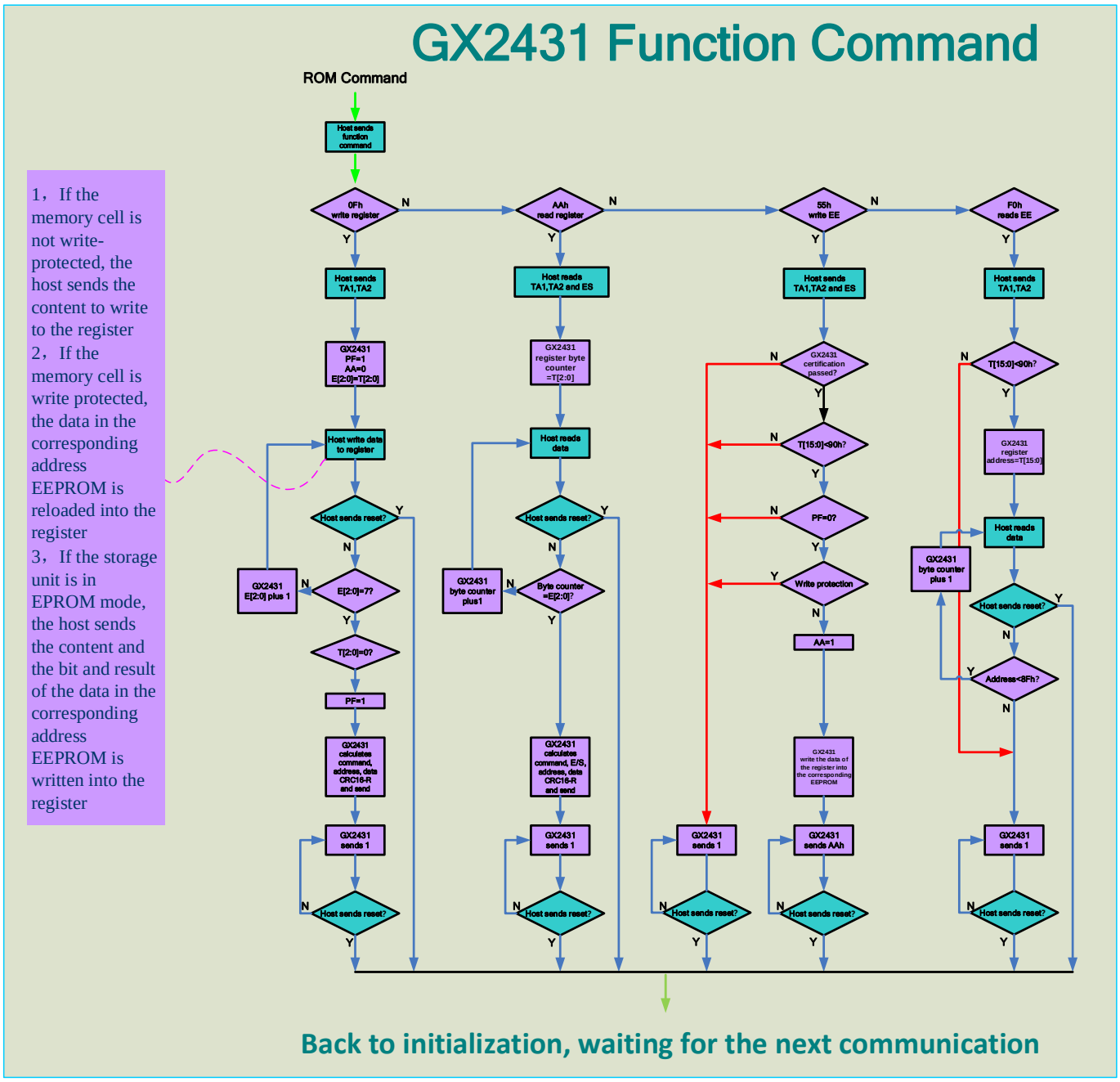


Figure 8. Function Command Flowchart

6.3 1-Wire Signaling

The GX2431 requires the user to follow the protocols to ensure data integrity. The protocol includes : reset pulse and presence pulse, write-zero, write-one, and read-data. The bus master initiates the falling edges of reset, write and read, while the slave initiates the falling edges of the present pulse.

1) Function Commands

All communications with the GX2431 begin with an initialization sequence shown in Figure 9. A reset pulse followed by a presence pulse indicates that the GX2431 is ready to transmit and receive data.

During the initialization sequence, the bus controller pulls the bus low for 480us to issue (TX) a reset pulse, then releases the bus and enters the receive state (RX). When the bus is released, a 1kΩ pull-up resistor pulls the bus high. When the GX2431 detects the rising edge on the IO pin, it waits for 15-60us, and then sends out a presence pulse consisting of a 60-240us low-level signal.

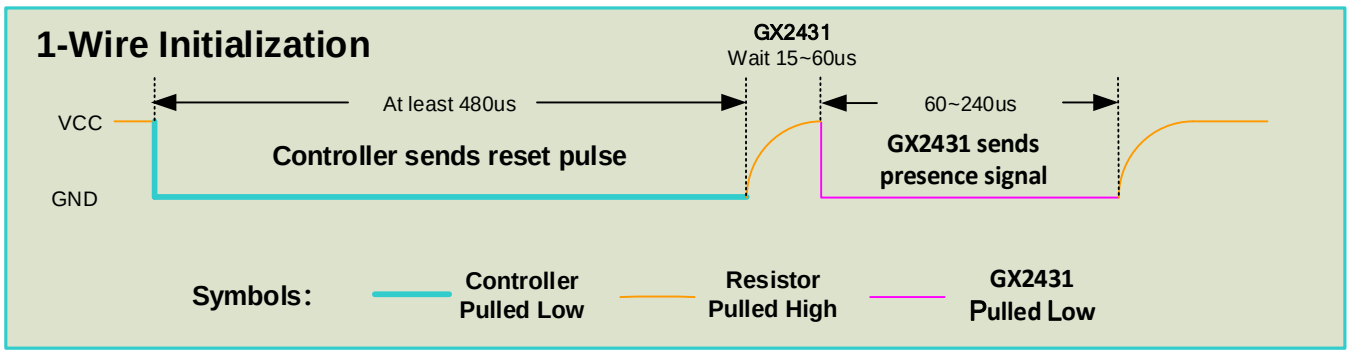


Figure 9. Initialization Timing

2) Read/Write Time Slots

Data communication with the GX2431 takes place in time slots that carry a single bit each.

Write Time Slots

The GX2431 has two write timings: write 1 and write 0. The bus controller writes logic 1 through the write 1 sequence; logic 0 is written through the write 0 sequence. The write sequence must last at least 60us, including a recovery time of at least 5us between two write cycles. The write sequence begins when the bus controller pulls the data line from logic high to low (see Figure 10).

To generate a write sequence by the bus controller, the data line must be pulled to a low level and then released, and the bus must be released within 15us. When the bus is released, the pull-up resistor pulls the bus high. To generate a write 0 sequence, the bus controller must pull the data line to a low level and continue to hold it for at least 60us.

After the bus controller initializes the write sequence, the GX2431 uses the signal lines within a 15us to 60us window. If the line is high, write 1. Conversely, if the line is low, write 0.

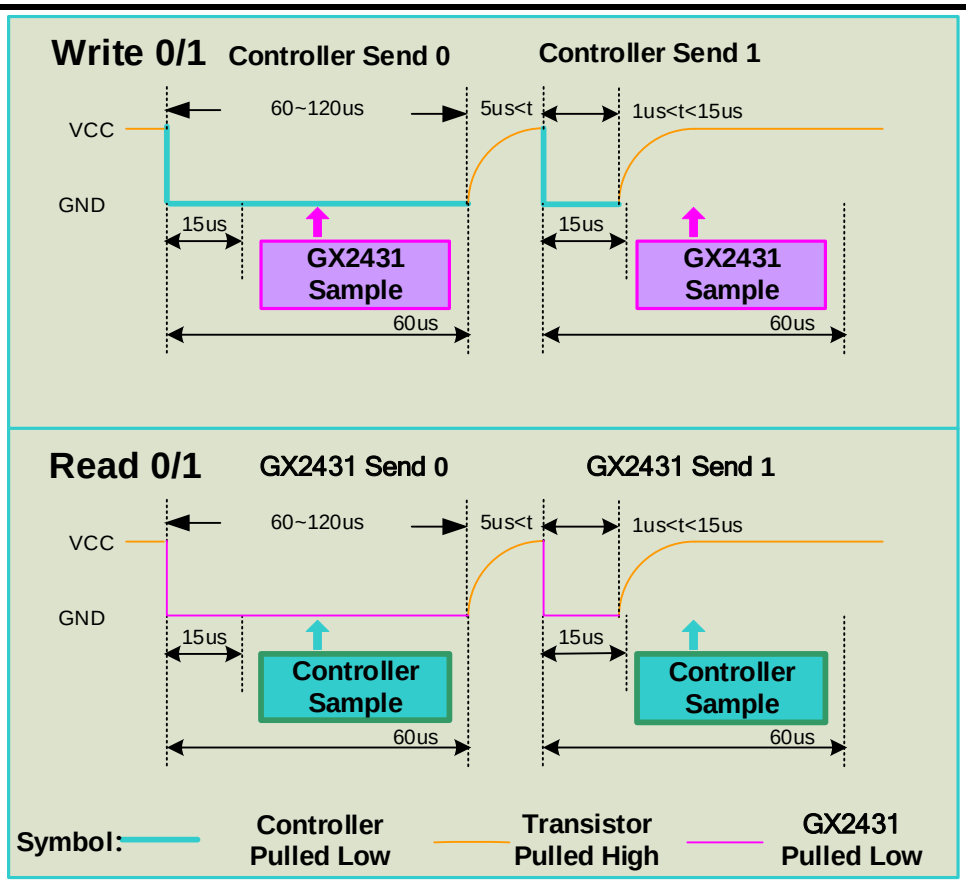


Figure 10. Read/Write Time Slot Timing Diagram

Read Time Slots

When the bus controller initiates a read sequence, the GX2431 is only used to transfer data to the controller. Therefore, the bus controller must start the read sequence immediately after issuing the read register command so that the GX2431 can provide the requested data. In addition, the bus controller reads the timing after sending the recalling the EEPROM command, see the **GX2431 Function Command** section for details.

All read sequences must be at least 60us, including a recovery time of at least 5us between two read cycles. When the bus control pulls the data line from high to low, the read sequence begins, the data line must be held for at least 1us, and then the bus is released (see Figure 10). After the bus controller issues a read sequence, the GX2431 transmits 1 or 0 by pulling high or low on the bus. When the transfer of 0 is completed, the bus will be released and return to the high-level idle state through the pull-up resistor. The data output by GX2431 is valid within 15us after the falling edge of the read timing. Therefore, the bus controller releases the bus within 15us from the beginning of the read sequence and then samples the bus state to read the state of the data line.

Figure 11 indicates that the sum of T_{INIT}, T_{RC}, and T_{SAMPLE} must be less than 15us. Figure 12 indicates that the system time can be maximized by keeping the T_{INIT} and T_{RC} as short as possible, and placing the controller sampling time at the end of the 15us period.

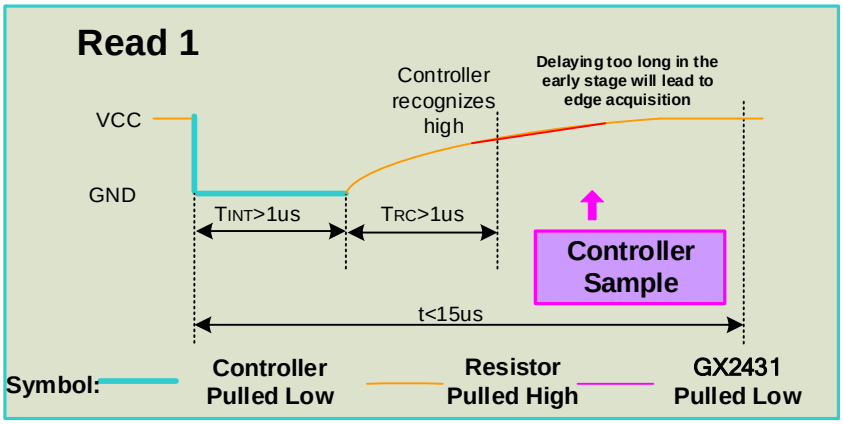


Figure 11. Detailed Timing of Controller Read 1

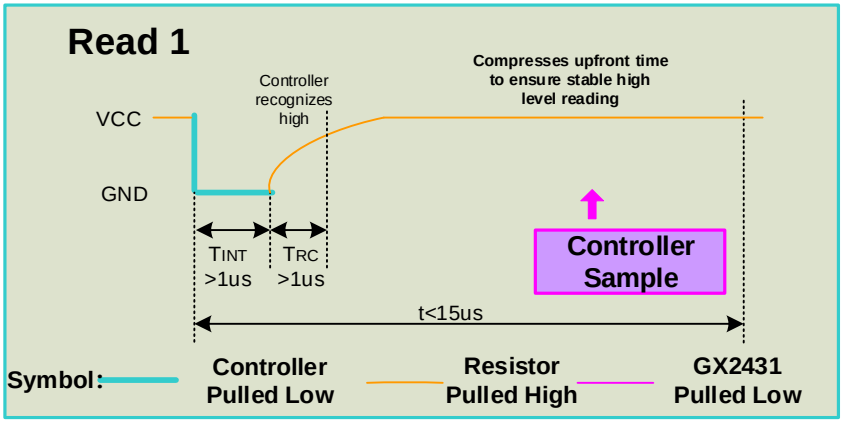


Figure 12. Recommended Controller 1 Timing

6.4 GX2431 Operation Example 1:

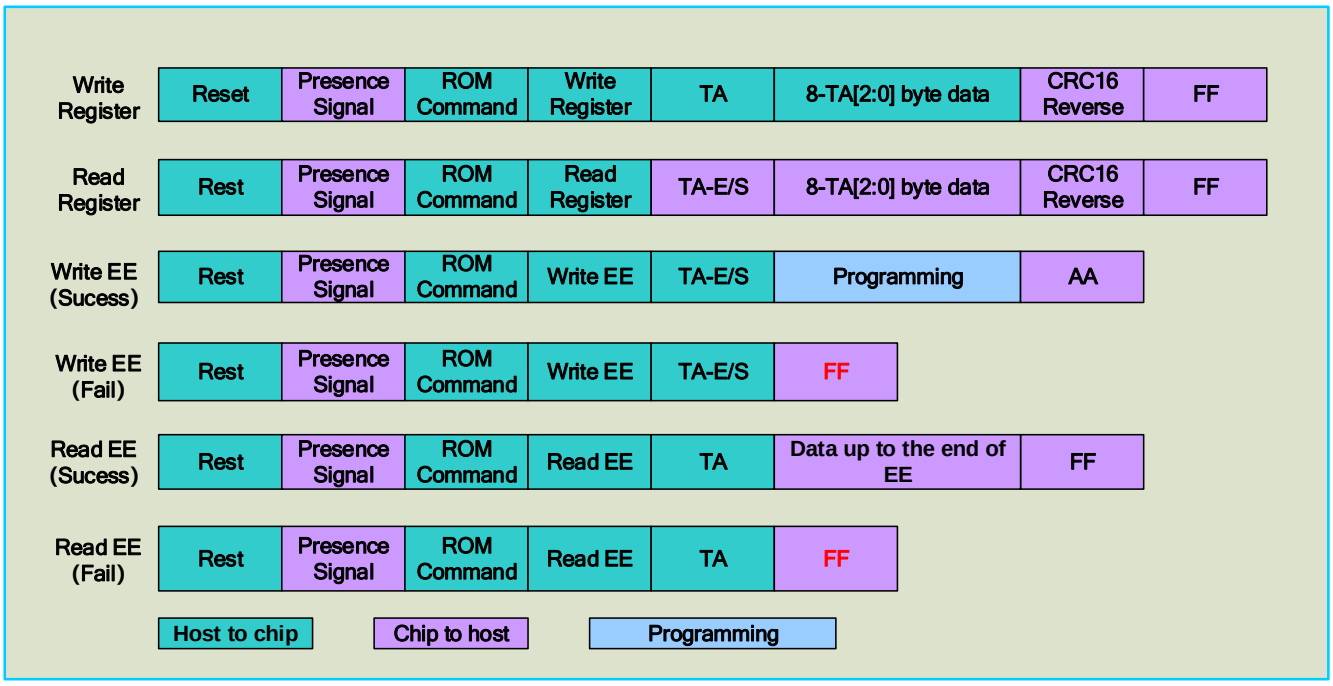


Figure 13. Schematic Diagram of Memory Operation

6.5 GX2431 Operation Example 2:

Write the first 8 bytes of page 1 of memory. Read the entire memory. There is only a single GX2431 connected to the host on the bus, and the communication process is as follows:

MASTER MODE	DATA (LSB FIRST)	WRITE VALUE
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue "Skip ROM" command
TX	0Fh	Issue "Write Scratchpad" command
TX	20h	TA1, beginning offset = 20h
TX	00h	TA2, address = 0020h
TX	<8 data bytes>	Write 8 bytes of data to scratchpad
RX	<2 bytes CRC16\>	Read CRC16 to check data integrity
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue "Skip ROM" command
TX	AAh	Issue "Write Scratchpad" command
RX	20h	Read TA1, start offset = 20h
RX	00h	Read TA2, address = 0020h
RX	07h	Read E/S, end offset = 111b, AA, PF = 0
RX	<8 data bytes>	Read scratchpad data and verify
RX	<2 bytes CRC16\>	Read CRC16 to check for data integrity
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue "Skip ROM" command
TX	55h	Issue "Write Scratchpad" command
TX	20h	TA1
TX	00h	TA2
TX	07h	E/S (authorization code)
----	<1-Wire idle high>	Wait $t_{PROGmax}$ for the copy function to complete
RX	AAh	Read copy status, AAh = success
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue "Skip ROM" command
TX	F0h	Issue "Write Scratchpad" command
TX	00h	TA1, beginning offset = 00h
TX	00h	TA2, address = 0000h
RX	<144 data bytes>	Read the entire memory
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse

7 Absolute Maximum Ratings

Voltage range of each pin to ground .....-0.5V to +6.0V

Range of working temperature.....-55°C to +125°C

Storage range.....-55°C to +150°C

Soldering temperature range ..... 300℃(10S)

8 DC Characteristics

Test conditions: (-55℃~+100℃; VDD = 2.5V~5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Pullup Supply	V_{PU}	Parasite Power	+2.5		+5.5	V	1,2
Input Logic-Low	V_{IL}		-0.3		+0.8	V	1,3,4
Input Logic-High	V_{IH}	Parasite Power	+2.5		The lower of 5.5 or VDD + 0.3	V	1,6
Sink Current	I_L	VI/O = 0.4V	4.0			mA	1
Standby Current	I_{DDS}			0.75	1	uA	6,7
Active Current	I_{DD}	VDD = 5V			0.8	mA	8

Notes:

1) All voltages are referenced to ground potential.

2) The pull-up voltage is obtained like this: Assuming that the pull-up device is perfect, the high level of the pull-up should be equal to VPU. In order to meet the VIH specification of the GX2431, the actual transistor pull-up power supply must include the limit of the voltage drop; thus $V_{PU\_ACTUAL} = V_{PU\_IDEAL} + V_{TRANSISTOR}$.

3) A logic 0 level is obtained when the sink current is 4mA.

4) Low voltage state in parasitic power mode, VILMAX may have to be lowered to 0.5V in order to guarantee the presence of pulses.

5) Logic 1 voltage is obtained when the source current is 1mA.

6) Standby current is defined at 70°C

7) To reduce IDDS, the range of DQ is as follows: GND ≤ DQ ≤ GND + 0.3V or VDD – 0.3V ≤ DQ ≤ VDD.

8) Dynamic current involves writing to EEPROM memory.

9 AC Characteristics- Non-Volatile Memory

Test conditions: (-55℃~+125℃; VDD = 2.5V~5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
NV Write Cycle Time	t_{WR}			8	10	ms	
EEPROM Writes	N_{EEWR}	25°C	200k			writes	
		85°C	50k			writes	
EEPROM Data Retention	t_{EEDR}	-55°C to +55°C	40			years	

10 AC Characteristics

Test conditions: (-55℃~+125℃; VDD = 2.5V~5.5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Time Slot	t_{SLOT}		60		120	µs	1
Recovery Time	t_{REC}		5			µs	1
Write 0 Low Time	t_{LOW0}		60		120	µs	1
Write 1 Low Time	t_{LOW1}		1		15	µs	1
Read Data Valid	t_{RDV}				15	µs	1
Reset Time High	t_{RSTH}		480			µs	1
Reset Time Low	t_{RSTL}		480		640	µs	1
Presence-Detect High	t_{PDHIGH}		15		60	µs	1
Presence-Detect Low	t_{PDLOW}		60		240	µs	1
Capacitance	$C_{IN/OUT}$				25	pF	

Notes

1) See Figure 14 for timing.

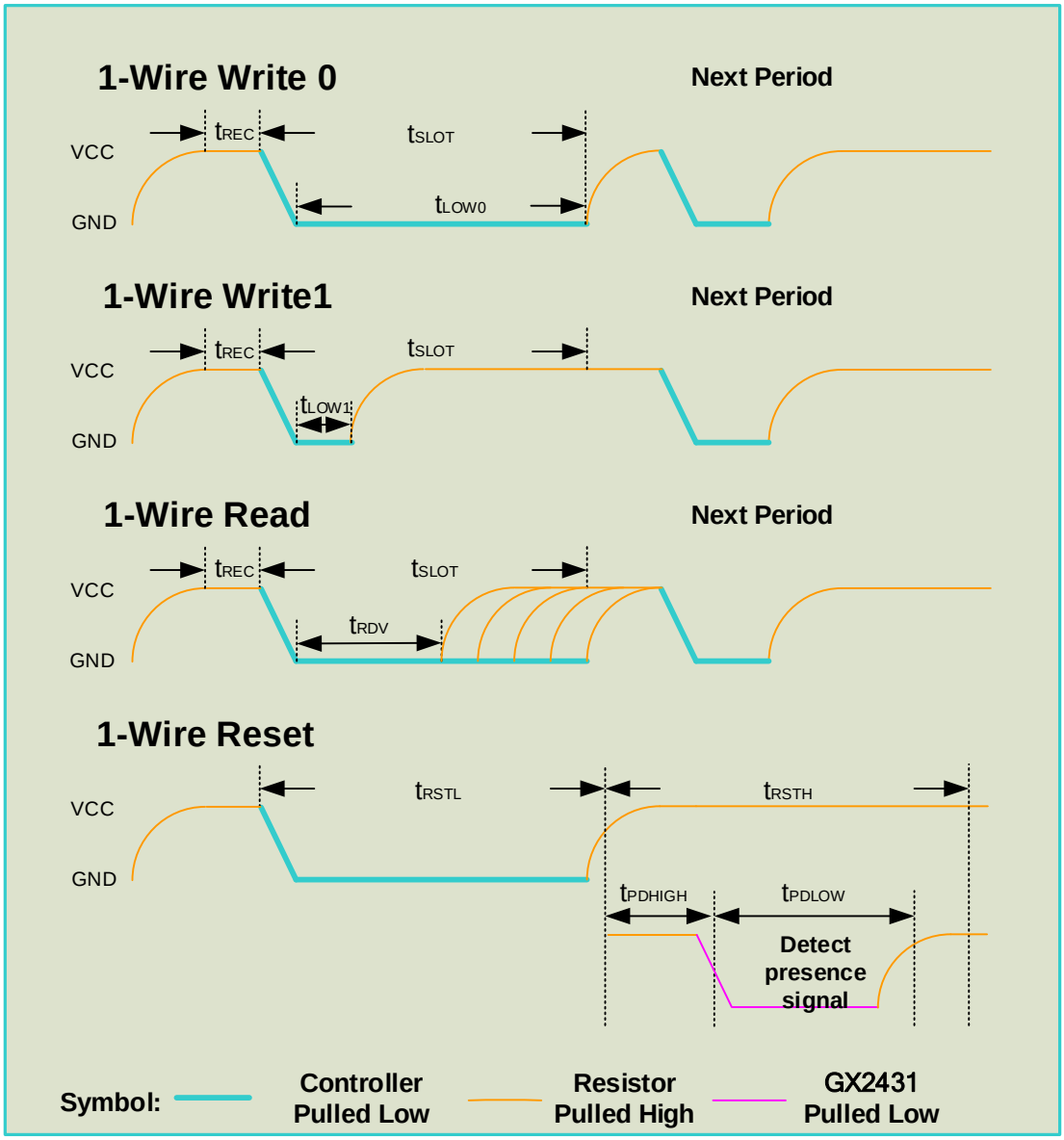
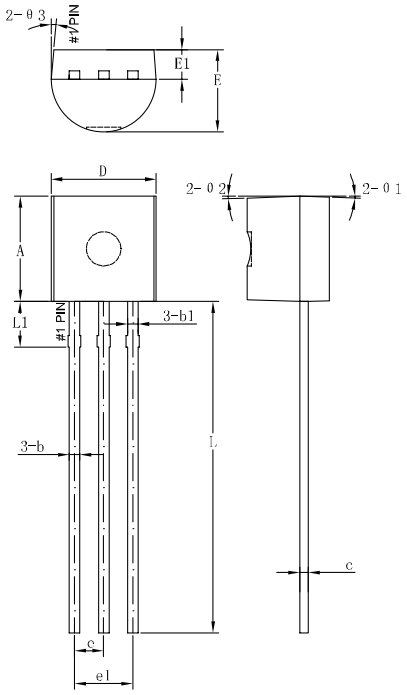


Figure 14. 1-Wire Timing

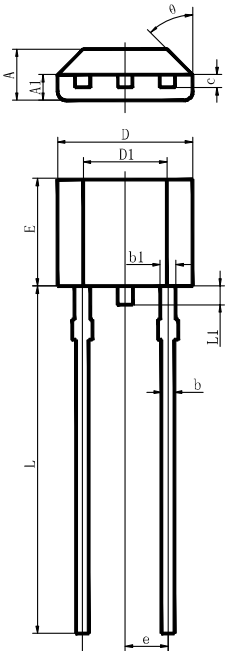
11 Product Package Model List

11.1 TO92 4.6*4.6*3.6 (GX2431)



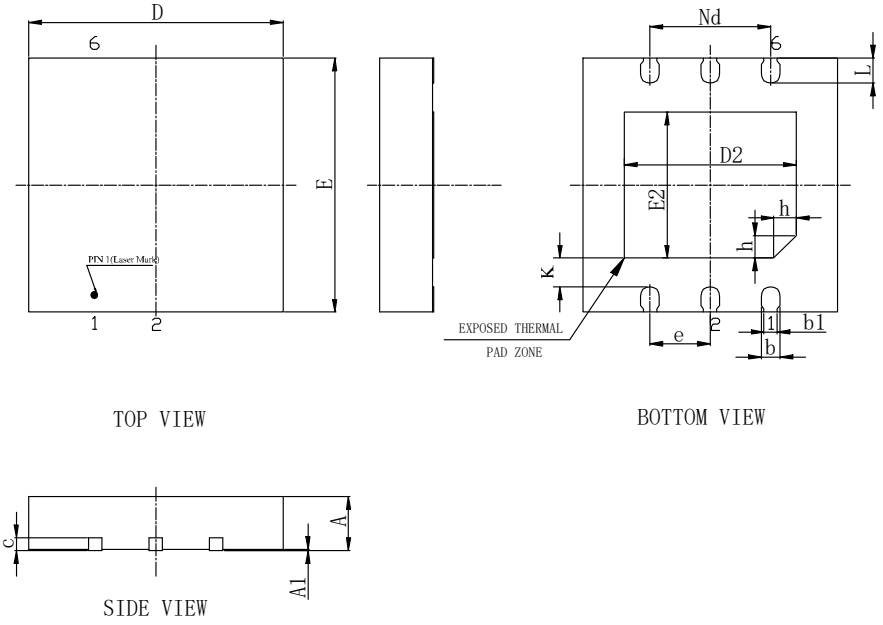
符号	机械尺寸/mm		
	最小值	典型值	最大值
A	4.5	4.6	4.7
b	0.38	0.45	0.56
b1		0.45	
c	0.36	0.38	0.51
D	4.5	4.6	4.7
E	3.45	3.6	3.75
E1	1.2	1.3	1.4
e		1.27	
e1		2.54	
L	13.5	14.5	15.3
L1		1.96	
θ1		2°	
θ2		2°	
θ3		5°	

11.2 TO92S-2 4.0*3.15*1.52 (GX2431WS)



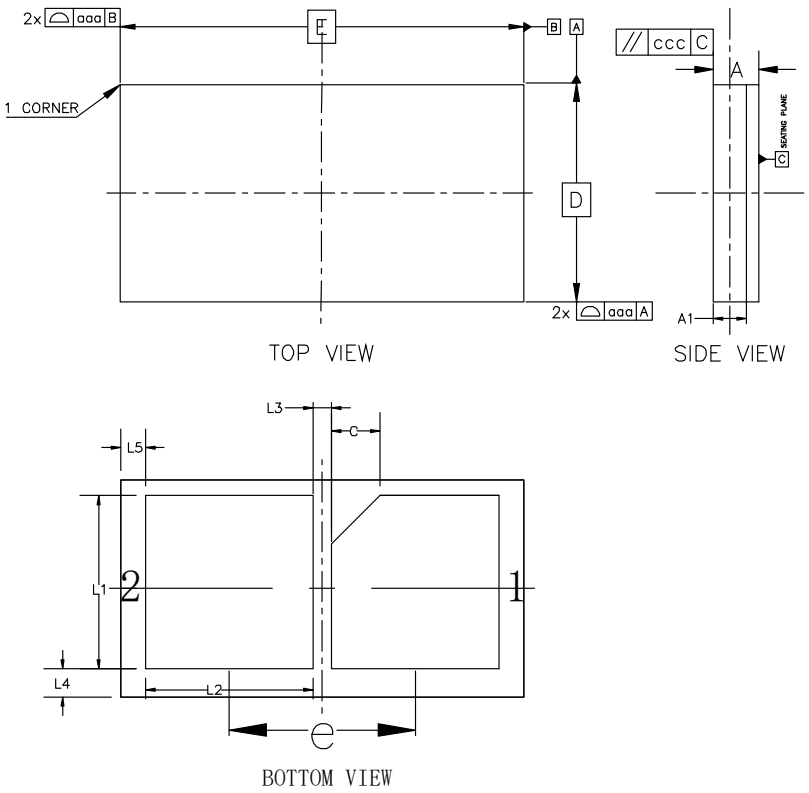
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.420	1.620	0.056	0.064
A1	0.660	0.860	0.026	0.034
b	0.330	0.480	0.013	0.019
b1	0.400	0.510	0.016	0.020
c	0.330	0.510	0.013	0.020
D	3.900	4.100	0.154	0.161
D1	2.280	2.680	0.090	0.106
E	3.050	3.250	0.120	0.128
e	1.270 TYP.		0.050 TYP.	
e1	2.440	2.640	0.096	0.104
L	15.100	15.500	0.594	0.610
L1	0.350	0.650	0.014	0.026
θ	45° TYP.		45° TYP.	

11.3 DFN6 4.0*4.0*0.75 (GX2431D, GX2431DVS)



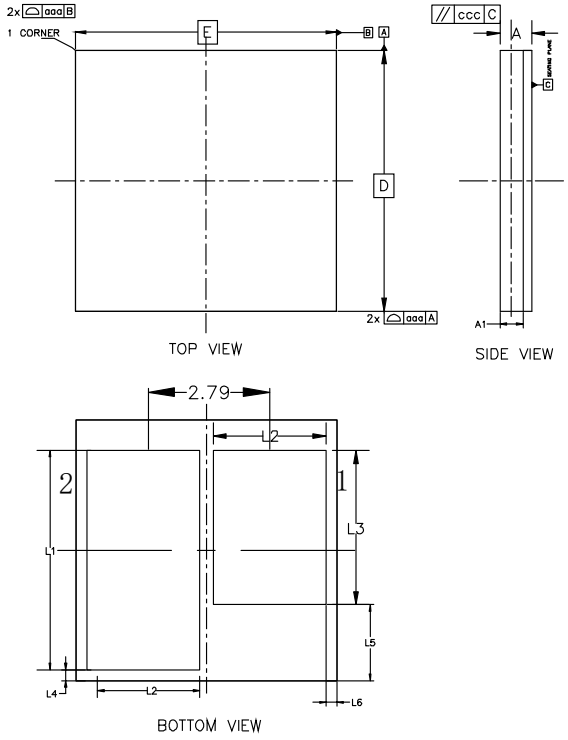
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.25	0.30	0.35
b1	0.21REF		
c	0.203REF		
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.95BSC		
Nd	1.90BSC		
E	3.90	4.00	4.10
E2	2.20	2.30	2.40
L	0.35	0.40	0.45
h	0.30	0.35	0.40
K	0.45REF		

11.4 SFN2 3.5*6.5*0.73 (GX2431GA)



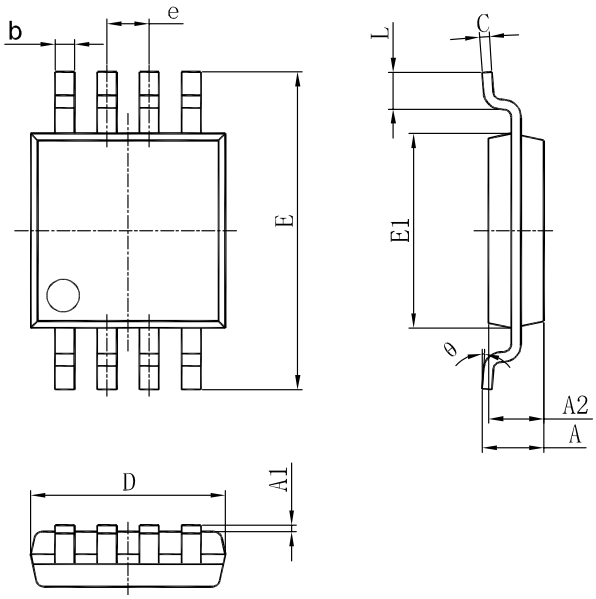
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.73	0.81
c	0.16	0.20	0.24
D	6.40	6.50	6.60
E	3.40	3.50	3.60
aaa	0.10		
ccc	0.25		
L1	2.80 REF		
L2	2.70 REF		
C	0.780 BASIC		
e	3.00 BASIC		
A1	0.48	0.53	0.58
L3	0.30 REF		
L4	0.450 REF		
L5	0.400 REF		

11.5 SFN2 6.0*6.0*0.73 (GX2431G)



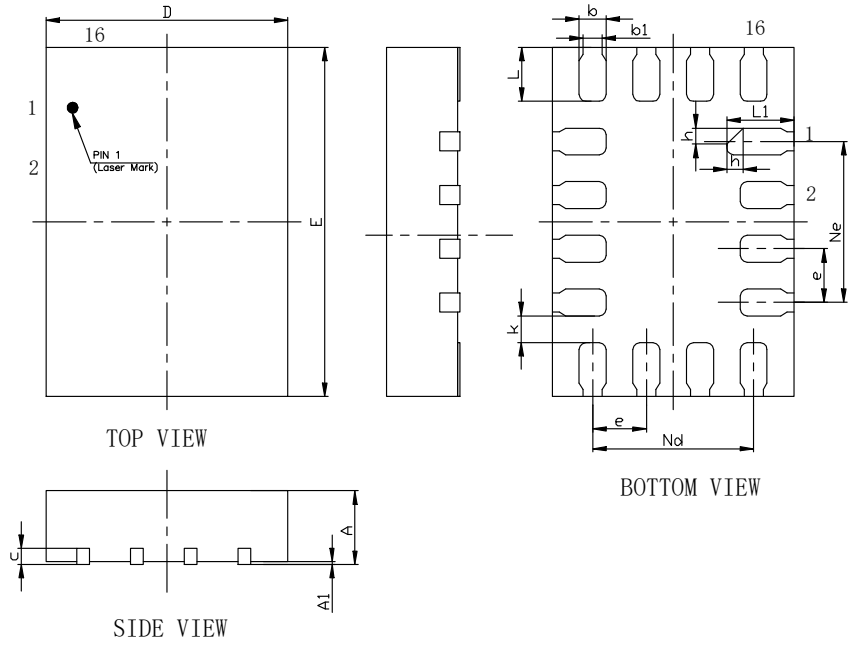
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.73	0.81
c	0.16	0.20	0.24
D	5.90	6.00	6.10
E	5.90	6.00	6.10
aaa	0.10		
ccc	0.25		
L1	5.05 REF		
L2	2.600 REF		
L3	3.550 BASIC		
e	0.310 BASIC		
A1	0.48	0.53	0.58
L4	0.250 BASIC		
L5	1.750 BASIC		
L6	0.245 BASIC		

11.6 MSOP-8 3.0*3.0*1.0 (GX2431P)



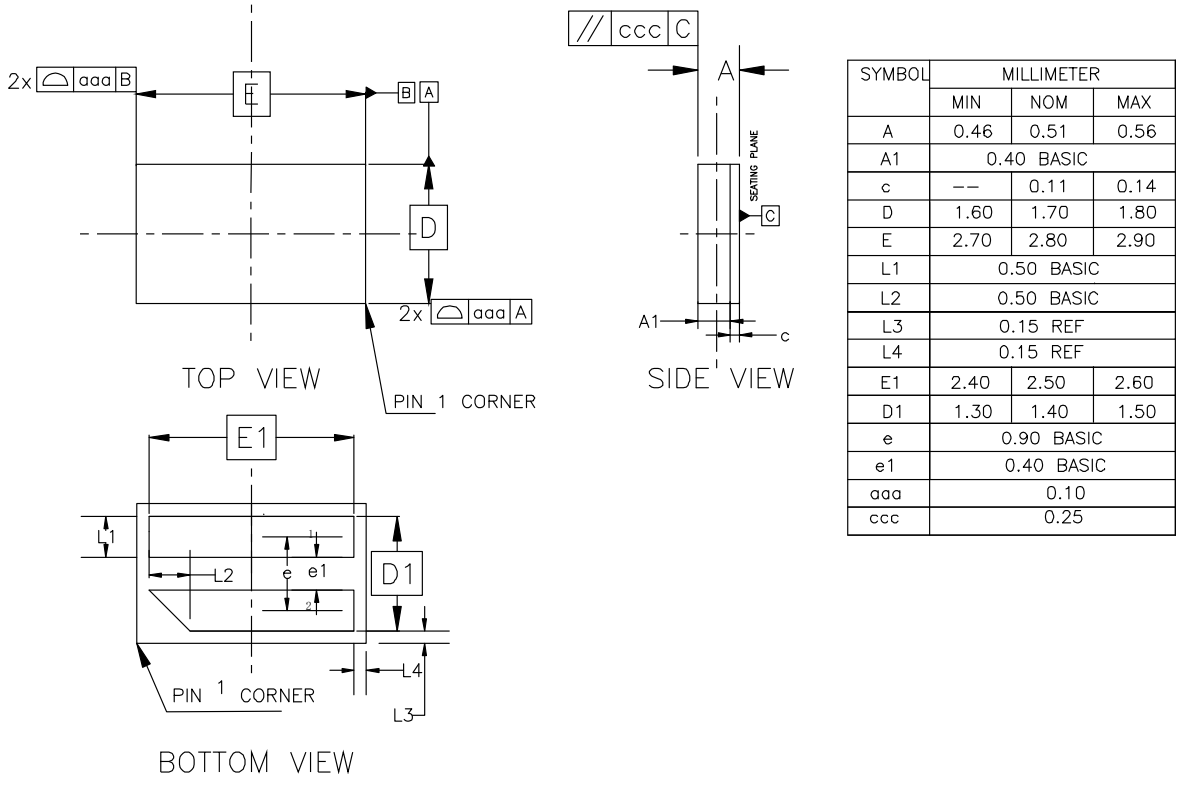
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	---	1.100	---	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650 (BSC)		0.026 (BSC)	
E	4.750	5.050	0.187	0.199
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

11.7 QFN16 1.8*2.6*0.55 (GX2431Q)



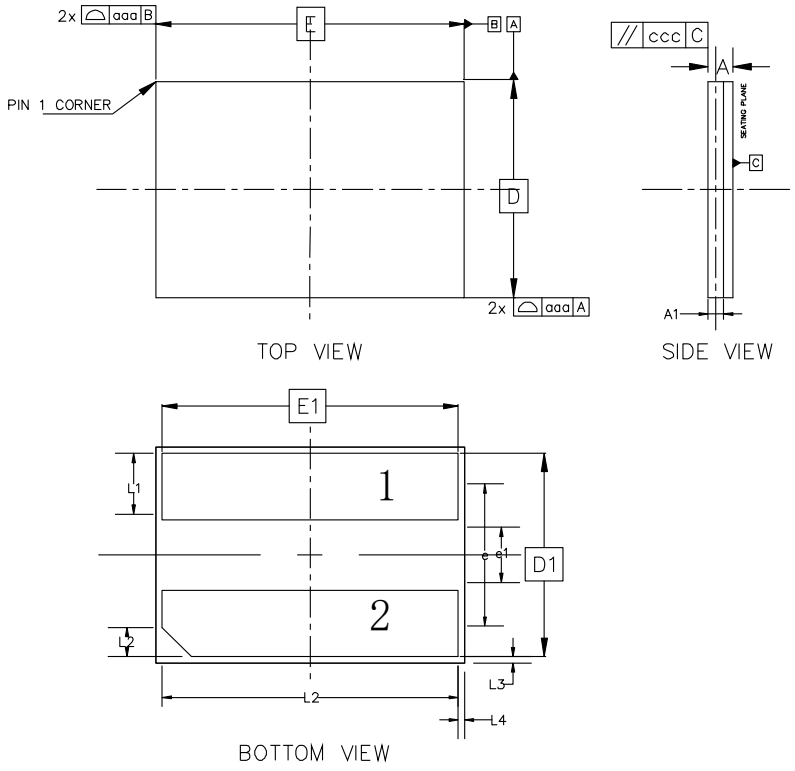
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.152REF		
D	1.75	1.80	1.85
e	0.40BSC		
Nd	1.20BSC		
Ne	1.20BSC		
E	2.50	2.60	2.70
L	0.35	0.40	0.45
L1	0.45	0.50	0.55
h	0.07	0.12	0.17
h	0.20REF		

11.8 SFN 1.7*2.8*0.51 (GX2431SP1)



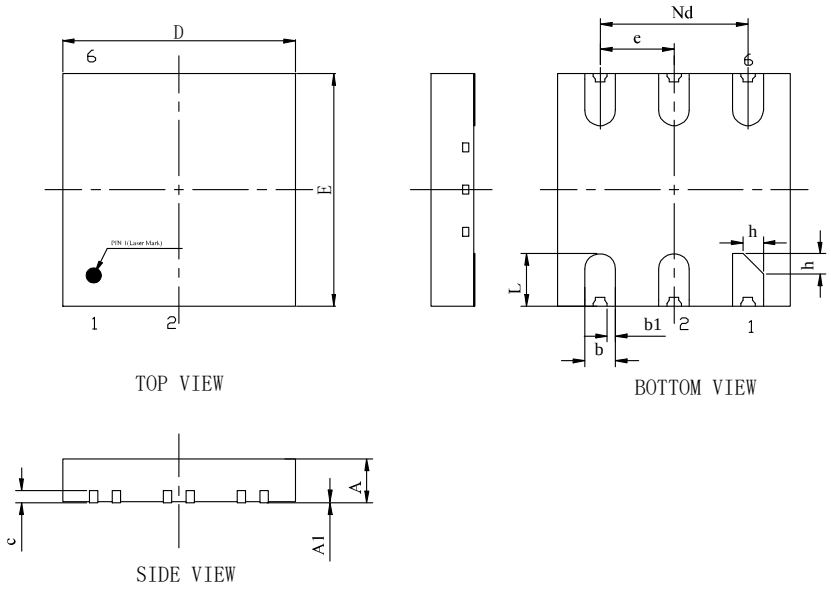
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.46	0.51	0.56
A1	0.40 BASIC		
c	--	0.11	0.14
D	1.60	1.70	1.80
E	2.70	2.80	2.90
L1	0.50 BASIC		
L2	0.50 BASIC		
L3	0.15 REF		
L4	0.15 REF		
E1	2.40	2.50	2.60
D1	1.30	1.40	1.50
e	0.90 BASIC		
e1	0.40 BASIC		
aaa	0.10		
ccc	0.25		

11.9 SFN2 5.0*3.5*0.4 (GX2431S)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.32	0.40	0.48
c	--	0.15	0.20
D	3.40	3.50	3.60
E	4.90	5.00	5.10
aaa	0.10		
ccc	0.25		
L1	0.991 REF		
L2	0.475 REF		
e1	0.90 BASIC		
e	2.309 BASIC		
A1	0.20	0.25	0.30
L3	1.20 REF		
L4	0.10 REF		
E1	4.70	4.80	4.90

11.10 DFN6 4.0*4.0*0.75 (GX2431T , GX2431TVS)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.48	0.53	0.58
b1	0.143REF		
c	0.203REF		
D	3.90	4.00	4.10
e	1.27BSC		
Nd	2.54BSC		
E	3.90	4.00	4.10
L	0.85	0.90	0.95
h	0.30	0.35	0.40

12 Ordering Information

Order Number	Device	Package	SPQ	Note
GX2431-2D-Bu	GX2431	TO92	2000	Bulk
GX2431-ADTW-Bu	GX2431	TO92	2000	Bulk
GX2431D-T&R	GX2431D	DFN-6	4000	Tape & Reel
GX2431DVS-T&R	GX2431DVS	DFN-6	4000	Tape & Reel
GX2431GA-ADTW-T&R	GX2431GA	SFN2(3.5*6.5)	4000	Tape & Reel
GX2431GA-T&R	GX2431GA	SFN2(3.5*6.5)	4000	Tape & Reel
GX2431G-Tr	GX2431G	SFN2(6*6)	490	Tray
GX2431P-T&R	GX2431P	MSOP-8	4000	Tape & Reel
GX2431Q-2D-T&R	GX2431Q	QFN16	3000	Tape & Reel
GX2431Q-2DTW-T&R	GX2431Q	QFN16	3000	Tape & Reel
GX2431Q-AD-T&R	GX2431Q	QFN16	3000	Tape & Reel
GX2431Q-ADTW-T&R	GX2431Q	QFN16	3000	Tape & Reel
GX2431SP2-T&R	GX2431S	SFN2	4000	Tape & Reel
GX2431-T&R	GX2431	TO92	2000	Tape & Reel
GX2431T-T&R	GX2431T	DFN6	4000	Tape & Reel
GX2431TVS-T&R	GX2431TVS	DFN6	4000	Tape & Reel
GX2431VS-Bu	GX2431	TO92	2000	Bulk
GX2431WS- Bu	GX2431WS	TO92S-2	2000	Bulk