CUSTOMER APPROVAL SHEET

MODEL IEH163QLN01.0

CUSTOMER **Title :**

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☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)**

☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)**

☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.____)**

☐ **CUSTOMER REMARK :**

艾顺佳科技 excellence

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Date :	2014/7/17

Product Specification

1.63" COLOR AMOLED MODULE

MODEL NAME: H163QLN01

< >Preliminary Specification

< ◆ >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	Mar. 5, 2014		First Draft
1.0	Mar.18,2014	17 21 22 23	Revise H. Specifications_Optical characteristics Add I. Reliability test items_Vibration test Add J.packing Revise K.2D/3D drawing;
2.0	Apr.16,2014	7 11 14, 15 16	Add Idle power consumption & revise panel power Revise TE description Revise Initial Code for display optimization B500=0x05 -> 0x03; B501=0x05 -> 0x03; B502=0x05 -> 0x03 BA00=0x13 -> 0x03; BA01=0x13 -> 0x03; BA02=0x13 -> 0x03 BE00=0x22 -> 0x32 Revise CF description
3.0	May 29,2014	13 14 15 16	Revise Initial Code for Power optimization F500=0x10 ED00~ED07 =0x48 00 E0 13 08 00 0C 00 C700~C707 =0x0F 05 00 0F 43 00 88 22 C200~C20B =0x0B 0B 0B 0B 0B 0B 0B 0B 0B 0B 0B 0B C000=0x28
4.0	July.3,2014	24	Revise K.2D/3D drawing;
5.0	July.17,2014	8 13 14 15 16	Update Idle mode VDD power @ page 8. Revise Initial Code for Power optimization F500=0x10 ED00~ED07 =0x48 00 E0 13 08 00 0C 00 C700~C707 =0x0F 05 00 0F 43 00 88 22 C200~C20B =0x0B 0B 0B 0B 0B 0B 0B 0B 0B 0B 0B 0B C000=0x28

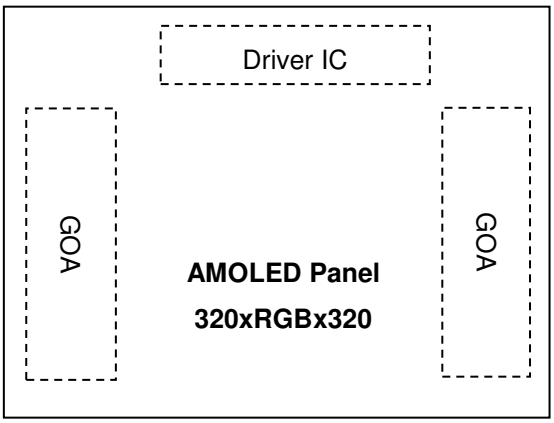
Contents

A. General Specification

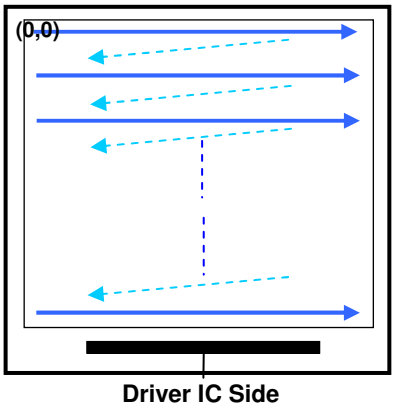
1. Physical Specifications

	Item	Description	Remark
1	Screen Size (inch)	1.63”	
2	Display Mode	AMOLED	
3	Display Resolution (dot)	320xRGBx320	
4	Active Area (mm*mm)	29.28 (H)×29.28(V)	
5	Pixel Configuration	Hyper R.G.B	
6	Display Color (M)	16.7	
7	Brightness (nits)	300	
8	Interface	MIPI DSI	
9	Outline Dimension (mm*mm*mm)	32.08 (H) × 36.48(V) × 0.7(T)	cell+foam

2. Module Block Diagram



3. Panel Scan direction



B. Electrical Specifications

1. Main FPC Pin assignment — AMOLED Panel Input/Output Signal Interface

Recommended connector: AXE520127 (Panasonic)

FPC	Pin_name	I/O	Description
1	**ELVSS**	P	AMOLED power Negative
2	**ELVSS**	P	AMOLED power Negative
3	**ELVSS**	P	AMOLED power Negative
4	**VDD**	P	Power supply for analog
5	**IOVDD**	P	Power supply for Interface system excep MIPI interface
6	**GND**	P	GND
7	**TE**	O	Vsync(vertical sync)signal output from panel to avoid tearing effect
8	**MTP**	I	MTP(need to indicate to connect GND or NC)
9	**RESX**	I	Device reset signal (0 : Enable ; 1: Disable)
10	**SWIRE**	O	SWIRE signal for PWR IC control
11	**ELVDD**	P	AMOLED power positive
12	**ELVDD**	P	AMOLED power positive
13	**ELVDD**	P	AMOLED power positive
14	**GND**	P	GND
15	**DSI_D0N**	I/O	MIPI data negative signal
16	**DSI_D0P**	I/O	MIPI data positive signal
17	**GND**	P	GND
18	**DSI_CLKN**	I	MIPI strobe negative signal
19	**DSI_CLKP**	I	MIPI strobe postive signal
20	**GND**	P	GND

Note: I = input ; O = output ; P = Power ; I/O = input / Output

2. Absolute maximum ratings

Item	Symbol	Min.	Max.	Unit	Remark
Digital Power supply	IOVDD	-0.3	5.5	V	
Analog Power supply	VDD	-0.3	5.5	V	
ELVDD power supply	ELVDD	-	5.0	V	
ELVSS power supply	ELVSS	-5.0	-	V	

Note : If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

C. Electrical Characteristics

1. DC Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Digital Power supply		IOVDD	1.65	1.8	1.95	V	Note1
Analog Power supply		VDD	2.8	3.0	3.1	V	Note1
ELVDD power supply		ELVDD	4.57	4.60	4.63	V	Note1,2
ELVSS power supply		ELVSS	-3.35	-3.40	-3.45	V	Note1
Input Signal Voltage	H Level	V_{IH}	0.8*IOVDD	-	IOVDD	V	Note1
	L Level	V_{IL} 0 - 0.2*IOVDD				V	
Output Signal Voltage	H Level	V_{OH}	0.8*IOVDD	-	IOVDD	V	Note1
	L Level	V_{OL}	0	-	0.2*IOVDD	V	Note1

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

Note 2 : TPS65631W Positive output voltage = 4.6V ± 0.8% at -40℃ ≦ Ta ≦ +85 ℃

2. Display Current Consumption

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Panel Power		P_{NL}	ELVDD:4.6V ELVSS:-3.4V	--	--	138.4	mW	Note1,2,
		I_{NL}		--	--	17.3	mA	Note1,2,
IC	**Normal**	P_{VDD}	VDD : 3.0V	--	25.2	39.3	mW	Note2,
		I_{VDD}		--	8.4	13.1	mA	Note2,
		P_{IOVDD}	IOVDD :1.8V	--	18.0	19.8	uW	Note2,
		I_{IOVDD}		--	10.0	11.0	uA	Note2,
	Idle	P_{VDD}	VDD : 3.0V	--	15.3	17.7	mW	Note3,
		I_{VDD}		--	5.1	5.9	mA	Note3,
		P_{IOVDD}	IOVDD :1.8V	--	18.0	19.8	uW	Note3,
		I_{IOVDD}		--	10.0	11.0	uA	Note3,

Note 1: Based on L255 (300nits) full white pattern

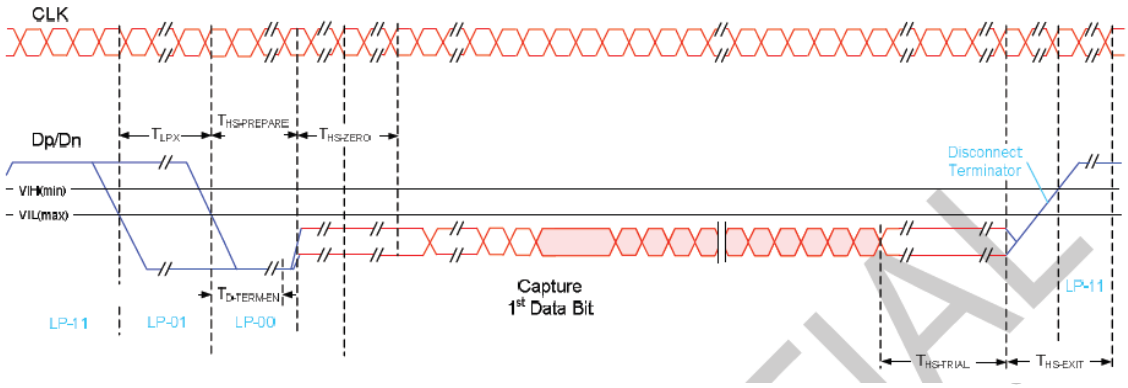
Note 2: Testing in MIPI-DSI frame rate 60Hz CMD mode.

Note 3: Testing in MIPI-DSI frame rate 30Hz CMD mode(Test Condition is 10% Brightness & 10% Pixel ratio.)

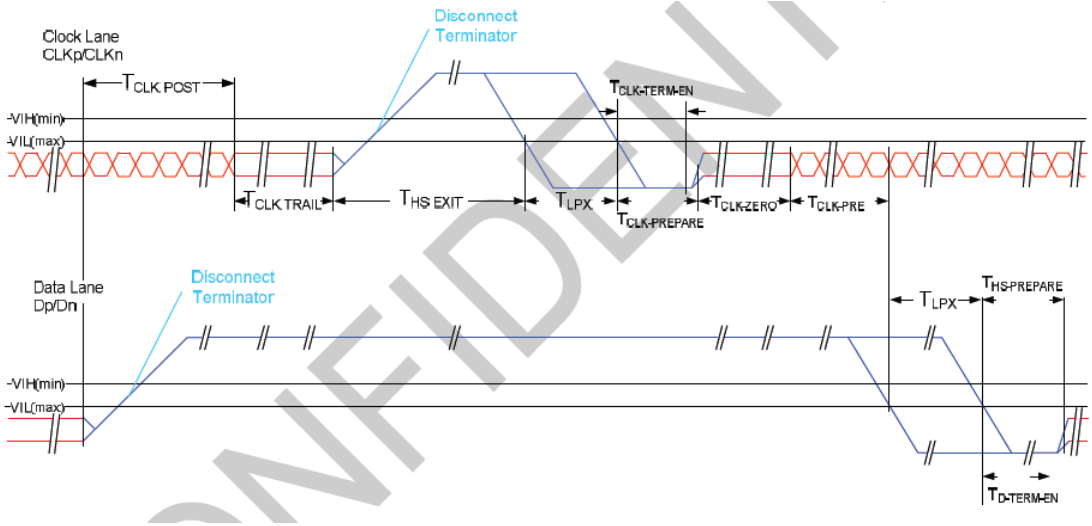
D. AC Characteristics

1. MIPI Interface Characteristics

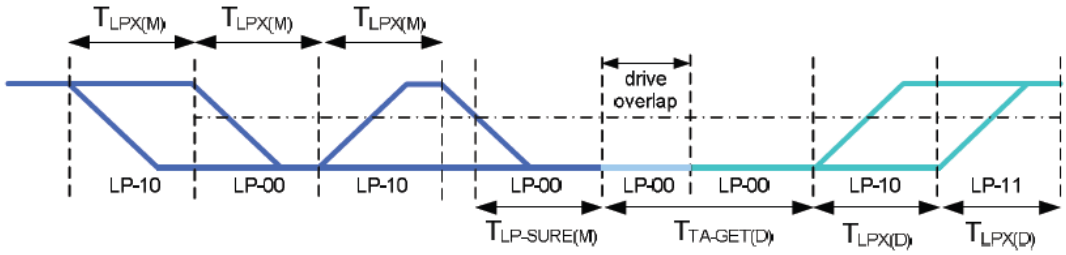
HS Data Transmission Burst



HS clock transmission



Turnaround Procedure



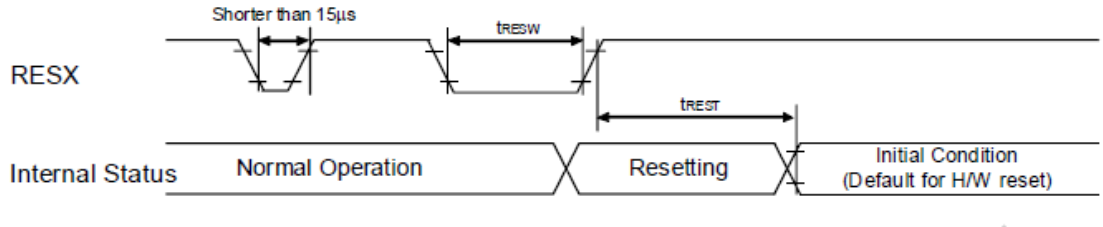
Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to Reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		60 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	96*UI			ns
$T_{LPX(M)}$	Transmitted length of any Low-Power state	100		150	ns

	period of MCU to display module				
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX(D)}$			ns
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX(D)}$			ns
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns

2. Display RESET Timing Characteristics

Reset input timing



IOVDD=1.65 to 1.95V, VDD=2.8 to 3.1V, AGND=DGND=0V, Ta=-40 to 85℃

Timing Parameters

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	15	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

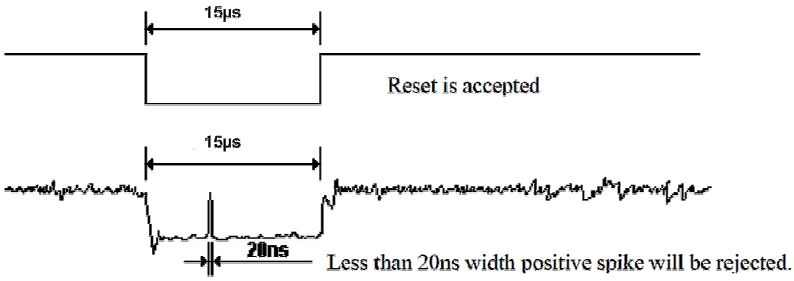
RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 15µs	Reset
Between 5µs and 15µs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display

remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

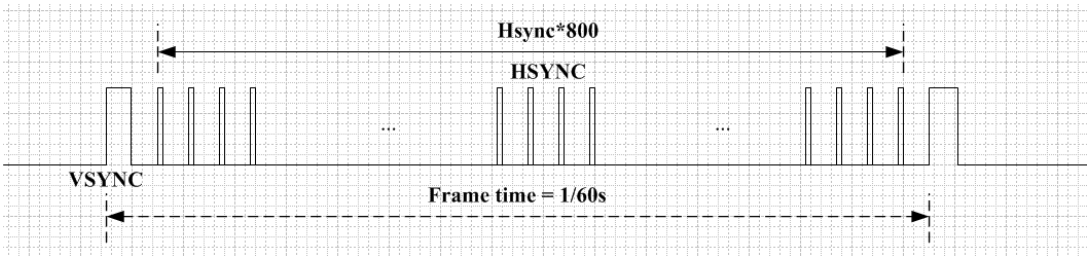
Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

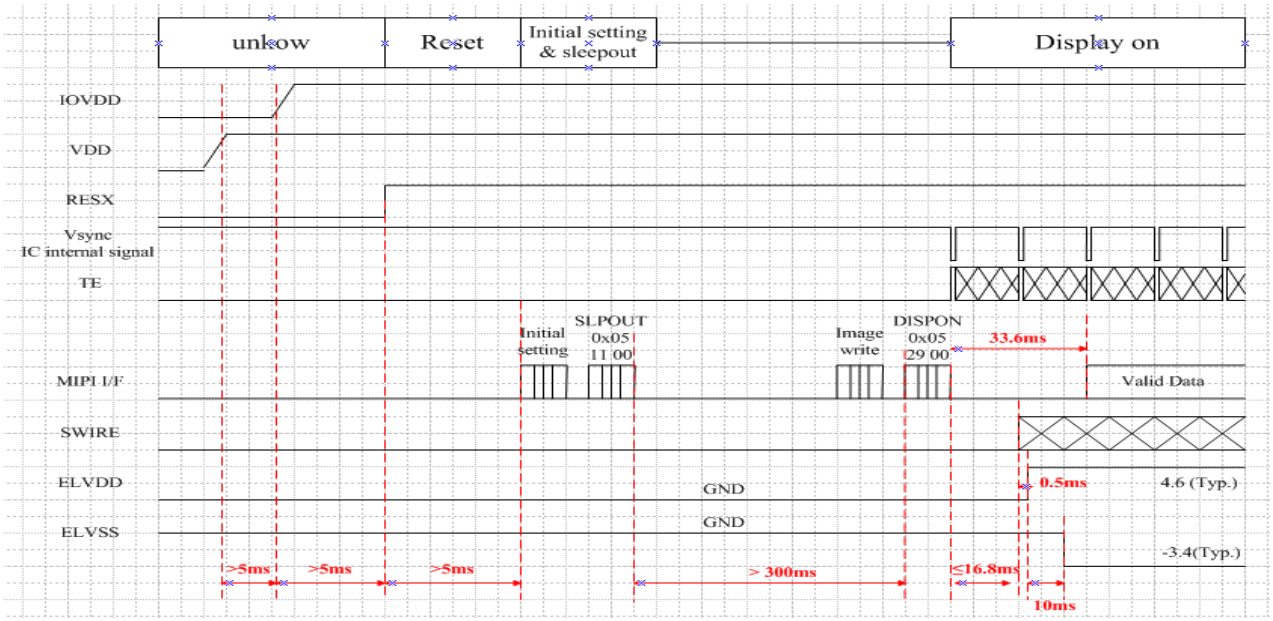
3. TE Timing Characteristics



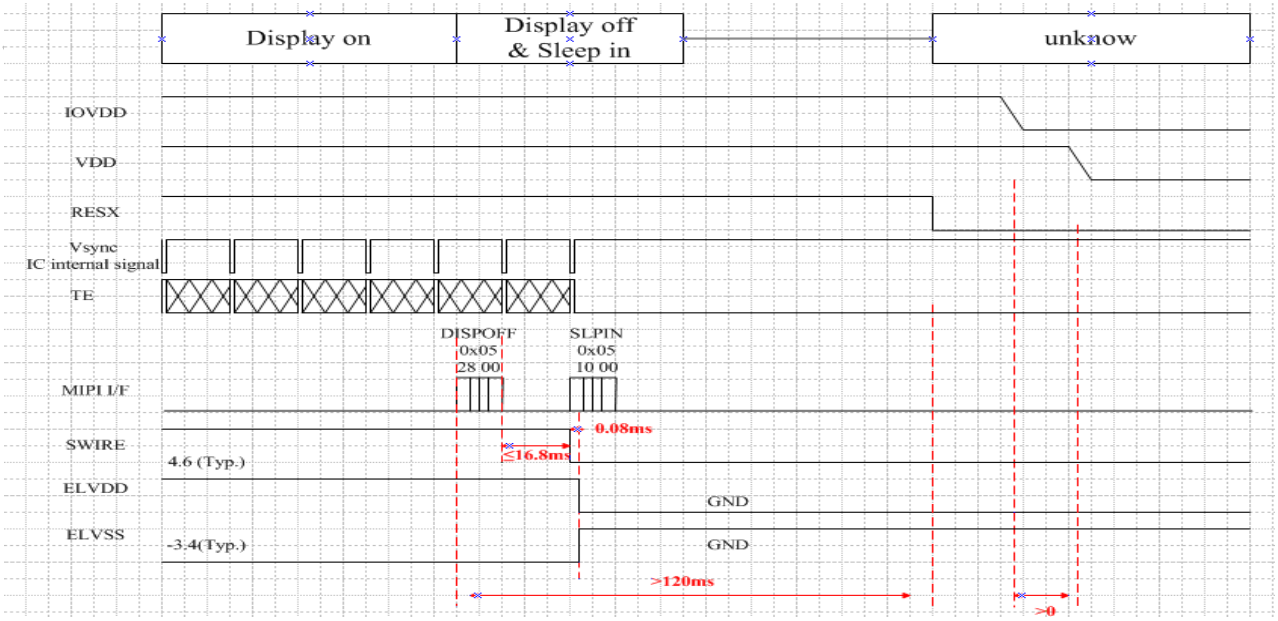
E. Recommended Operating Sequence

1. Display Power on / off Sequence

Power on sequence



Power off sequence



2. Display Initial code

Recommended Power on Initial Sequence								
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	Turn on V_{DD}							VDD=2.8V~3.1V
2	Turn on V_{IOVDD}							IOVDD=1.8V
3	Delay	no limit						
4	REST pin low	20us						
5 6	REST pin high Delay	5 ms						
7			W	0x39	F0	F000	55	
8			W			F001	AA	
9			W			F002	52	
10			W			F003	08	
11			W			F004	00	
12			W	0x39	BD	BD00	01	
13			W			BD01	90	
14			W			BD02	14	
15			W			BD03	14	
16			W			BD04	00	
17			W	0x39	BE	BE00	01	
18			W			BE01	90	
19			W			BE02	14	
20			W			BE03	14	
21			W			BE04	01	
22			W	0x39	BF	BF00	01	
23			W			BF01	90	
24			W			BF02	14	
25			W			BF03	14	
26			W			BF04	00	
27			W	0x39	BB	BB00	07	
28			W			BB01	07	
29			W			BB02	07	
30			W	0x39	D0	D000	00	
31			W	0x39	D1	D100	00	
32			W			D101	00	
33			W			D102	00	
34			W	0x39	D2	D100	00	

35			W			D101	00	
36			W			D102	00	
37			W			D100	00	
38			W	0x39	D3	D101	00	
39			W			D102	00	
40			W	0x39	C7	C700	40	
41			W			F000	55	
42			W			F001	AA	
43			W	0x39	F0	F002	52	
44			W			F003	08	
45			W			F004	02	
46			W	0x15	F5	F500	10	
47			W			ED00	48	
48			W			ED01	00	
49		W	ED02				E0	
50			W	0x39	ED	ED03	13	
51			W			ED04	08	
52			W			ED05	00	
53			W			ED06	0C	
54			W			ED07	00	
55			W			C700	0F	
56			W			C701	05	
57			W			C702	00	
58			W	0x39	C7	C703	0F	
59			W			C704	43	
60			W			C705	00	
61			W			C706	88	
62			W			C707	22	
63			W	0x39	FE	FE00	08	
64			W			FE01	50	
65			W			C300	F2	
66			W	0x39	C3	C301	95	
67			W			C302	04	
68			W	0x15	CA	CA00	04	
69			W			F000	55	
70			W			F001	AA	
71			W	0x39	F0	F002	52	
72			W			F003	08	
73			W			F004	01	

74			W	0x39	B0	B000	03	
75			W			B001	03	
76			W			B002	03	
77			W	0x39	B1	B100	05	
78			W			B101	05	
79			W			B102	05	
80			W	0x39	B2	B200	01	
81			W			B201	01	
82			W			B202	01	
83			W	0x39	B4	B400	07	
84			W			B401	07	
85			W			B402	07	
86			W	0x39	B5	B500	03	
87			W			B501	03	
88			W			B502	03	
89			W	0x39	B6	B600	53	
90			W			B601	53	
91			W			B602	53	
92			W	0x39	B7	B700	33	
93			W			B701	33	
94			W			B702	33	
95			W	0x39	B8	B800	23	
96			W			B801	23	
97			W			B802	23	
98			W	0x39	B9	B900	03	
99			W			B901	03	
100			W			B902	03	
101			W	0x39	BA	BA00	03	
102			W			BA01	03	
103			W			BA02	03	
104			W	0x39	BE	BE00	32	
105			W			BE01	30	
106			W			BE02	70	
107			W	0x39	C2	C200	0B	
108			W			C201	0B	
109			W			C202	0B	
110			W			C203	0B	
111			W			C204	0B	
112			W			C205	0B	

113			W			C206	0B	
114			W			C207	0B	
115			W			C208	0B	
116			W			C209	0B	
117			W			C20A	0B	
118			W			C20B	0B	
119			W			CF00	FF	
120			W			CF01	D4	
121			W			CF02	95	
122			W	0x39	CF	CF03	EF	
123			W			CF04	4F	
124			W			CF05	00	
125			W			CF06	04	
126			W	0x15	35	3500	01	TE (00 : Vsync ; 01 : Vsync+Hsync)
127			W	0x15	36	3600	00	
128			W	0x15	C0	C000	28	
129	Turn on peripheral packet			0x32				Video Turn On
130	Sleep out		W	0x05	11	1100	00	
131	Delay	300 ms						
132	Display on		W	0x05	29	2900	00	

Recommended Power off Mode Sequence

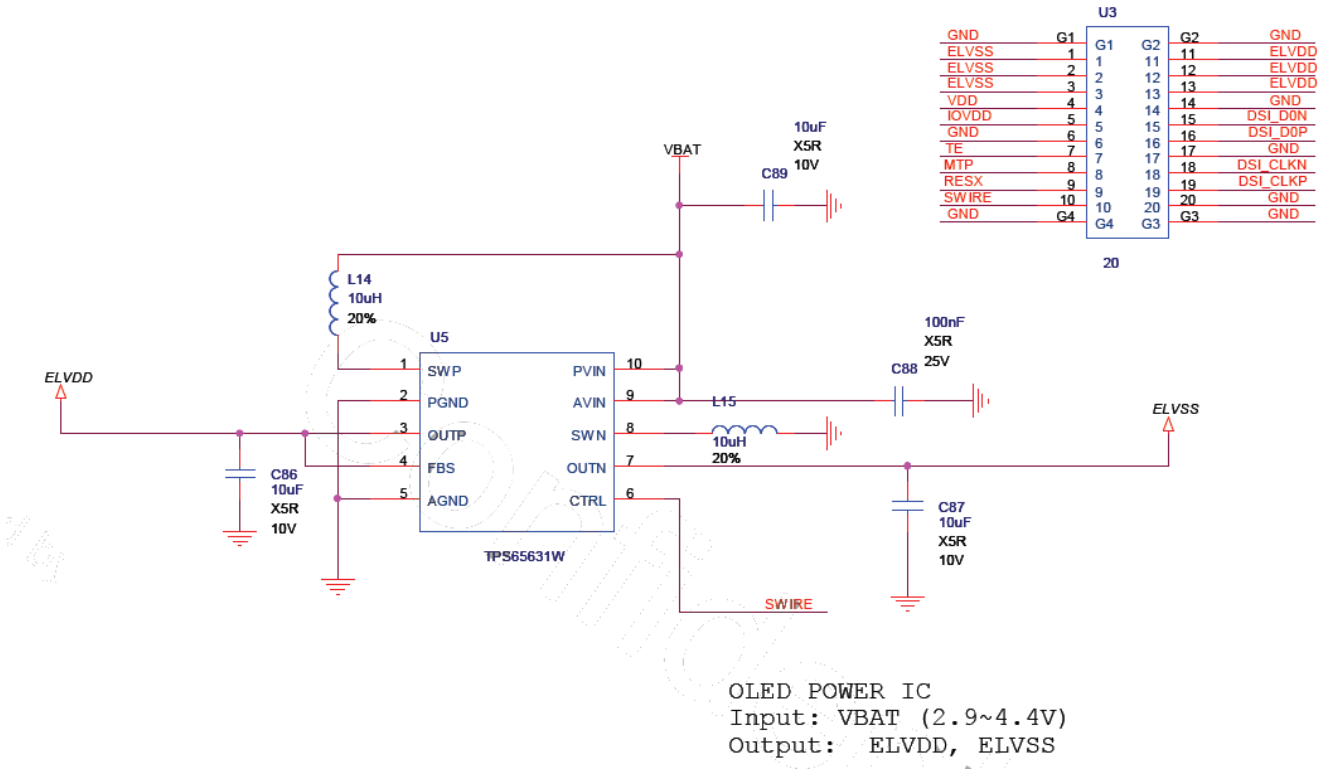
Step	Instruction/Parameters	Delay time	R/W	MIPI Data Type	Address		Data hex.	Description
					MIPI	Others		
1	DIPOFF		W	0x05	28	2800	00	
2	SLPIN		W	0x05	10	1000	00	
3	delay	120ms						
4	Power off							

F. Brightness Control

Recommended Power on Initial Sequence							
Step	Delay time	R/W	MIPI Data Type	Address MIPI	Address Others	Data hex.	Description
1		W	0x39	F0	F000	55	
2		W			F001	AA	
3		W			F002	52	
4		W			F003	08	
5		W			F004	01	
6		W	0x39	CF	CF00	FF	CF00 control Max Brightness
7		W			CF01	D4	
8		W			CF02	95	
9		W			CF03	EF	
10		W			CF04	4F	
11		W			CF05	00	
12		W			CF06	04	

Address MIPI	Address Others	Data hex.	Gray Level
CF	CF00	00	L0
⋮	⋮	⋮	⋮
CF	CF00	80	L128
⋮	⋮	⋮	⋮
CF	CF00	FF	L255

G. Application Circuit



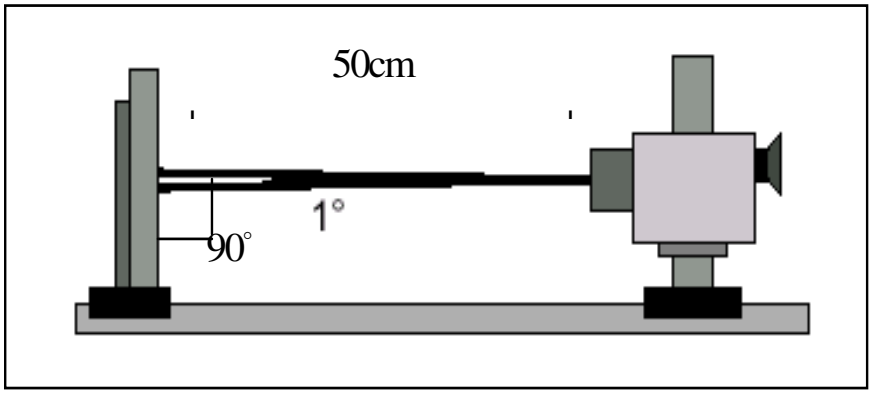
H. Specifications

Item		Abbr.	Min.	Typ.	Max.	Unit	Remark
Optical Characteristic (w/o Cover Lens)		Brightness	270	300	330	nits	Note 3
		Wx	0.275	0.305	0.335		
		Wy	0.290	0.320	0.350		
Contrast ratio @25deg 10000 -- -- Note 4							
Brightness Uniformity		300nits	75%	--	--		Note 5
Viewing angle CR>1600		Top	80°	--	--	deg	Note 6
		Bottom	80°	--	--	deg	
		Left	80°	--	--	deg	
		Right	80°	--	--	deg	
Color	Red	CIE1931 x	0.645	0.675	0.705	Red	Note 7
	Red	CIE1931 y	0.295	0.325	0.355	Red	
	Green	CIE1931 x	0.186	0.236	0.286	Green	
	Green	CIE1931 y	0.661	0.711	0.761	Green	
	Blue	CIE1931 x	0.090	0.130	0.170	Blue	
	Blue	CIE1931 y	0.025	0.065	0.105	Blue	
NTSC		CIE x , y	90	100	--	%	
Life time	T95	25℃	100	--	--	hrs	Note 8
Crosstalk	L128	Vertical	--	--	5.0	%	Note 9
Flicker			--	--	-30	db	Note 10
Optical Switching Time		+25℃B/W(Tr+Tf)/2	--	--	1	ms	Note 11
Gamma		γ	2.0	2.2	2.4		

Note 1: Ambient temperature =25 ºC±2 ºC

Note 2: To be measured in the dark room.

Note 3: The brightness measurement shall be done at the center of the display with a full white image. The brightness shall meet the following spec, at 100% check.

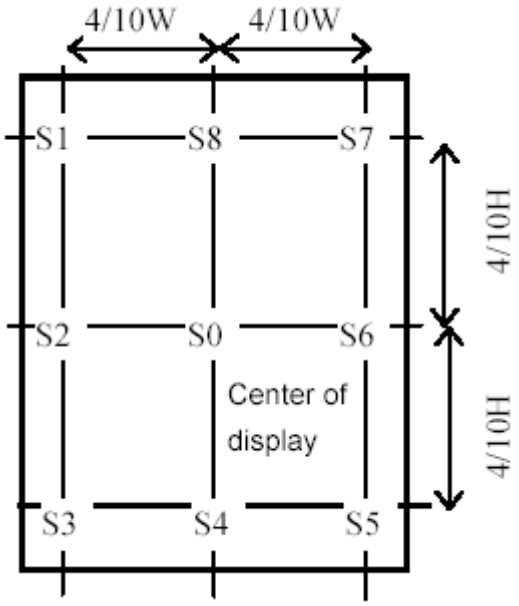


Note 4: Definition of contrast ratio:

Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at “White” state}}{\text{Photo detector output when OLED is at “Black}}$$

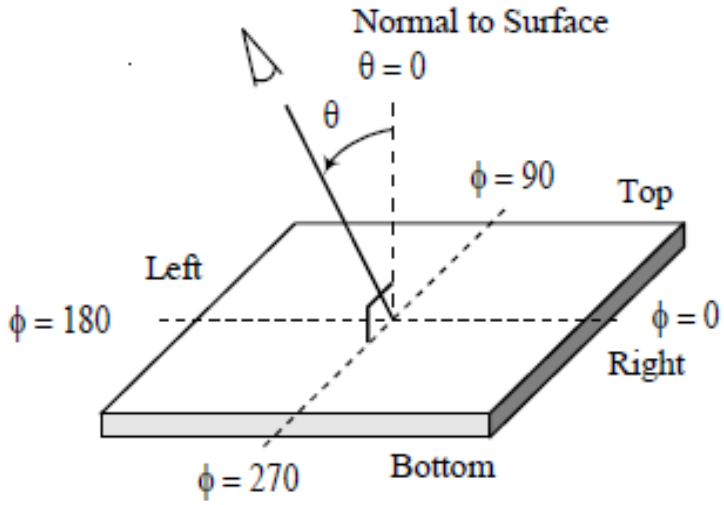
Note 5: Uniformity. Refer to figure as below



$$\text{Luminance uniformity} = \frac{\text{Minimum value from S0 to S8}}{\text{Maximum value from S0 to S8}} \times 100(\%)$$

Note 6: Definition of viewing angle :

The optical performance is specified as the driver IC located at =270°

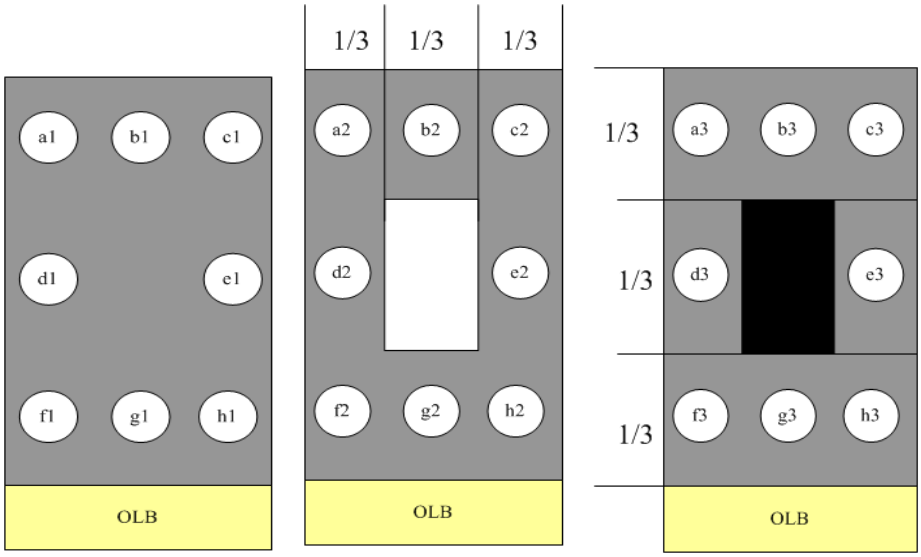


Note 7: The color chromaticity should be based on sample performance because new OLED material should be verified later.

Note 8: Time to 95% Luminance

To measure the burn-in effect, a test pattern with white background applied to the AMOLED display at 30% loading

Note 9: Cross-talk



$$CrossTalk\_White = \begin{cases} 1-\left(\frac{b2}{a2}\div\frac{b1}{a1}\right)\times 100\%, 1-\left(\frac{b2}{c2}\div\frac{b1}{c1}\right)\times 100\%, \\ 1-\left(\frac{d2}{a2}\div\frac{d1}{a1}\right)\times 100\%, 1-\left(\frac{d2}{f2}\div\frac{d1}{f1}\right)\times 100\%, \\ 1-\left(\frac{e2}{c2}\div\frac{e1}{c1}\right)\times 100\%, 1-\left(\frac{e2}{h2}\div\frac{e1}{h1}\right)\times 100\%, \\ 1-\left(\frac{g2}{f2}\div\frac{g1}{f1}\right)\times 100\%, 1-\left(\frac{g2}{h2}\div\frac{g1}{h1}\right)\times 100\% \end{cases}$$

$$CrossTalk\_Black = \begin{cases} 1-\left(\frac{b3}{a3}\div\frac{b1}{a1}\right)\times 100\%, 1-\left(\frac{b3}{c3}\div\frac{b1}{c1}\right)\times 100\%, \\ 1-\left(\frac{d3}{a3}\div\frac{d1}{a1}\right)\times 100\%, 1-\left(\frac{d3}{f3}\div\frac{d1}{f1}\right)\times 100\%, \\ 1-\left(\frac{e3}{c3}\div\frac{e1}{e1}\right)\times 100\%, 1-\left(\frac{e3}{h3}\div\frac{e1}{h1}\right)\times 100\%, \\ 1-\left(\frac{g3}{f3}\div\frac{g1}{f1}\right)\times 100\%, 1-\left(\frac{g3}{h3}\div\frac{g1}{h1}\right)\times 100\% \end{cases}$$

$$CrossTalk = MAX\{CrossTalk\_White, CrossTalk\_Black\}$$

Note 10: Flicker

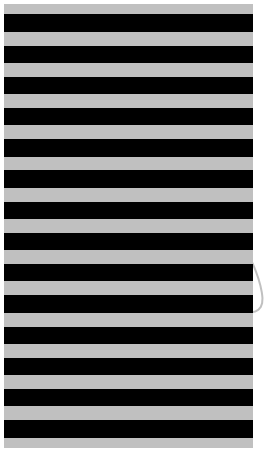
The flicker level is defined using Fast Fourier Transformation (FTT) as follows:

$$Flicker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad \text{(dB)}$$

where fFFTC(n) is the nth FFT coefficient, and fFFTC(0) is the 0th FFT coefficient which is DC component. FS(Hz) is the flicker sensitivity as a function of frequency.

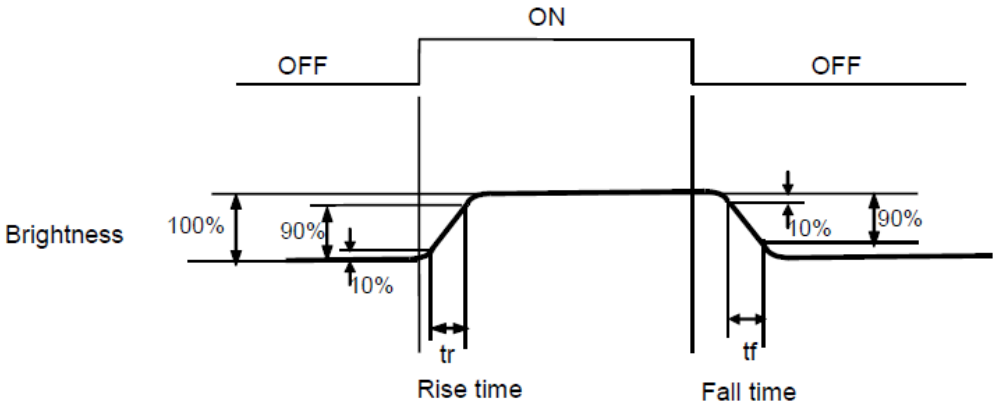
The flicker level shall be measured with the test pattern in below.

The gray leves of test pattern is 128.



Note 11: Optical Switching Time:

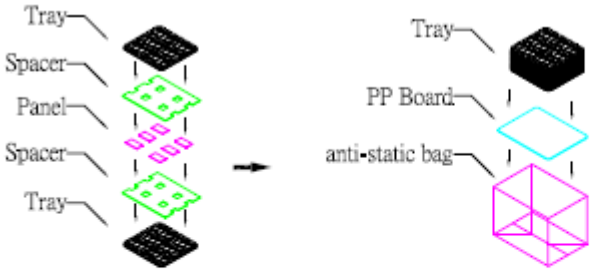
The optical switching time measurements should be performed at driven BLACK and driven WHITE at typ. brightness setting by the driving techniques specified. The luminance should be measured with the emitting display and the detector at θ=0°and ψ=90°. The rise time tr is the time between a 10% optically response of the display and a 90% optically response of the display. The fall time tf is the time between a 10% optically response of the display and a 90% optically response to the display. The response time is defined as the average of the rise time and the fall time.



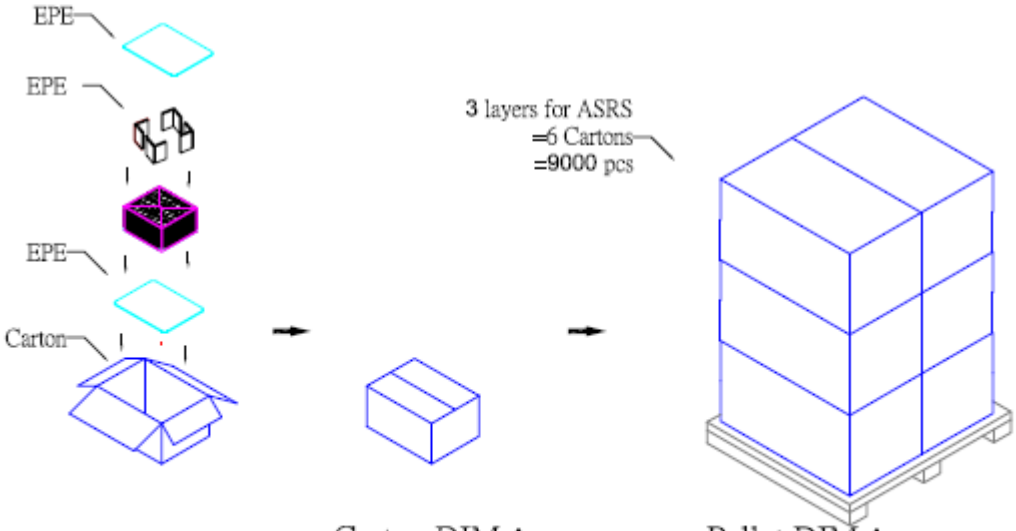
I. Reliability Test Items

Category	No.	Test items	Conditions	Remark
Reliability (Environment)	1	High Temp. Operation	Ta= 60ºC 240hrs	Ta: Ambient temperature.
	2	High Temp. Storage	Ta= 70 ºC 240hrs	Non-operation
	3	Low Temp. Operation	Ta= -20 ºC 240hrs	
	4	Low Temp. Storage	Ta= -30 ºC 240hrs	Non-operation
	5	High Temp./Humi. Operation	Ta= 40 ºC. 95% RH 240hrs	
	6	Thermal Shock	-30 ºC ~70 ºC, Dwell for 30 min. 30 cycles.	Non-operation
	7	Vibration test	Random 1.5G,10~200Hz,30min/axis	Non-operation

J. Packing



1 tray for 60 pcs Panels 1 set for 25+1 pcs trays
=1500 pcs panels



Carton DIM：
715*447*306 mm

Pallet DIM：
980*740*132 mm

K. Outline Demension (Tentative)