16 Gb NAND Flash
H27UAG8T2A

Document Title

16 Gbit (2048 M x 8 bit) NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft.	Jul. 16. 2008	Preliminary
0.1	Deleted ULGA PKG	Feb. 25. 2009	Preliminary
0.2	Changed 1. ICC2 current: Typ 15mA/ Max 30mA => 20mA/40mA 2. Added AC parameter values for cache operation	Mar. 30. 2009	Preliminary
0.3	1. Corrected Table 10 & Table 11. 5th byte of Device Identifier & Data 2. Changed Figure 31 : Power on Reset 3. Corrected Bad Block Management SLC to MLC	Apr. 24. 2009	Preliminary
0.4	Deleted supply voltage for I/O buffer (VCCQ)	Apr. 29. 2009	Preliminary
0.5	1. Corrected 5th cycle command from 34h to 44h at figure28. Read ID operation. 2. Changed tADL. Min. from 200 to 70 at Table 18:AC Timing Characteristics.	Jul. 21. 2009	Preliminary

FEATURES SUMMARY

HIGH DENSITY NAND FLASH MEMORIES

- Cost effective solutions for mass storage applications

MULTIPLANE ARCHITECTURE

- Array is split into two independent planes. Parallel operations on both planes are available, halving program, read and erase time.

NAND INTERFACE

- x8 bus width.
- Address / Data Multiplexing
- Pin-out compatibility for all densities

SUPPLY VOLTAGE

- 3.3 V device : Vcc = 2.7 V ~ 3.6 V

MEMORY CELL ARRAY

- (4 K + 224) bytes x 128 pages x 4096 blocks

PAGE SIZE

- (4 K + 224 spare) Bytes

BLOCK SIZE

- (512 K + 28 K spare) Bytes

PAGE READ / PROGRAM

- Random access : 60 us (max.)
- Sequential access : 25 ns (min.)
- Page program time : 800(TBD) us (typ.)
- Multi-Plane Program time (2 pages) : 800(TBD) us (typ.)

FAST BLOCK ERASE

- Block erase time: 2.5ms (typ.)
- Multi-Block Erase time (2 blocks) : 2.5ms (typ.)

CACHE PROGRAM

- Internal (4K + 224) bytes data buffer to improve program throughput

CACHE READ

- Automatic block download without latency time

ELECTRONIC SIGNATURE

- 1st cycle : Manufacturer Code
- 2nd cycle : Device Code
- 3rd cycle : Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
- 4th cycle : Page size, Block size, Organization, Spare size
- 5th cycle : Multiplane Information
- 6th cycle : Technology (Design Rule), EDO, Interface

COPY BACK PROGRAM

- Fast Data Copy without external buffer
- Multi-plane copy-back program

CHIP ENABLE DON'T CARE

- Simple interface with microcontroller

STATUS REGISTER

- Normal Status Register (Read/Program/Erase)

HARDWARE DATA PROTECTION

- Program/Erase locked during Power transitions.

DATA RETENTION

- 5,000 Program/Erase cycles
  (with 12 bit / 528 byte ECC)
- 10 years Data Retention

PACKAGE

- H27UAG8T2ATR
  : 48-pin TSOP1(12 x 20 x 1.2 mm)
  - H27UAG8T2ATR (Lead & Halogen free)

1. SUMMARY DESCRIPTION

The H27UAG8T2A is a 2048Mx8bit with spare 116Mx8 bit capacity. The device is offered with 3.3V Vcc Core Power Supply and 3.3V Input-Output Power Supply.

Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 4096 blocks, composed by 128 pages consisting in two NAND structures of 32 series connected Flash cells. Every cell holds two bits.

Like all other 4 KB page NAND Flash devices, a program operation allows to download 4,320 bytes of the page into the page register in 60 usec (max), write the 4,320 byte page in typical 800us, and erase one (512K+28k) byte block in 2.5ms (typ).

Thanks to multi-plane architecture, it is possible to read 2 pages, or program 2 pages or to erase 2 blocks at a time; the two pages/blocks belong to the two different physical planes of the array. As a consequence, multi-plane architecture increase memory throughput .

Data in the page can be read out or input in the internal register at the following speeds, 25nsec per byte.

The I/O pins serve as the ports for address and data input / output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, ALE and CLE input pin. The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the WP Input.

The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation.

In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal.

The chip supports $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.

The copy-back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase; however, source page data download is possible after copyback read, thus bit manipulation prior to program to the target page is allowed.

The cache program feature is implemented; it allows data insertion in the cache register while the data register is copied into the flash array. This pipelined program operation improves the program throughput when long files are written inside the memory.

The cache program feature is supported also in multi-plane , in order to further increase device performance.

The cache read feature is also implemented. This feature allows to dramatically improve read throughput when consecutive pages have to be streamed out.

The cache read feature is supported also in multi-plane , in order to further increase device performance.

Even the write-intensive systems can take advantage of the H27UAG8T2A extended reliability of 5 K program/erase cycles by providing 12 bit / 512byte ECC (Error Correcting Code) with real time mapping-out algorithm.

This device includes also extra Features like OTP/Unique ID area, Read ID2 extension.

The H27UAG8T2A is available in the following packages: TSOP48 (12x20)

1.1 Product List

PART NUMBER	ORGANIZATION	Vcc RANGE	PACKAGE
H27UAG8T2A	x8	2.7V ~ 3.6V	48-TSOP1

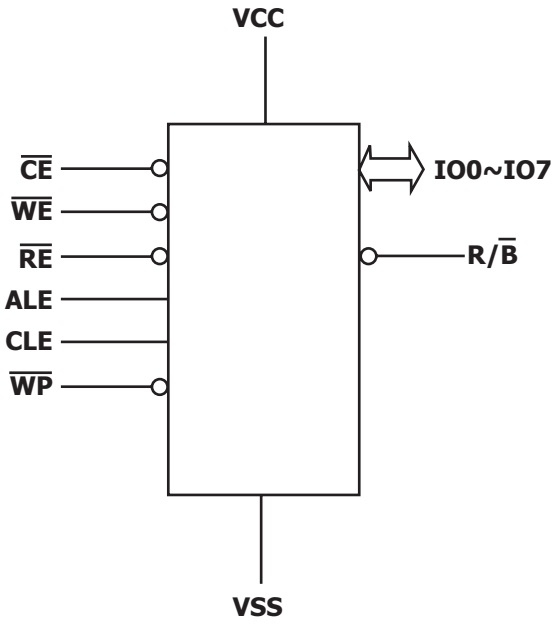


Figure 1 : Logic Diagram

IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Table 1 : Signal Names

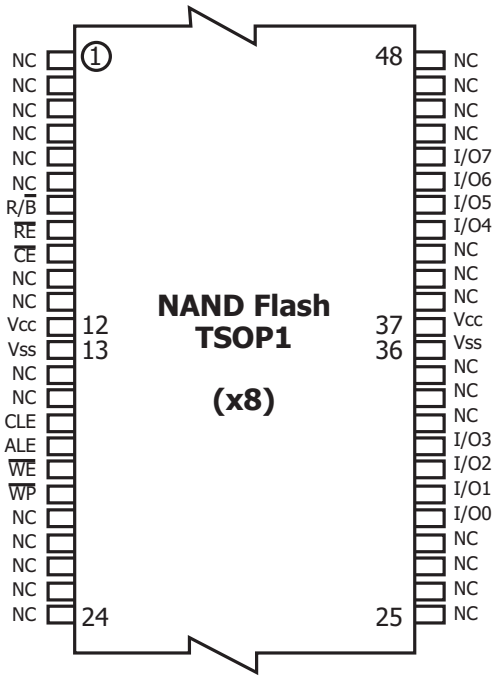


Figure 2 : 48-TSOP1 Contact, x8 Device

1.2 PIN DESCRIPTION

Pin Name	Description
IO0 ~ IO7	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$	**CHIP ENABLE** This input controls the selection of the device.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B}$	**READY BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
Vcc	**SUPPLY VOLTAGE** The Vcc supplies the power for all the operations (Read, Write, Erase).
Vss	**GROUND**
NC	**NO CONNECTION**

Table 2 : Pin Description

NOTE :

1. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

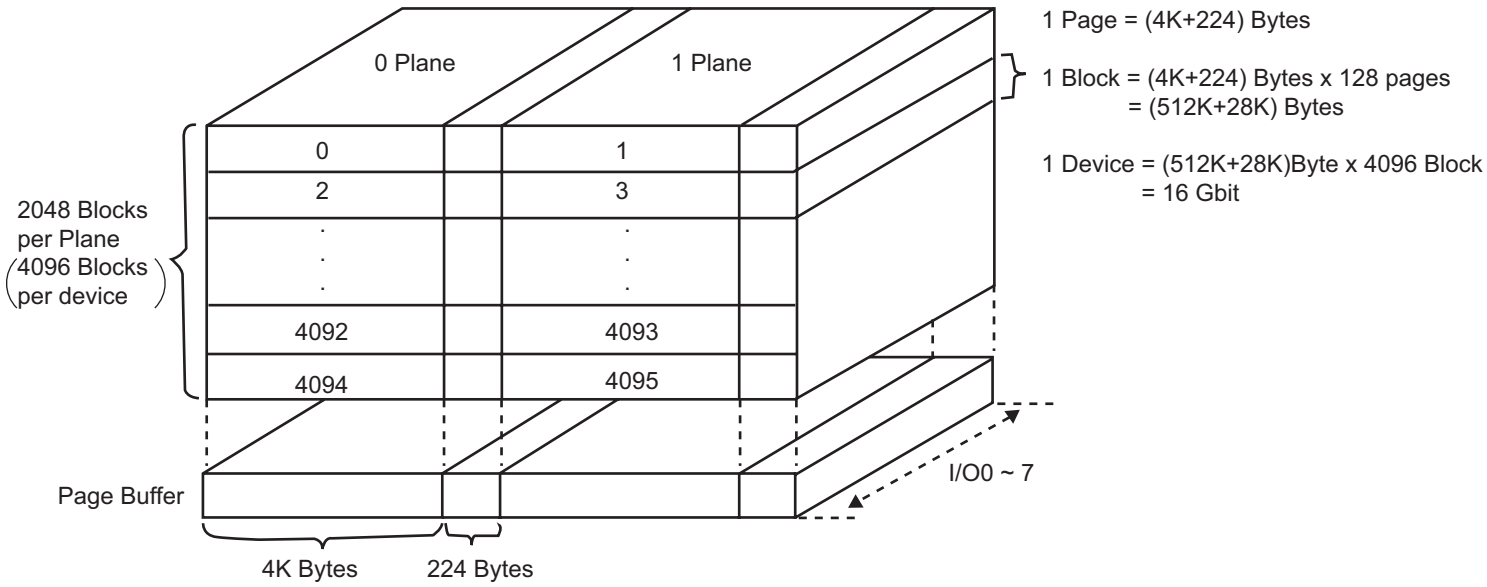


Figure 3 : Array Organization

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	A12	L(1)	L(1)	L(1)
3rd Cycle	A13	A14	A15	A16	A17	A18	A19	A20
4th Cycle	A21	A22	A23	A24	A25	A26	A27	A28
5th Cycle	A29	A30	A31	L(1)	L(1)	L(1)	L(1)	L(1)

Table 3 : Address Cycle Map

NOTE:

1. L must be set to Low.
2. the device ignores any additional input of address cycles than required
3. Row address consists of page address (A13-A19) & Plane address (A20) & Block Address (A21 - the last address)

FUNCTION	1st	2nd	3rd	4th	Acceptable Command During Busy
PAGE READ	00h	30h	-	-	
MULTI-PLANE READ	60h	60h	30h	-	
MULTI-PLANE CACHE READ START	60h	60h	33h	-	
SINGLE/MULTI PLANE CACHE READ	31h	-	-	-	
SINGLE/MULTI PLANE CACHE READ END	3Fh	-	-	-	
RANDOM DATA OUTPUT	05h	E0h	-	-	
PAGE PROGRAM (START) /CACHE PROGRAM (END)	80h	10h	-	-	
RANDOM DATA INPUT	85h	-	-	-	
BLOCK ERASE	60h	D0h	-	-	
READ FOR COPY-BACK	00h	35h	-	-	
COPY BACK PROGRAM	85h	10h	-	-	
CACHE PROGRAM (START)	80h	15h	-	-	
READ STATUS REGISTER	70h	-	-	-	YES
MULTI-PLANE PAGE PROGRAM / MULTI-PLANE CACHE PROGRAM (END)	80h	11h	81h	10h	
MULTI-PLANE BLOCK ERASE	60h	60h	D0h	-	
MULTI-PLANE READ FOR COPY BACK	60h	60h	35h	-	
MULTI-PLANE COPY BACK PROGRAM	85h	11h	81h	10h	
MULTI-PLANE CACHE PROGRAM (START)	80h	11h	81h	15h	
MULTI-PLANE DATA OUTPUT	00h	05h	E0h	-	
MULTI-PLANE READ STATUS REGISTER	F1h	-	-	-	YES
READ ID	90h	-	-	-	
RESET	FFh	-	-	-	YES

Table 4 : Command Set

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input (5 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input (5 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L	H	Falling	X	Data Output	
X	X	X	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0 V / Vcc	Stand By	

NOTE : With the $\overline{CE}$ don't care option $\overline{CE}$ high during latency time does not stop the read operation

Table 5 : Mode Selection

1. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Typically glitches less than 5ns on Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover, for commands that start a modifying operation (write/erase) the Write Protect pin must be high. See Figure 5 and Table 18 for details of the timings requirements. Command codes are always applied on IO<7:0>, disregarding the bus configuration.

2.2 Address Input

Address Input bus operation allows the insertion of the memory address. Five cycles are required to input the addresses for the 16 G bit devices. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable high and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 6 and Table 18 for details of the timings requirements. Addresses are always applied on IO(7:0), disregarding the bus configuration.

In addition, addresses over the addressable space are disregarded even if the user sets them during command insertion.

2.3 Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See

Figure 7 and Table 18 for details of the timings requirements.

2.4 Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See figures 8, 9, 10,11, 12, 13, 14 and Table 18 for details of the timings requirements.

2.5 Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up phases.

2.6 Standby

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced. Stand-by is obtained holding $\overline{CE}$ pin high at least for 10us.

3. DEVICE OPERATION

3.1 Page Read

Upon initial device power up, the device defaults to page read mode. This operation is also initialized by 00 h to the command register along with followed by five address input cycles. In consecutive read operations, 00h command is needed for the following page read operations.

Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 4,320 bytes of data within the selected page are transferred to the data registers in less than 60us (tR). The system controller may detect the completion of this data transfer by either checking the R/$\overline{B}$ pin level, or issuing the Read Status Register commands (70h or F1h) and monitoring IO<6> (ready/busy) through $\overline{RE}$ toggling. In the latter case, the device will keep on outputting the Read Status until the command 00h is issued .

Once the data in a page is loaded into the data registers, they may be read out by sequentially pulsing $\overline{RE}$ (every 25nsec) The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

3.2 Multi Plane Read

Multi-Plane Page Read is an extension of Page Read, for a single plane with 4,320 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 4,320 byte page resisters enables a random read of two pages. Multi-Plane Page Read is initiated by repeating command 60h followed by three address cycles twice. In this case only same page of same block can be selected from each plane, as shown in Figure 14.

After Read Confirm command (30h) the 8,640 bytes of data within the selected two pages are transferred to the data registers in less than 60us (tR). The system controller may detect the completion of this data transfer by either checking the R/$\overline{B}$ pin level, or issuing the Read Status Register commands (70h or F1h) and monitoring IO<6> (ready/busy) through $\overline{RE}$ toggling. In the latter case, the device will keep on outputting the Read Status until the command 00h is issued .

Once the data is loaded into the data registers, the data output of first plane can be read out by issuing command 00h with Five Address Cycles (A20=0), command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences (but with A20=1).

Grey area :

a) the device allows to revert the order of the two pages at all times (first read from plane 1 (A20=1) and then from plane0 (A20=0).

b) Multi-Plane Page Read is allowed also in the blocks which have NOT been programmed with Multi-Plane Page Program.

3.3 Page Program

The device is programmed by page. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 times. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 4,320 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will initiate the programming process anyway. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register.

The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit I/O<6> (busy/ready bit) of the Status Register (70h or F1h). Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit I/O<0> (pass/fail) may be checked.

The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s.

The command register remains in Read Status command mode until another valid command is written to the command register. Figure 15 details the sequence.

NOTE : the device support program operation with 2kByte data to offer the backward compatibility to the controller which uses the Nand with 2Kbyte page.

3.4 Multi Plane Program

Device supports multiple-plane program: it is possible to program in parallel 2 pages, one per each plane. Page and block address for the two pages must be the same .

A multiple plane program cycle consists of a double serial data loading period in which up to 8,640bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A<20>=0). The data of 1st page other than those to be programmed do not need to be loaded.

The device supports random data input exactly like page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).

Once it has become ready again, 81h command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (A<20>=1);the data of 2nd page other than those to be programmed do not need to be loaded.

Program Confirm command (10h) initiates parallel programming of both pages .

User can check operation status by R/$\overline{B}$ pin or read status register commands (70h or F1h).

If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes (IO<6>= ready / busy, IO<0> = pass / fail)

If user opts for F1h, Status register read will provide information about the operation in each of the two planes (IO<0> : Global pass/fail, IO<1>: Plane0 pass/fail, IO<2>: Plane1 pass/fail).

Please note that only Reset (FFh) or Status register commands (70h / F1h) can be issued during Dummy Busy time (tDBSY); in the latter case please refer to Status register command section for further information.

Multi-plane program sequence is described in Figure 16.

Grey area :

a) Please note that page and block address for the pages in the two planes must be the same. If the user fails to do so the device will program the data in location based on the page and block address of the page issued during the sequence 81h - 10h.

b) plane order in the command sequence can be swapped; in other words, user may input first the data of the page in plane 1 (A20=1) and then the data of the corresponding page in plane 0 (A20=0)

3.5 Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only addresses A20 to A32 are valid while A13 to A19 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify.

Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/$\overline{B}$ output, or the Status bit I/O<6> (ready/busy) of the Status Register (commands 70h or F1h). Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit I/O<0> (pass/fail)) may be checked.

Figure 18 details the sequence.

3.6 Multi Plane Erase.

Multiple plane erase, allows parallel erase of two block, one per each memory plane.

Block erase setup command (60h) must be repeated two times, each time followed by 1st block and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. Multi plane erase does not need any Dummy Busy Time between 1st and 2nd block address insertion.

Block address for the two blocks must be the same

User can check operation status by R/$\overline{B}$ pin or read status register commands (70h or F1h).

If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes (IO<6>= ready / busy, IO<0> = pass / fail)

If user opts for F1h, Status register read will provide information about the operation in each of the two planes (IO<0> : Global pass/fail, IO<1>: Plane0 pass/fail, IO<2>: Plane1 pass/fail)

Multi-plane erase sequence is described in Figure 19.

Grey area :

a) Please note that the block address in the two planes must be the same. If the user fails to do so the device will erase the data in location based on the block address issued last (during the sequence 60h - D0h).

b) plane order in the command sequence can be swapped; in other words, sequences such as
60h <block address (A20=1)> 60h <block address (A20=0)> D0h Or
60h <block address (A20=0)> 60h <block address (A20=1)> D0h are both accepted .

3.7 Copy-Back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block.

Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 4,320-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit I/O<6> of the Status Register (commands 70h or F1h) . When the Copy-Back Program is complete, the Write Status Bit(I/O<0>) may be checked (Figure 20 & Figure 21). The command register remains in Read Status command mode until another valid command is written to the command register.

During copy-back program, data modification is possible using random data input command (85h) as shown in.

Copy-Back is allowed only within the same memory plane .

NOTE : the device support copy back program operation with 2kByte data to offer the backward compatibility to the controller which uses the Nand with 2Kbyte page.

3.8 Multi-Plane Copy-Back Program

Two-Plane Copy-Back Program is an extension of Copy-Back Program for a single plane with 4,320 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 4,320 byte page registers enables a simultaneous programming of two pages.

The first step for Multi-Plane Copy Back is to perform Multi-plane read for copyback, by repeating command 60h followed by three address cycles twice. In this case only the same page of same block can be selected from each plane.

After Read Confirm command (35h) the 8,640 bytes of data within the selected two pages are transferred to the data registers in less than 60us (tR). The system controller may detect the completion of this data transfer by either checking the R/$\overline{B}$ pin level, or issuing the Read Status Register commands (70h or F1h) and monitoring IO<6> (ready/busy) through $\overline{RE}$ toggling. In the latter case, the device will keep on outputting the Read Status until another valid command is written to the command register.

Once the data is loaded into the data registers, the data output of first plane can be read out by issuing command 00h with Five Address Cycles (with A20=0), command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences (this time with A20=1).

The sequence 60h-60h-35h is allowed also in the blocks which have NOT been programmed with Multi-Plane Page Program.

In the case where there is no bit error, the data do not need to be reloaded.

The second step for Multi-Plane copy back is to perform Multi-plane copyback program.The operation is initiated by issuing Page-Copy Data-Input command (85h) followed by the five cycle address cycles for destination page in the first plane. Address for this page must be within 1st plane (A<20>=0).

The device supports random data input exactly as the page program operation.

The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).

Once it has become ready again, 81h command must be issued, followed by 2nd page address (5 cycles) . Address for this page must be within 2nd plane (A<20>=1). Again, random data input is allowed during this phase

Program Confirm command (10h) initiates the parallel programming of both pages.

User can check operation status by R/$\overline{B}$ pin or read status register commands (70h or F1h).

If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes (IO<6>= ready / busy, IO<0> = pass / fail)

If user opts for F1h, Status register read will provide information about the operation in each of the two planes (IO<0> : Global pass/fail, IO<1>: Plane0 pass/fail, IO<2>: Plane1 pass/fail)

Status register commands can be issued during Dummy Busy time (tDBSY); Please refer to Status register command section for further information.

Copy-Back is allowed only within the same memory plane .

Figure 22 describes the command sequence for the multi-plane copy-back operation; it refers to controllers which can handle 8k bytes of data : in this case the copy back program sequence 85h is issued after finishing random data output of the source pages is complete.

NOTE : the device support copy-back program operation with 4kByte data to offer the backward compatibility to the controller which uses the Nand with 2Kbyte page.

Grey area :

a) Multi-Plane Page Read for copy-back is allowed also in the blocks which have NOT been programmed with Multi-Plane Page Program.
b) during the copy-back program , page and block address for the pages in the two planes must be the same. If the user fails to do so the device will program the data in location based on the page and block address of the page issued during the sequence 81h - 10h.
c) plane order in the command sequence can be swapped; in other words, user may input first the page in plane 1 (A20=1) and then the the corresponding page in plane 0 (A20=0). This is allowed both during Multi-Plane Page Read for copy-back and Multi-plane copy back program sequences.
d) any command between 11h and 81h is prohibited except 70h, F1h and FFh

3.9 Cache Read

Cache Read is an extension of Page Read,which is available only within a block. Since the device has one cache register, serial data output may be executed while data in the memory is read into cache register,

Cache Read is initiated by the page read sequence (00-30h).

After random access to the first page is complete (R/$\overline{B}$ returned to high), 31h command can be latched into the command register. At this time, data of the first page is transferred from the data register to the cache register, while device goes busy for short time (tCBSYR)

At the end of this phase cache register data can be output by toggling $\overline{RE}$ while the next page is read from the memory array into data register.

Subsequent pages are read by issuing additional 31h command sequences.

If serial data output time of one page exceeds random access time (tR), the random access time of the next page is hidden by data downloading of the previous page.

On the other hand, if 31h is issued prior to complete the random access to the next page, the device will stay busy as long as needed to complete random access to this page, transfer its contents into the cache register, and trigger the random access to the following page.

To terminate cache read, 3Fh command should be issued. This command transfer data from data register to the cache register without issuing next page read.

During the Cache Read Operation, device doesn't allow any other command except of 31h and 3Fh or Read SR.

To carry out other operations Cache read must be ended either by 3Fh command or device must be reset by issuing FFh.

Read Status command (70h) may be issued to check the status of the different registers, and the busy/ready status of the cached read operations. More in detail:

a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to output new data.

b) the status bit I/O<5> can be used to determine when the cell reading of the current data register contents is complete

See Table 8 and Figure 24 for more details.

3.10 Multi Plane Cache Read

Multi-Plane Cache Read is an extension of Cache Read, and is available only within two paired blocks belonging to the two planes. Since the device has one cache register in each plane, serial data output from the data registers of the two planes may be executed while data in the memory is read into the cache registers,

Multi-Plane Cache Read is initiated by the following sequence :

a) 60h followed by three address cycles of the page of the first plane

b) 60h followed the three address cycles of the corresponding page of the second plane

c) 33h (confirm cycle)

After random access to the first pages is complete (R/$\overline{B}$ returned to high), 31h command can be latched into the command register. At this time, data of the first pages is transferred from the data registers to the cache registers, while device goes busy for short time (tCBSYR) .

At the end of this phase cache register data of the first page can be output by issuing the following sequence :

a) 00h followed by the five address cycles related to this page

b) 05h followed by two address cycles related to the column address to start the read out

c) E0h, followed by toggling $\overline{RE}$

Similarly the cache register data of the second page can be output by issuing the following sequence :

d) 00h followed by the five address cycles related to this page

e) 05h followed by two address cycles related to the column address to start the read out

f) E0h, followed by toggling $\overline{RE}$

Subsequent pages are read from the memory array into the data registers by issuing additional 31h command sequences.

If serial data output time of the two pages exceeds random access time (tR), the random access time of the next pages is hidden by data downloading of the previous pages.

On the other hand, if 31h is issued prior to complete the random access to the next pages, the device will stay busy as long as needed to complete random access to these pages, transfer their contents into the cache register, and trigger the random access to the following pages.

To terminate cache read, 3Fh command should be issued. This command transfer data from data registers to the cache registers without issuing next page read.

During the Cache Read Operation, device doesn't allow any other command except of 31h and 3Fh or Read SR.

To carry out other operations Cache read must be ended either by 3Fh command or device must be reset by issuing FFh.

User can check operation status by R/$\overline{B}$ pin or read status register commands (70h or F1h).

More in detail:

a) I/O<6> indicates when both cache registers are ready to output new data.

b) I/O<5> indicates when the cell reading of the current data registers is complete

See Table 8 and Table 9 for more details

Figure 25 shows the command sequence for the multi-plane cache read operation.

Grey area :

a) Please note that page and block address for the pages in the two planes must be the same. If the user fails to do so the device will read the data in location based on the page and block address of the last page issued during the sequence 60h - 60h - 33h.

b) plane order in the command sequence 60h - 60h - 33h can be swapped; in other words, user may input first the address of the page in plane 1 (A20=1) and then the data of the corresponding page in plane 0 (A20=0).

c) plane order in the command sequence for data readout (00h - 05h - E0h) can be swapped. in other words, user may output first the address of the page in plane 1 (A20=1) and then the data of the corresponding page in plane 0 (A20=0).

3.11 Cache program

Cache Program is an extension of the standard page program which is executed with two 4,320 bytes registers, the data and the cache register.

In short, the cache program allows data insertion for one page while program of another page is under execution.

Cache program is available only within a block

After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register.

Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state For a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h).

The Busy time following the first sequence 80h - 15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model.

In case of any subsequent sequence 80h - 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state (tCBSYW usec).

Read Status command (70h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations. More in detail:

a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.

b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete

c) the cache program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O<6> status bit changing to "1" .

d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while programming page N. The latter can be polled upon I/O<5> status bit changing to "1".

I/O<1> may be read together with I/O<0> .

If the system monitors the progress of the operation only with R/$\overline{B}$, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

See Table 8 and Figure 26 for more details.

3.12 Multi Plane Cache program

The device supports multi-plane cache program, which enables high program throughput by programming two pages in parallel while exploiting the data and cache registers of both planes to implement cache.

The command sequence can be summarized as follows :

a) Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A<20>=0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation.
b) The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).
c) Once device returns to ready again, 81h command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (A<20>=1). The data of 2nd page other than those to be programmed do not need to be loaded.
d) Cache Program confirm command (15h) Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence.

The sequence 80h-...- 11h...-...81h...-...15h can be iterated, and any new time the device will be busy for a for the tCBSYW time needed to complete cell programming of current data registers contents, and transfer from cache registers can be allowed.

The sequence to end multi-plane cache program is 80h-...- 11h...-...81h...-...10h .

Figure 27 shows the command sequence for the multi plane cache program operation.

Multi-plane Cache program is available only within two paired blocks belonging to the two planes..

Grey area :

a) page and block address for the pages in the two planes must be the same. If the user fails to do so the device will program the data in location based on the page and block address of the page issued during the sequence 81h - 15h (or 81h - 10h)
b) plane order in the command sequence can be swapped; in other words, user may input first the data of the page in plane 1 (A20=1) and then the data of the corresponding page in plane 0 (A20=0)

User can check operation status by R/$\overline{B}$ pin or read status register commands (70h or F1h).

If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes . More in detail:

a) I/O<6> indicates when both cache registers are ready to accept new data.
b) I/O<5> indicates when the cell programming of the current data registers is complete
c) I/O<1> identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. The latter can be polled upon I/O<6> status bit changing to "1" .
d) I/O<0> identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O<5> status bit changing to "1".

See Table 8 for more details.

If user opts for F1h, Status register read will provide information about the operation in each of the two planes . More in detail :

a) I/O<6> indicates when both cache registers are ready to accept new data.
b) I/O<5> indicates when the cell programming of the current data registers is complete
c) I/O<0> identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O<5> status bit changing to "1".
d) I/O<1> is the pass/fail flag for current page (N) programming in plane0
e) I/O<2> is the pass/fail flag for current page (N) programming in plane1

Both d) and e) can be polled upon I/O<5> status bit changing to "1".

f) I/O<3> is the pass/fail flag for the previous page (N-1) programming in plane0
g) I/O<2> is the pass/fail flag for the previous page (N-1) programming in plane1

Both f) and g) can be polled upon I/O<6> status bit changing to "1".

If the system monitors the progress of the operation only with R/$\overline{B}$, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.
Refer to the Read Status Register section for further information.

See Table 9 for more details

3.13 Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h or F1h (multi-plane read status command) command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status.
The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.
User can check operation through two different read status register commands (70h or F1h).
If user opts for 70h, Status register read will provide a "global" information about the operation in the device ; more precisely, during a multi-plane each status register bit of Status register read command (70h) provides a combined information (OR or AND) of the events occurring in the two planes .

The table below summarizes the logic function for each 70h Status register bit in a multi-plane operation :

Status Register Bit	Logic combination between planes
IO<0>	OR
IO<1>	OR
IO<5>	AND
IO<6>	AND

Table 6 below describes the meaning of each Status Register bit

IO	Program	Erase	Read	Cache Read	Cache Program	Coding 70h
0	Pass / Fail	Pass / Fail	NA	NA	Pass / Fail	N page : Pass : '0' Fail : '1'
1	NA	NA	NA	NA	Pass / Fail	N -1 page : Pass : '0' Fail : '1'
2	NA	NA	NA	NA	NA	-
3	NA	NA	NA	NA	NA	-
4	NA	NA	NA	NA	NA	-
5	NA	NA	NA	Ready/Busy	Ready/Busy	Ready/Busy Busy: '0' Ready: '1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : '0', Not Protected : '1'

Table 6 : Normal (70h) Read Status Register Coding

NOTE : I/Os defined as NA are recommended to be masked out when Read Status is being executed.
If user opts for F1h, Status register read will provide additional information about multi-plane operations, as it allows to check the outcome of the operation in each of the two planes .

Table 7 describes the meaning of each Status Register bit during "non cached" multiplane operations, while Table 8 refers to the Cached multi-plane ones

IO	Multi-plane Page Program	Multi-plane Block Erase	Multi-plane Read	Coding : F1h
0	Pass / Fail	Pass / Fail	NA	Pass : '0' Fail : '1'
1	Pass / Fail	Pass / Fail	NA	Plane0 : Pass : '0' Fail : '1'
2	Pass / Fail	Pass / Fail	NA	Plane1 : Pass : '0' Fail : '1'
3	NA	NA	NA	-
4	NA	NA	NA	-
5	NA	NA	NA	-
6	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Write Protect	Protected : '0' Not Protected : '1'

Table 7 : Multi-plane Read Status Register Coding (non cached operations)

NOTE : I/Os defined as NA are recommended to be masked out when Read Status is being executed.

IO	Multi-plane Page Program	Multi-plane Block Erase	Coding : F1h
0	Pass / Fail	NA	Pass : '0' Fail : '1'
1	Pass / Fail	NA	N page / Plane 0 Pass : '0' Fail : '1'
2	Pass / Fail	NA	N page / Plane 1 Pass : '0' Fail : '1'
3	Pass / Fail	NA	N-1 page / Plane 0 Pass : '0' Fail : '1'
4	Pass / Fail	NA	N-1 page / Plane 1 Pass : '0' Fail : '1'
5	Ready / Busy	Ready / Busy	Ready/Busy Busy : '0' Ready : '1'
6	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Protected : '0' Not Protected : '1'

Table 8 : Multi-plane Read Status Register Coding (cached operations)

NOTE : I/Os defined as NA are recommended to be masked out when Read Status is being executed.

3.14 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.

Six read cycles sequentially output the manufacturer code (Numonyx), the device code and 3rd, 4th, 5th, 6th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it.

Figure 28 shows the operation sequence, while Table 9, Table 10 and Table 11 explain the byte meaning.

Parameter	Symbol
Device Identifier Byte	Description
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell Type, Number of Simultaneously Programmed Pages, Interleaved Program, Write Cache.
4th	Page size, Block size, Redundant area size
5th	Plane Number, ECC Level
6th	Technology (Design Rule), EDO, Interface

Table 9 : Device Identifier Coding

3rd cycle	Description	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
Internal Chip Number	1 2 4 Reserved							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleaved Program between Multiple dice	Not Supported Supported		0 1						
Write Cache	Not Supported Supported	0 1							

Table 10 : 3rd, 4th, 5th and 6th byte of Device Identifier

4th cycle	Description	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
Page Size	2 KB							0	0
	4 KB							0	1
	8 KB							1	0
	Reserved							1	1
Block Size	128 KB	0		0	0				
	256 KB	0		0	1				
	512 KB	0		1	0				
	768 KB	0		1	1				
	1 MB	1		0	0				
	Reserved	1		0	1				
	Reserved	1		1	0				
	Reserved	1		1	1				
Redundant Area Size	128 B		0			0	0		
	224 B		0			0	1		
	Reserved		0			1	0		
	Reserved		0			1	1		
	Reserved		1			0	0		
	Reserved		1			0	1		
	Reserved		1			1	0		
	Reserved		1			1	1		

5th cycle	Description	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
ECC Level	1 bit / 512 Bytes		0	0	0				
	2 bit / 512 Bytes		0	0	1				
	4 bit / 512 Bytes		0	1	0				
	8 bit / 512 Bytes		0	1	1				
	12 bit / 512 Bytes		1	0	0				
	16 bit / 512 Bytes		1	0	1				
	Reserved		1	1	0				
	Reserved		1	1	1				
Reserved		0						0	0

6th cycle	Description	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
NAND Technology	48 nm						0	0	0
	41 nm						0	0	1
	Reserved						0	1	0
	Reserved						0	1	1
	Reserved						1	0	0
	Reserved						1	0	1
	Reserved						1	1	0
	Reserved						1	1	1
EDO Support	Not Support		0						
	Support		1						
NAND Interface	SDR	0							
	DDR	1							
Reserved				0	0	0			

Part Number	VCC	Bus Width	Manufacture Code	Device Code	3rd	4th	5th	6th
H27UAG8T2A	3.3V	X8	ADh	D5h	94h	25h	44h	41h

Table 11 : Read ID Data Table

3.15 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased.

After a Reset command is issued to, the R/$\overline{B}$ pin will stay low for tRST as explained in Figure 29. At the end of this time, the command register is ready to process the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high.

Refer to Table 6 for device status after reset operation.

If the device is already processing a reset, another reset command will not be accepted by the command register .

4. OTHER FEATURES

4.1 Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions.

An internal voltage detector disables all functions whenever the power supply (supplies) are below about 2.0V(3.3V device).

$\overline{WP}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down.

The Ready/Busy signal shall be valid within 100us since the power supplies have reached the minimum values (as specified on Table 14), and shall return to one within 5msec (max) .

The power-up and power-down sequence is shown in Figure 30.

During this busy time, the device can accept Read Status Register commands (70h or F1h). At the end of this busy time, the device is ready to accept any other command sequences,

The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/ Busy

The Ready/Busy output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process, and returns to high state upon completion.

The pin is an open-drain driver thereby allowing the R/$\overline{B}$ outputs of two or more devices to be shorted in a "wired-or" configuration.

As the pull-up resistor value is related to tR (R/$\overline{B}$) and current drain during busy (Ibusy), an appropriate value can be obtained with the reference chart in Figure 32. Its value can be determined by the guideline detailed in the figure.

4.3 Initialization after power up

After power-up, a reset command must be issued before any other command. As opposed to usual reset commands, this first reset command issues an initialization process on the device. The device stays busy for a maximum of 5ms and consumes a maximum of 40mA current during this process. 70h and F1h (Read Status Register) are the only commands allowed during this initialization process.

4.4 Write Protect ($\overline{WP}$) handling

Erase and program operations are aborted if $\overline{WP}$ is driven low during busy time, and kept low for about 100 nsec.
Switching $\overline{WP}$ low during this time will be equivalent to issuing a Reset command (FFh)
The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased.
The R/$\overline{B}$ pin will stay low for tRST. At the end of this time, the command register is ready to process the next command, and the Status Register bit IO<6> will be cleared to "1", while IO<7> value will be related to the $\overline{WP}$ value.
Refer to Table 7 for more information on device status.

Erase and program operations are enabled or disabled by setting $\overline{WP}$ to high or low respectively prior to issuing the set-up commands (80h or 60h) .
The level of $\overline{WP}$ shall be set tWW nsec prior to raising the $\overline{WE}$ pin for the set up command, as explained in Figure 35, 36, 37 and 38.

Grey area :
Switching $\overline{WP}$ to VIL during any cycle (command, address or data) of a program or erase command sequence will abort the sequence .

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	3996		4096	Blocks

Table 12 : Valid Blocks Number

NOTES :
1. the device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.
3. the number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	°...
	Ambient Operating Temperature (Extended Temperature Range)	-25 to 85	°...
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	°...
T_{BIAS}	Temperature Under Bias	-50 to 125	°...
T_{STG}	Storage Temperature	-65 to 150	°...
V_{IO}	Input or Output Voltage	-0.6 to 4.6	V
V_{CC}	Supply Voltage	-0.6 to 4.6	V

Table 13 : Absolute maximum ratings

NOTES:
1. Stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

Parameter		Symbol	Test Condition	VCC = 3.0V (1,2)			Unit
				Min	Typ	Max	
Core and I/O Supply voltage		Vcc	-	2.7	3.3	3.6	V
Power on reset current		Icc0	FFh COMMAND input after power on	-	15	30	mA
Power on reset current	Read	Icc1	tRC=25ns CE=VIL, Iout=0mA	-	15	30	mA
	Program (Normal)	Icc2		-	15	30	mA
	Program (Cache)	Icc2		-	20	40	mA
	Erase	Icc3		-	15	30	mA
Stand-by Current (TTL)		Icc4	$\overline{CE}$=VIH, $\overline{WP}$=0V/Vcc	-	-	1	mA
Stand-by Current (CMOS)		Icc5	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc max	-	-	±10	uA
Output Leakage Current		ILO	Vout=0 to Vcc max	-	-	±10	uA
Input High Voltage		VIH	-	Vccx0.8	-	Vcc+0.3	V
Input Low Voltage		Icc0	-	-0.3	-	0.2xVcc	V
Output High Voltage Level		VOH	IOH=-400uA	2.4	-	-	V
Output Low Voltage Level		VOL	IOL=2.1mA	-	-	0.4	VC
Output Low Current (R/$\overline{B}$)		IOL(R/$\overline{B}$)	VOL=0.4V	8	10	-	mA

Table 14 : DC and Operating Characteristics

NOTES :

1. Measurements are performed with a 0.1uF capacitor connected between the Vcc Supply Voltage pin and the Vss Ground pin

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc / 2
Output Load (1.7 V – 1.95Volt & 2.7V-3.6V)	1 TTL GATE and CL=50pF

Table 15 : AC Conditions

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	-	10	pF
$C_{I/O}$	Input/Output Capacitance	V_{IL} = 0V	-	10	pF

Table 16 : Pin Capacitance (TA = 25 F = 1.0 MHz)

MLC VERSION					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Random Page read	tR			60	us
Program (following 10h)	t_{PROG}	-	800(TBD)	2000	us
Cache Program (following 15h)	t_{CBSYW}	-	-	2000(TBD)	us
Multi-Plane Program / Multi-Plane Cache Program / Multi-Plane Copy-Back Program (following 11h)	t_{DBSY}	-	3	5	us
Cache Read / Multi-Plane Cache Read	t_{CBSYR}		3	60	us
Block Erase / Multi-Plane Block Erase	t_{BERS}	-	2.5	10	ms
Number of partial Program Cycles in the same page	NOP	-	-	1	cycles

Table 17 : Program / Read / Erase Characteristics for the MLC version.

Parameter	Symbol	3.3V		Unit
		Min	Max	
CLE setup time(Non-Cache Operation)	tCLS	12		ns
CLE setup time(Cache Operation)	tCLS	15		ns
CLE Hold time	tCLH	5		ns
CE# setup time(Non-Cache Operation)	tCS	20		ns
CE# setup time(Cache Operation)	tCS	25		ns
CE# hold time	tCH	5		ns
WE# pulse width(Non-Cache Operation)	tWP	12		ns
WE# pulse width(Cache Operation)	tWP	15		ns
ALE setup time(Non-Cache Operation)	tALS	12		ns
ALE setup time(Cache Operation)	tALS	15		ns
ALE hold time	tALH	5		ns
Data setup time(Non-Cache Operation)	tDS	12		ns
Data setup time(Cache Operation)	tDS	15		ns
Data hold time	tDH	5		ns
Write cycle time(Non-Cache Operation)	tWC	25		ns
Write cycle time(Cache Operation)	tWC	30		ns
WE# high hold time	tWH	10		ns
Data transfer from cell to register	tR		60	us
ALE to RE# delay	tAR	10		ns
CLE to RE# delay	tCLR	10		ns
Ready to RE# low	tRR	20		ns
RE# pulse width(Non-Cache Operation)	tRP	12		ns
RE# pulse width(Cache Operation)	tRP	15		ns
WE# high to busy	tWB		100	ns
Read cycle time(Non-Cache Operation)	tRC	25		ns
Read cycle time(Cache Operation)	tRC	30		ns
RE# access time(Non-Cache Operation)	tREA		20	ns
RE# access time(Cache Operation)	tREA		25	ns
RE# high to output high Z	tRHZ		100	ns
CE# high to output high Z	tCHZ		50	ns
RE# high to output hold	tRHOH	15		ns
RE# low to output hold	tRLOH	5		ns
RE# or CE# high to output hold	tCOH	15		ns
RE# high hold time	tREH	10		ns
CE# low to RE# low	tCR	10		ns
WE# high to RE# low	tWHR	80		ns

Parameter	Symbol	3.3V		Unit
		Min	Max	
RE# high to WE# low	tRHW	100		ns
Output high Z to RE# low	tIR	0		ns
Address to data loading time	tADL	70		ns
Device resetting time (Read/Program/Erase)	tRST		5/10/500(1)	us
Write protection time	tWW(2)	100		ns

Table 18 : AC Timing Characteristics

NOTE:
(1): If Reset Command(FFh) is written at Ready state, the device goes into Busy for maximum 5us
(2): Write protection time to be intended about the following two scenarios:
Program / Erase Enable Operation : WP high to WE High.
Program / Erase Disable Operation : WP Low to WE High.

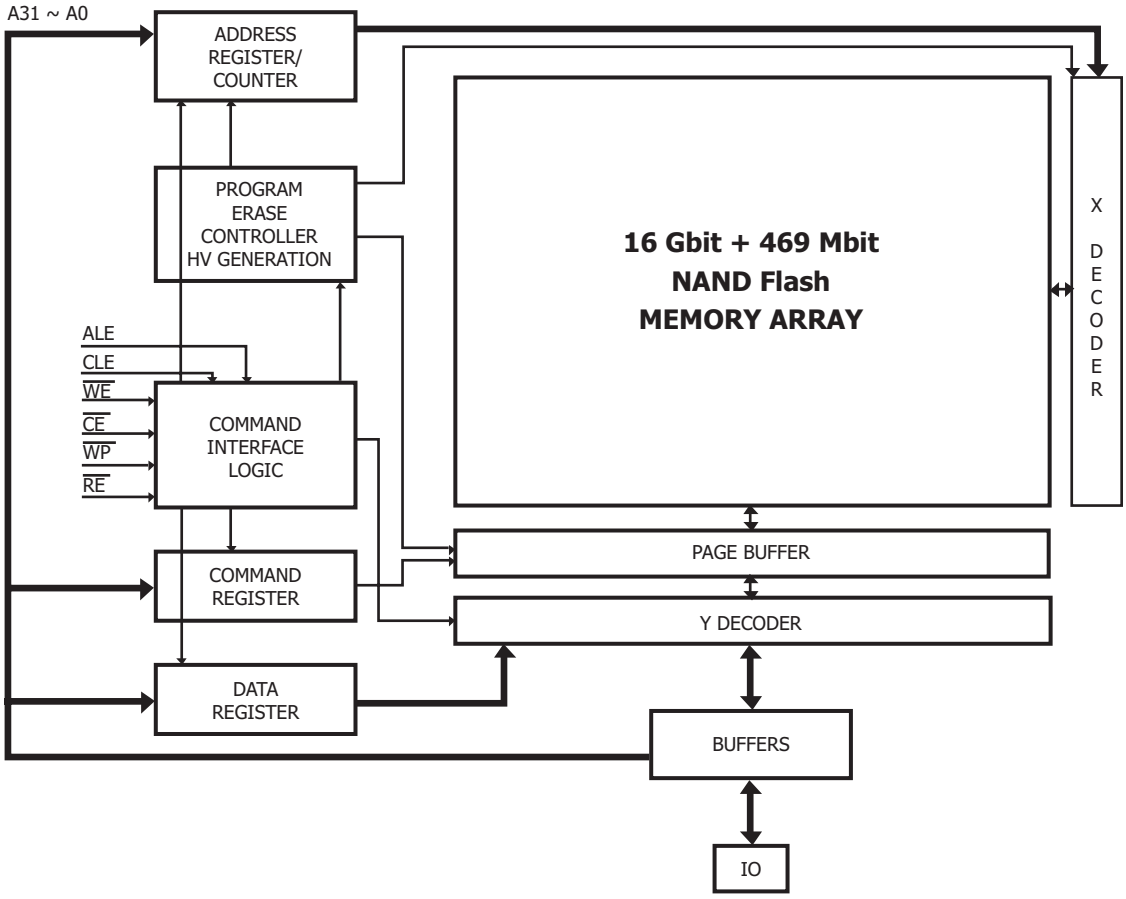


Figure 4 : Block Diagram

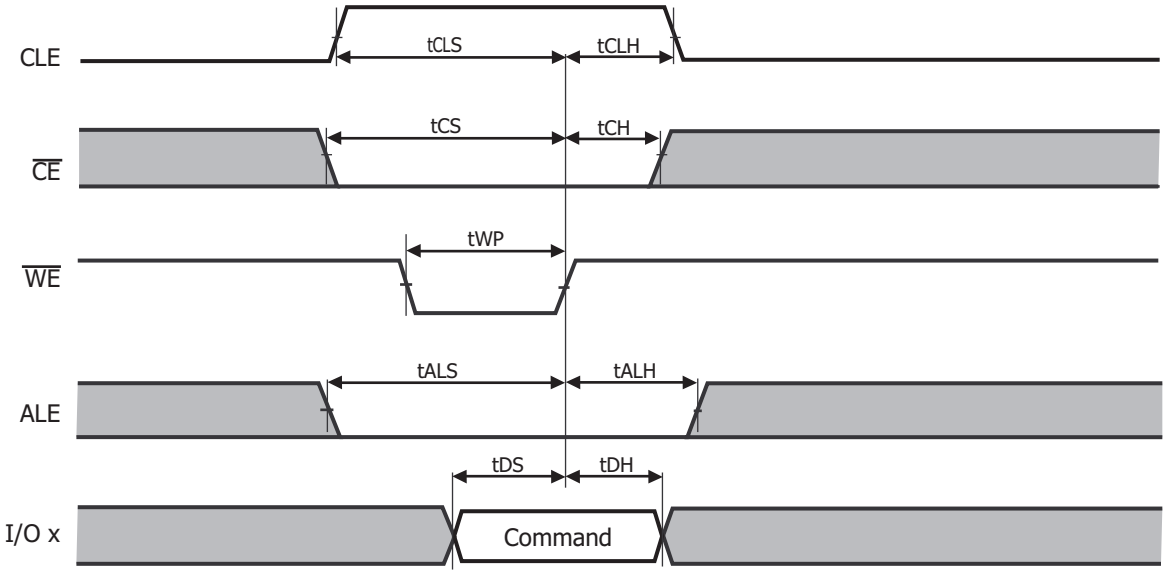


Figure 5 : Command Latch Cycle

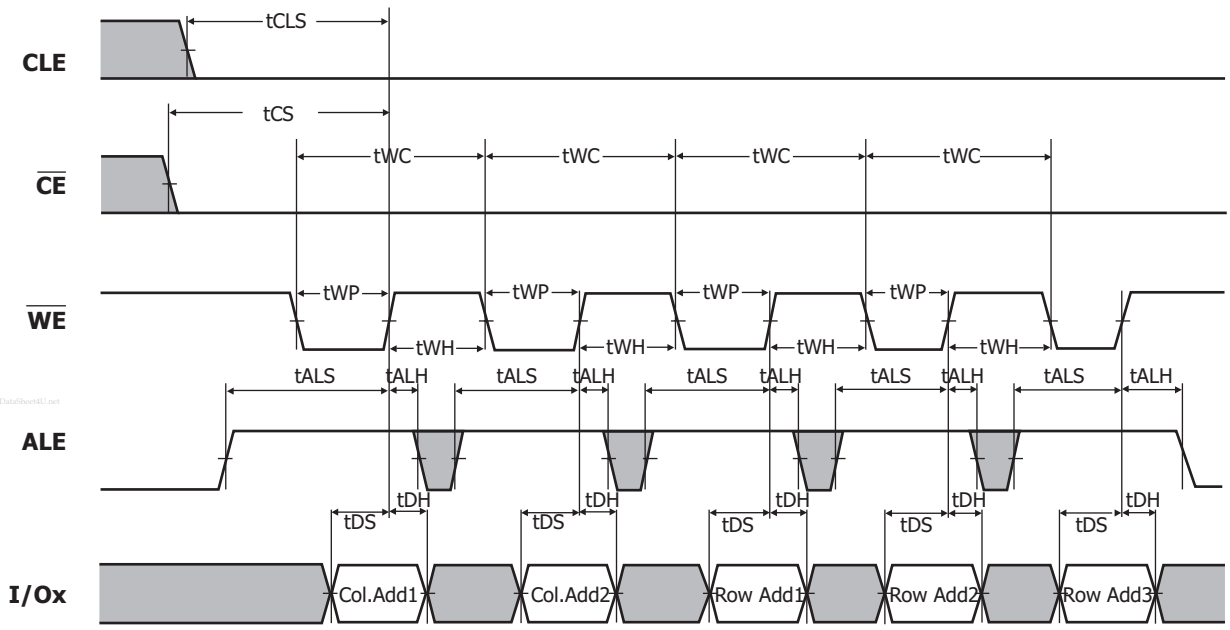
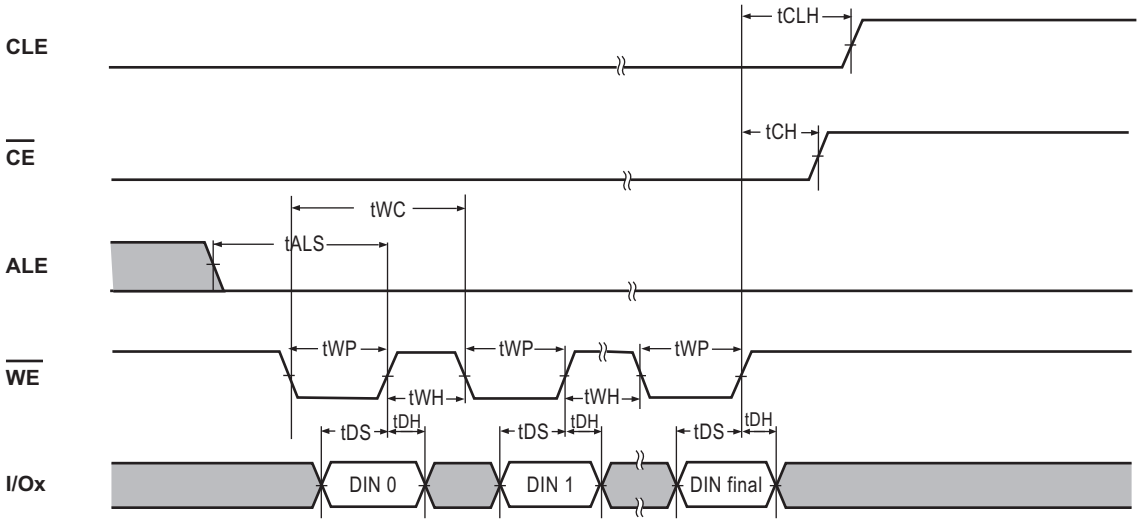
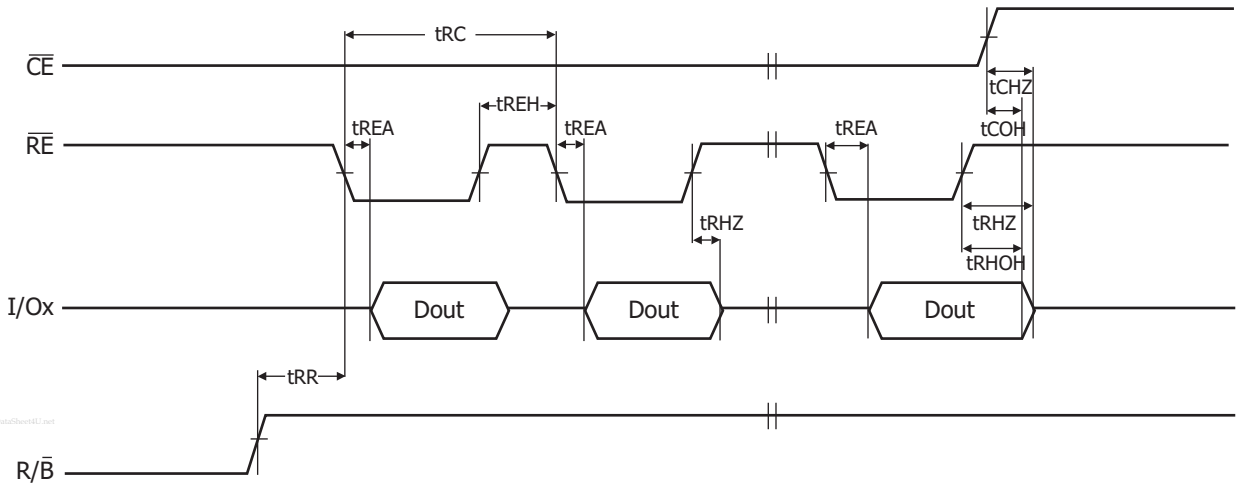


Figure 6 : Address Latch Cycle



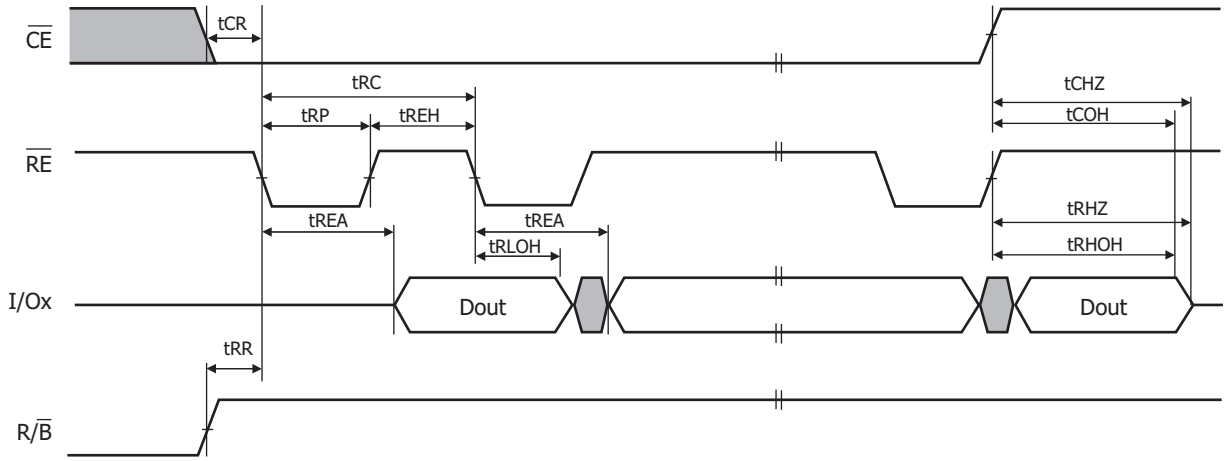
Notes: DIN final means 4,224Bytes

Figure 7 : Input Data Latch Cycle



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRHOH starts to be valid when frequency is lower than 33MHz.
tRLOH is valid when frequency is higher than 33 MHz

Figure 8 : Sequential Out Cycle after Read (CLE = L, $\overline{WE}$ = H, ALE = L)



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 9 : Sequential Out Cycle after Read (EDO type CLE = L, $\overline{WE}$ = H, ALE = L)

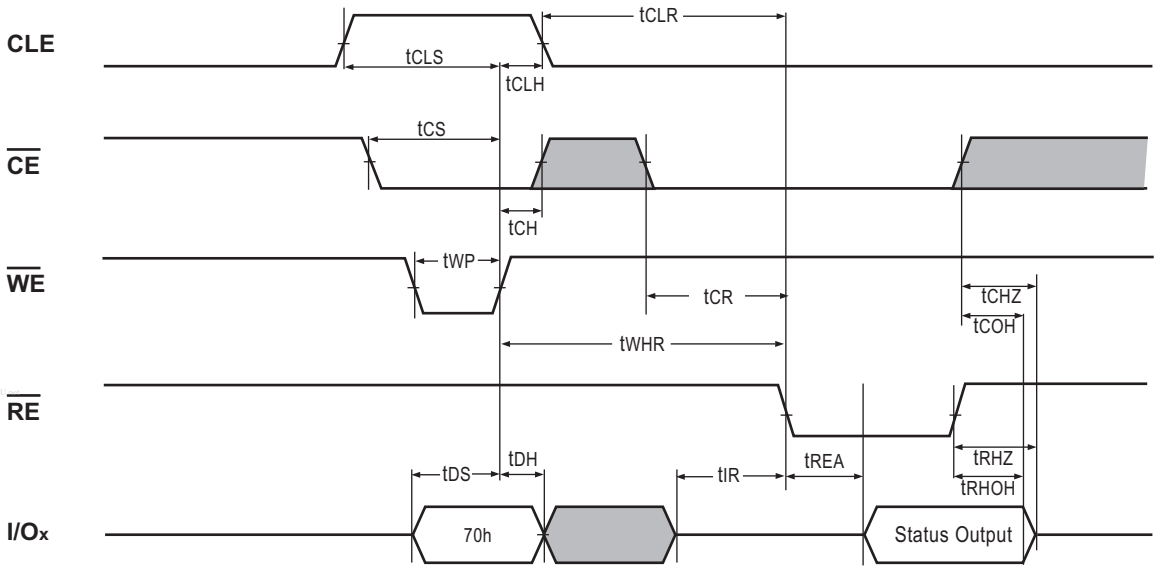


Figure 10 : Read Status Register

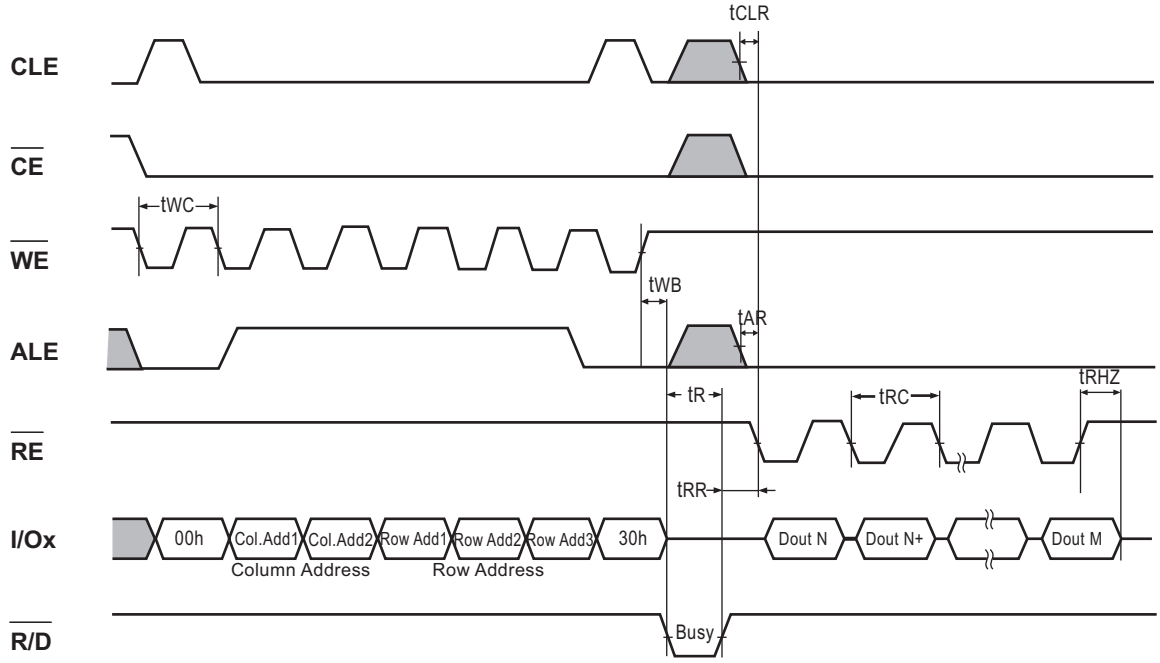


Figure 11 : Page Read Operation

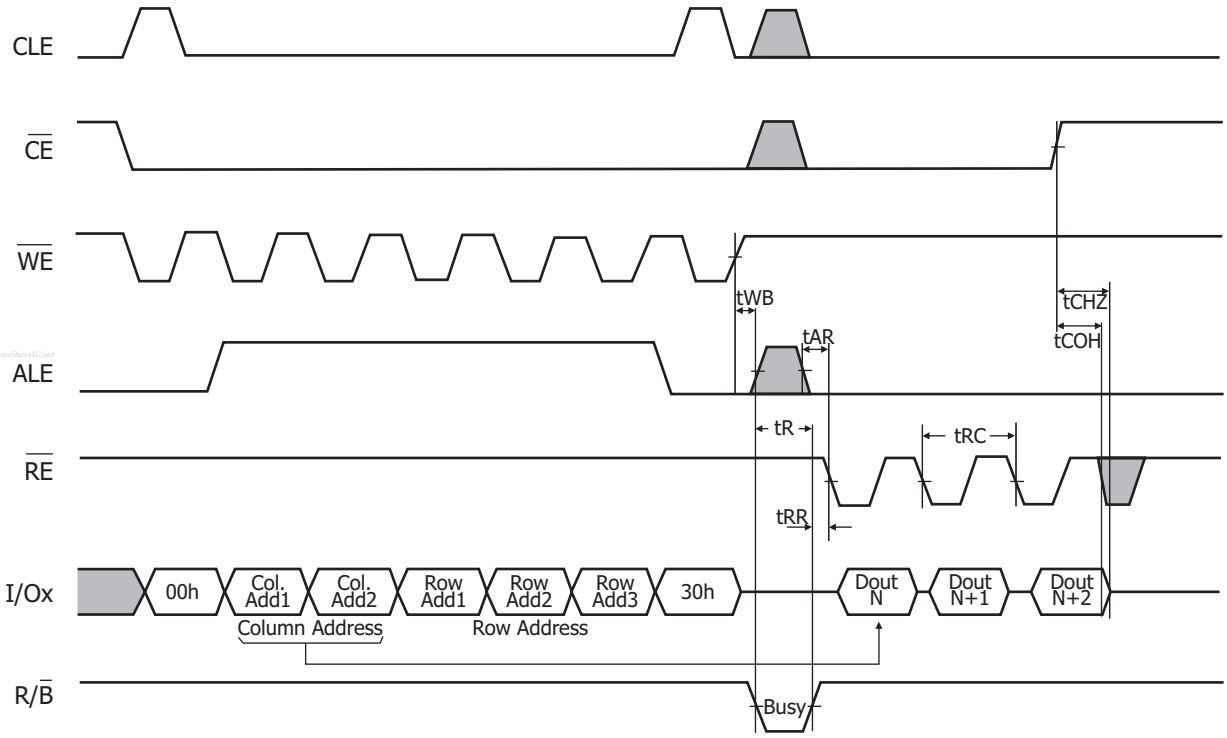


Figure 12 : Page Read Operation (Intercepted by $\overline{CE}$)

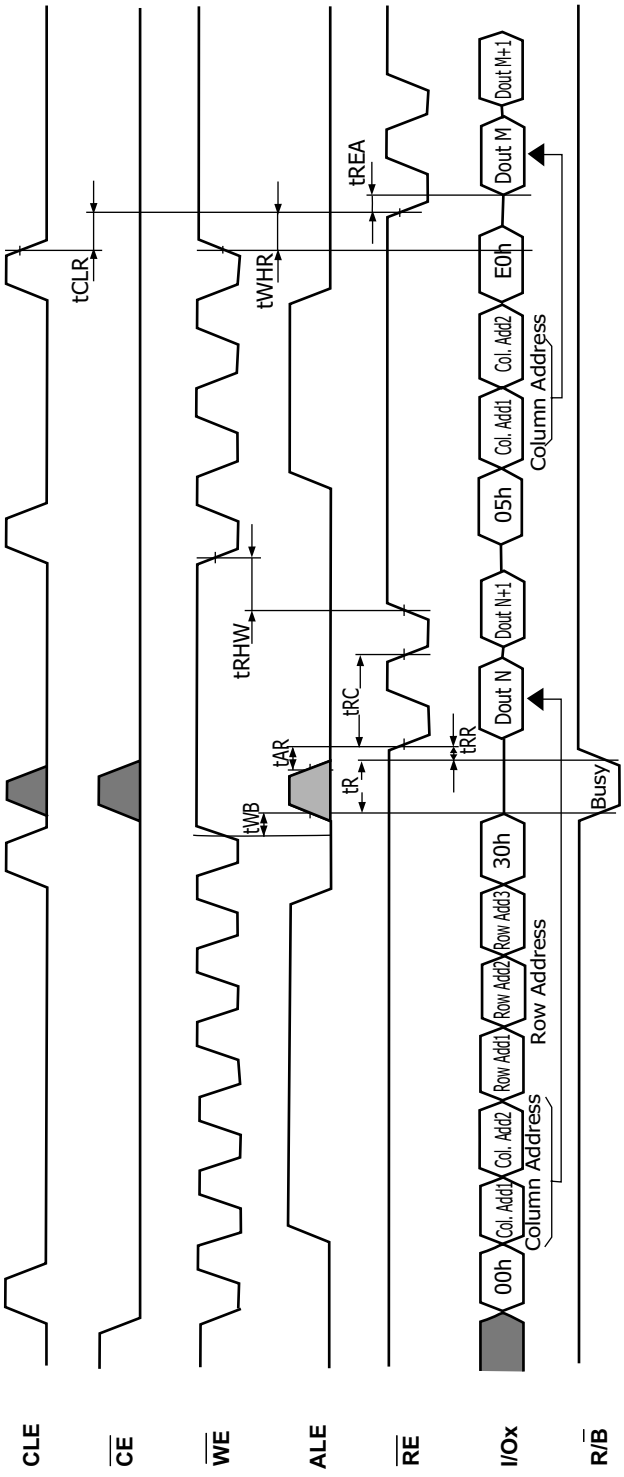


Figure 13 : Random Data Output

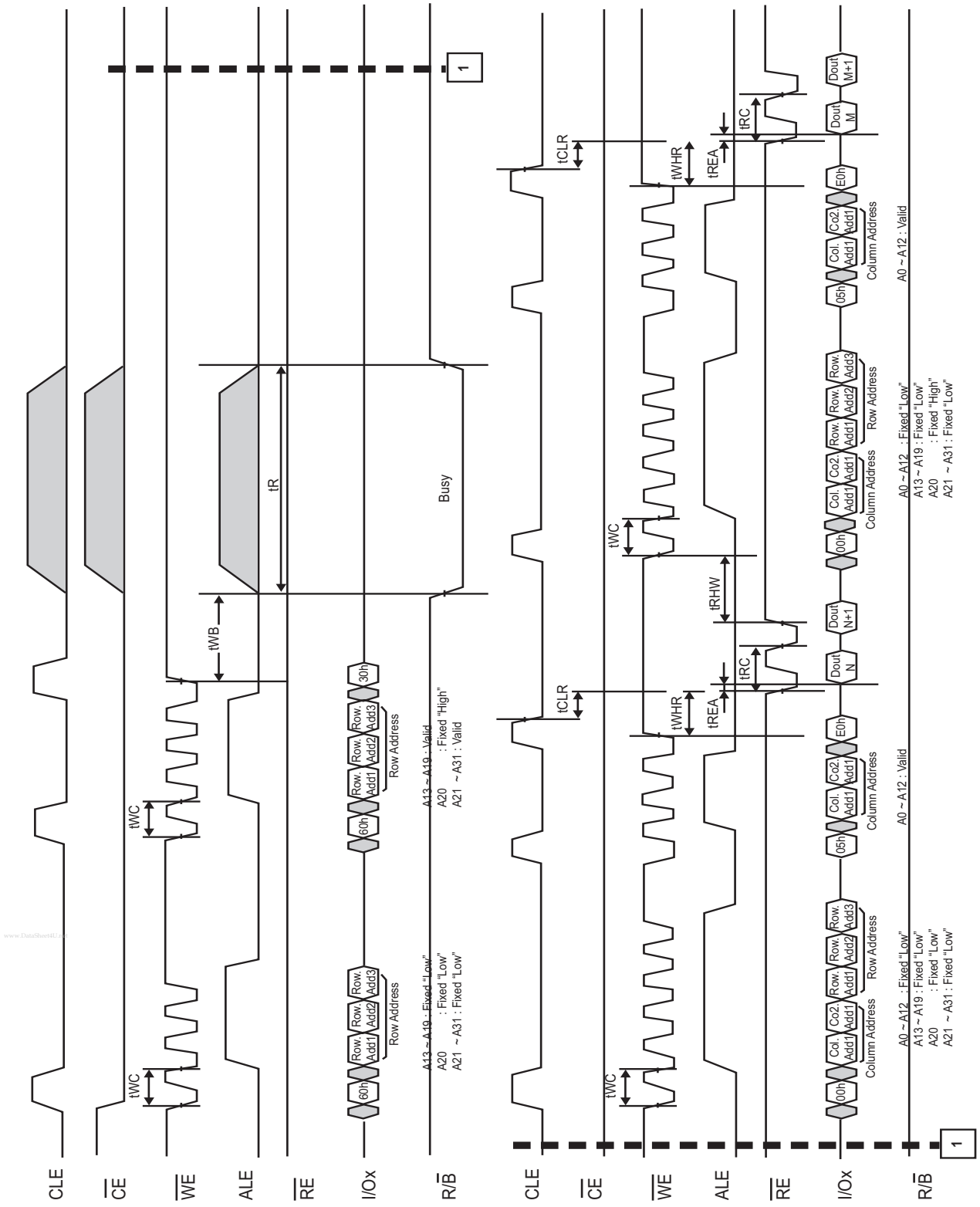
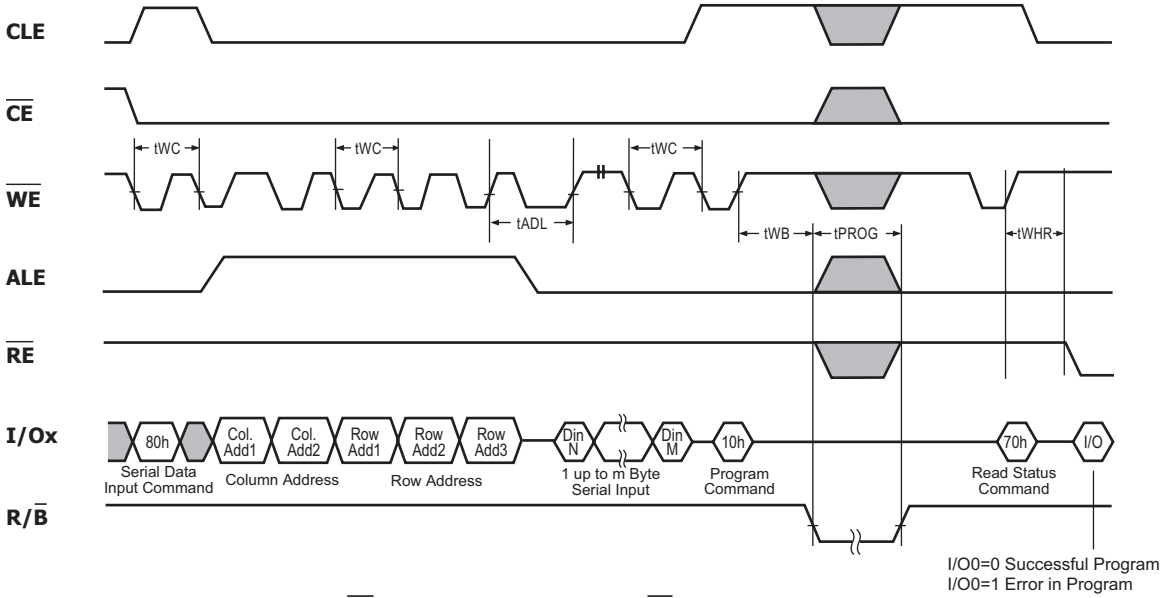


Figure 14 : Multiplane Read Operation with Random Data Output



NOTES : tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

Figure 15 : Page Program Operation

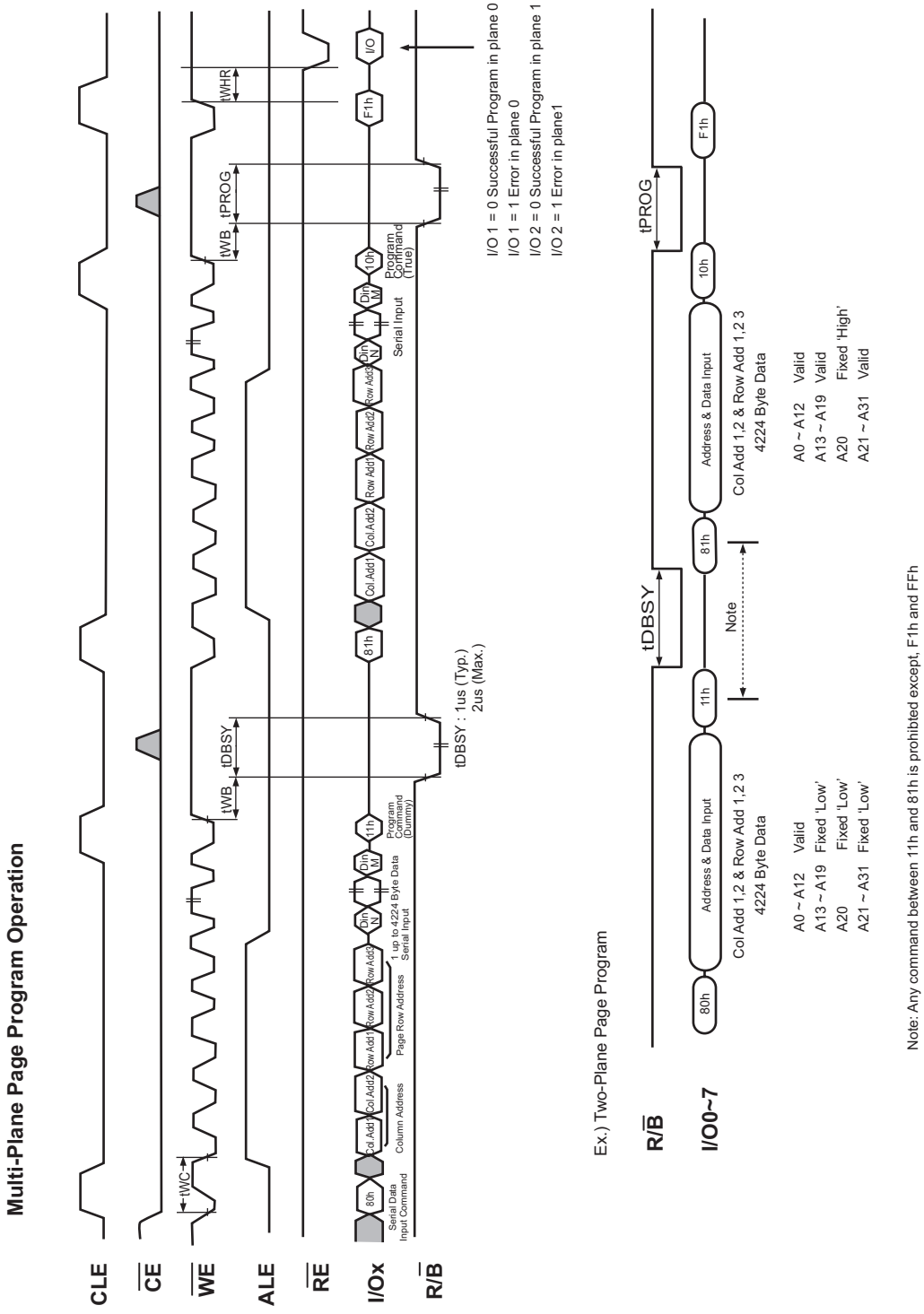


Figure 16 : Multiplane Page Program

NOTE: Any command between 11h and 81h is prohibited except, F1h and FFh.

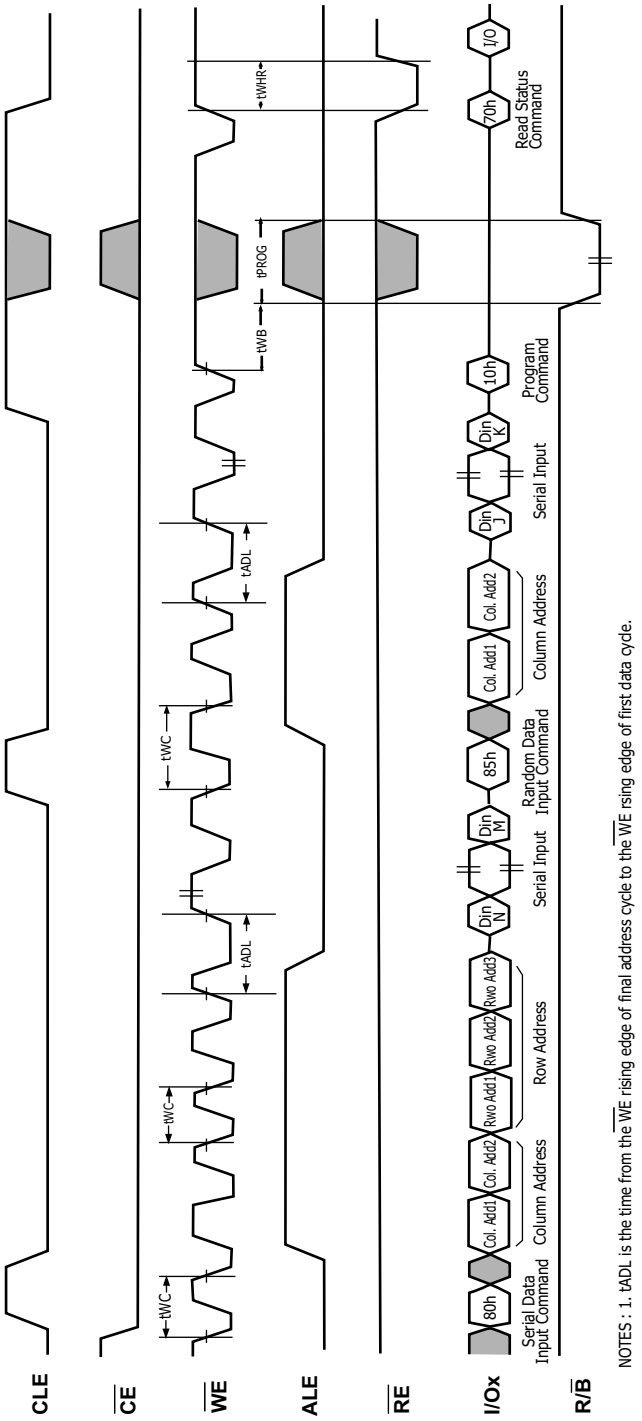


Figure 17 : Random Data Input

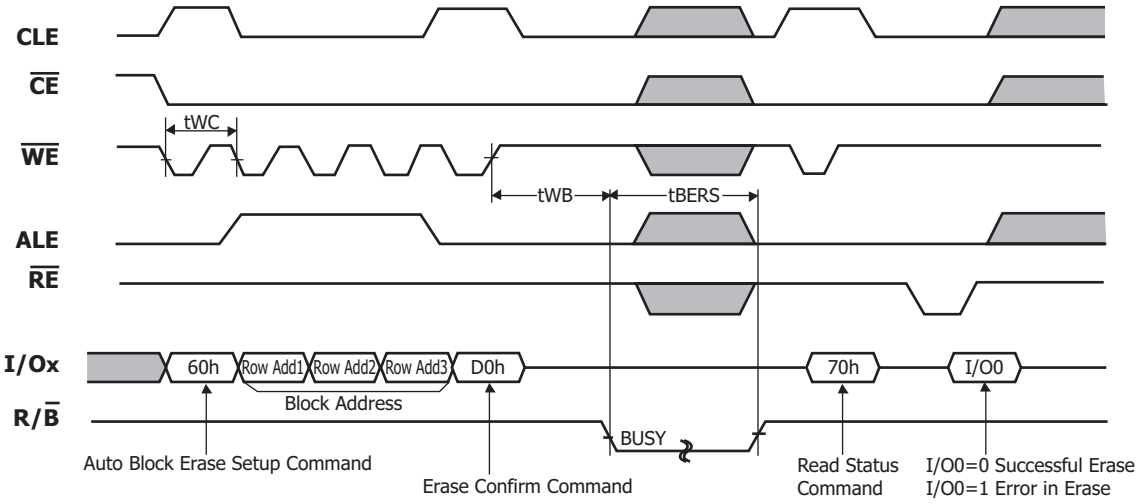
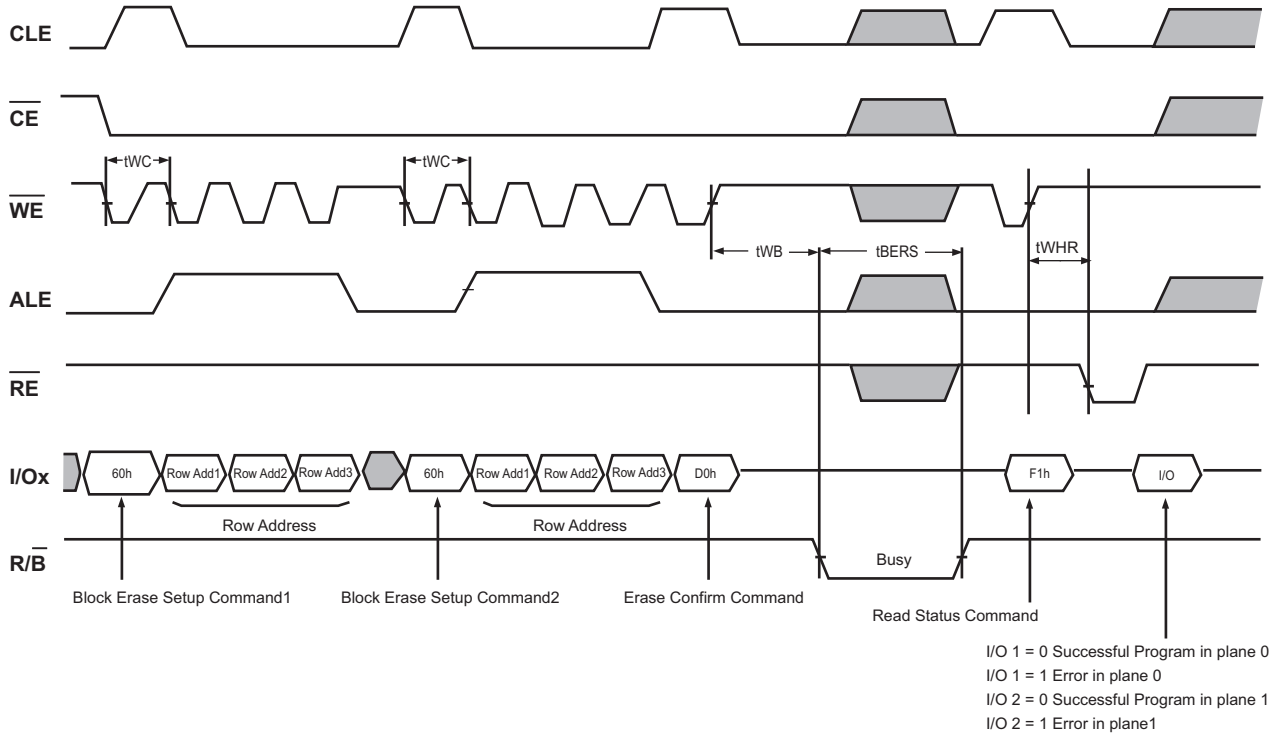


Figure 18 : Block Erase



Ex.) Address Restriction for Two-Plane Block Erase Operation

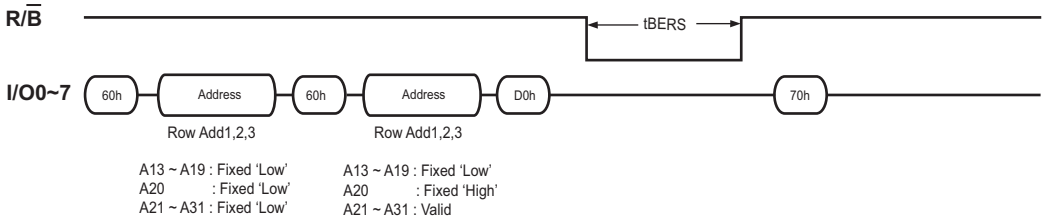


Figure 19 : Multiplane Block Erase

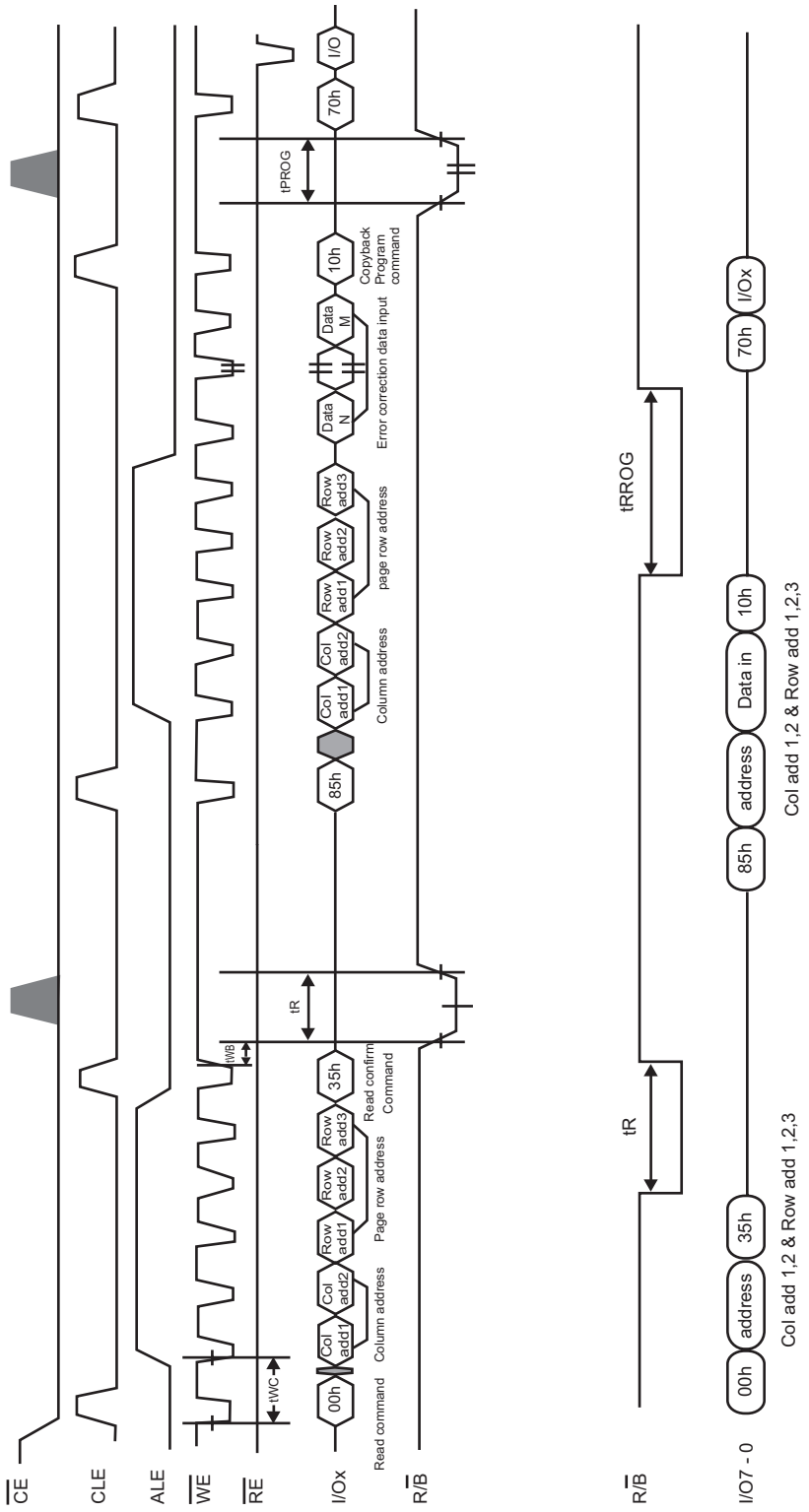


Figure 20 : Copy Back Program Operation

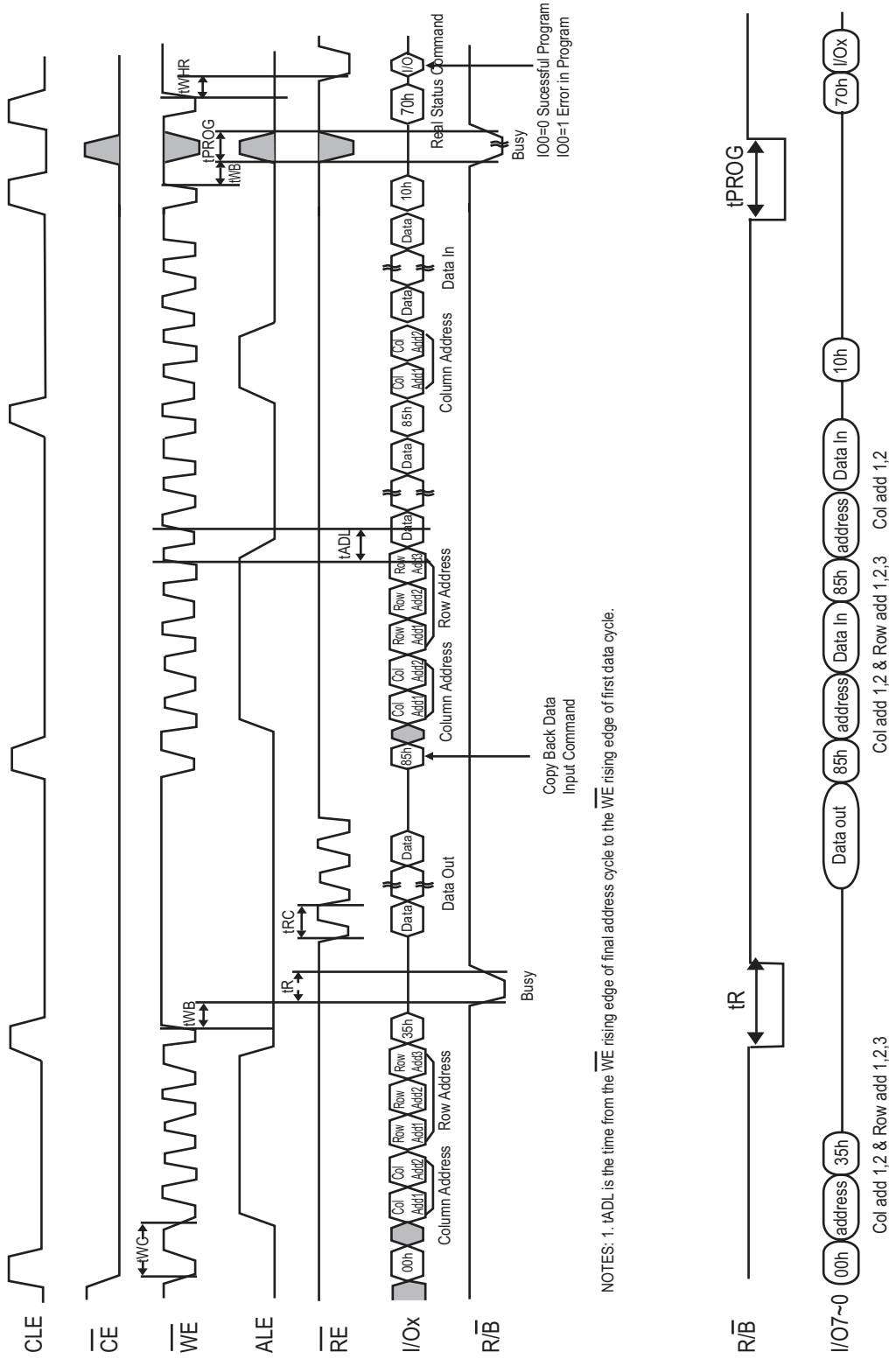
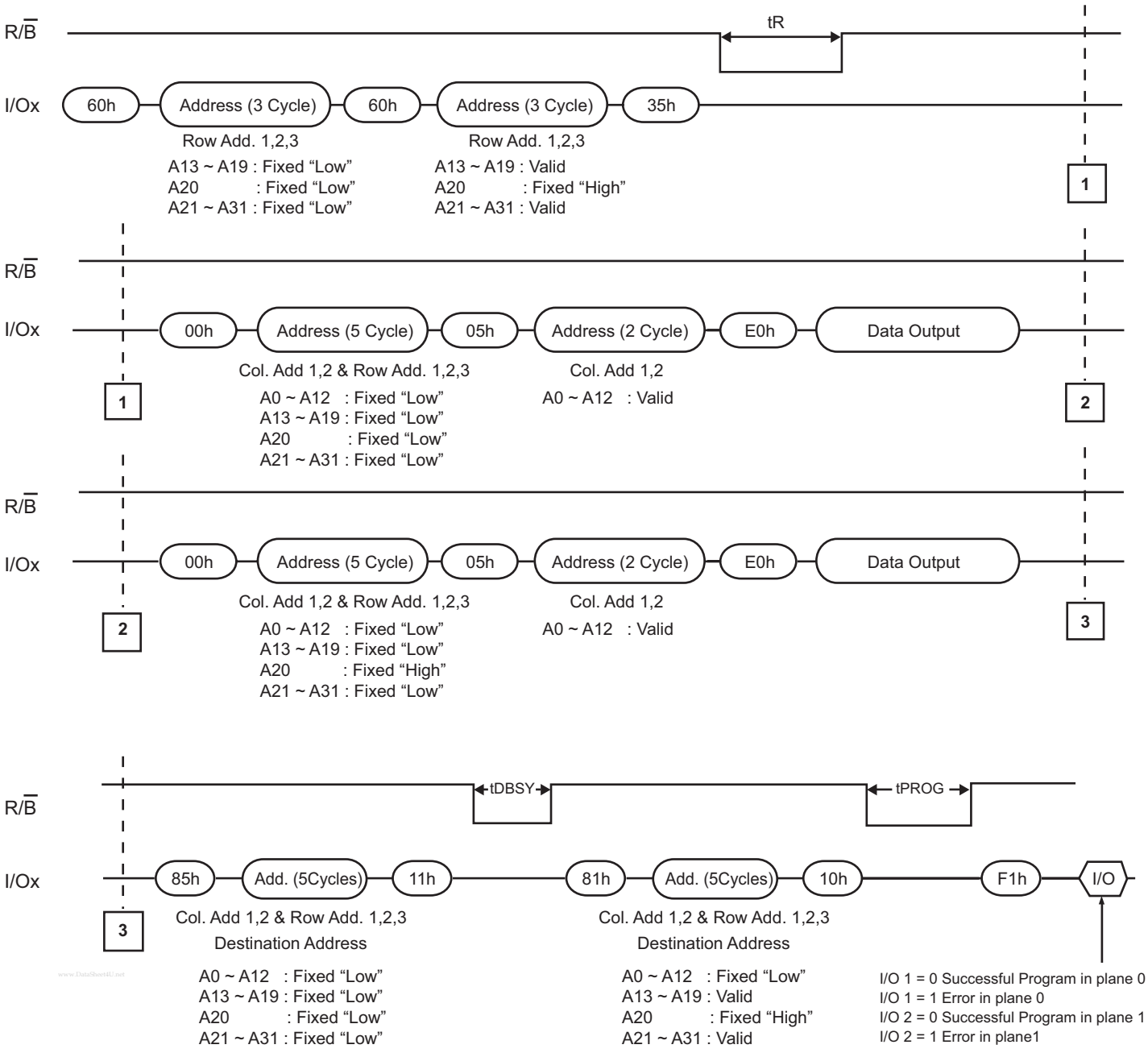
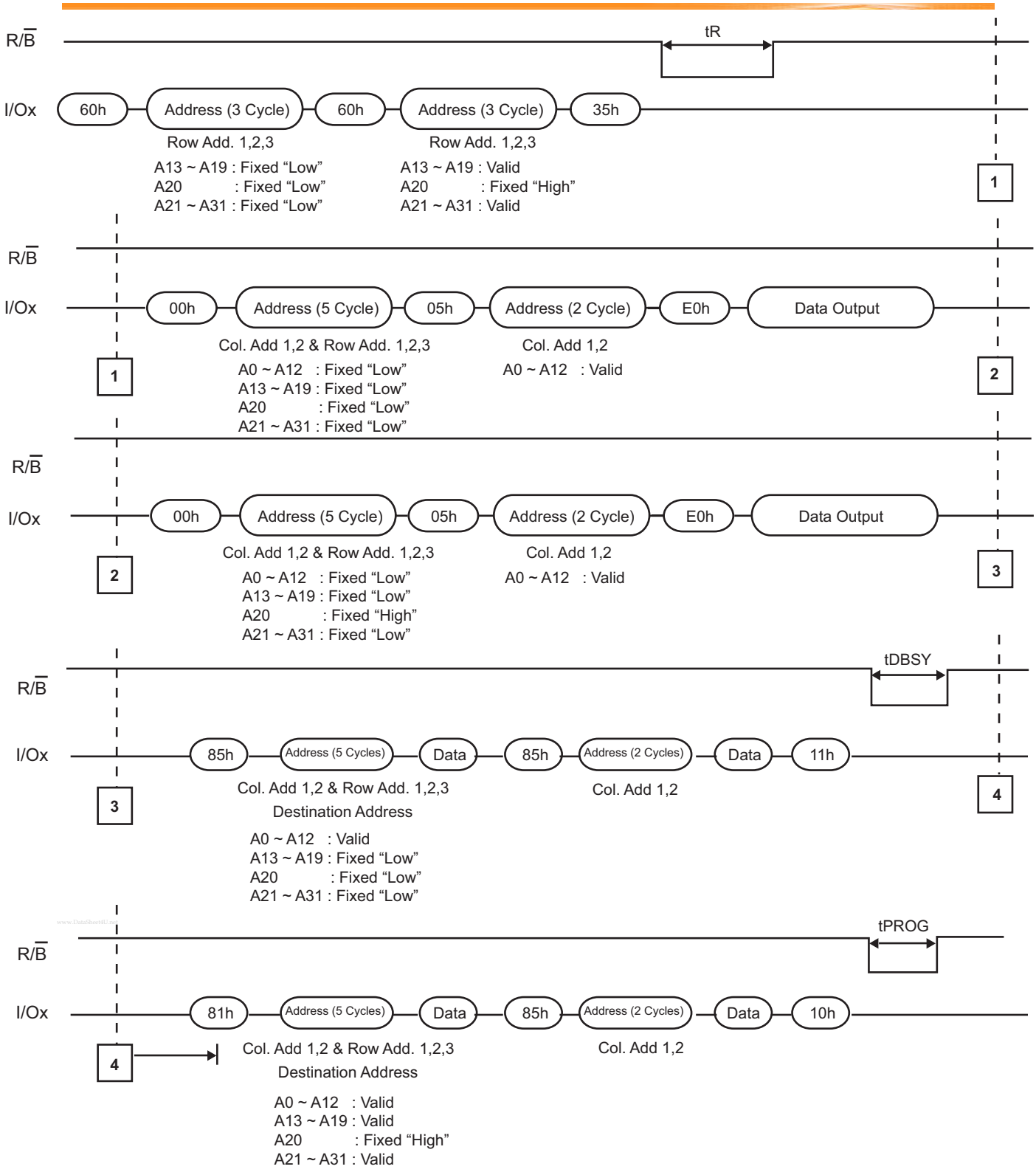


Figure 21 : Copy Back with Random Data Input



Note : 1. Copy back operation is allowed only within the same memory plane
2. Any command between 11h and 81h is prohibited except 70h, F1h and FFh

Figure 22 : Multiplane Copy Back



NOTE
1. Copy Back Program operation is allowed only within the same memory plane.
2. Any Command between 11h and 81h is prohibited except 70h FFh and F1h

Figure 23 : Multiplane Copy Back with Random Data Input

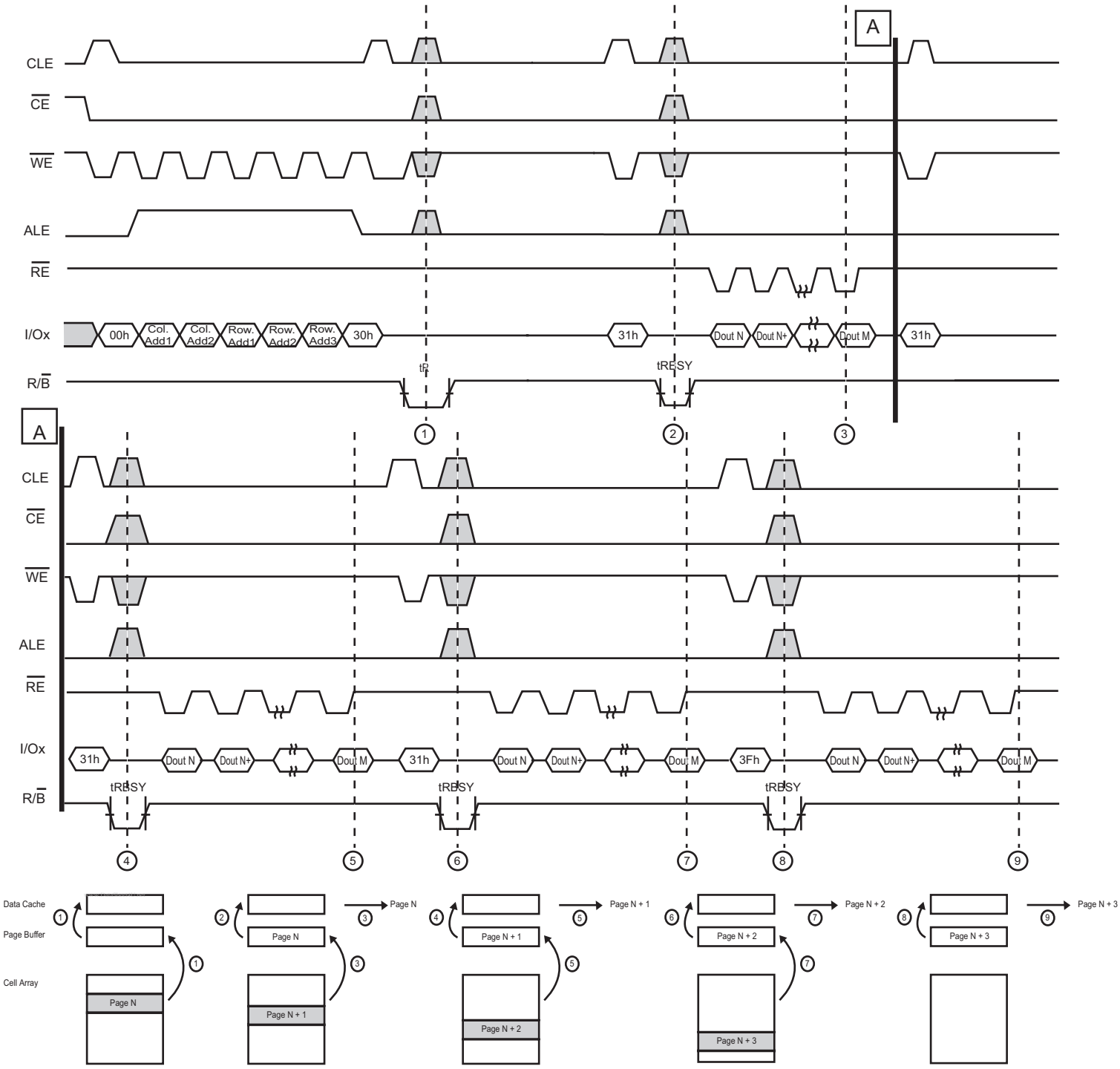


Figure 24 : Read Operation with Cache

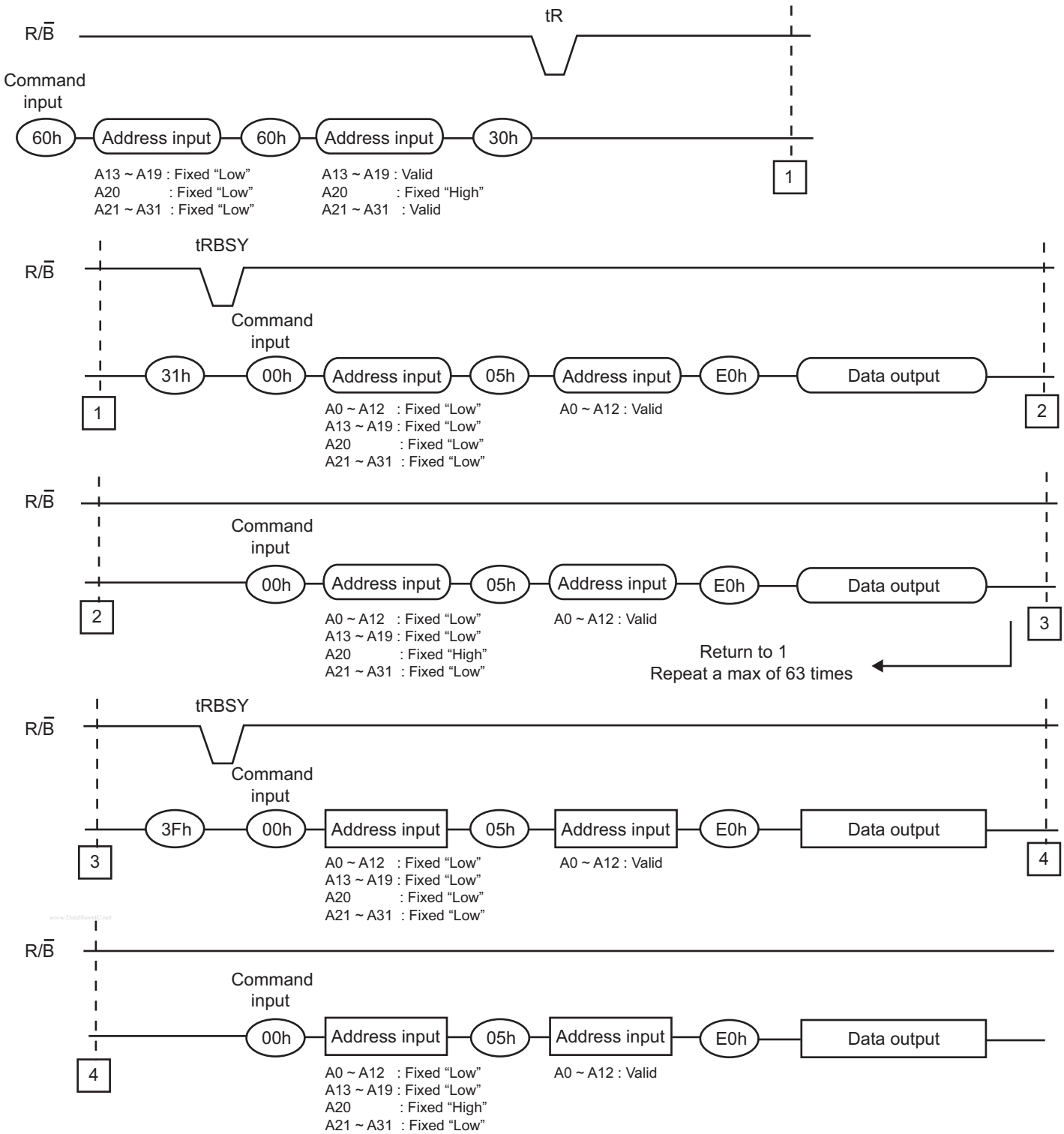


Figure 25 : Multi Plane Read Operation with Cache

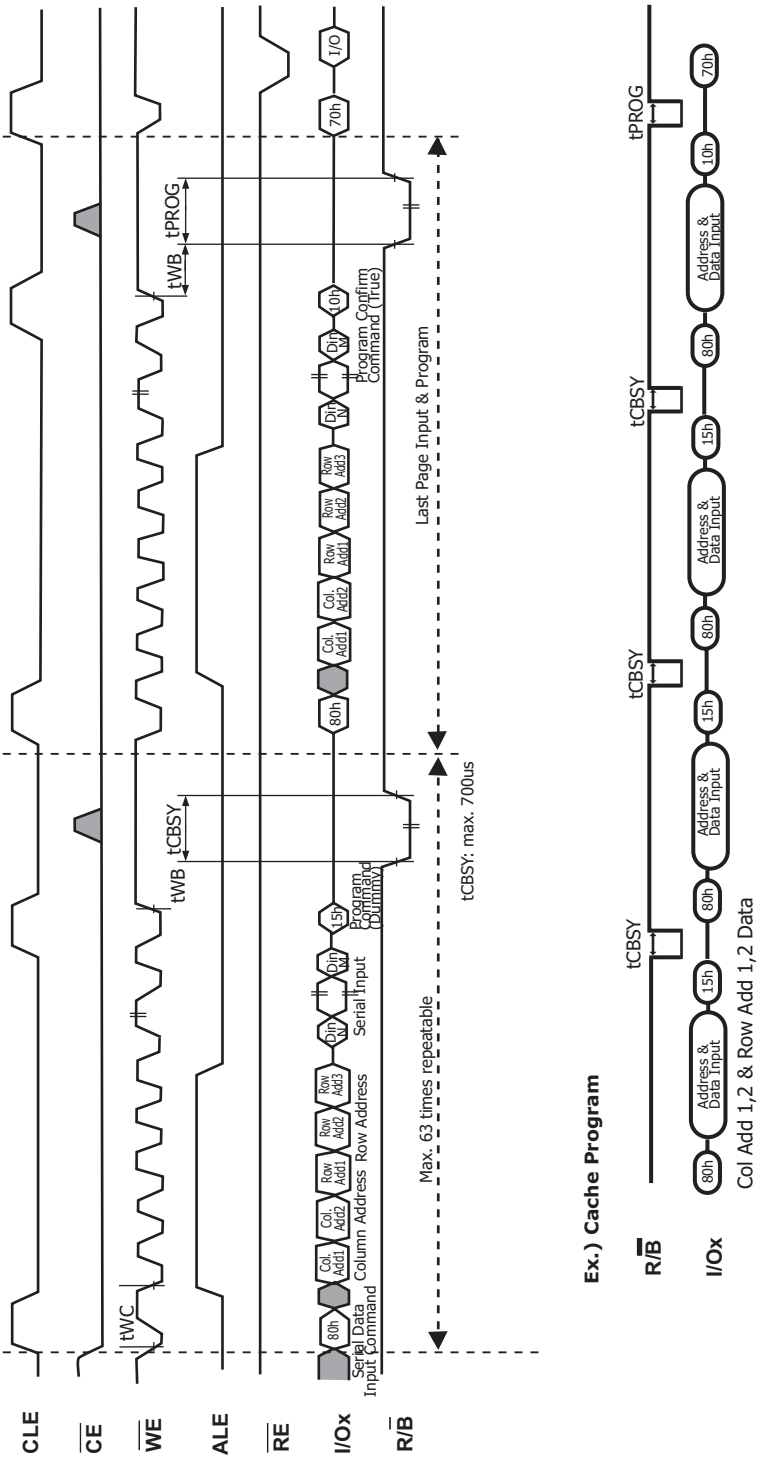


Figure 26 : Program Operation with Cache

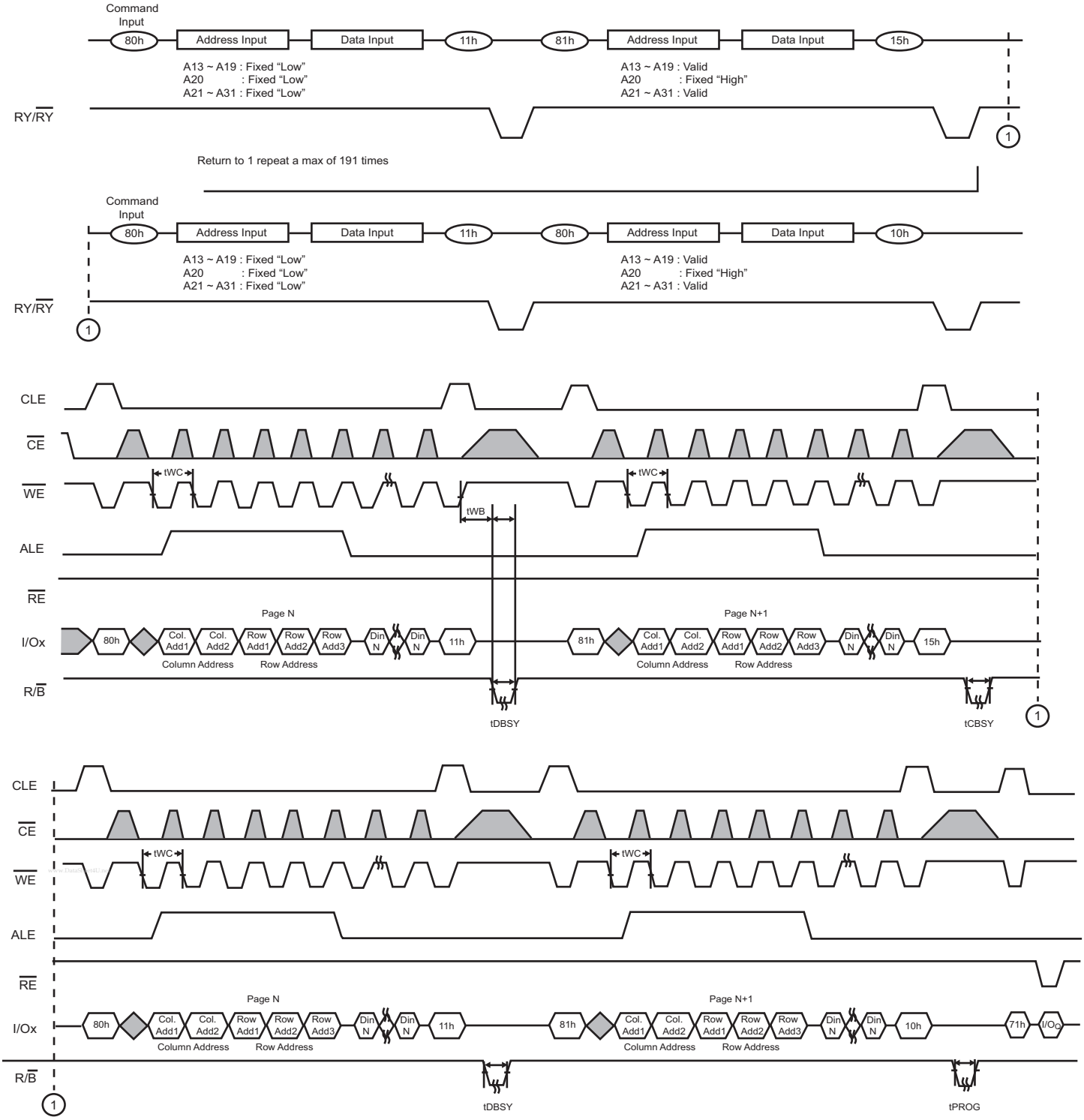


Figure 27 : Multi Plane Cache Program

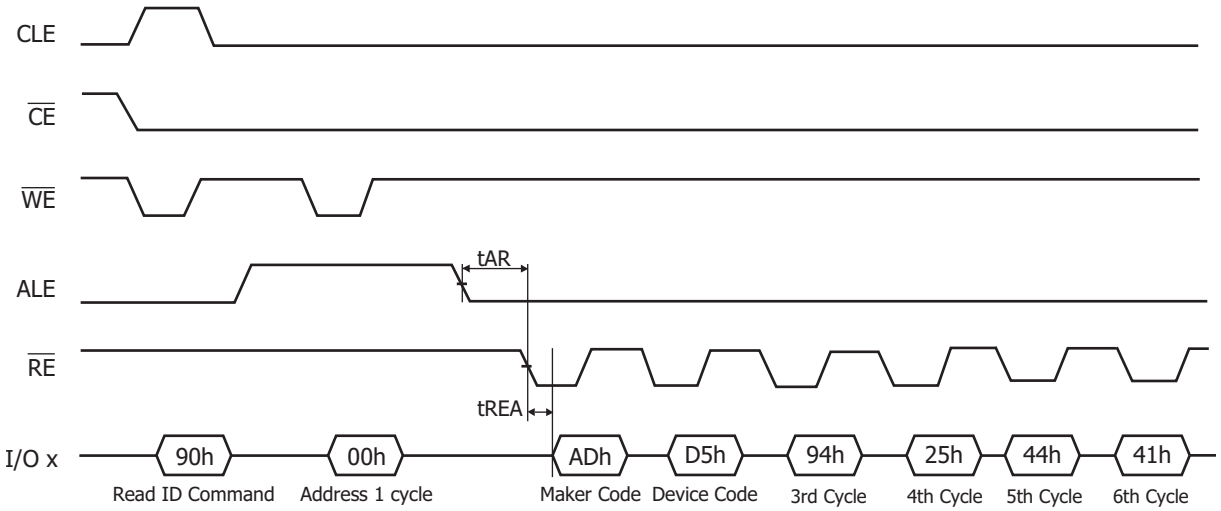


Figure 28 : Read ID Operation

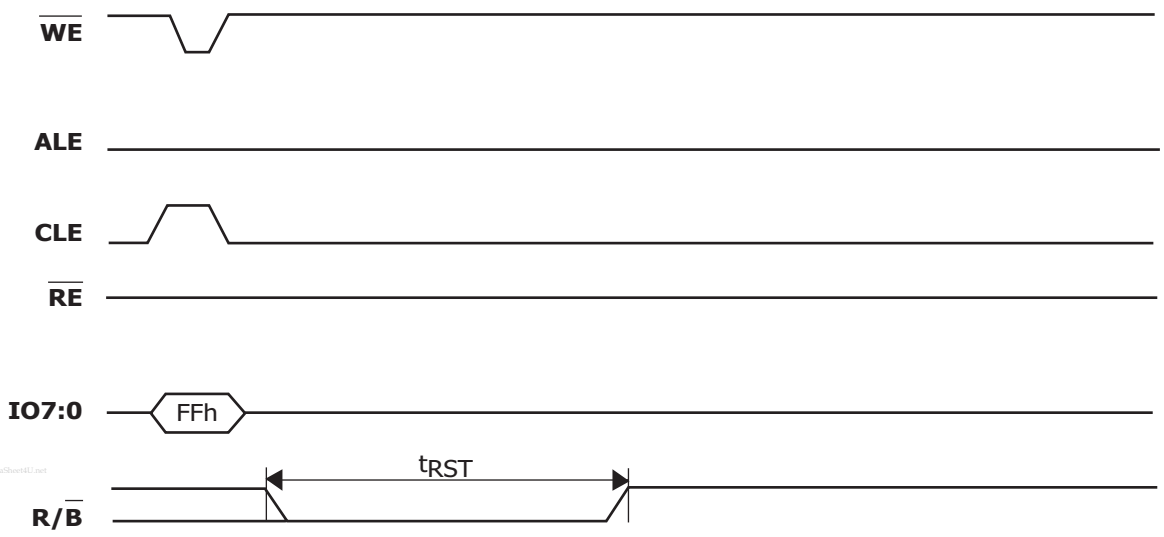


Figure 29 : Reset Operation

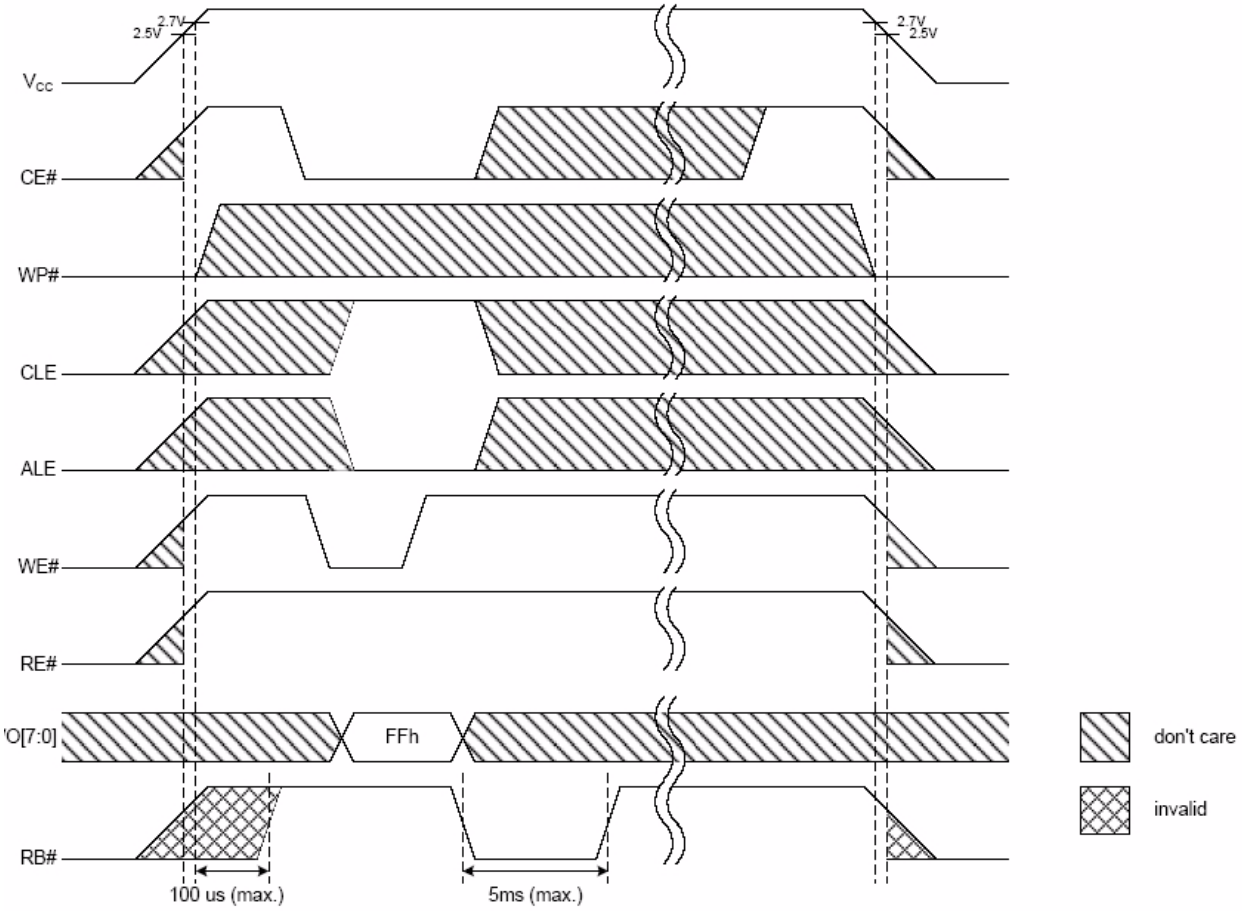


Figure 30 : Power on and Data Protection Timing

Figure 31 : Power on Reset

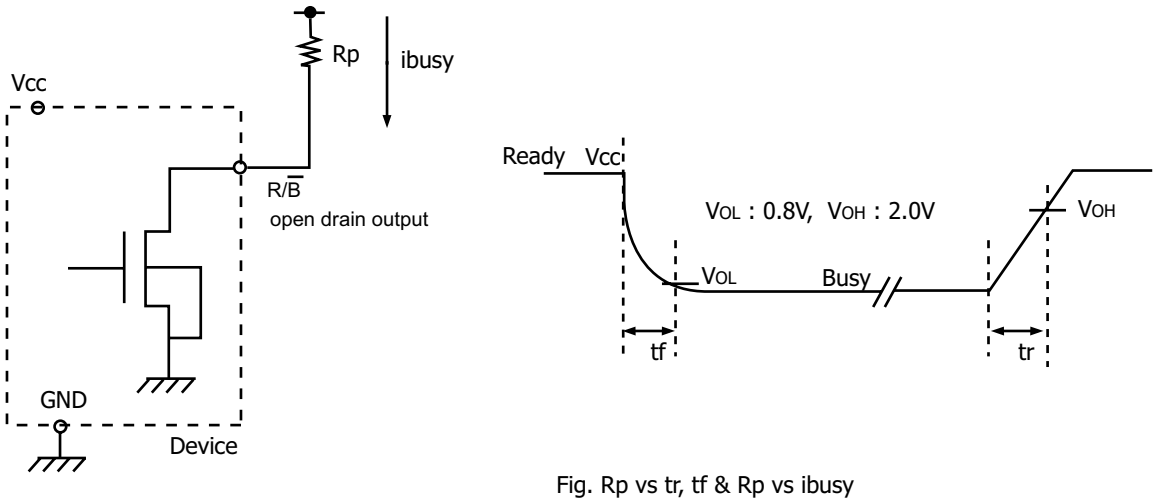
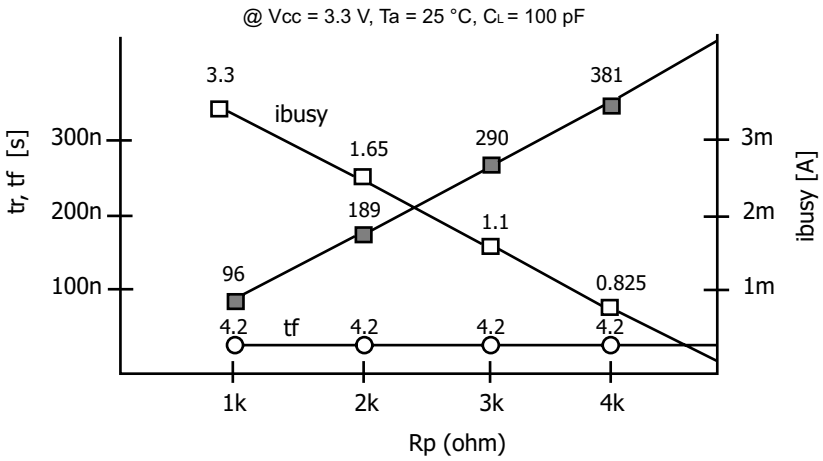


Fig. Rp vs tr, tf & Rp vs ibusy



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 32 : Ready / Busy Pin Electrical Specifications

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the Last and (Last-2)th page (if the last page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 34. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

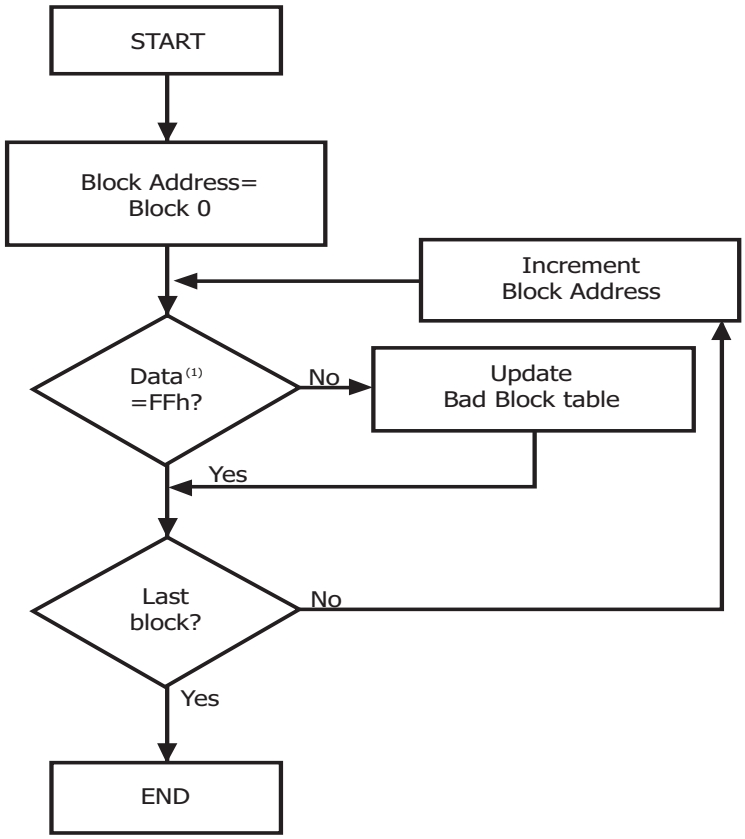


Figure 33 : Bad Block Management Flowchart

NOTE :

1. Make sure that FFh at the column address 4096 of the last page and last - 2th page.

Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

The failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Refer to Table 19 and Figure 34 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (with 12 bit/512byte)

Table 19 : Block Failure

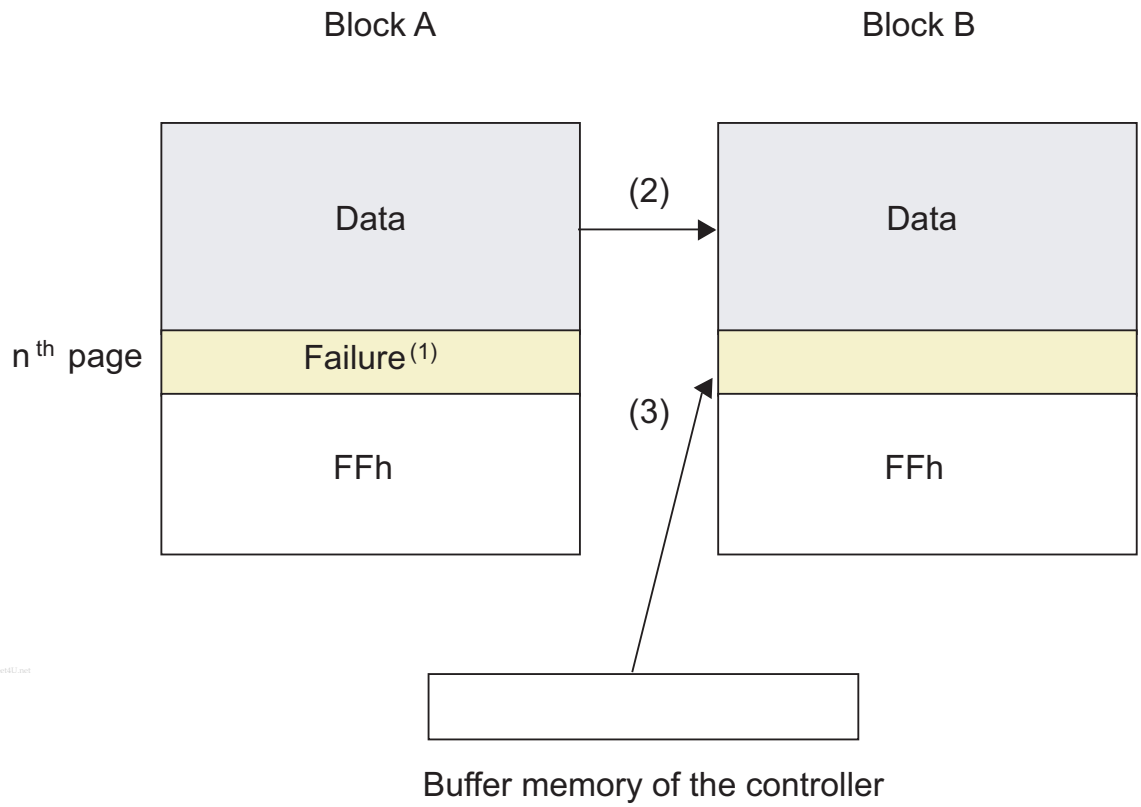


Figure 34 : Bad Block Replacement

NOTE :
1. An error occurs on the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. N^{th} data of block A which is in controller buffer memory is copied into n^{th} page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A

Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 35~38)

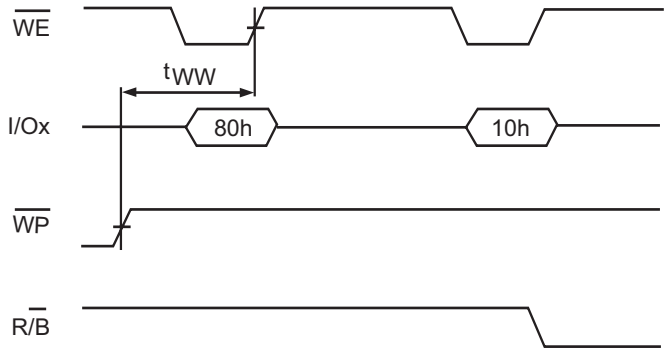


Figure 35 : Enable Programming

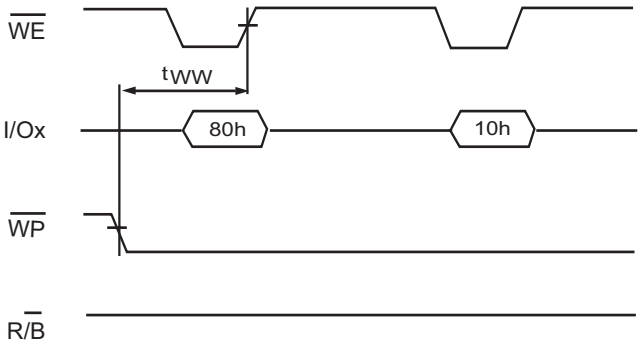


Figure 36 : Disable Programming

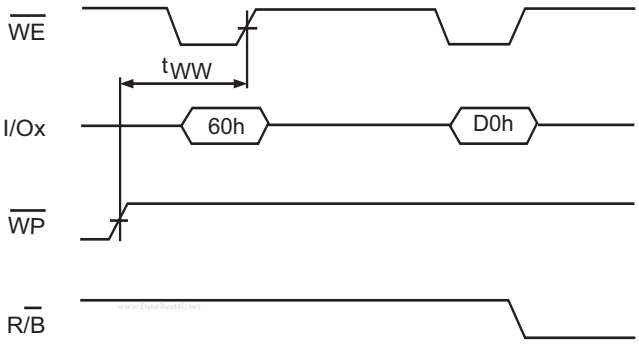


Figure 37 : Enable Erasing

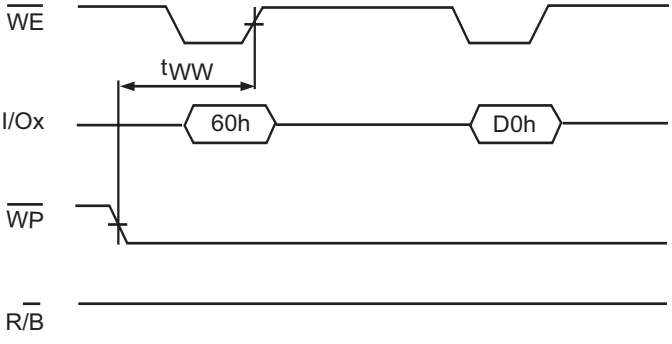


Figure 38 : Disable Erasing

Paied Page Address Information

Paired Page Address		Paired Page Address	
Group A	**Group B**	**Group A**	**Group B**
00h	04h	01h	05h
02h	08h	03h	09h
06h	0Ch	07h	0Dh
0Ah	10h	0Bh	11h
0Eh	14h	0Fh	15h
12h	18h	13h	19h
16h	1Ch	17h	1Dh
1Ah	20h	1Bh	21h
1Eh	24h	1Fh	25h
22h	28h	23h	29h
26h	2Ch	27h	2Dh
2Ah	30h	2Bh	31h
2Eh	34h	2Fh	35h
32h	38h	33h	39h
36h	3Ch	37h	3Dh
3Ah	40h	3Bh	41h
3Eh	44h	3Fh	45h
42h	48h	43h	49h
46h	4Ch	47h	4Dh
4Ah	50h	4Bh	51h
4Eh	54h	4Fh	55h
52h	58h	53h	59h
56h	5Ch	57h	5Dh
5Ah	60h	5Bh	61h
5Eh	64h	5Fh	65h
62h	68h	63h	69h
66h	6Ch	67h	6Dh
6Ah	70h	6Bh	71h
6Eh	74h	6Fh	75h
72h	78h	73h	79h
76h	7Ch	77h	7Dh
7Ah	7Eh	7Bh	7Fh

NOTE: When program operation is abnormally aborted (ex. power-down, reset), not only page data under program but also paired page data may be damaged.

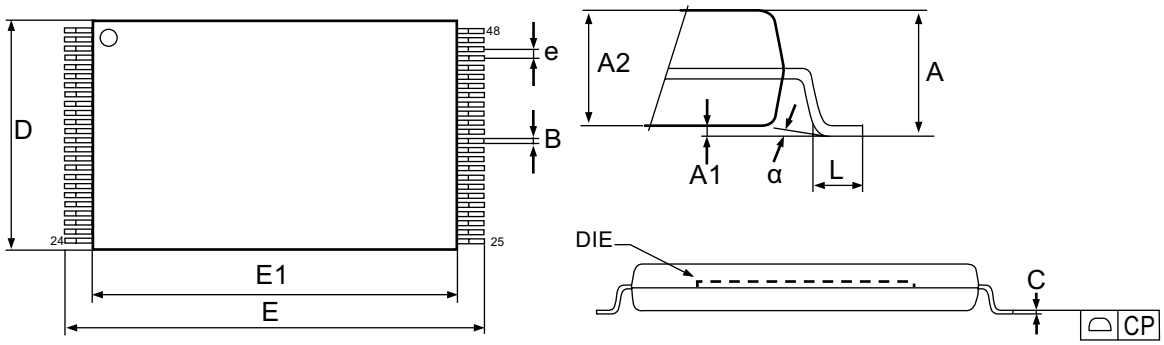


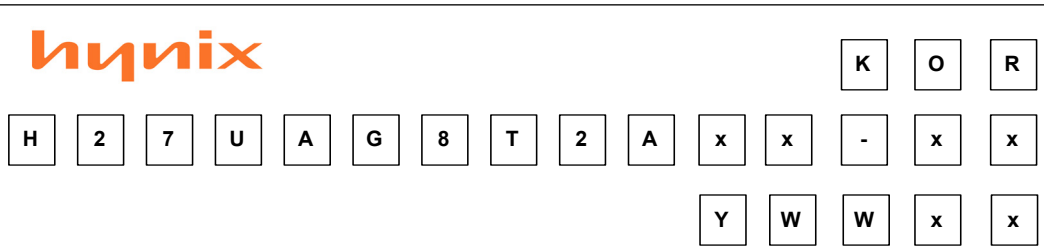
Figure 39 : 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Table 20 : 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

MARKING INFORMATION - TSOP1

Marking Example



- hynix	: Hynix Symbol
- KOR	: Origin Country
- H27U1G8F2Bxx-xx	: Part Number
H: Hynix	
27: NAND Flash	
U: Power Supply	: U (2.7 V~3.6 V)
AG: Density	: 16 Gbit
8 : Bit Organization	: 8(x8)
T: Classification	: Multi Level Cell+Single Die+Large Block
2: Mode	: 2(1nCE & 1R/nB; Sequential Row Read Disable)
A: Version	: 2nd Generation
x: Package Type	: T(48-TSOP1)
x: Package Material	: Blank(Normal), R(Lead & Halogen Free)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)
x: Operating Temperature	: C(0℃~70℃), I(-40℃~85℃)

- Y: Year (ex: 8=year 2008, 9= year 2009)
- ww: Work Week (ex: 12= work week 12)
- xx: Process Code

Note

- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item