128 Gb NAND Flash
H27UDG8VEM

Document Title

128 Gbit (16 G x 8 bit) NAND Flash Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft.	FEB. 9. 2009	Preliminary
0.1	1) Removing the PSL pin and related material - Modified Figures: 1, 2, 3, 31 - Modified Tables: 1, 2, 5, 8 - Modified Text: Section 4.3	FEB.18.2009	Preliminary
0.2	1) Modified tCBSYR - 60us-> 70us - Modified Part:Table 11 2) Modified Status Register Coding - Modified text: Section 3.7, 3.11 and 3.13 - Modified Part: Table4, Table13,Table14, Figure9, Figure14, Figure15, Figure16, Figure17, Figure18, Figure19, Figure20, Figure 25 and Figure 26 - Deleted Part: Table15	Apr.6.2009	Priliminary

FEATURES SUMMARY

HIGH DENSITY NAND Flash MEMORIES

- Cost effective solutions for mass storage applications

NAND INTERFACE

- x8 bus width.
- Multiplexed Address/ Data
- Pin-out compatibility for all densities

SUPPLY VOLTAGE

- 3.3V device : VCC = 2.7 V ~3.6 V

Memory Cell Array

- (4K + 224) bytes x 128 pages x 16384blocks

PAGE SIZE

- x8 device: (4096 + 224 spare) bytes

BLOCK SIZE

- x8 device: (512K +28K) bytes

PAGE READ / PROGRAM

- Random access : 60us (max.)
- Sequential access: 25ns (min.)
  30ns(min.) for Cache Operation
- Page program time: 1000us (typ.)
- Multi-Plane page program time: 1000us (typ.)

COPY BACK PROGRAM

- Fast page copy without external buffer
- Multi-Plane copy-back program

CACHE PROGRAM

- Internal (4K + 224) bytes buffer to improve the program throughput

CACHE READ

- Automatic block download without latency time

FAST BLOCK ERASE

-Block erase time: 3ms (Typ.)
-Multi-Plane block erase time(2 block): 3ms(Typ.)

STATUS REGISTER

ELECTRONIC SIGNATURE

- 1st cycle: Manufacturer Code
- 2nd cycle: Device Code
- 3rd cycle: Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Interleaved Program, Write Cache
- 4th cycle: Page size, Block size, Redundant area size
- 5th cycle: Plane Number, ECC Level
- 6th cycle: Technology (Design Rule), EDO, Interface

MULTI-PLANE OPERATION

- Multiple plane operation to improve the program/read /erase/cache read/cache program throughput

CHIP ENABLE DON'T CARE OPTION

- Simple interface with microcontroller

HARDWARE DATA PROTECTION

- Program/Erase locked during Power transitions

DATA RETENTION

- 5 K Program / Erase Cycles (with 12 bit / 512 byte ECC)
- 10 years data retention

PACKAGE

- VLGA (14x18x1.0), Dual Interface

Dual Interface

- Descriptions,including diagrams and tables, apply to each individual CE#

1. SUMMARY DESCRIPTION

The H27UDG8VEM (TBD) is a 16384Gx8bit with spare 224Mx8 bit capacity. The device is offered in 3.3V Vcc Core Power Supply, 3.3V Input-Output Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 32768 blocks, composed by 128 pages consisting in two NAND structures of 32 series connected Flash cells. Every cell holds two bits. Like all other 4KB page NAND Flash devices, a program operation allows to write the 4,320 byte page in typical 1000(TBD)us and an erase operation can be performed in typical 3ms on a 512K-byte block. In addition to this, thanks to multi-plane architecture, it is possible to program 2 pages a time (one per each plane) or to erase 2 blocks a time (again, one per each plane). As a consequence, multi-plane architecture allows time reduction. Data in the page can be read out at 25ns cycle time per byte.(30ns for cache Read)

The I/O pins serve as the ports for address and data input / output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using $\overline{CE}$, $\overline{WE}$, ALE and CLE input pin. The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the $\overline{WP}$ Input.

The output pin R/$\overline{B}$ (open drain buffer) signals the status of the device during each operation.

In a system with multiple memories the R/$\overline{B}$ pins can be connected all together to provide a global status signal. Even the write-intensive systems can take advantage of the H27UDG8VEM (TBD) extended reliability of 5K program/erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.

The chip supports $\overline{CE}$ don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the $\overline{CE}$ transitions do not stop the read operation.

The copy-back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase.

The cache program feature allows the data insertion in the cache register while the data register is copied into the flash array. This pipelined program operation improves the program throughput when long files are written inside the memory.

A cache read feature is also implemented. This feature allows to dramatically improve read throughput when consecutive pages have to be streamed out.

This device includes also extra Features like OTP/Unique ID area, Read ID2 extension.

The H27UDG8VEM (TBD) is available in 52 - VLGA(TBD)

1.1 Product List

PART NUMBER	ORGANIZATION	Vcc RANGE	PACKAGE
H27UDG8VEM	x8	2.7~3.6 Volt	52 - VLGA

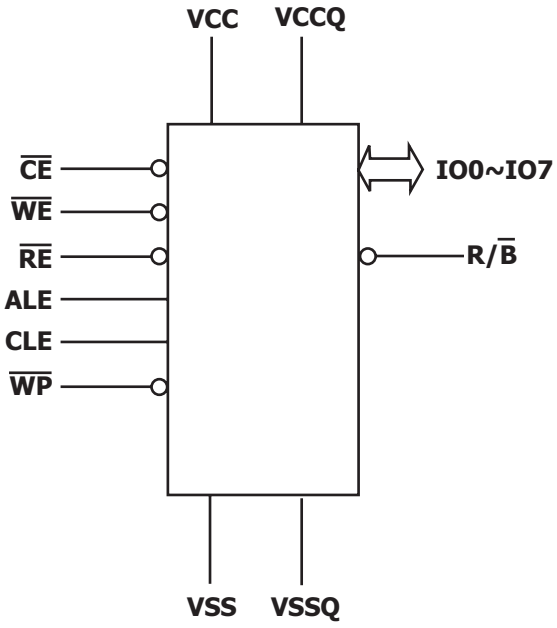


Figure 1 : Logic Diagram

IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready / Busy
VCCQ	I/O Power
VCC	Power Supply
VSSQ	I/O Ground
VSS	Ground
NC	No Connection

Table 1 : Signal Name

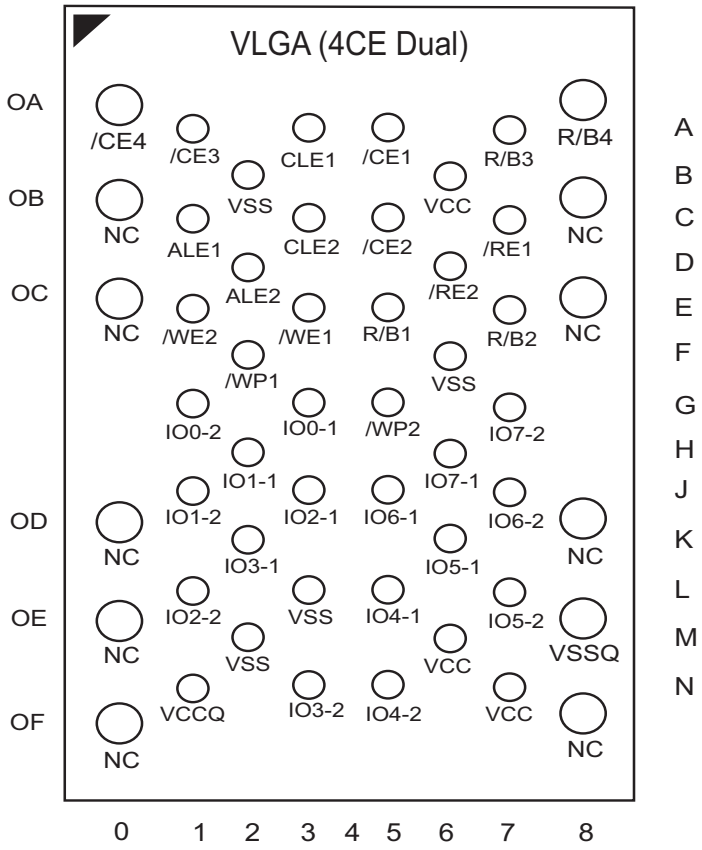


Figure 2 : 52 - VLGA Contact, X8 Device (Top View Through Package)

1.2 PIN DESCRIPTION

Pin Name	Description
IO0-1~IO7-1, IO0-2~IO7-2	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE}$1, $\overline{CE}$2, $\overline{CE}$3 & $\overline{CE}$4	**CHIP ENABLE** This input controls the selection of the device.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B}$1, R/$\overline{B}$2, R/$\overline{B}$3 & R/$\overline{B}$4	**READY BUSY** The R/$\overline{B}$1, R/$\overline{B}$2 output is an Open Drain pin that signals the state of the memory.
VCCQ	**SUPPLY VOLTAGE FOR IO BUFFER**
VCC	**SUPPLY VOLTAGE** The Vcc supplies the power for all the operations (Read, Write, Erase).
VSSQ	**GROUND FOR IO BUFFER**
VSS	**GROUND**
NC	**NO CONNECTION**

Table 2 : Pin Description

NOTE:

1. IO-1~IO7-1,CLE1, ALE1, WE#1, RE#1 and WP#1 constitute the first channel, while IO-2~IO7-2, CLE2, ALE2, WE#2, RE#2 and WP#2 constitute the second channel.
2. CE#1 with R/B#1 and CE#3 with R/B#3 are mapped to the first channel, while CE#2 with R/B#2 and CE#4 with R/B#4 are mapped to the second channel.
3. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	A12	L(1)	L(1)	L(1)
3rd Cycle	A13	A14	A15	A16	A17	A18	A19	A20
4th Cycle	A21	A22	A23	A24	A25	A26	A27	A28
5th Cycle	A29	A30	A31	A32	L(1)	L(1)	L(1)	L(1)

Table 3 : Address Cycle Map(x8)

NOTE:
1. L must be set to Low.

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
PAGE READ	00h	30h			
PAGE PGM (start) / CACHE PGM (end)	80h	10h			
BLOCK ERASE	60h	D0h			
READ FOR COPY-BACK	00h	35h			
COPY-BACK PGM	85h	10h			
MULTI-PLANE CACHE READ START	60h	60h	33h		
SINGLE/MULTI-PLANE CACHE READ	31h				
SINGLE/MULTI-PLANE CACHE READ END	3Fh				
CACHE PGM (start)	80h	15h			
READ STATUS REGISTER	70h/F1h				Yes
RANDOM DATA INPUT	85h				
RANDOM DATA OUTPUT	05h	E0h			
MULTI-PLANE PAGE READ	60h	60h	30h		
MULTI-PLANE PAGE PGM / MULTI-PLANE CACHE PGM (end)	80h	11h	81h	10h	
MULTI-PLANE BLOCK ERASE	60h	60h	D0h		
MULTI-PLANE READ FOR COPY-BACK	60h	60h	35h		
MULTI-PLANE COPY-BACK PGM	85h	11h	81h	10h	
Multi-Plane CACHE PGM (start)	80h	11h	81h	15h	
Multi-Plane Data Output	00h	05h	E0h		
READ ID	90h				
RESET	FFh				Yes

Table 4 : Command Set

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input(5 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input(5 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L(1)	H	Falling	X	Data Output	
X	X	X	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc	Stand By	

Table 5 : Mode Selection

NOTE:
1. With the $\overline{CE}$ don't care option $\overline{CE}$ high during latency time does not stop the read operation

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

Typically glitches less than 5ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover, for commands that start a modifying operation (write/erase) the Write Protect pin must be high. See Figure 4 and Table12 for details of the timings requirements. Command codes are always applied on IO7:0, disregarding the bus configuration.

2.2 Address Input

Address Input bus operation allows the insertion of the memory address. Five cycles are required to input the addresses for the 32Gbit devices. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable high and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 5 and Table 12. AC Timing Characteristics for details of the timings requirements. Addresses are always applied on IO(7:0), disregarding the bus configuration.

In addition, addresses over the addressable space are disregarded even if the user sets them during command insertion.

2.3 Data Input

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 6 and Table 12 for details of the timings requirements.

2.4 Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See figures 7, 8, 10, 11, 12 and Table 12 for details of the timings requirements.

2.5 Write Protect

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up phases.

2.6 Standby

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced. Stand-by is obtained holding high, at least for 10us, $\overline{CE}$ pin.

3. DEVICE OPERATION

3.1 Page Read

Upon initial device power up, the device defaults to page read mode. This operation is also initialized by 00 h to the command register along with followed by five address input cycles. In consecutive read operations, 00h command does not need to be written for the followed page read operation.

Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 4,320 bytes of data within the selected page are transferred to the data registers in less than 60us (tR). The system controller may detect the completion of this data transfer 60us (tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns cycle time by sequentially pulsing RE. The repetitive high to low transitions of the $\overline{RE}$ clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

3.2 Multi Plane Read

Multi-Plane Page Read is an extension of Page Read, for a single plane with 4,320 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 4,320 byte page resisters enables a random read of two pages. Multi-Plane Page Read is initiated by repeating command 60h followed by three address cycles twice. The page and block addresses for both planes must be identical.

After Read Confirm command (30h) the 8,640 bytes of data within the selected two pages are transferred to the data registers in less than 60us (tR). The system controller can detect the completion of data transfer (tR) by monitoring the output of R/$\overline{B}$ pin.

Once the data is loaded into the data registers, the data output of first plane can be read out by issuing command 00h with Five Address Cycles, command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences. The restrictions for Multi-Plane Page Read are shown in Figure 13. Multi-Plane Page Read must be used in the block which has been programmed with Multi-Plane Page Program.

3.3 Page Program

The device is programmed by page. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 times. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 4,320bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register.

The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked.

The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s.

The command register remains in Read Status command mode until another valid command is written to the command register. Figure 14 details the sequence.

3.4 Multi Plane Program

Device supports multiple plane program: it is possible to program in parallel 2 pages, one per each plane.

A multiple plane program cycle consists of a double serial data loading period in which up to 8,640bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A<20>=0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY). Once it has become ready again, 81h command must be issued, followed by 2nd page address(5 cycles) and its serial data input.The page and block addresss for this page must be the same as the first page, except that it must be within the 2nd plane (A<20>=1). The data of 2nd page other than those to be programmed do not need to be loaded. Program Confirm command (10h) makes parallel programming of both pages start. User can check operation status by R/$\overline{B}$ pin or read status register command, as if it were a normal page program; status register command is also available during Dummy Busy time (tDBSY). In case of fail in 1st or 2nd page program, fail bit of status register will be set: Device supports pass/fail status of each plane. (IO0 : Total, IO1: Plane0, IO2: Plane1). Figure 16 details the sequence.

3.5 Block Erase

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60h). Only address A20 to A32 is valid while A13 to A19 is ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify.

Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. Figure 17 details the sequence.

3.6 Multi Plane Erase.

Multiple plane erase, allows parallel erase of two block, one per each memory plane.

Block erase setup command (60h) must be repeated two times, each time followed by 3 Address cycles in which the block address should be indentical except the plane address (AX<20>). As for block erase, D0h command makes embedded operation start. Multi plane erase does not need any Dummy Busy Time between 1st and 2nd block address insertion. Address limitation required for multiple plane program applies also to multiple plane erase, as well as operation progress can be checked like for multiple plane program. Figure 18 details the sequence

3.7 Copy-Back Program

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 4,320-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h or F1h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked (Figure 19 & Figure 20). The command register remains in Read Status command mode until another valid command is written to the command register. During copy-back program, data modification is possible using random data input command (85h) as shown in Figure 20.

3.8 Multi-Plane Copy-Back Program

Two-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 4,320 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 4,320 byte page registers enables a simultaneous programming of two pages. Figure 21 and Figure 22 show command sequence for the multi-plane copy-back operation. First case, Figure 21, shows random data input of two planes which started right after finishing random data output of previous two planes. Second case, Figure 22, shows the random data input of each plane which started right after finishing the random data output of each plane. Multi-Plane copyback function must be used in the block which has been programmed with Multi-Plane Page Program. The page and block address restrictions for multi-plane page read and program operations apply as well.

3.9 Cache Read

To improve page read throughput, sequential pages within a block, cache register is used. First step is same as normal page read, issuing a page read sequence (00-30h). After random access (R/$\overline{B}$ returns to high), 31h command is latched into the command register. Data is being transferred from the data register to the cache register. While cache register data is outputted, next page is transferred from memory cell to data register. R/$\overline{B}$ will stay low during present page random accessing and previous page transferring to cache register. Because it is not necessary to output a whole page data before issuing another 31h command, if serial data output time exceeds random access time (tR), the random access time can be hidden. The subsequent pages are issued additional 31h commands. To terminate cache read, 3Fh command should be issued. This command transfer data from data register to the cache register without issuing next page read. During the Cache Read Operation, device doesn't allow any other command except Cache Read command. To carry out other operations Cache read must be ended by 3Fh command or operation must be reset.

3.10 Multi Plane Cache Read

The device supports multi-plane cache read, which enables high read throughput by reading two pages in parallel. Figure 24 shows the command sequence for the multi-plane cache read operation. Both confirm commands, 30h and 33h, are valid for the first page read sequence.The page and block address restrictions for multi-plane page read operation apply as well.

3.11 Cache program

Cache Program is an extension of the standard page program, which is executed with two 4,320 bytes registers, data registers and cache register. After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register, and then the cache write command (15h) is loaded to the command register. After that sequence, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state. After all data of the cache register is transferred into the data register, the device goes to the Ready state to load the next data into the cache register by issuing another cache program command sequence (80h-15h).

There are some restrictions for cache program operation.

1. The cache program command is available only within a block.
2. User must give address and data after 80h command.

The Busy time of first sequence equals the time it takes to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed as a pipeline method. On the second and cascading sequence, transfer from the cache register to the data register is held off until cell programming of current data register contents has been done.

Read Status command (70h or F1h) may be issued to find out when the cache register is ready by polling the Cache-Busy status bit (I/O 6). Also, the status bit (I/O 5) can be used to determine when the cell programming of the current data register contents is complete. Pass/fail status of only the previous page (I/O 1) is available upon the return to Ready state.

If the system monitors the progress of programming only with R/$\overline{B}$, the last page of the target programming sequence must be programmed with actual Page Program command (10h). If the Cache Program command (15h) is used instead, status bit (I/O5) must be polled to find out when the last programming is actually finished before starting other operations such as read. Pass/fail status is available in two steps. I/O 1 returns with the status of the previous page upon Ready or I/O6 status bit changing to "1", and later I/O 0 with the status of current page upon true Ready (returning from internal

programming) or I/O 5 status bit changing to "1". I/O 1 may be read together when I/O 0 is checked. See Table 5 and Figure 25 for more details.

3.12 Multi Plane Cache program

The device supports multi-plane cache program, which enables high program throughput by programming two pages The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A<20>=0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY). Once it has become ready again, 81h command must be issued, followed by 2nd page address (5 cycles) and its serial data input.The page and block address for this page must be the same as the first page, except that it must be within the 2nd plane (A<20>=1). The data of 2nd page other than those to be programmed do not need to be loaded. Cache Program confirm command (15h) makes parallel programming of both pages start. And last page inputs Program confirm command(10h). Figure 26 shows the command sequence for the multi plane cache program operation.

3.13 Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h or F1h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to Table 13 and 14 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.Table 13 and 14 apply to both single and multi plane operations

3.14 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, 5th, 6th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 27 shows the operation sequence, while tables 15 explain the byte meaning.

3.15 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to Table 13 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/$\overline{B}$ pin goes low for tRST after the Reset command is written. Refer to Figure 30.

4. OTHER FEATURES

4.1 Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2.0V (3.3V device). WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 31. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready / Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/$\overline{B}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tR (R/$\overline{B}$) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Figure 33). Its value can be determined by the following guidance.

4.3 Initialization after power up

After power-up, a reset command must be issued before any other command as denoted in Fiqure 32. As opposed to usual reset commands, this first reset command issues an initialization process on the device. The device stays busy for a maximum of 5ms and consumes a maximum of 40mA current during this process. 70h and F1h (Read Status Register) are the only commands allowed during this initialization process

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	N_{VB}	31968 (TBD)		32768	Blocks

Table 6 : Valid Blocks Number

NOTE :
1. The 1st block is guaranteed to be a valid block at the time of shipment.

Symbol	Parameter	Value	Unit
		Min	
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	℃
	Ambient Operating Temperature (Extended Temperature Range)	-25 to 85	℃
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	℃
V_{IO}	Input or Output Voltage	-0.6 to 4.6	V
V_{CC}	Supply Voltage	-0.6 to 4.6	V

Table 7 : Absolute maximum ratings

NOTE :
1. Except for the rating Operating Temperature Range, stresses above those listed in the Table Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Hynix SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

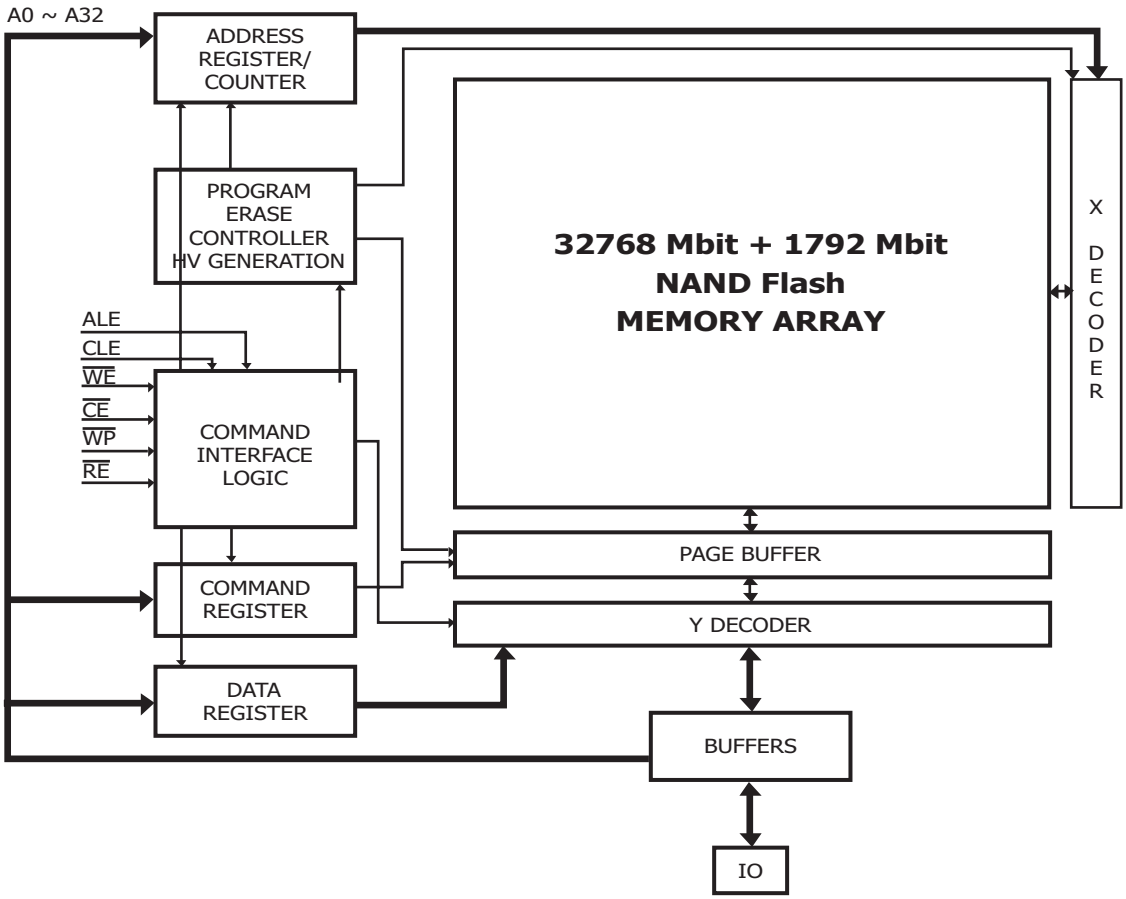


Figure 3 : Block Diagram

NOTE :
1. This block diagram applies to each CE#

Parameter		Symbol	Test Condition	3.3V			Unit
				Min	Typ	Max	
Power On Reset Command		Icc0	FFh COMMAND input after power on	-	20	40	mA
Operating Current	Read	Icc1	tRC=25ns CE#=VIL, Iout=0mA	-	20	40	mA
	Program (Normal)	Icc2		-	20	40	mA
	Program (Cache)	Icc2		-	30	50	mA
	Erase	Icc3		-	20	40	mA
Stand-by Current (TTL)		Icc4	CE#=VIH, WP#=0V/ Vcc	-	-	1	mA
Stand-by Current (CMOS)		Icc5	CE#=Vcc-0.2, WP#=0V/Vcc	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc max	-	-	10	uA
Output Leakage Current		ILO	Vout=0 to Vcc max	-	-	10	uA
Input High Voltage		VIH	-	Vccx0.8	-	Vcc+0.3	V
Input Low Voltage		VIL	-	-0.3	-	0.2xVcc	V
Output High Voltage Level		VOH	IOH=-400uA	2.4	-	-	V
Output Low Voltage Level		VOL	IOL=2.1mA	-	-	0.4	V
Output Low Current (R/ B#)		IOL (R/B#)	VOL=0.4V	8	10	-	mA

Table 8 : DC and Operating Characteristics

Parameter	Value
	3.3V
Input Pulse Levels	0 V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc / 2
Output Load (2.7V-3.6V)	1 TTL GATE and CL=50pF

Table 9 : AC Conditions

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	-	40	pF
$C_{I/O}$	Input/Output Capacitance	V_{IL} = 0V	-	40	pF

Table 10 : Pin Capacitance (TA=25C, F=1.0MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Program (following 10h)	t_{PROG}	-	1000(TBD)	3000(TBD)	us
Cache Program (following 15h)	t_{CBSYW}	-	-	3000(TBD)	us
Multi-Plane Program / Multi-Plane Cache Program / Multi-Plane Copy-Back Program (following 11h)	t_{DBSY}	-	3	5	us
Cache Read / Multi-Plane Cache Read / Copy (2) Cache Read (following 31h/3Ah/3Fh)	t_{CBSYR}		3	70	us
Block Erase / Multi-Plane Block Erase	t_{BERS}	-	3	10	ms
Number of partial Program Cycles in the same page	NOP	-	-	1	cycles

Table 11 : Program / Read / Erase Characteristics

Parameter	Symbol	3.3V		Unit
		Min	Max	
CLE setup time(Non-Cache Operation)	tCLS	12		ns
CLE setup time(Cache Operation)	tCLS	15		ns
CLE Hold time	tCLH	5		ns
CE# setup time(Non-Cache Operation)	tCS	20		ns
CE# setup time(Cache Operation)	tCS	25		ns
CE# hold time	tCH	5		ns
WE# pulse width(Non-Cache Operation)	tWP	12		ns
WE# pulse width(Cache Operation)	tWP	15		ns
ALE setup time(Non-Cache Operation)	tALS	12		ns
ALE setup time(Cache Operation)	tALS	15		ns
ALE hold time	tALH	5		ns
Data setup time(Non-Cache Operation)	tDS	12		ns
Data setup time(Cache Operation)	tDS	15		ns
Data hold time	tDH	5		ns
Write cycle time(Non-Cache Operation)	tWC	25		ns
Write cycle time(Cache Operation)	tWC	30		ns
WE# high hold time	tWH	10		ns
Data transfer from cell to register	tR		60	us
ALE to RE# delay	tAR	10		ns
CLE to RE# delay	tCLR	10		ns
Ready to RE# low	tRR	20		ns
RE# pulse width(Non-Cache Operation)	tRP	12		ns
RE# pulse width(Cache Operation)	tRP	15		ns
WE# high to busy	tWB		100	ns
Read cycle time(Non-Cache Operation)	tRC	25		ns
Read cycle time(Cache Operation)	tRC	30		ns
RE# access time(Non-Cache Operation)	tREA		20	ns
RE# access time(Cache Operation)	tREA		25	ns
RE# high to output high Z	tRHZ		100	ns
CE# high to output high Z	tCHZ		50	ns
RE# high to output hold	tRHOH	15		ns
RE# low to output hold	tRLOH	5		ns
RE# or CE# high to output hold	tCOH	15		ns
RE# high hold time	tREH	10		ns
CE# low to RE# low	tCR	10		ns
WE# high to RE# low	tWHR	80		ns
RE# high to WE# low	tRHW	100		ns
Output high Z to RE# low	tIR	0		ns
Address to data loading time	tADL	200		ns
Device resetting time (Read/Program/Erase)	tRST		20/50/500(1)	us

Write protection time	tWW(2)	100		ns

Table 12 : AC Timing Characteristics

NOTE:

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us
2. Program / Erase Enable Operation : $\overline{WP}$ high to $\overline{WE}$ High.
   Program / Erase Disable Operation : WP Low to $\overline{WE}$ High.

IO	Page Program	Block Erase	Read	Cache Read	Cache Program	Coding
0	Pass / Fail	Pass / Fail	NA	NA	Pass / Fail(N)	Pass : '0' Fail : '1'
1	NA	NA	NA	NA	Pass / Fail(N-1)	Pass : '0' Fail : '1'
2	NA	NA	NA	NA	NA	-
3	NA	NA	NA	NA	NA	-
4	NA	NA	NA	NA	NA	-
5	NA	NA	NA	Ready / Busy	Ready / Busy	Ready / Busy Busy : '0' Ready : '1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : '0' Not Protected : '1'

Table 13 : Status Register Coding For 70h

IO	Page Program	Block Erase	Read	Cache Read	Cache Program	Coding
0	chip Pass / Fail	Chip Pass / Fail	NA	NA	Chip Pass / Fail(N)	Pass : '0' Fail : '1'
1	Plane 0 Pass / Fail	Plane 0 Pass / Fail	NA	NA	Plane 0 Pass / Fail(N)	Pass : '0' Fail : '1'
2	Plane 1 Pass / Fail	Plane 1 Pass / Fail	NA	NA	Plane 1 Pass / Fail(N)	Pass : '0' Fail : '1'
3	NA	NA	NA	NA	Plane 0 Pass / Fail(N-1)	Pass : '0' Fail : '1'
4	NA	NA	NA	NA	Plane 1 Pass / Fail(N-1)	Pass : '0' Fail : '1'
5	NA	NA	NA	Ready / Busy	Ready / Busy	Ready / Busy Busy : '0' Ready : '1'
6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Ready / Busy Busy : '0' Ready : '1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : '0' Not Protected : '1'

Table 14 : Status Register Coding For F1h

Parameter	Symbol
Device Identifier Byte	Description
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell Type, Number of Simultaneously Programmed Pages, Interleaved Program, Write Cache.
4th	Page size, Block size, Redundant area size
5th	Plane Number, ECC Level
6th	Technology (Design Rule), EDO, Interface

Table 15 : Device Identifier Coding

Part Number	Voltage	Bus Width	Manufacture Code	Device Code	3rd	4th	5th	6th
H27UDG8VEM	3.3 V	x8	ADh	D7h	94h	25h	44h	41h

Table 16 : Read ID Data Table

3rd cycle	Description	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
Internal Chip Number	1 2 4 Reserved							0 0 1 1	0 1 0 1
Cell Type	1 bit / Cell 2 bit / Cell 3 bit / Cell 4 bit / Cell					0 0 1 1	0 1 0 1		
Number of Simutaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleaved Program between Multiple dice	Not Supported Supported		0 1						
Write Cache	Not Supported Supported	0 1							

4th cycle	Description	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
Page Size (without Spare Area)	2 KB 4 KB 8 KB Reserved							0 0 1 1	0 1 0 1
Block Size (without Spare Area)	128 KB 256 KB 512 KB 768 KB 1 MB Reserved Reserved Reserved	0 0 0 0 1 1 1 1		0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Redundant Area Size	128 B 224 B Reserved Reserved Reserved Reserved Reserved Reserved		0 0 0 0 1 1 1 1			0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1		

5th cycle	Description	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
ECC Level	1 bit / 512 B 2 bit / 512 B 4 bit / 512 B 8 bit / 512 B 12 bit / 512 B 16 bit / 512 B Reserved Reserved		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Reserved		0						0	0

6th cycle	Description	I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
NAND Technology	48 nm 41 nm Reserved Reserved Reserved Reserved Reserved Reserved						0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1
EDO Supported	Not Supported Supported		0 1						
NAND Interface	SDR DDR	0 1							
Reserved				0	0	0			

Table 17 : 3rd, 4th, 5th and 6th bytes of Device Identifier Description

5. AC Timing Diagrams

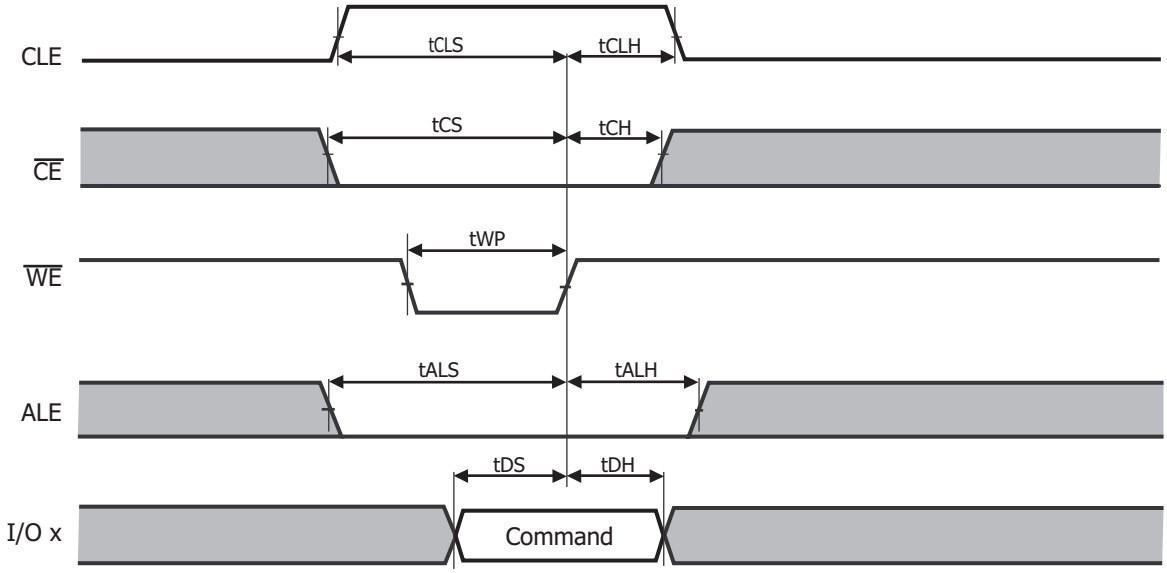


Figure 4 : Command Latch Cycle

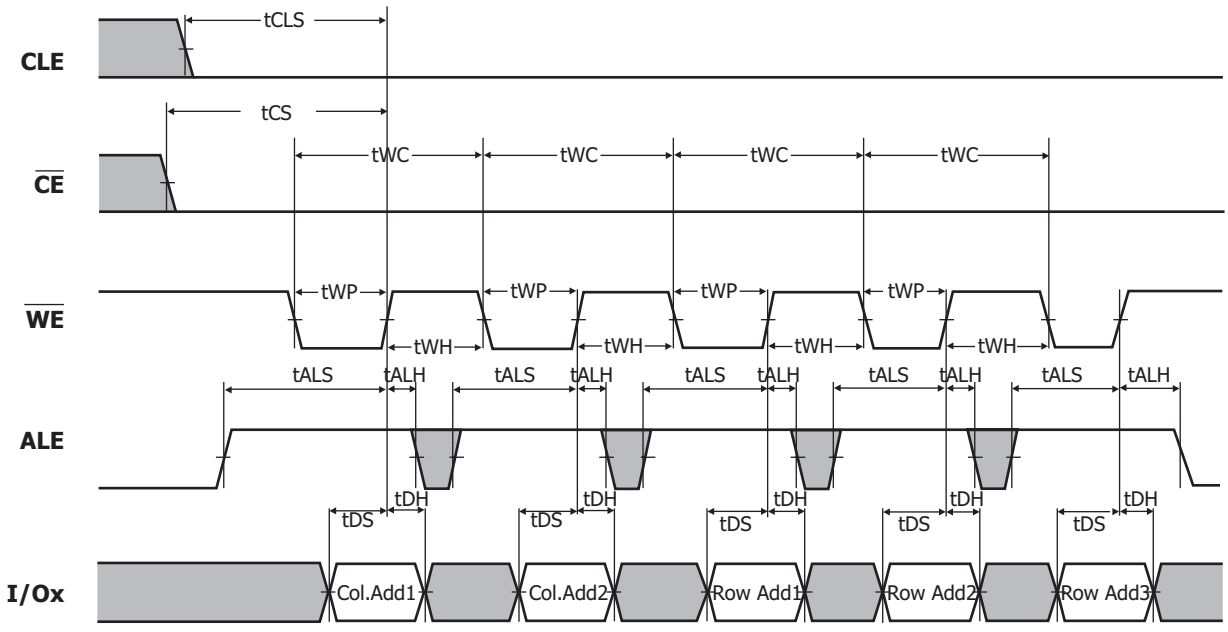


Figure 5 : Address Latch Cycle

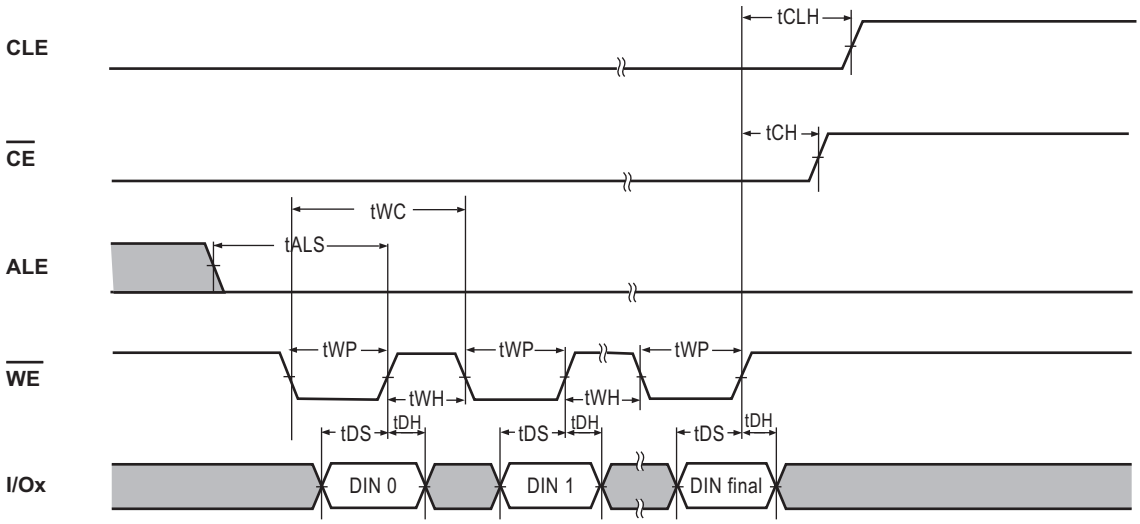
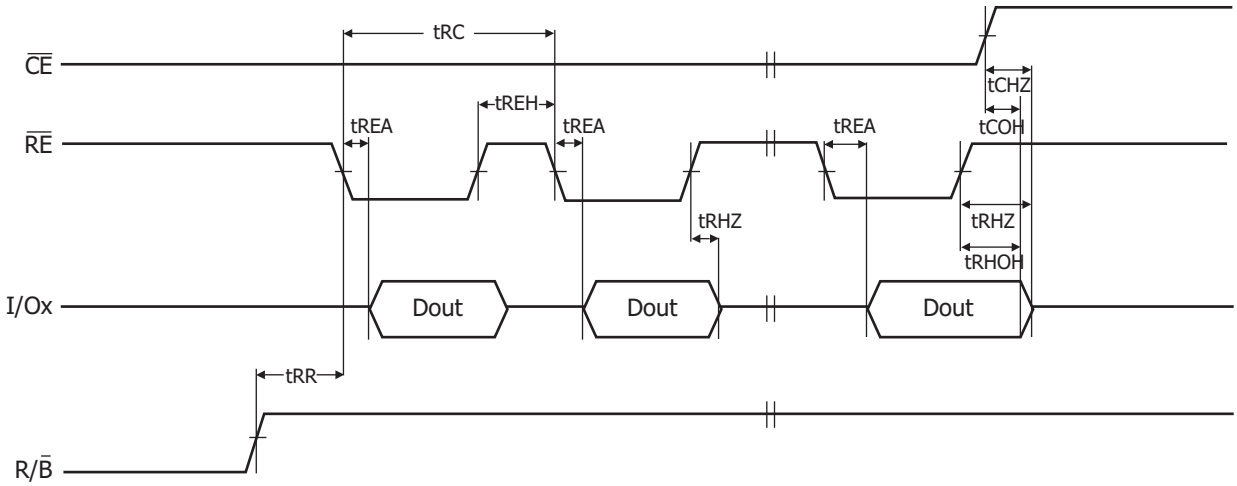
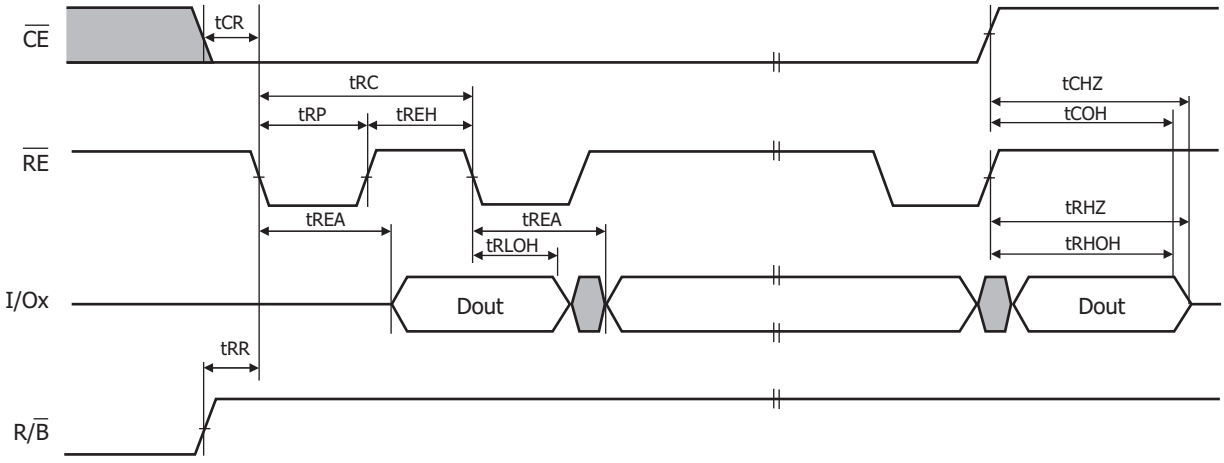


Figure 6 : Input Data Latch Cycle



Notes: 1. Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
2. tRHOH starts to be valid when frequency is lower than 33MHz.
3. tRLOH is valid when frequency is higher than 33MHZ.

Figure 7 : Sequential Out Cycle after Read (CLE=L, WE#=H, ALE=L)



Notes: 1. Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
2. tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 8 : Sequential Out Cycle after Read (EDO Type CLE=L, $\overline{WE}$=H, ALE=L)

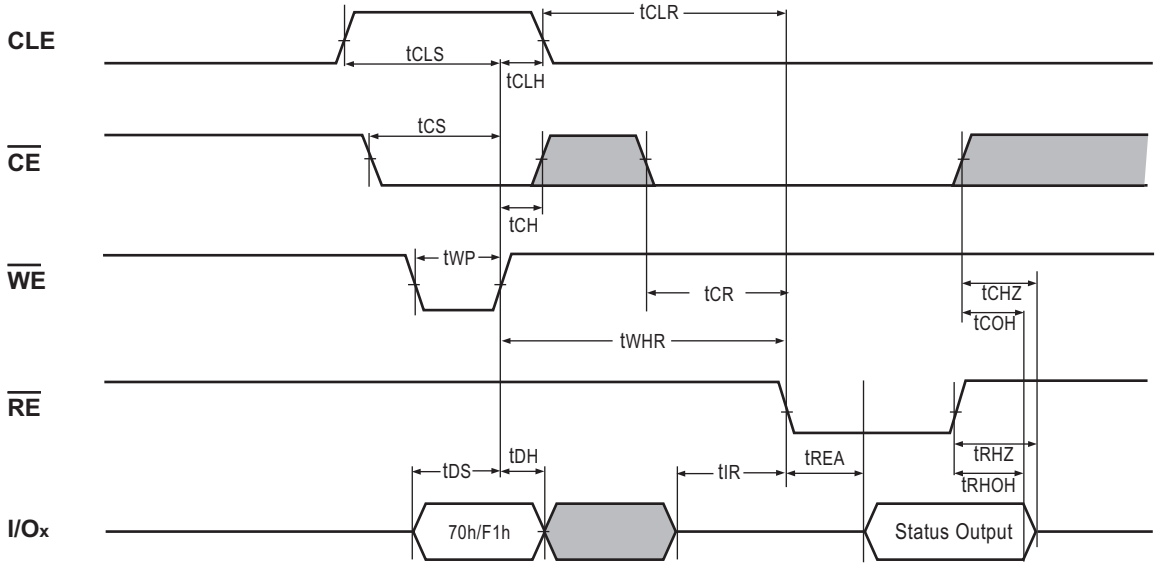


Figure 9 : Status Read Cycle

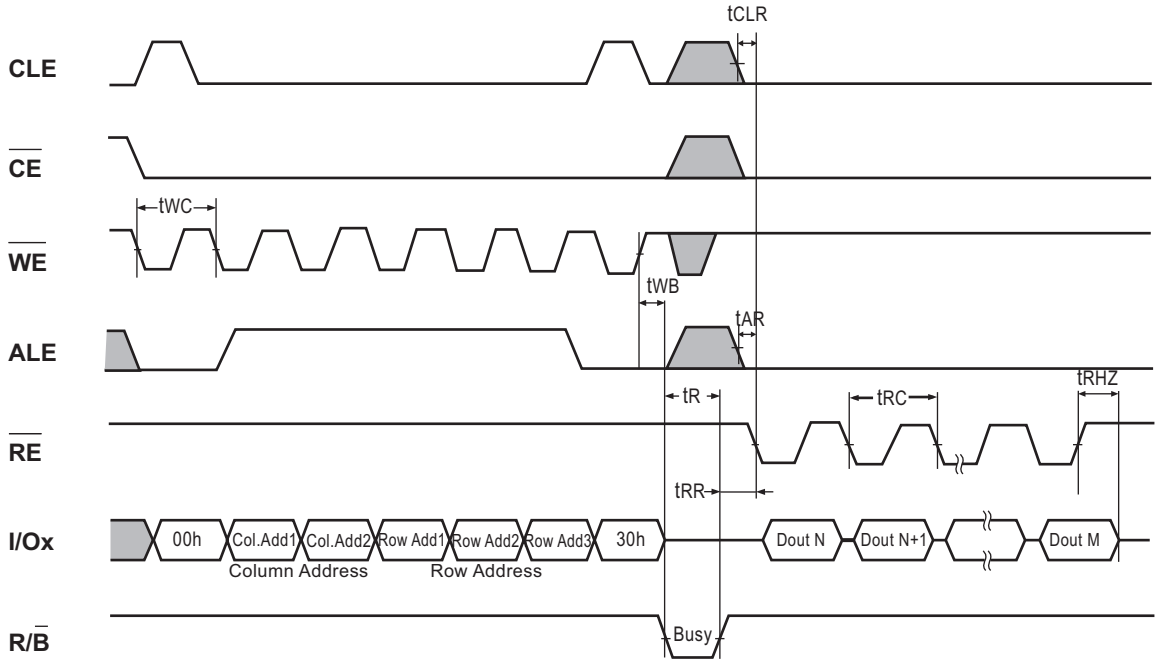


Figure 10 : Page Read Operation (Read One Page)

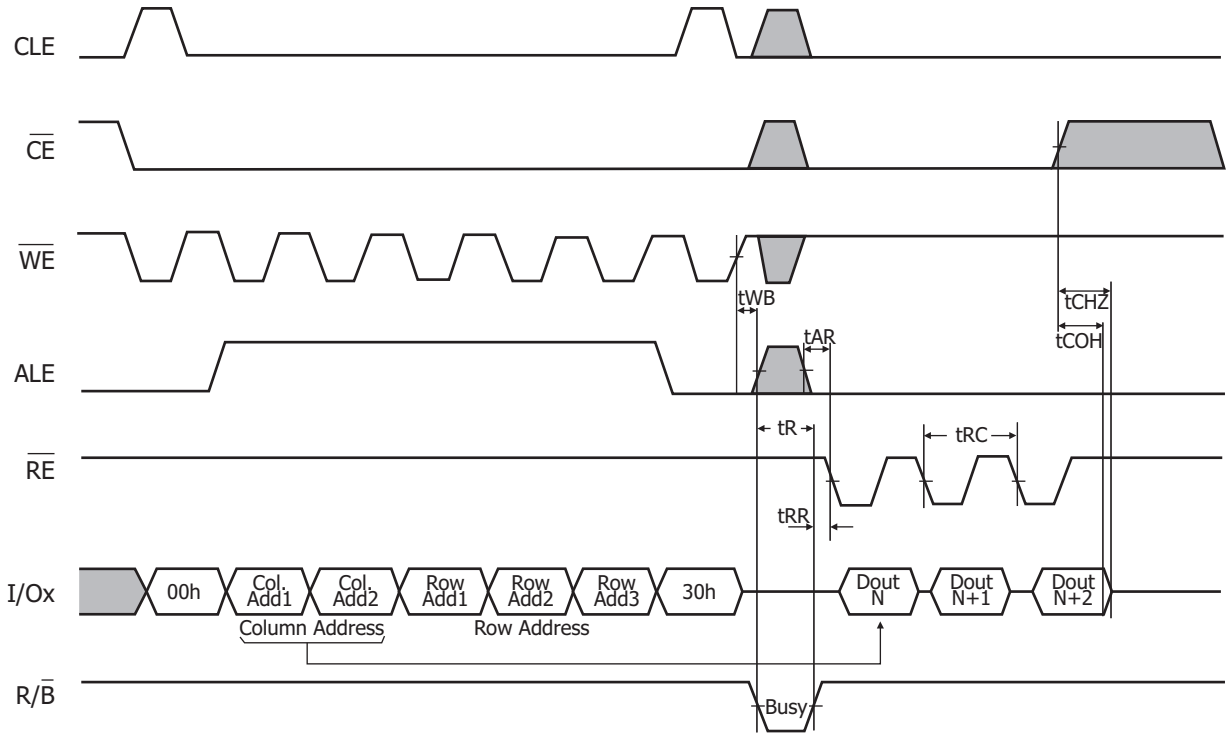


Figure 11 : Page Read Operation intercepted by $\overline{CE}$

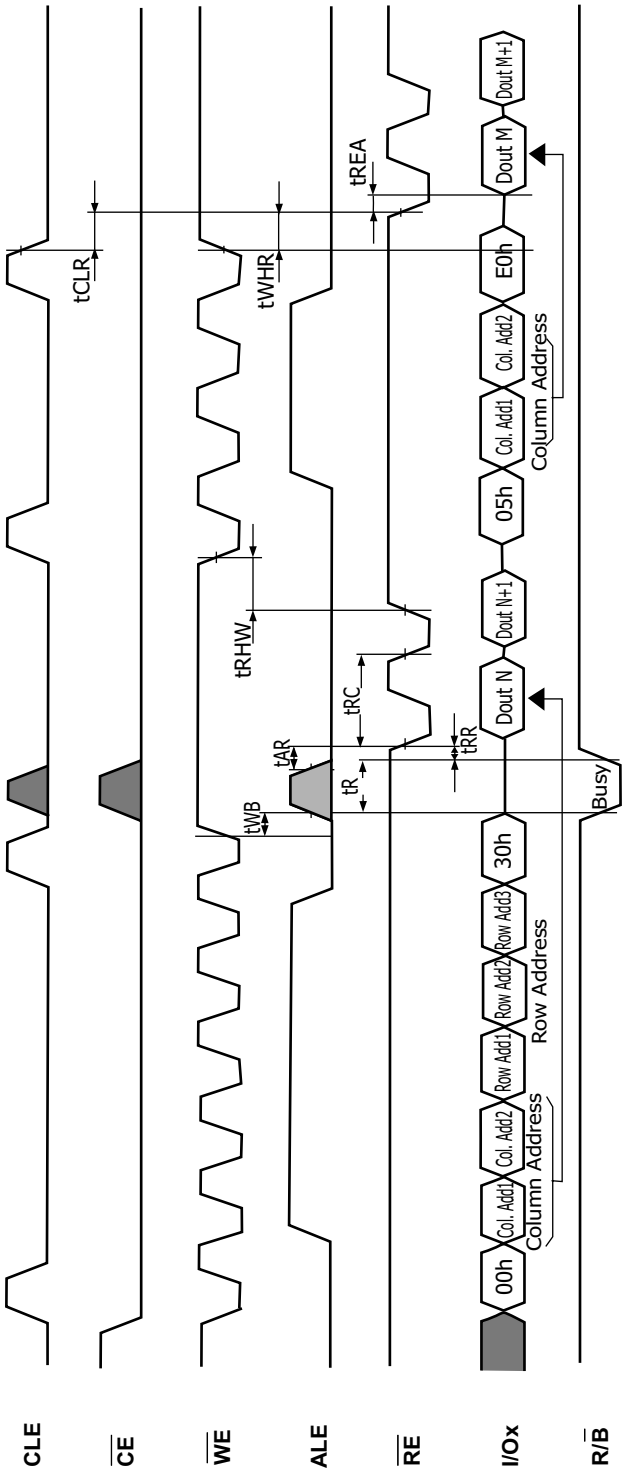


Figure 12 : Random Data Output

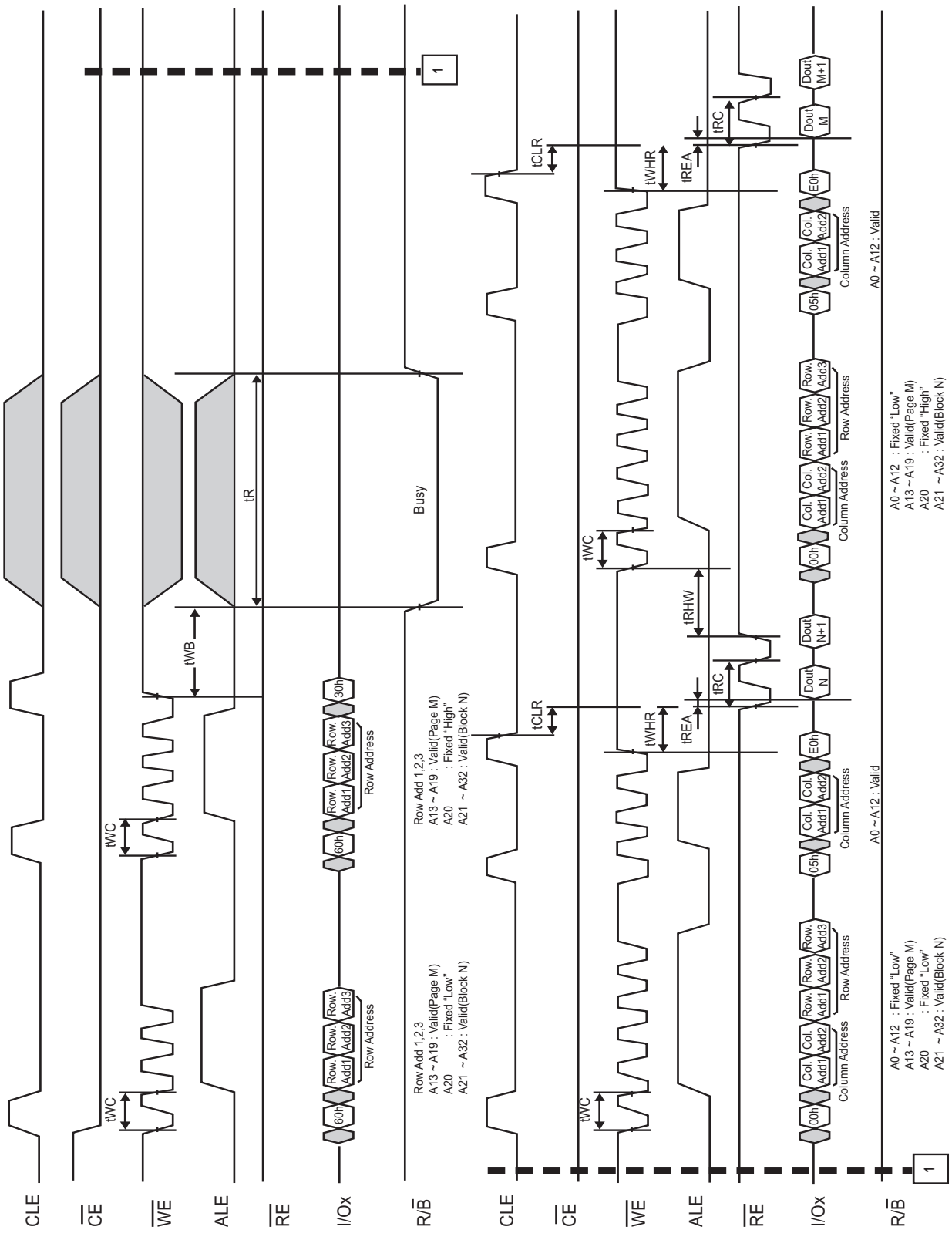
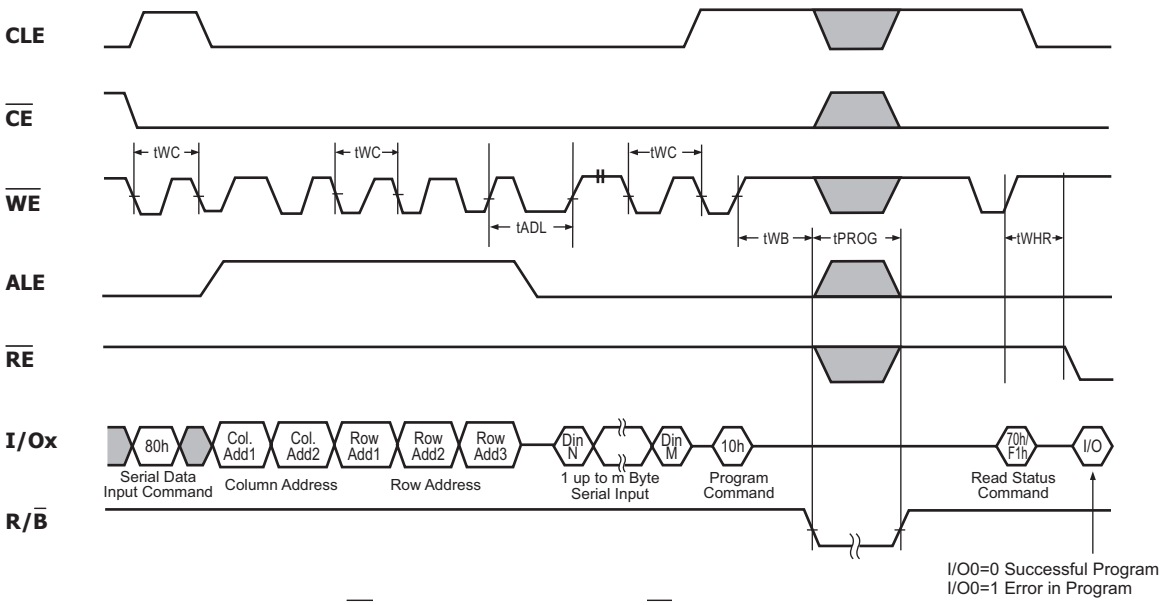
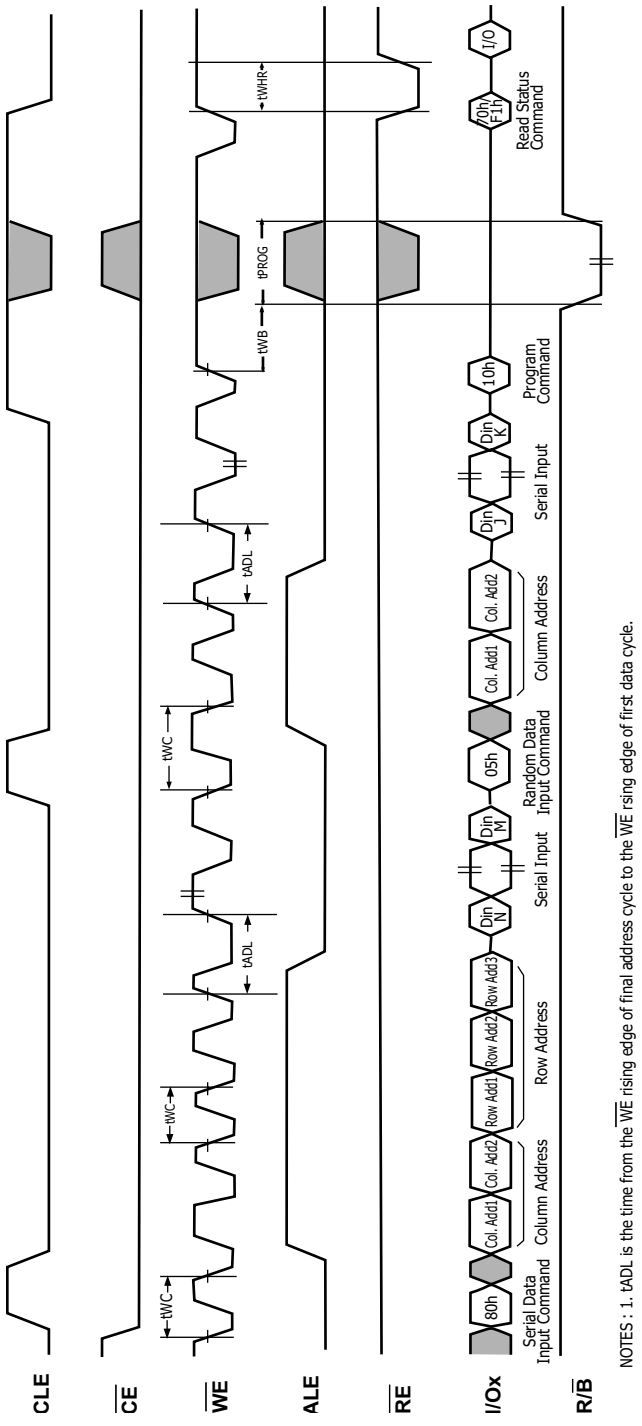


Figure 13 : Multi Plane Page Read Operation with Random Data Output



NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Figure 14 : Page Program Operation



NOTES : 1. tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Figure 15 : Random Data Input

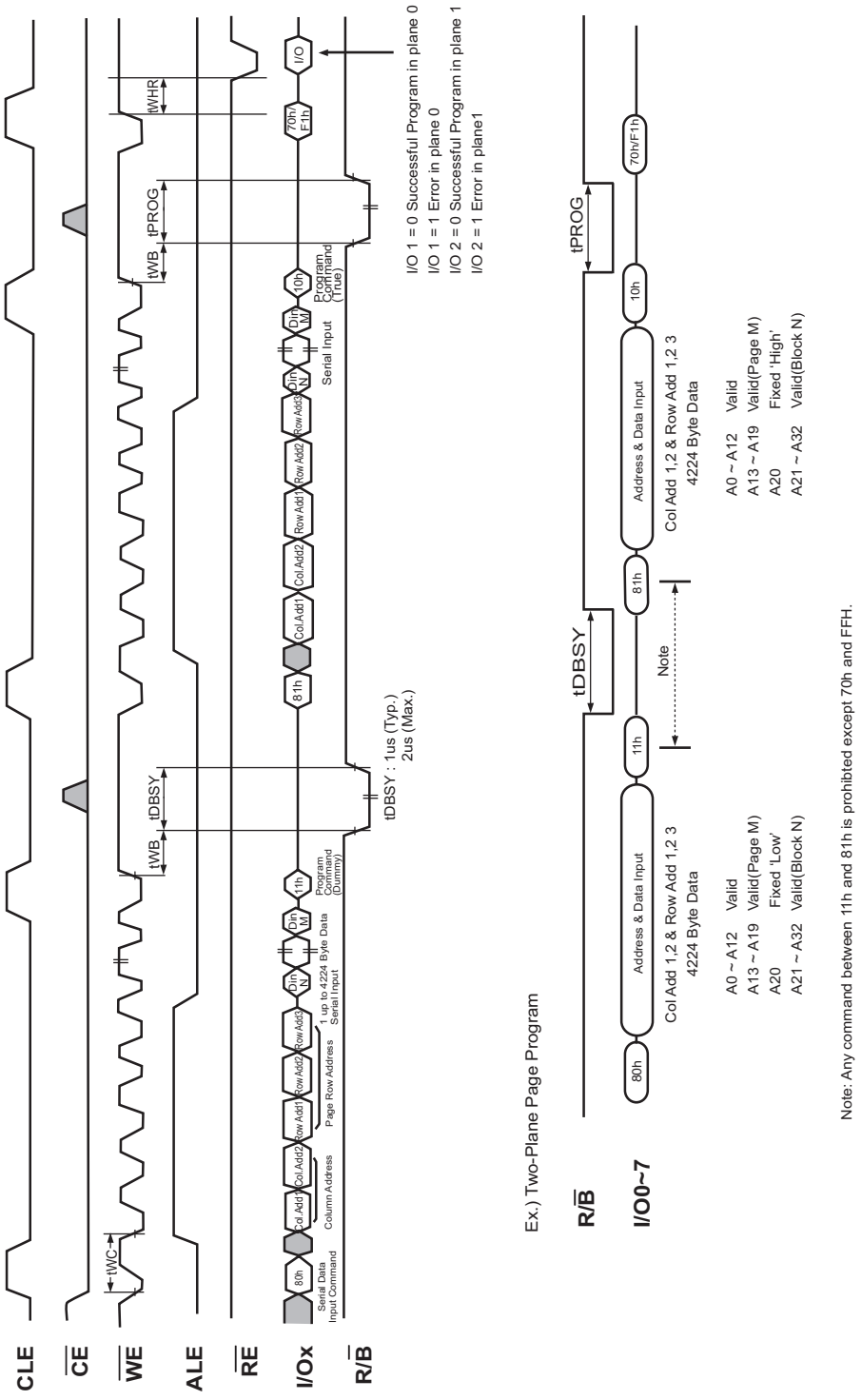


Figure 16 : Multi Plane Page Program Opeartion

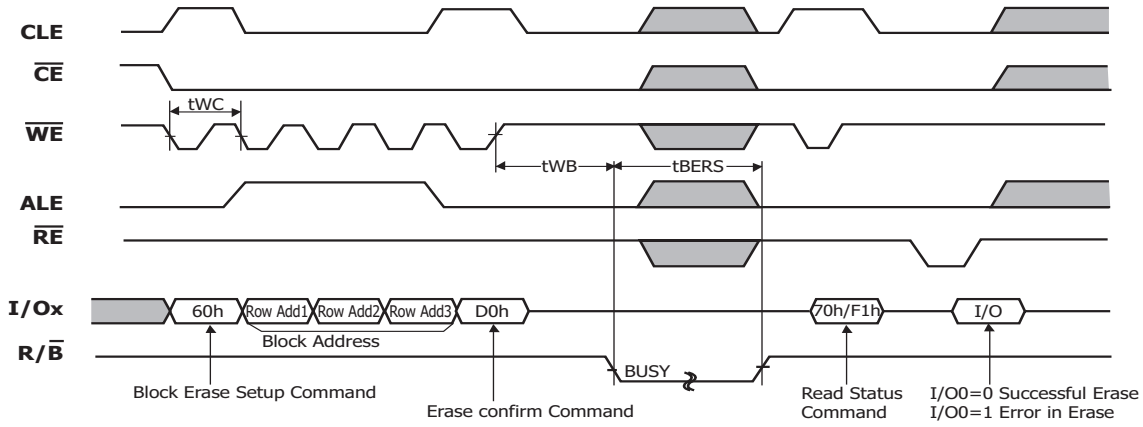
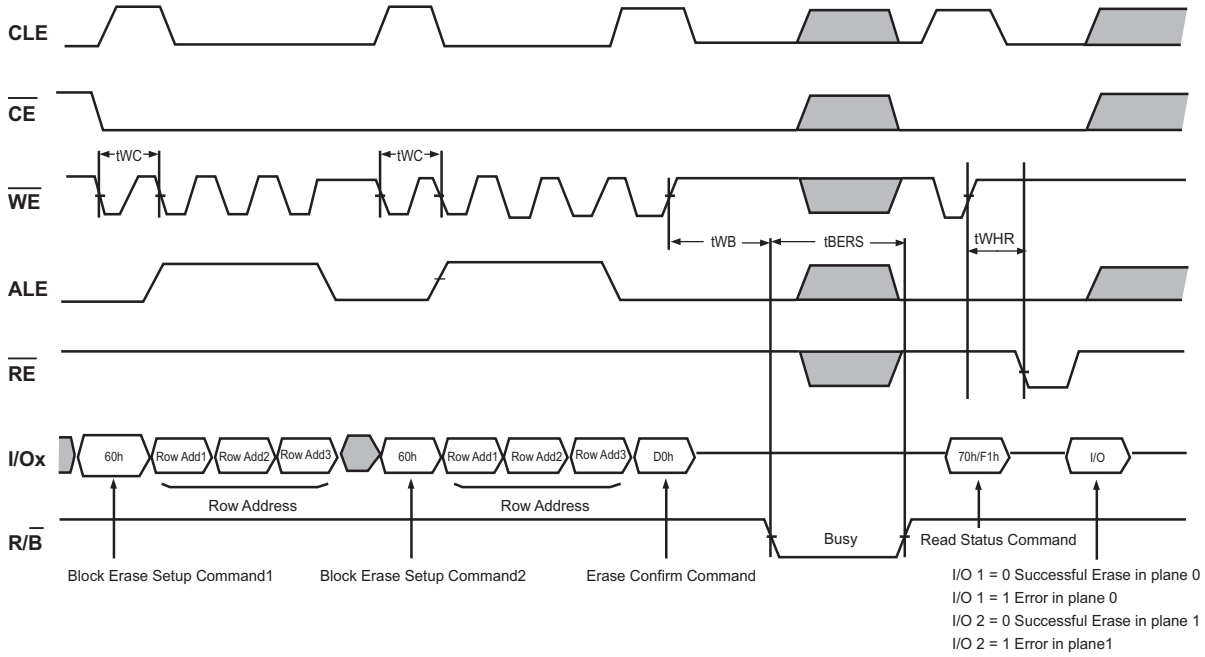


Figure 17 : Block Erase Operation (Erase One Block)



Ex.) Address Restriction for Two-Plane Block Erase Operation

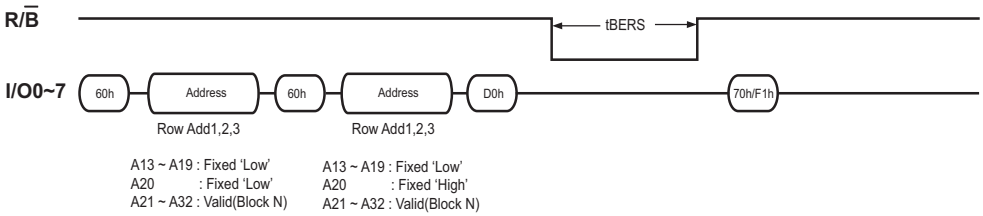


Figure 18 : Multi Plane Block Erase Operation

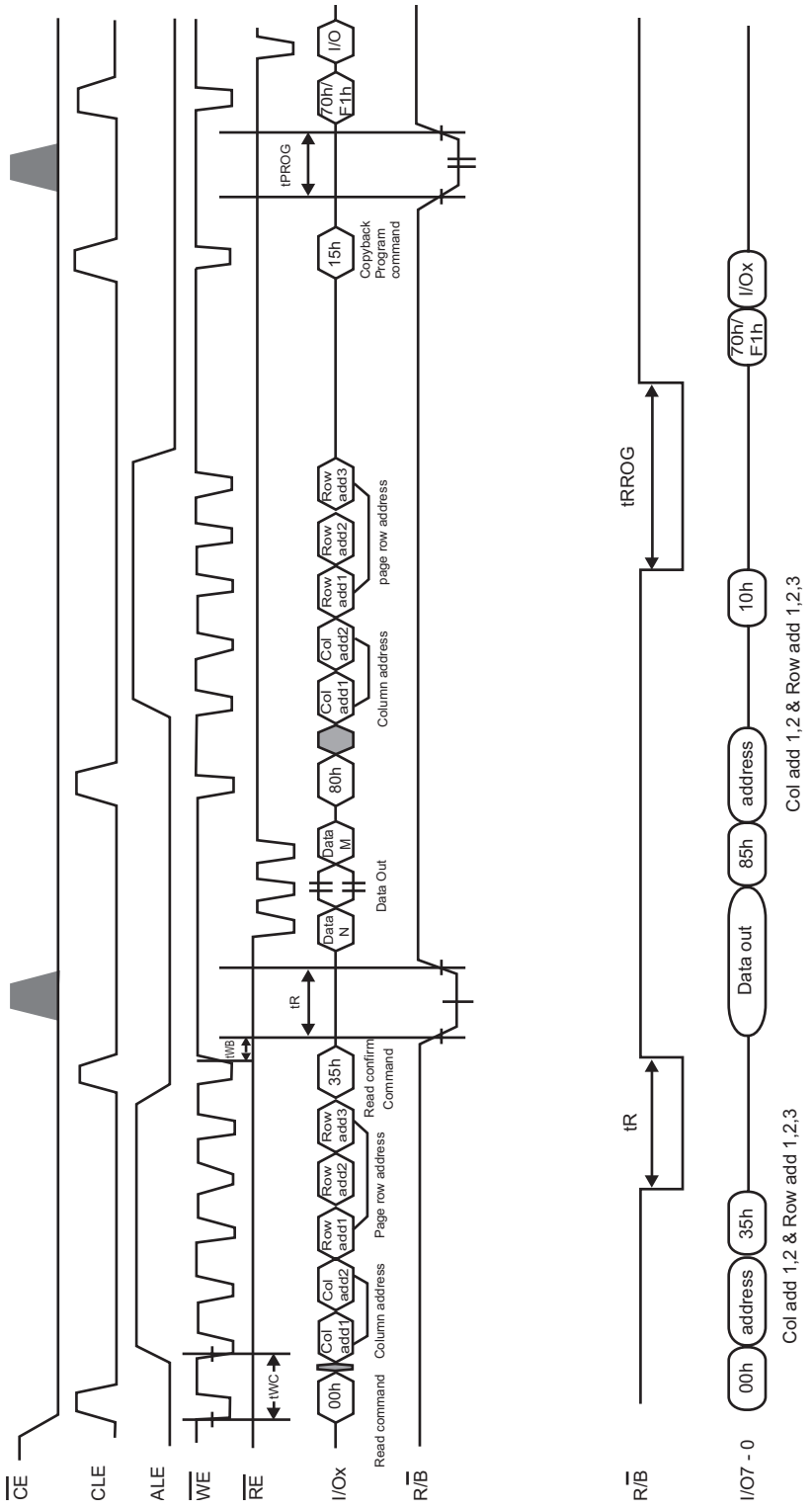


Figure 19 : Copy-Back Program Operation

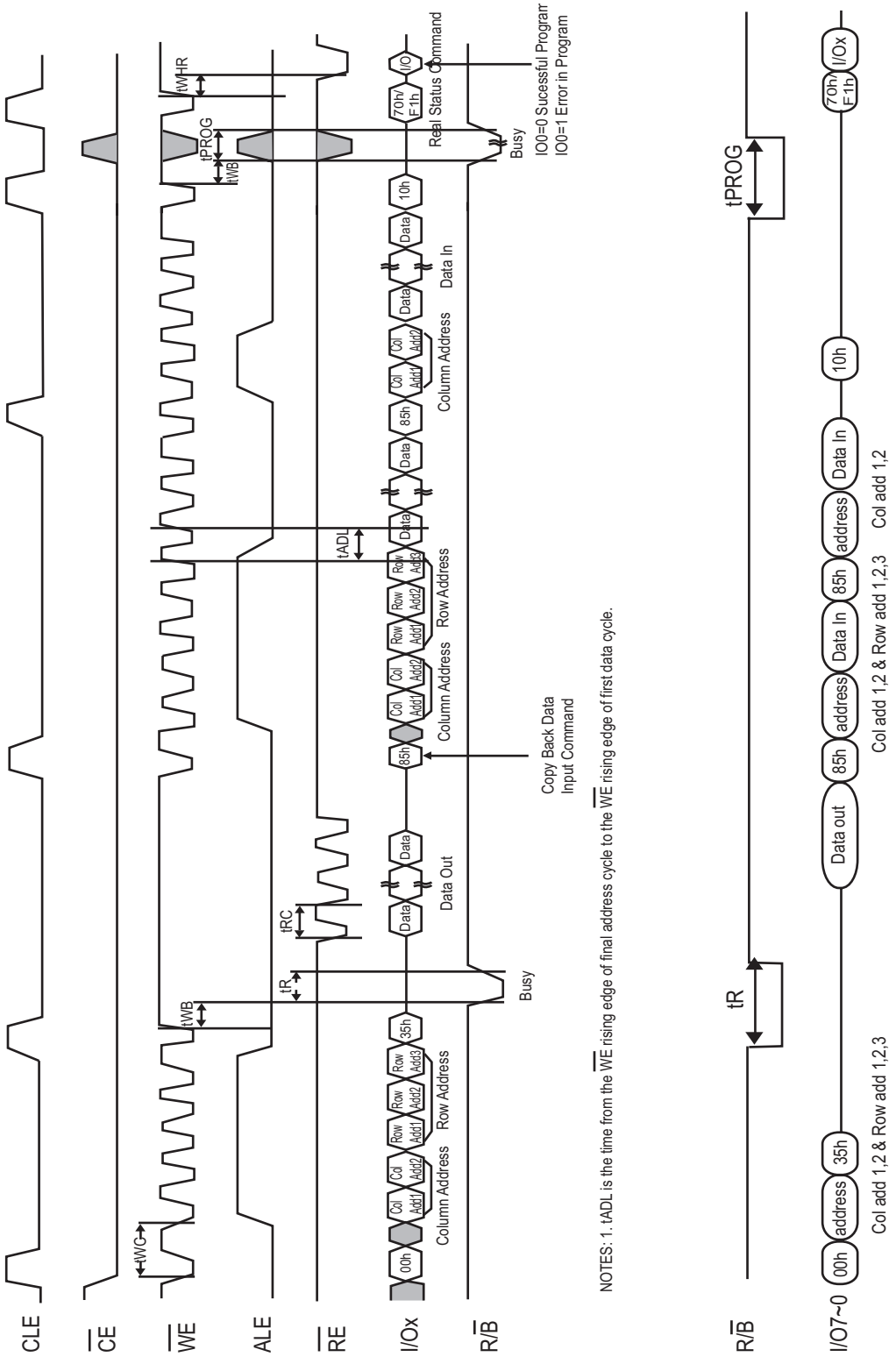
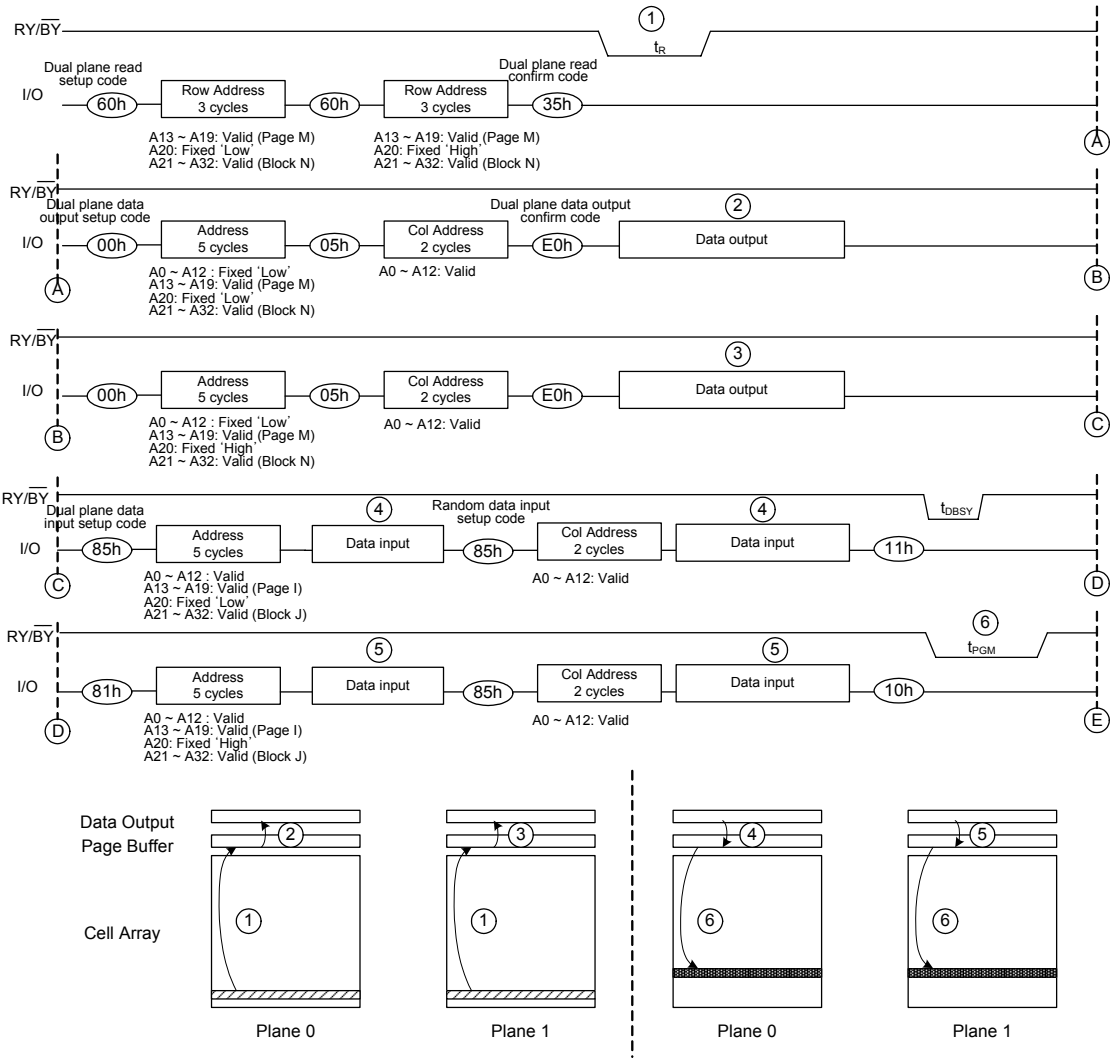


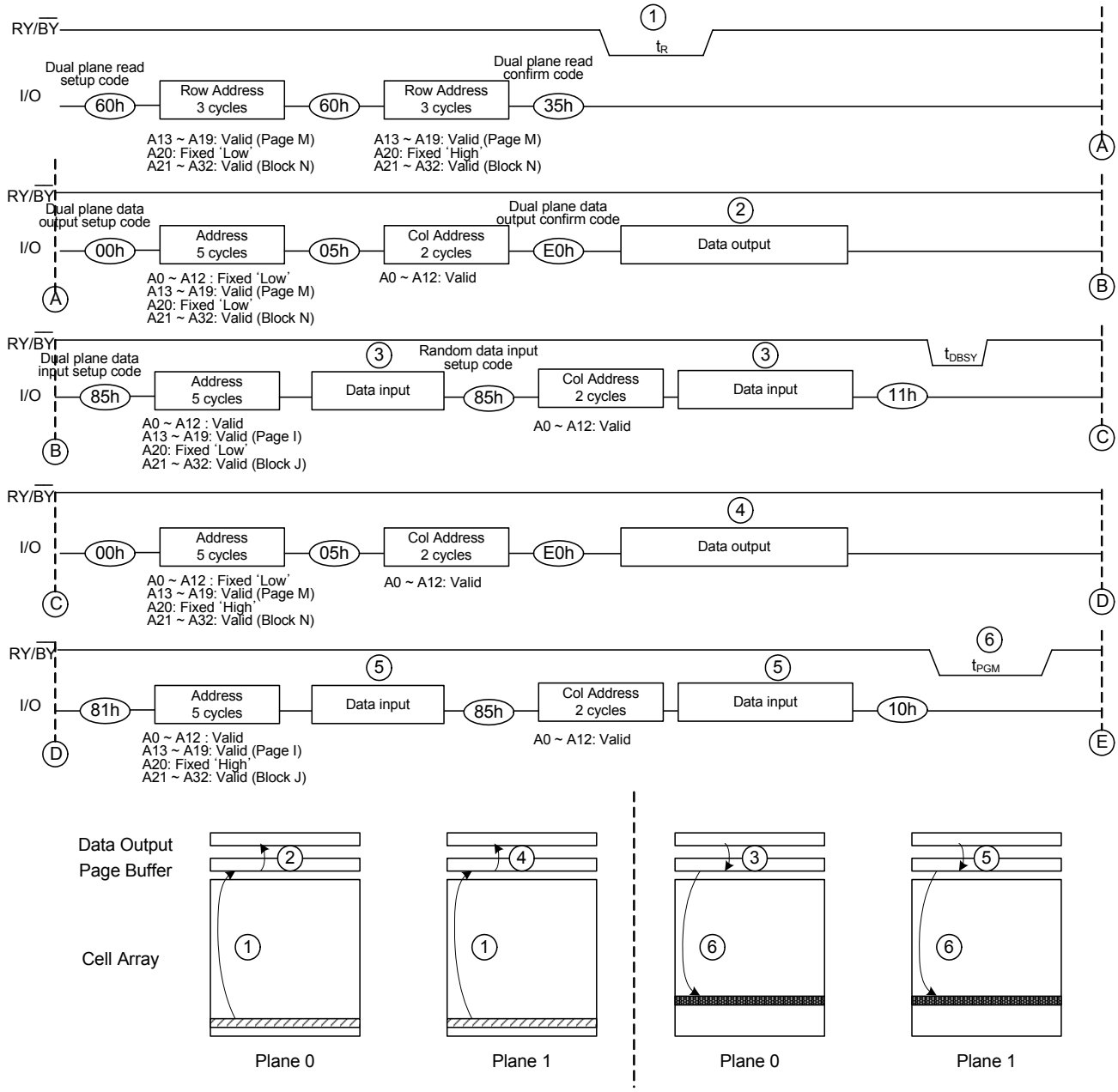
Figure 20 : Copy-Back Program Operation with Random Data Input



Note:

1. Copy back operation is allowed only within the same memory plane.
2. Any command between 11h and 81h is prohibited except 70h, F1h and FFh.

Figure 21 : Multi Plane Copy-Back Program Sequence



Note:

1. Copy back operation is allowed only within the same memory plane.

Figure 22 : Multi Plane Copy-Back Program Sequence with 4 KB Buffer

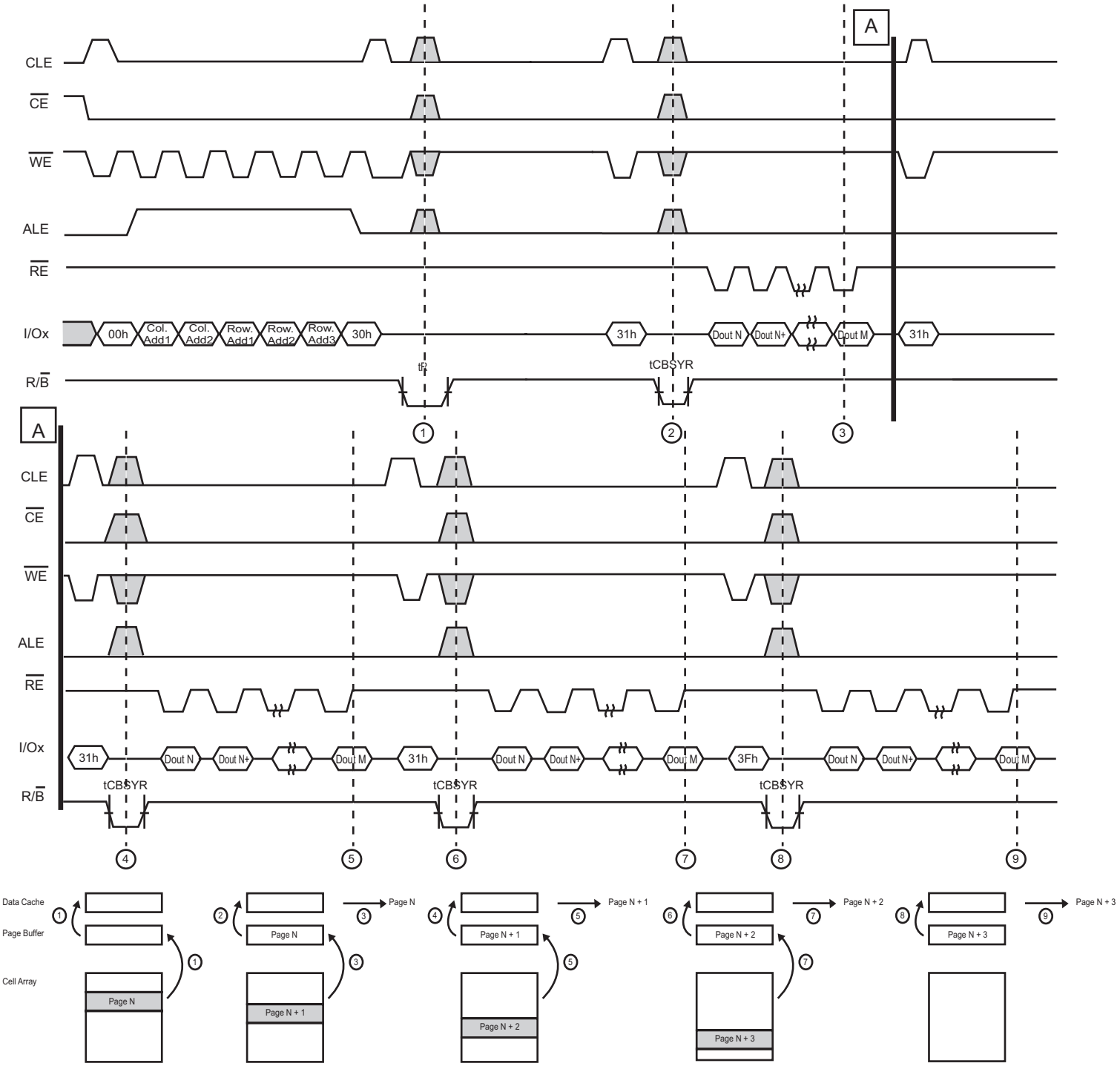


Figure 23 : Cache Read

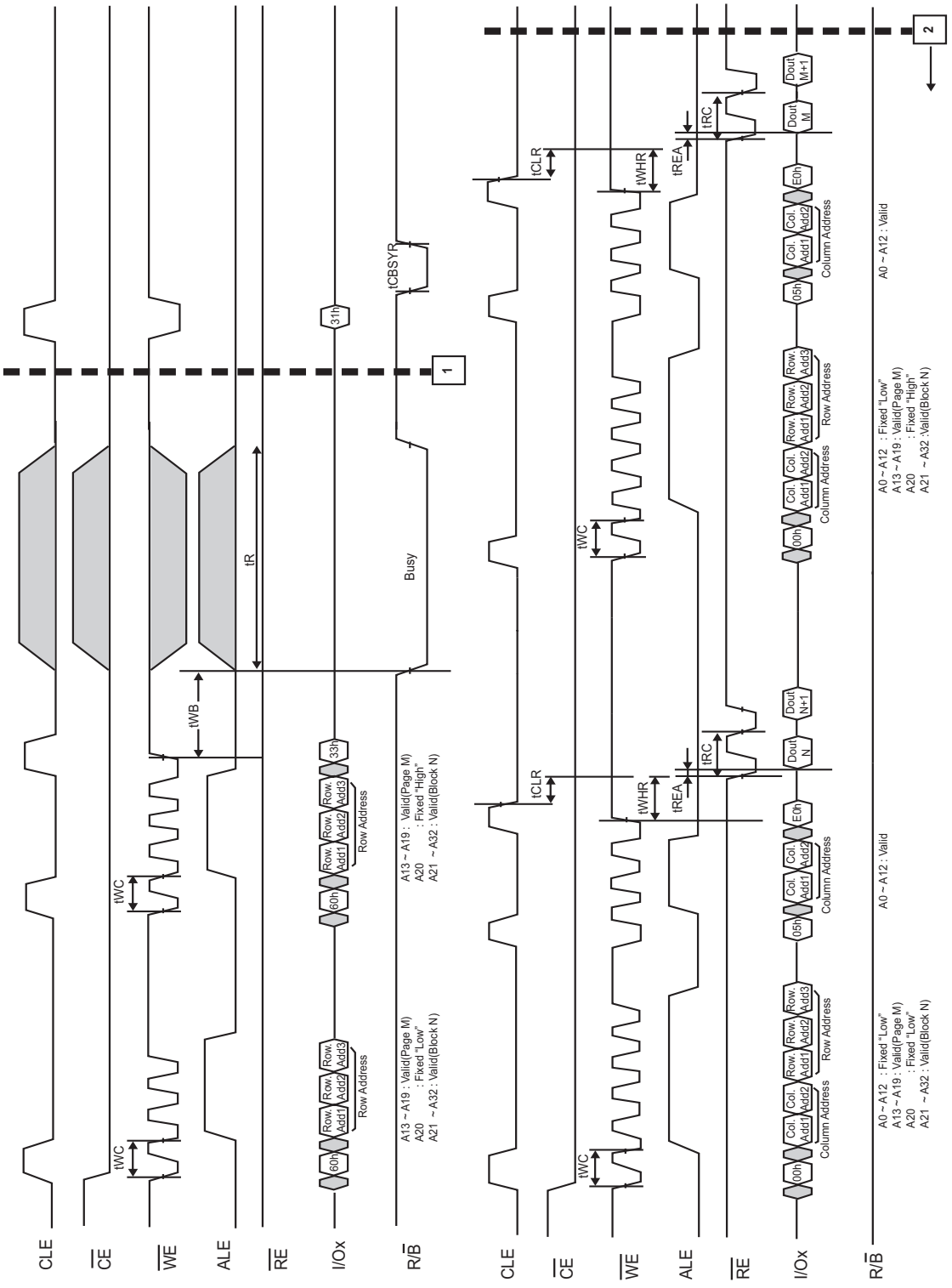


Figure 24 : Multi Plane Cache Read - 1

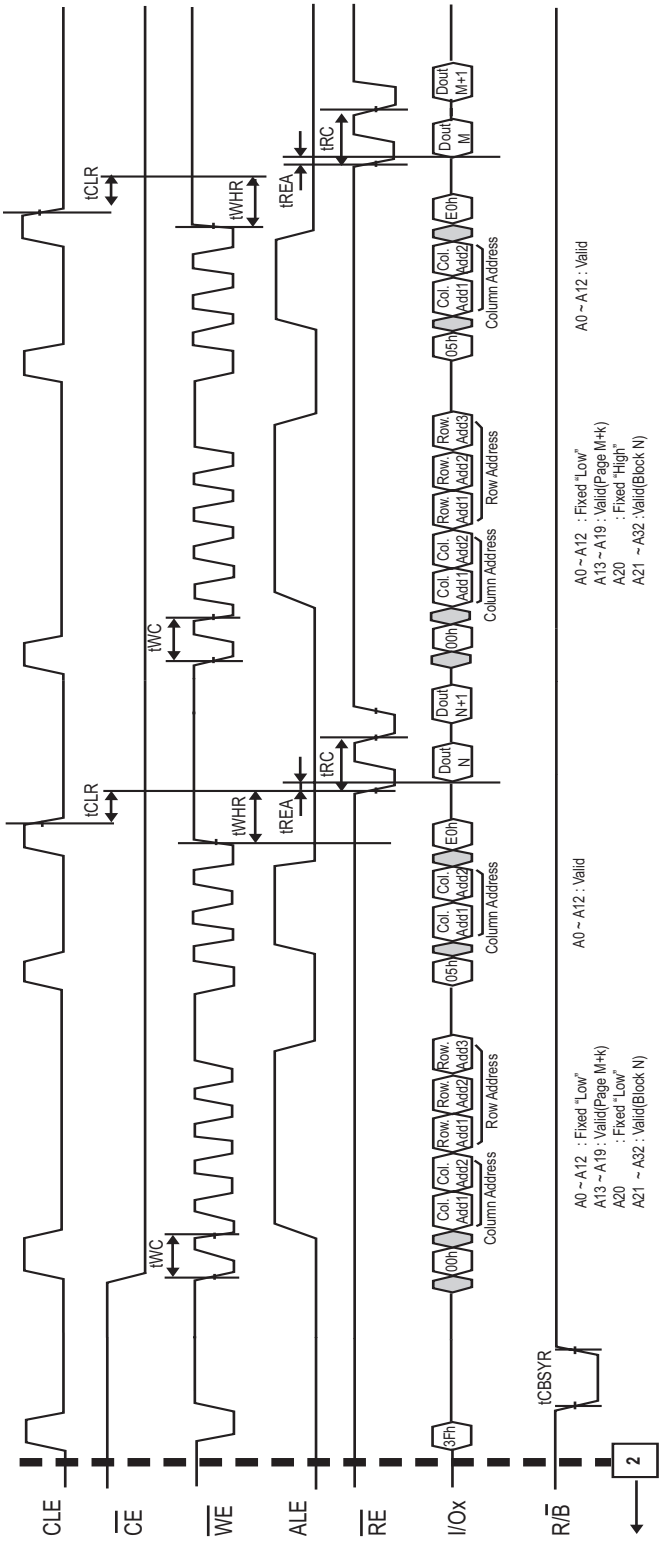


Figure 24 : Multi Plane Cache Read - 2

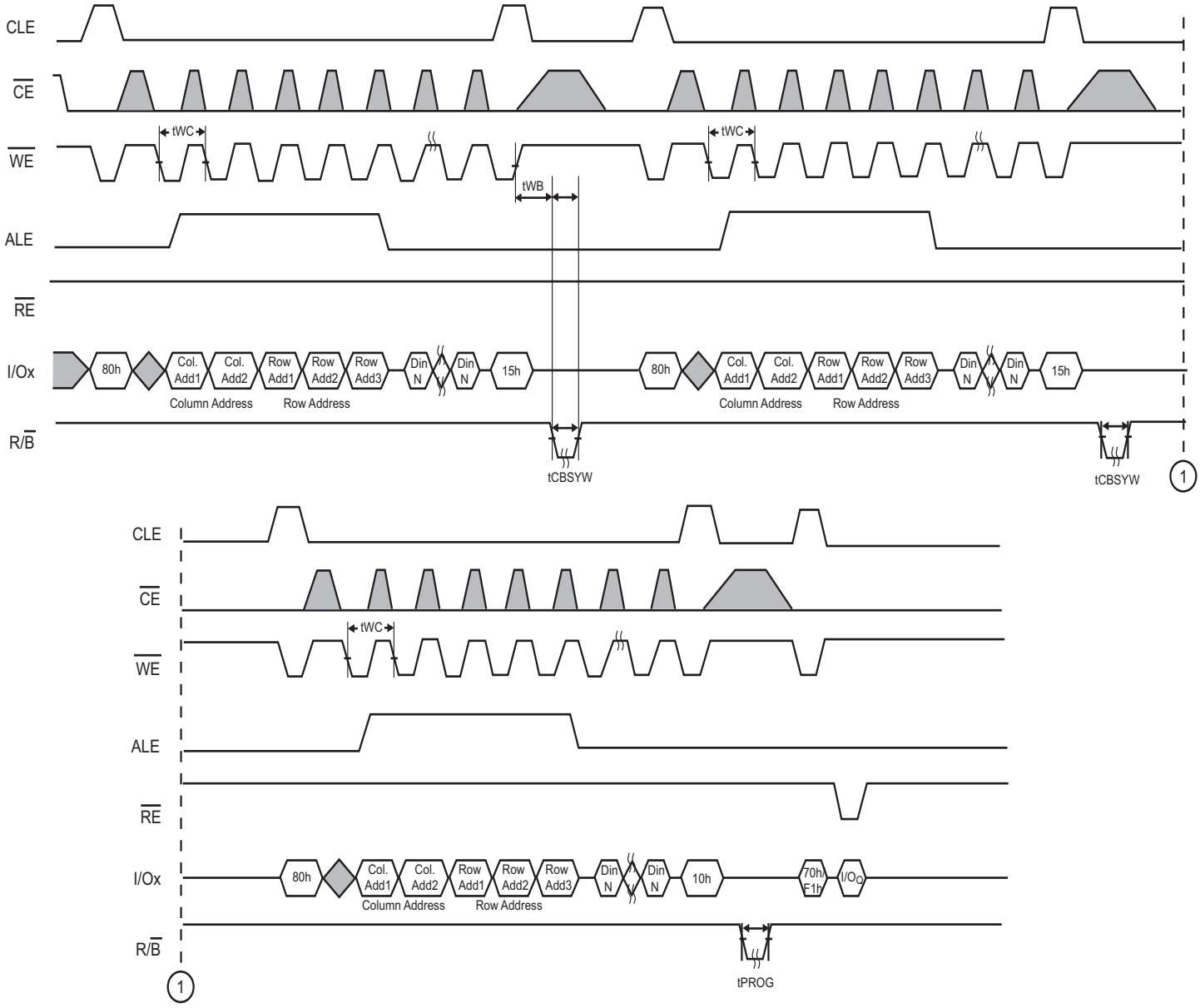


Figure 25 : Cache Program

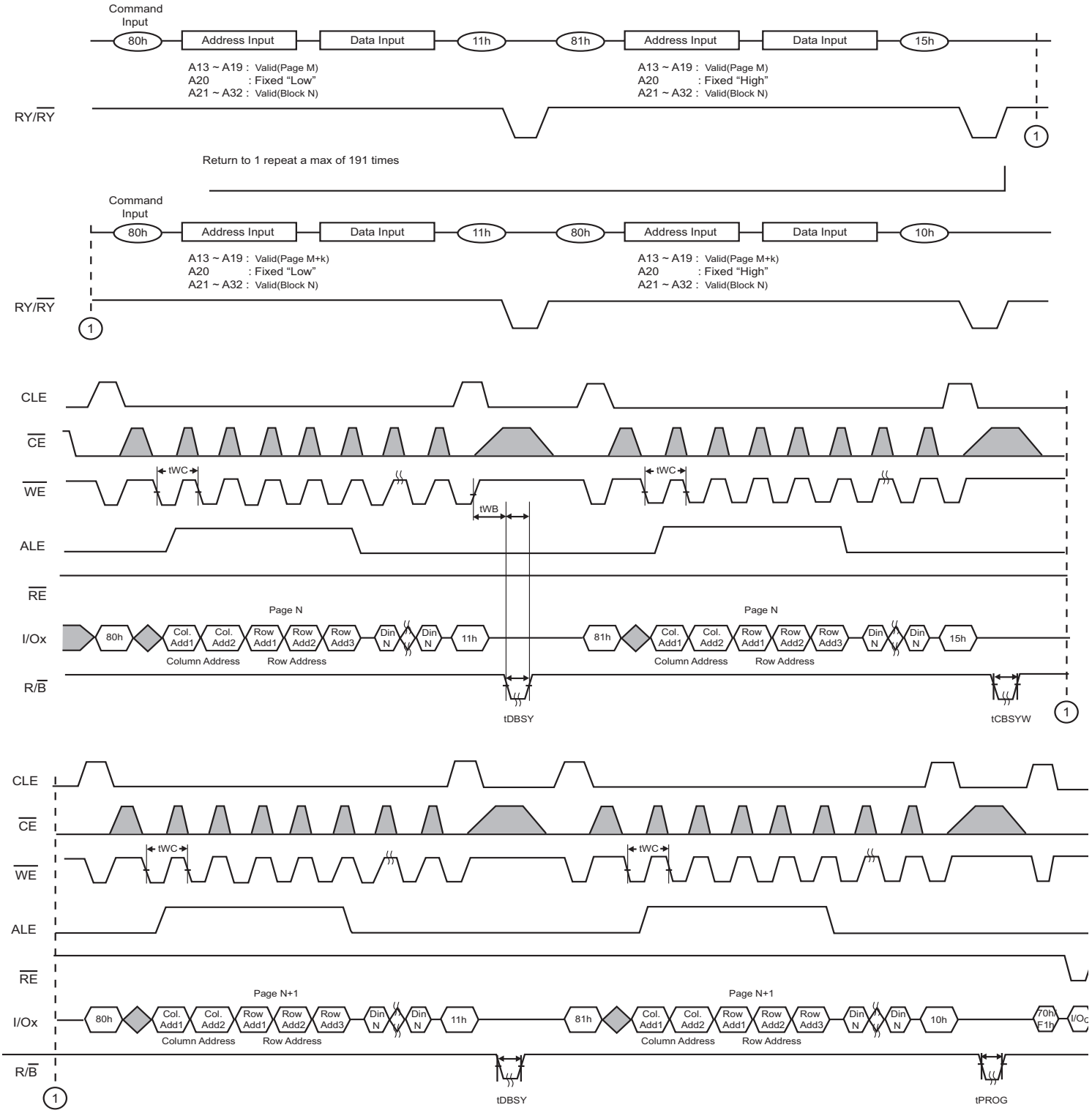


Figure 26 : Multi Plane Cache Program

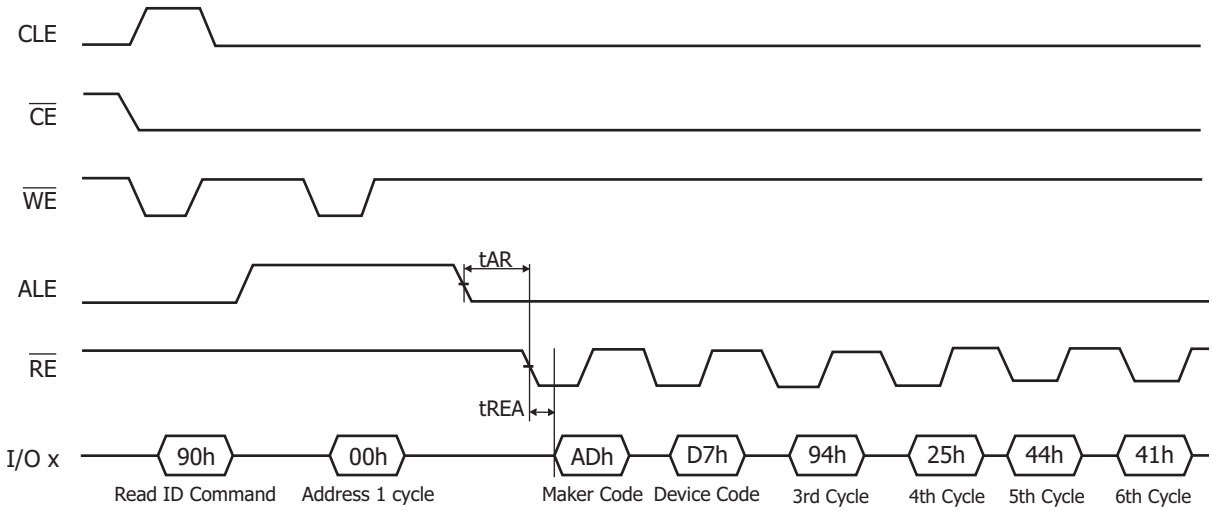


Figure 27 : Read ID Opeartion

System Interface Using $\overline{CE}$ don't care

To simplify system interface, $\overline{CE}$ may be deasserted during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microprocessor. The only function that was removed from standard NAND Flash to make $\overline{CE}$ don't care read operation was disabling of the automatic sequential read function.

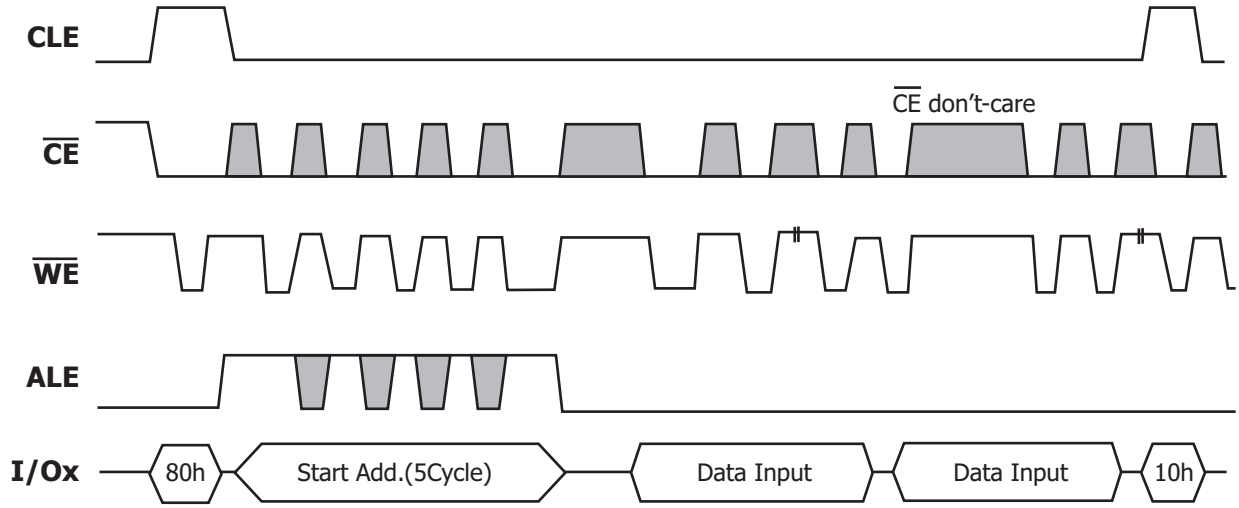


Figure 28 : Program Operation with $\overline{CE}$ Don't Care

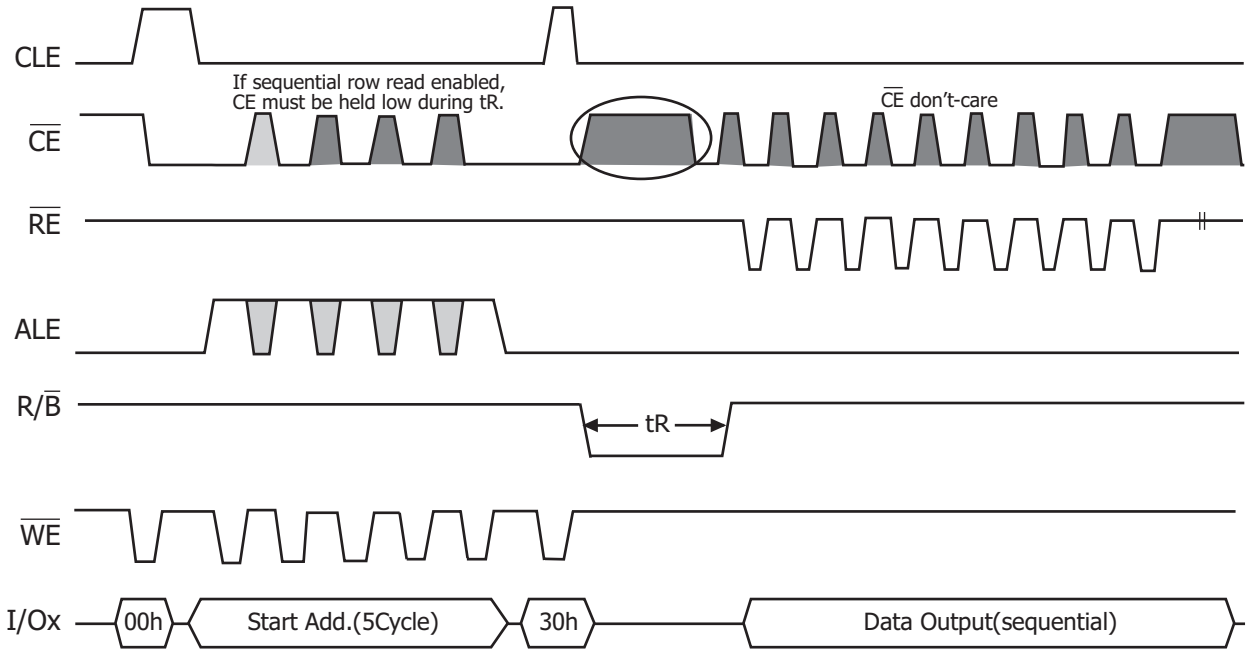


Figure 29 : Read Opeartion with $\overline{CE}$ Don't Care

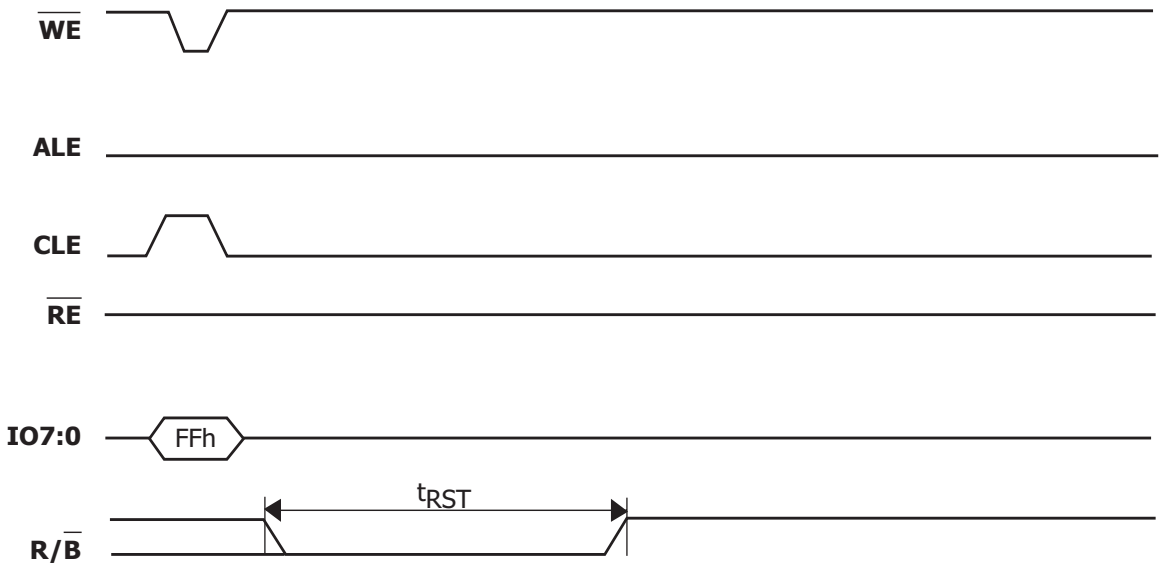


Figure 30 : Reset Operation

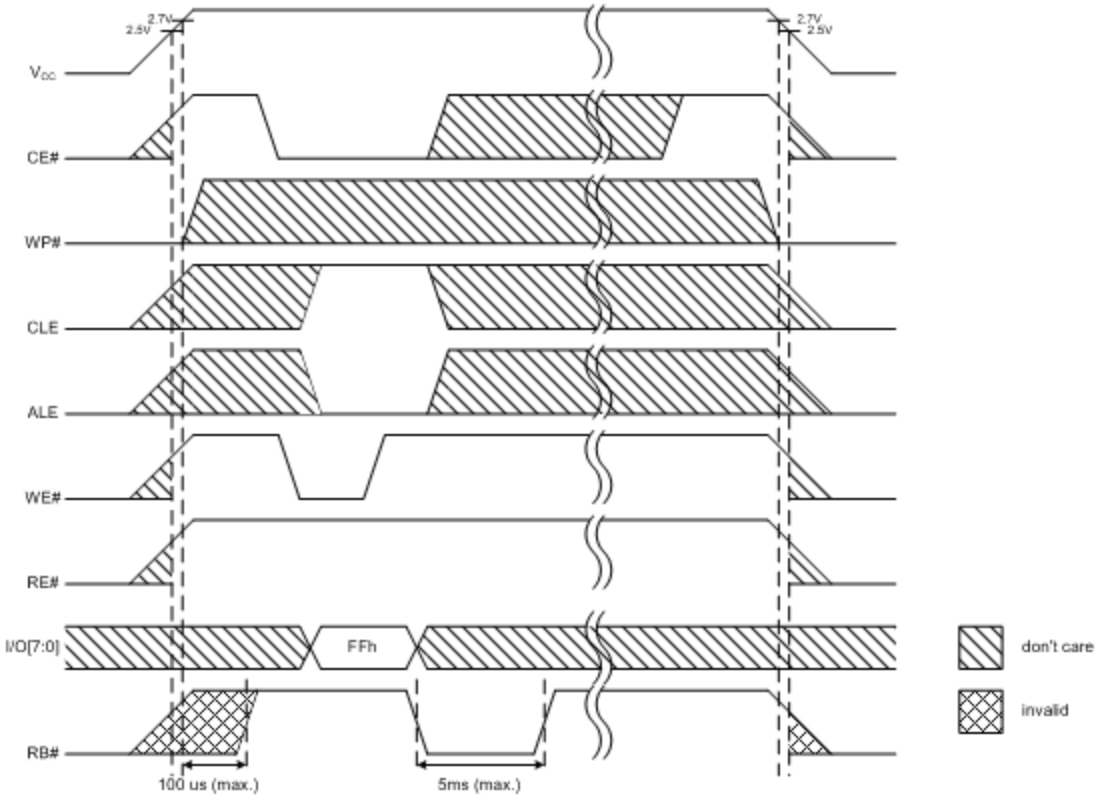


Figure 31 : Power on and Data Protecting Timing

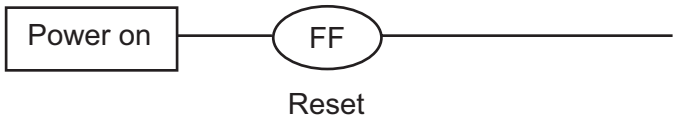


Figure 32 : Power on Reset

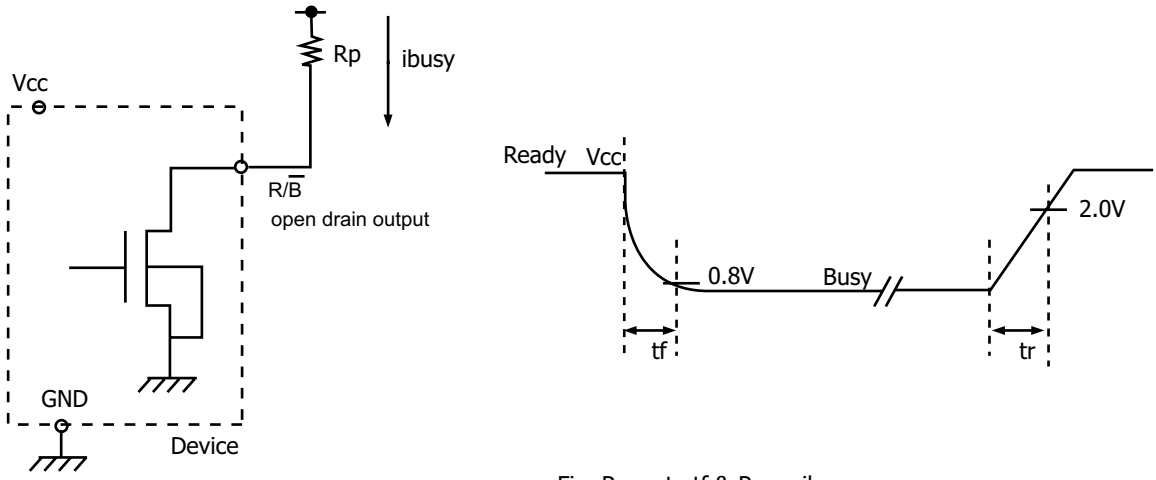
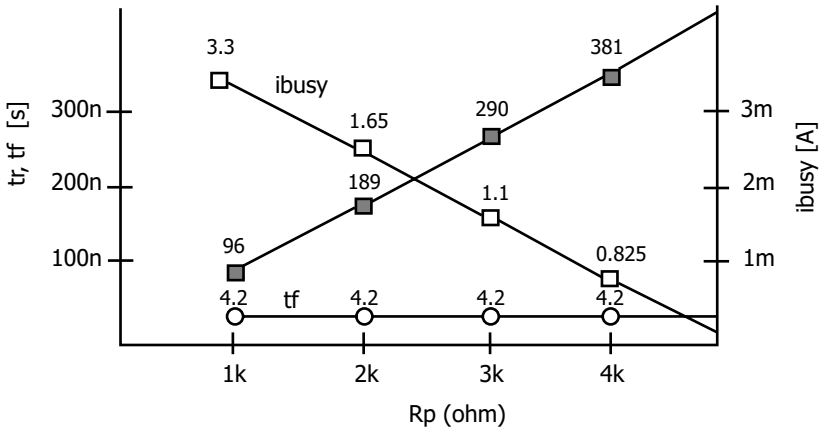


Fig. Rp vs tr, tf & Rp vs ibusy

@ Vcc = 3.3V, Ta = 25°C, CL=50pF



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 33 : Ready/Busy Pin Electrical Specifications.

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the Last and (Last-2)th page (if the last page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 34. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

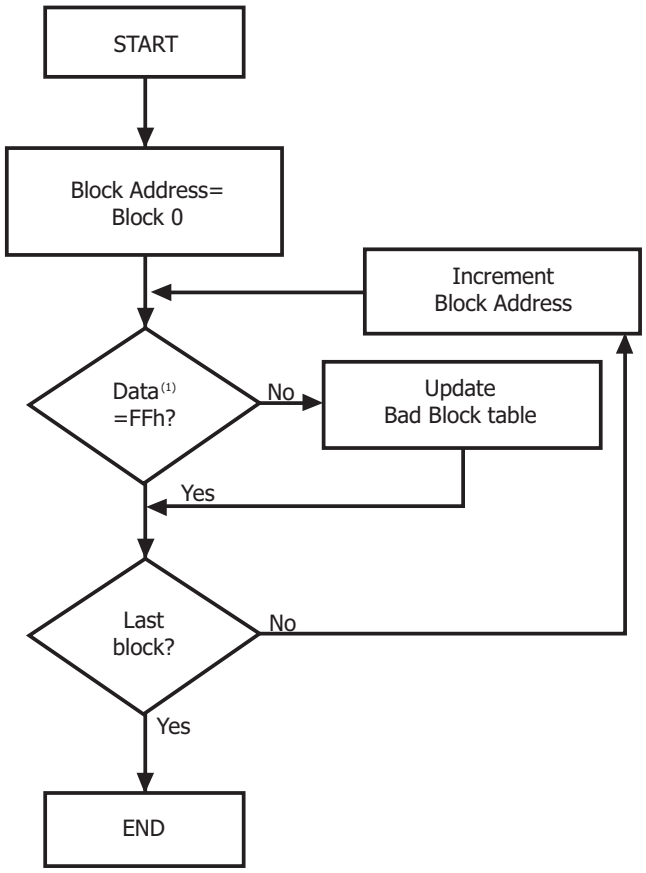


Figure 34: Bad Block Management Flowchart

NOTE :

1. Make sure that FFh at the column address 4096 of the last page and last - 2th page.

Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.

The failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Refer to Table 18 and Figure 35 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (with 12 bit/512byte)

Table 18 : Block Failure

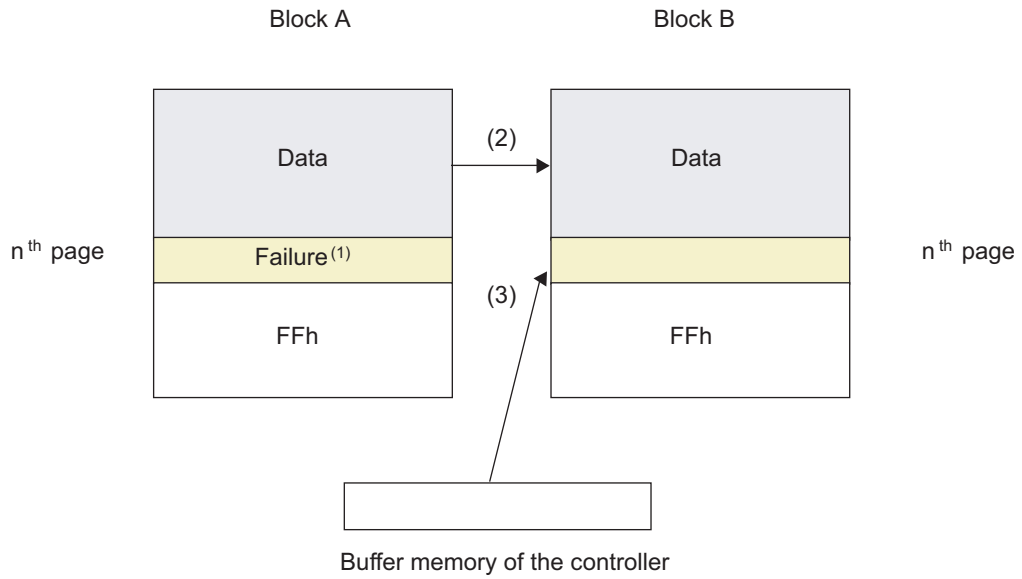


Figure 35 : Bad Block Replacement

NOTE :
1. An error occurs on nth page of the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. Nth page of block A which is in controller buffer memory is copied into nth page of Block B
4. Bad block table should be updated to prevent from erasing or programming Block A

Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 36~39)

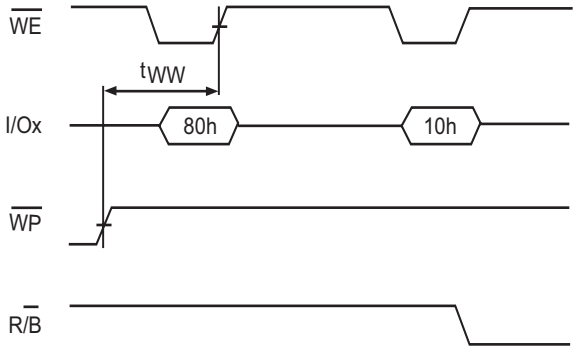


Figure 36 : Enable Programming

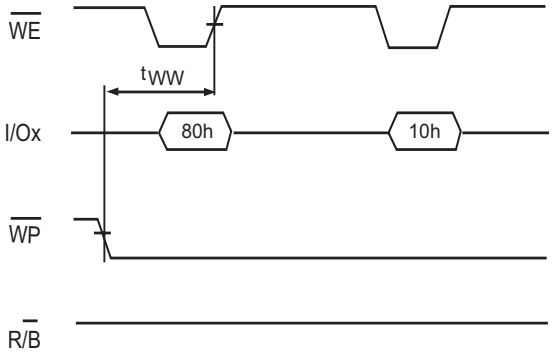


Figure 37 : Disable Programming

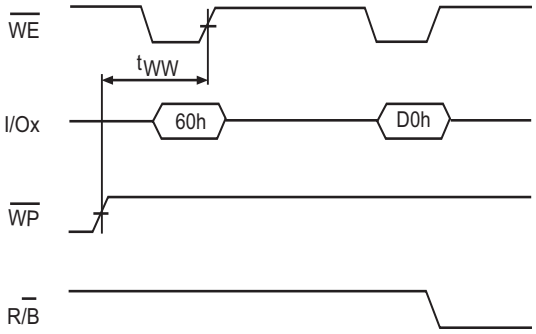


Figure 38 : Enable Erasing

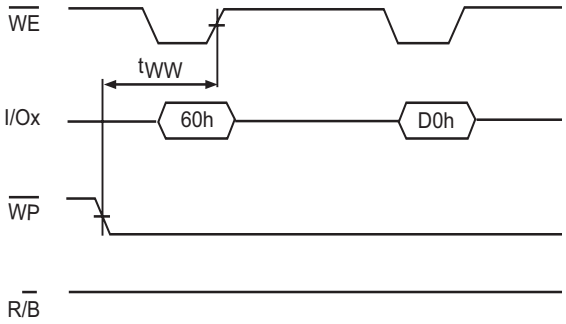


Figure 39 : Disable Erasing

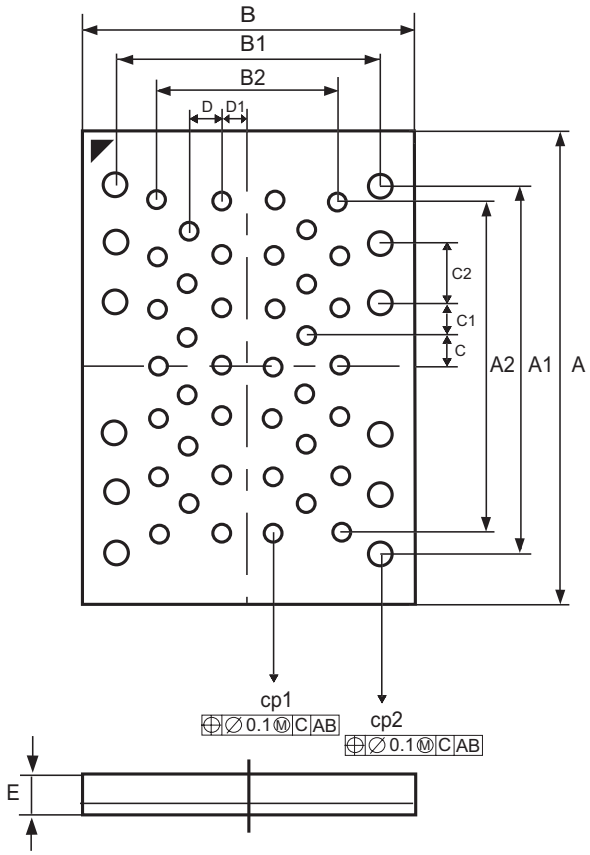


Figure 40 : 52-VLGA, 14 x 18mm, Package Outline(Top view through package)

Symbol	millimeters		
	Min	Typ	Max
A	17.90	18.00	18.10
A1		13.00	
A2		12.00	
B	13.90	14.00	14.10
B1		10.00	
B2		6.00	
C		1.00	
C1		1.50	
C2		2.00	
D		1.00	
D1		1.00	
E	0.80	0.90	1.00
CP1	0.65	0.70	0.75
CP2	0.95	1.00	1.05

Table 19 : 52-VLGA, 14 x 18mm, Package Mechanical Data

6. Application Notes and Comment

6.1 Paired Page Address Information

Paired Page Address		Paired Page Address	
Group A	**Group B**	**Group A**	**Group B**
ooh	04h	01h	05h
02h	08h	03h	09h
06h	0Ch	07h	0Dh
0Ah	10h	0Bh	11h
0Eh	14h	0Fh	15h
12h	18h	13h	19h
16h	1Ch	17h	1Dh
1Ah	20h	1Bh	21h
1Eh	24h	1Fh	25h
22h	28h	23h	29h
26h	2Ch	27h	2Dh
2Ah	30h	2Bh	31h
2Eh	34h	2Fh	35h
32h	38h	33h	39h
36h	3Ch	37h	3Dh
3Ah	40h	3Bh	41h
3Eh	44h	3Fh	45h
42h	48h	43h	49h
46h	4Ch	47h	4Dh
4Ah	50h	4Bh	51h
4Eh	54h	4Fh	55h
52h	58h	53h	59h
56h	5Ch	57h	5Dh
5Ah	60h	5Bh	61h
5Eh	64h	5Fh	65h
62h	68h	63h	69h
66h	6Ch	67h	6Dh
64h	70h	6Bh	71h
6Eh	74h	6Fh	75h
72h	78h	73h	79h
76h	7Ch	77h	7Dh
7Ah	7Eh	7Bh	7Fh

Figure 41 : Paired Page Address Information

Note:
When program operation is abnormally aborted (ex. power-down, reset), not only page data under program but also paired page data may be damaged

6.2 Extra Block Description

Device includes extra features like user OTP, Unique ID and Read ID2, User OTP, Unique ID can be programmed only once and can not be erased. The user OTP used one block which locates the second block of plane 0 (address<32:20> =0002h. Unique ID block has 64pages, locates the first block of plane 0 and the first 64pages of the block (address<32:20> = 0000h, address<19:13>=00h~3Fh). Read ID2 can be only read, the size is one page. Physically, Read ID2 are exists in plane 1, but user block address doesn't care internally. To exit extra features, 06h of FFh command can be used

6.3 Cache Program Limitation

Whenever a setup command(80h) is issued during cache program operation, subsequent addresss inputs, data inputs and confirm commands(15h or 10h) must be inputted for proper operation. the cache status remains busy until the confirm command (15h or 10h) is issued properly.

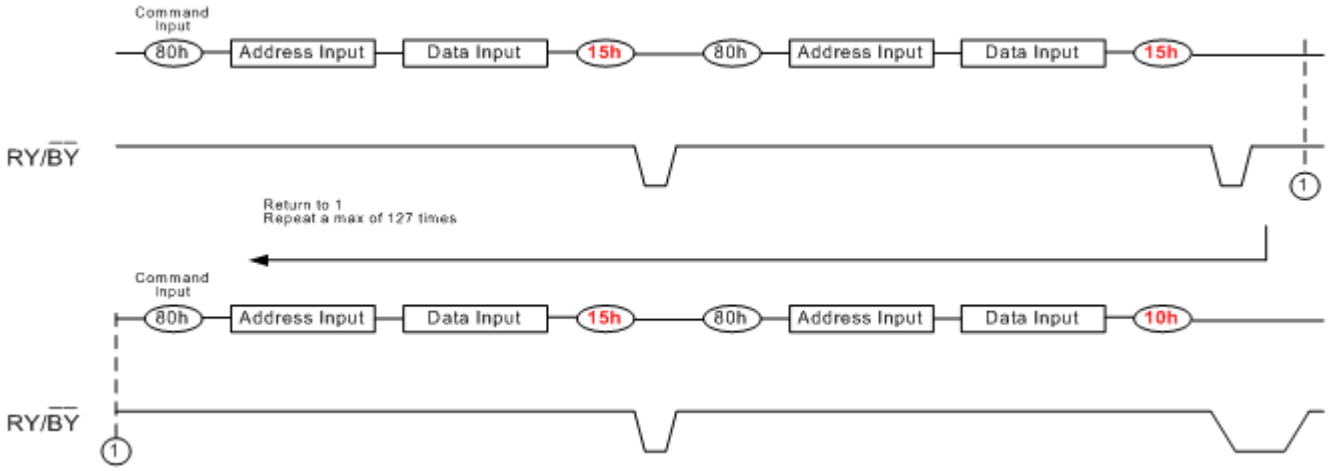
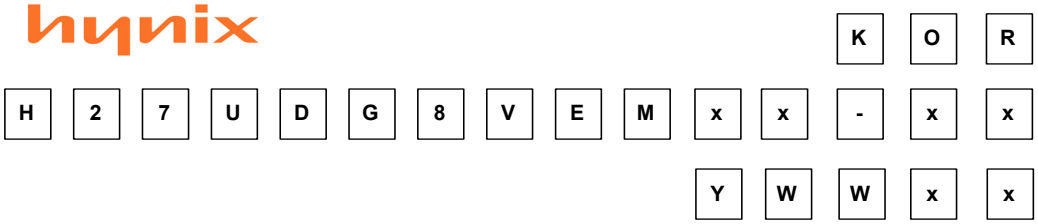


Figure 42 : Cache Program Limitation

MARKING INFORMATION - VLGA

Marking Example



- hynix	: Hynix Symbol
- KOR	: Origin Country
- H27UDG8VEMxx-xx	: Part Number
H: Hynix	
27: NAND Flash	
U: Power Supply	: U(2.7V~3.6V)
DG: Density	: 128Gbit
8 : Bit Organization	: 8(x8)
V: Classification	: Multi Level Cell+Quad Die+Large Block
E: Mode	: 4CE Dual Interface (Sequential Read Disable)
M: Version	: 1st Generation
x: Package Type	: Y(52-VLGA)
x: Package Material	: Blank(Normal), P(Lead Free)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)
x: Operating Temperature	: C(0℃~70℃), I(-40℃~85℃)

- **Y:** Year (ex: 8=year 2008, 9= year 2009)
- **ww:** Work Week (ex: 12= work week 12)
- **xx:** Process Code

Note

- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item