READ-ONLY CONTACTLESS IDENTIFICATION DEVICE

Features

- 64 bit memory array laser programmable
- Wide dynamic range due to on chip buffer capacitance & voltage limiter on chip.
- Full wave rectifier on chip
- Big modulation depth due to a low impedance modulation device
- 50'000 baud reading speed at 3 MHz
- Very small chip size convenient for implantation
- Unsensitive close to metal
- Large distance even without resonance capacitor
- No external buffer capacitance needed due to low power consumption

Description

The H4001 is a CMOS integrated circuit for use in transponders. The circuit is powered by an external coil placed in a magnetic field, and gets its clock from the same field via one of the coil terminals. The other coil terminal is affected by the modulator, turning on and off the modulation current in order to send back the 64 bits of information contained in a factory pre-programmed memory array.

The programming of the chip is performed by laser fusing of polysilicon links in order to store a unique code on each chip.

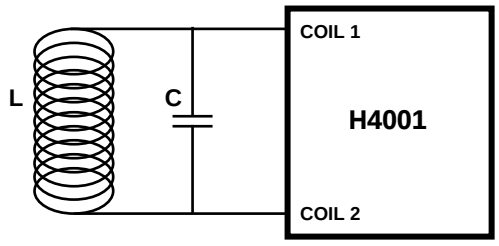
The serial output data string contains a 9 bits header, 40 bits of data, 14 parity bits, and 1 stop bit.

Due to the low power consumption of the logic core, no supply buffer capacitor is required. Only an external coil is required to obtain the chip function. A parallel capacitor adjusted with the coil to obtain resonnance, will increase the read distance.

Applications

- Industrial transponder
- Animal transponder
- ID Cards
- Serial Number Identification ROM

Typical Operating Configuration

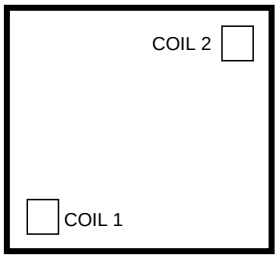


Typical value of inductance at 125 KHz is 2 mH

The capacitor is adjusted to the resonance

Fig. 1

Pin Assignment



COIL 1	coil terminal/ clock input
COIL 2	coil terminal/ data transmisssion

Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Condition
Maximum AC peak current induced on COIL1 and COIL2	Icoil	30 mA
Maximum storage temperature	Tstoremax	+200 °C
Minimum storage temperature	Tstoremin	- 55 °C
Electrostatic discharge maximum to MIL-STD-883C method 3015	VESD	750 V

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component.
Unless otherwise specified proper operation can only occur when all terminal voltages are kept within the supply voltage range.
Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	TA	-40		+85	°C
AC Supply Voltage	Vcoil	3.5			Vpp
Supply Frequency	fcoil	50	130	400	KHz

Table 2

Electrical Characteristics

Vcoil = 3.5Vpp ±5% fcoil =130KHz Sine Wave TA = 25°C unless otherwise specified

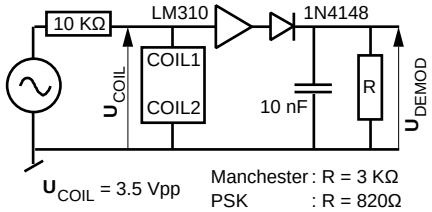
Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Demodulated Voltage	Udemod		0.25			VAC
Dynamic Current	Idyn			50		µA

Table 3

Timing Characteristics

VCOIL2 = 0V VCOIL1 = 3.5Vpp Sine Wave

Parameter	Symbol	Min	Typ	Max	Unit
Coil Clock frequency	fCOIL	50	130	400	kHz
Ratio between coil period and bit period Manchester code PSK	 Rmch Rpsk		 64 16		

Table 4

Timing Waveforms

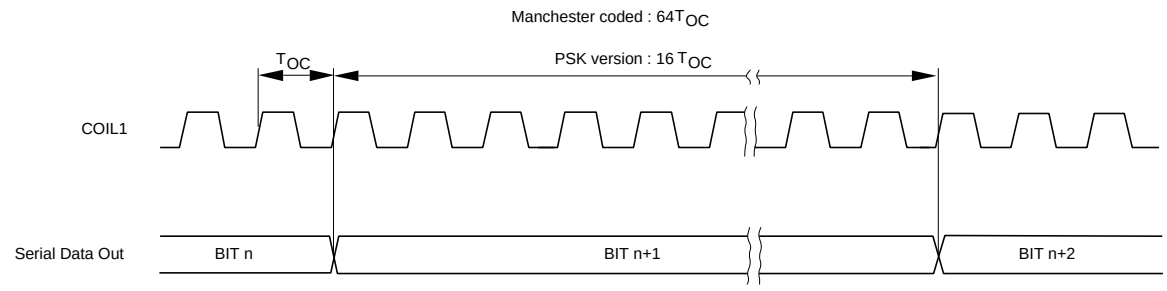


Fig. 3

Manchester coded version

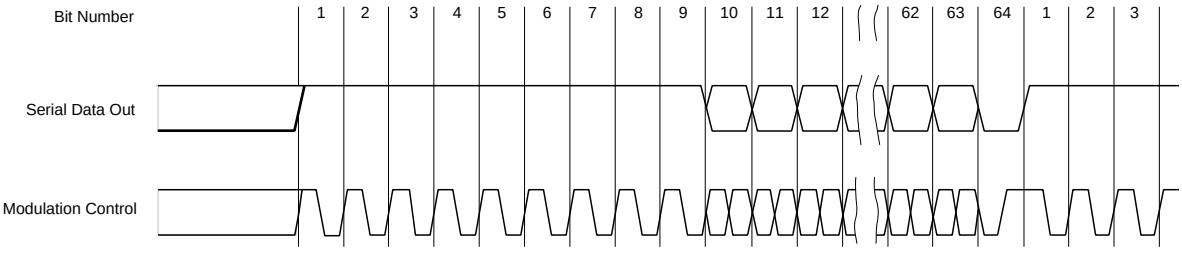


Fig. 4

PSK version

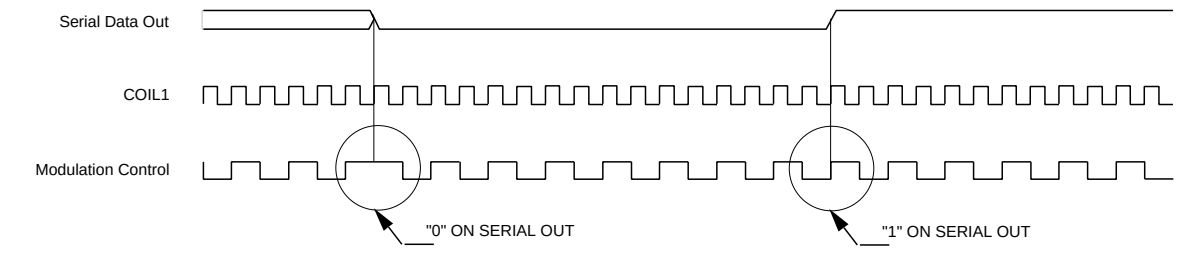


Fig. 5

Block Diagram

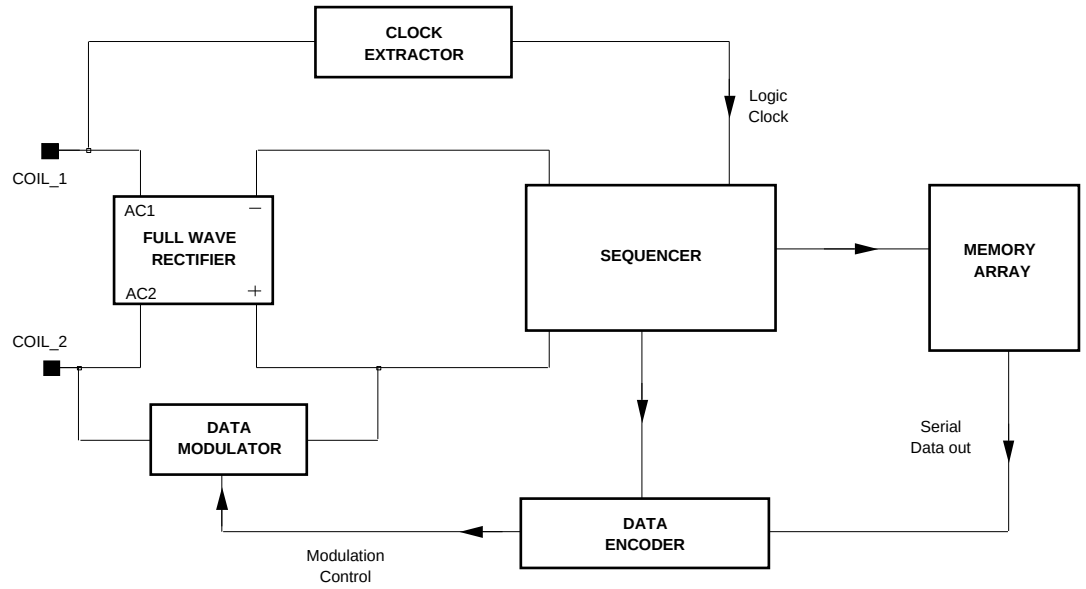


Fig. 6

Functional Description

Full Wave Rectifier
The AC input induced in the external coil by an incident magnetic field is rectified by a Graetz bridge

Memory Array
The H4001 contains 64 bits divided in five groups of information. 9 bits are used for the header, 10 row parity bits (P0 - P9), 4 column parity bits (PC0 - PC3), 40 data bits (D00 - D93), and 1 stop bit set to logic 0.

1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	- 9 Bits Header
8 Version bits or Customer ID				**D00**	**D01**	**D02**	**D03**	**P0**	- 4 data bits & associated even row parity bit
				D10	**D11**	**D12**	**D13**	**P1**	
32 Data Bits allowing 4 billion of combinations				**D20**	**D21**	**D22**	**D23**	**P2**	
				D30	**D31**	**D32**	**D33**	**P3**	
				D40	**D41**	**D42**	**D43**	**P4**	
				D50	**D51**	**D52**	**D53**	**P5**	
				D60	**D61**	**D62**	**D63**	**P6**	
				D70	**D71**	**D72**	**D73**	**P7**	
				D80	**D81**	**D82**	**D83**	**P8**	
				D90	**D91**	**D92**	**D93**	**P9**	
				PC0	**PC1**	**PC2**	**PC3**	**0**	- 4 column even parity bits, NO row parity bit

The header is composed by the 9 first bits which are mask programmed to 111111111. Due to the data and parity organisation, this sequence can not be reproduced in the data string. The header is followed by 10 groups of 4 data bits and 1 even row parity bit. Then, the last group consists of 4 even column parity bits without row parity bit.

Bits D00 to D03 and bits D10 to D13 are customer specific identification.

These 64 bits are outputted serially in order to control the modulator used to modify the current at one of the coil terminals.
When the 64 bits data string is outputted, the output sequence is repeated continuously until power goes off.

Control Logic

Two mask programmed versions of logic are available. The first one will modulate the amplitude of the magnetic field with a bit rate corresponding to 64 periods of the field frequency (Manchester coding). The second version is using half of the field frequency to transmit data by shifting the signal phase (PSK coding).

One of the coil terminals (COIL1 in Fig.6) is used to generate the clock signal for the logic. The output of the clock extractor drives a sequencer providing all necessary signals to address the Memory Array, and serially output the data.

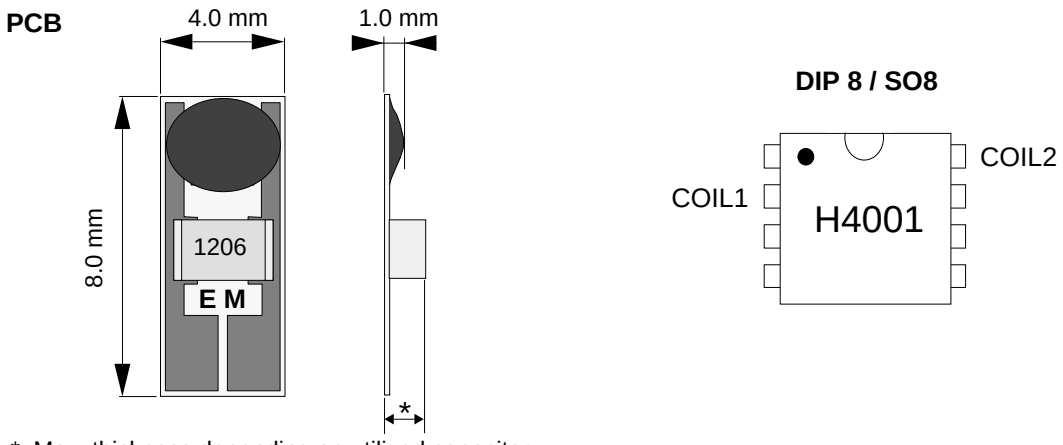
PSK version

The serial data output of the Memory array connects the modulation control to the output or inverted output of a flip-flop which input is the signal from the clock extractor.
When a logic 0 is output, the modulation control signal is changed to the other output of the flip-flop, and when a logic 1 is output, the modulation control signal remains on the same flip-flop output.

Data Modulator

The data modulator is controlled by the signal Modulation Control (see above fig. 4 & 5) in order to induce a high current on COIL_2 terminal when this signal is at logic 0. This will affect the magnetic field according to the data stored in the Memory Array.

Package Information



* Max. thickness depending on utilized capacitor

Fig. 7

Ordering Information
The H4001 is available in the following packages

DIP 8-pin package	H4001	8P
SO 8-pin package	H4001	8S
PCB 2 connections	H4001	PCB

Chip form and others on request