

256Mb Synchronous DRAM based on 4M x 4Bank x16 I/O

# 256M (16Mx16bit) Hynix SDRAM Memory

## **Memory Cell Array**

- Organized as 4banks of 4,194,304 x 16

---

This document is a general product description and is subject to change without notice. Hynix does not assume any responsibility for use of circuits described. No patent licenses are implied.

**Rev 1.0 / Aug. 2009**

**1**

**H57V2562GFR**  
**Document Title****256Mbit (16M x16) Synchronous DRAM****Revision History**

<b>Revision No.</b>	<b>History</b>	<b>Draft Date</b>	<b>Remark</b>
0.1	Preliminary	Jun. 2009	
1.0	Release	Aug. 2009	



## DESCRIPTION

The Hynix H57V2562GFR Synchronous DRAM is 268,435,456bit CMOS Synchronous DRAM, ideally suited for the consumer memory applications which requires large memory density and high bandwidth. It is organized as 4banks of 4,194,304 x 16 I/O.

Synchronous DRAM is a type of DRAM which operates in synchronization with input clock. The Hynix Synchronous DRAM latch each control signal at the rising edge of a basic input clock (CLK) and input/output data in synchronization with the input clock (CLK). The address lines are multiplexed with the Data Input/ Output signals on a multiplexed x16 Input/ Output bus. All the commands are latched in synchronization with the rising edge of CLK.

The Synchronous DRAM provides for programmable read or write Burst length of Programmable burst lengths: 1, 2, 4, 8 locations or full page. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access. The Synchronous DRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

Read and write accesses to the Hynix Synchronous DRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

All inputs are LVTTTL compatible. Devices will have a VDD and VDDQ supply of 3.3V (nominal).



## 256Mb Synchronous DRAM(16M x 16) FEATURES

- Standard SDRAM Protocol
- Internal 4bank operation
- Power Supply Voltage : VDD = 3.3V, VDDQ = 3.3V
- All device pins are compatible with LVTTTL interface
- Low Voltage interface to reduce I/O power
- 8,192 Refresh cycles / 64ms
- Programmable CAS latency of 2 or 3
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Commercial Temp : 0°C ~ 70°C Operation
- Package Type : 54ball, 0.8mm pitch FBGA
- **This product is in compliance with the directive pertaining of RoHS.**

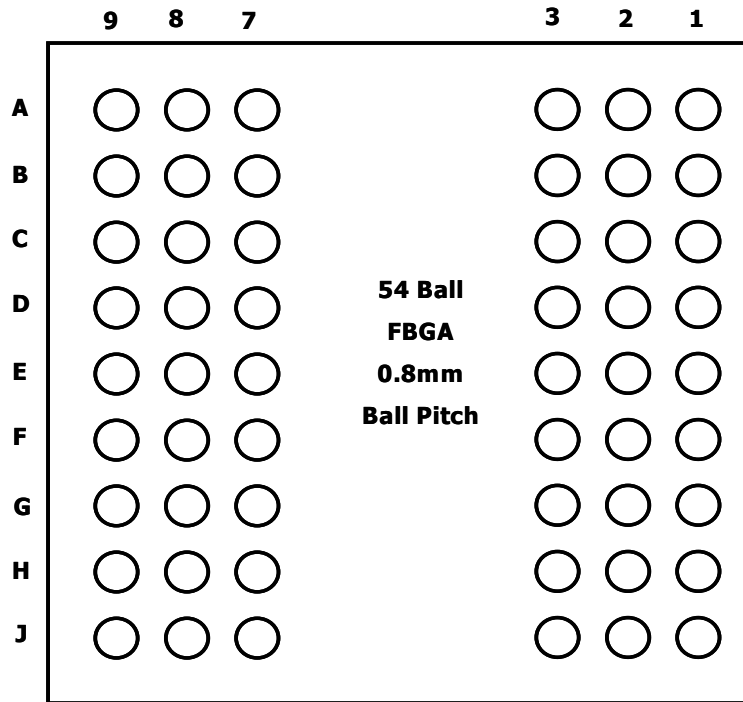
## ORDERING INFORMATION

Part Number	Clock Frequency	CAS Latency	Power	Voltage	Organization	Interface
H57V2562GFR-60C	166MHz	3	Normal	3.3V	4Banks x 4Mbits x16	LVTTTL
H57V2562GFR-75C	133MHz	3				
H57V2562GFR-60L	166MHz	3	Low Power			
H57V2562GFR-75L	133MHz	3				

### Note:

1. H57V2562GFR-XXC Series: Normal power & Commercial temp.
2. H57V2562GFR-XXL Series: Low Power & Commercial temp.

BALL CONFIGURATION



<Bottom View>

1	2	3	A	7	8	9
VSS	DQ15	VSSQ	A	VDDQ	DQ0	VDD
DQ14	DQ13	VDDQ	B	VSSQ	DQ2	DQ1
DQ12	DQ11	VSSQ	C	VDDQ	DQ4	DQ3
DQ10	DQ9	VDDQ	D	VSSQ	DQ6	DQ5
DQ8	NC	VSS	E	VDD	LDQM	DQ7
UDQM	CLK	CKE	F	/CAS	/RAS	/WE
A12	A11	A9	G	BA0	BA1	/CS
A8	A7	A6	H	A0	A1	A10
VSS	A5	A4	J	A3	A2	VDD

< Top View >

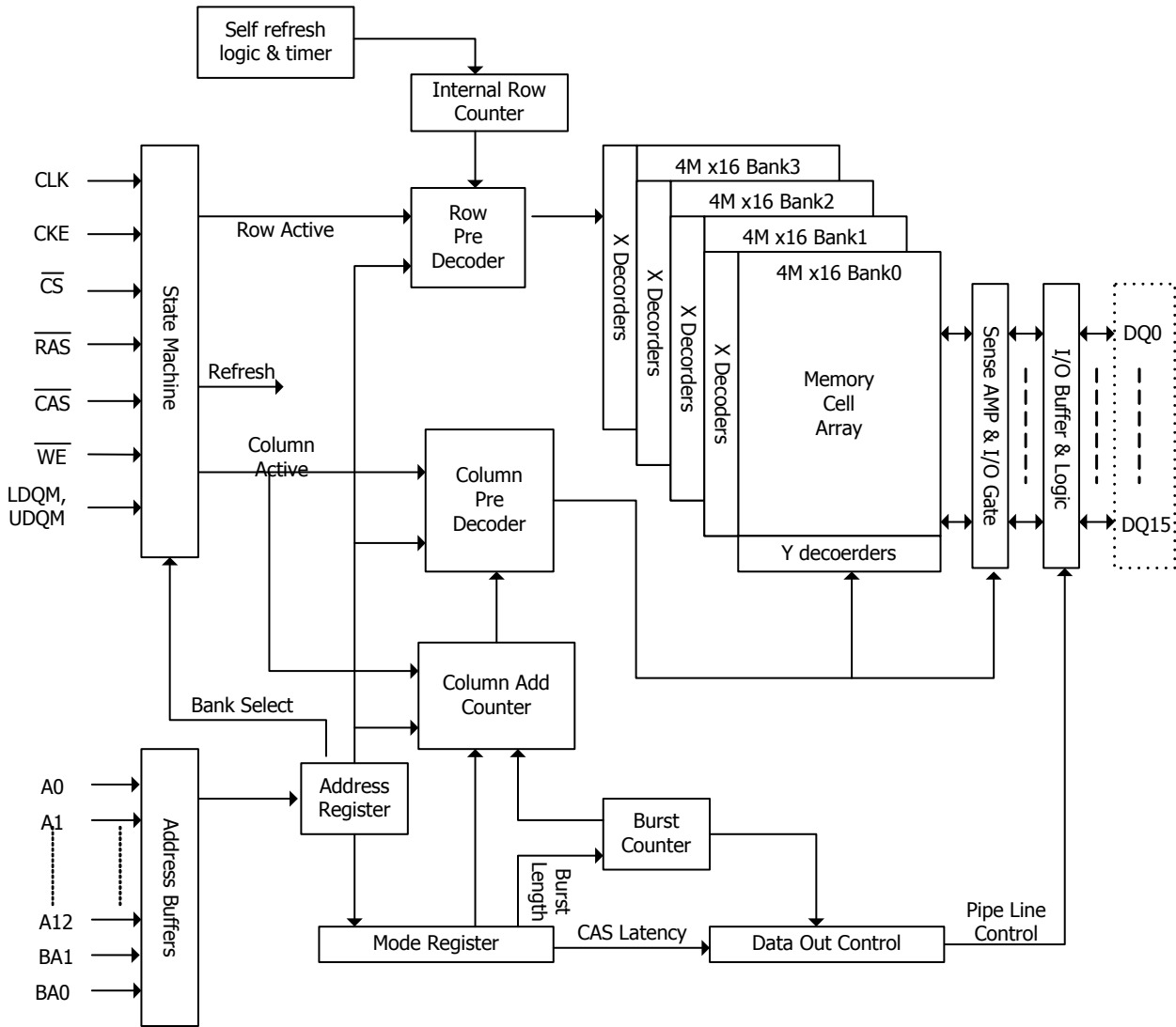


## 54\_TSOPII Pin DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CLK	INPUT	Clock : The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	INPUT	Clock Enable: Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	INPUT	Chip Select: Enables or disables all inputs except CLK, CKE and DQM
BA0, BA1	INPUT	Bank Address: Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during CAS activity
A0 ~ A12	INPUT	Row Address: RA0 ~ RA12, Column Address: CA0 ~ CA8 Auto-precharge flag: A10
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	INPUT	Command Inputs: $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	I/O	Data Mask: Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	I/O	Data Input / Output: Multiplexed data input / output pin
VDD / VSS	SUPPLY	Power supply for internal circuits and input buffers
VDDQ / VSSQ	SUPPLY	Power supply for output buffers
NC	-	No connection : These pads should be left unconnected



FUNCTIONAL BLOCK DIAGRAM  
4Mbit x 4banks x 16 I/O Synchronous DRAM





## ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD supply relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W

Note : Operation at above absolute maximum rating can adversely affect device reliability

## DC OPERATING CONDITION

Parameter	Symbol	Min	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.6	V	1
Input High Voltage	VIH	2.0	VDDQ + 0.3	V	1, 2
Input Low Voltage	VIL	-0.3	0.8	V	1, 3

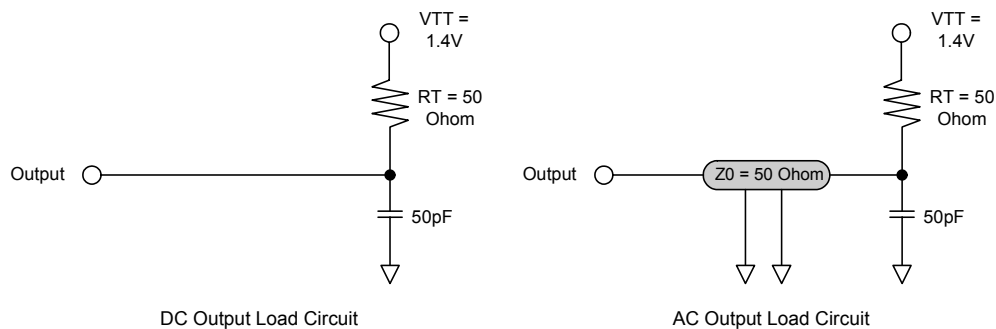
**Note:** 1. All voltages are referenced to VSS = 0V.  
 2. VIH(Max) is acceptable VDDQ + 2V for a pulse width with <= 3ns of duration.  
 3. VIL(min) is acceptable -2.0V for a pulse width with <= 3ns of duration.

## AC OPERATING TEST CONDITION (TA= 0 to 70°C, VDD=3.3±0.3V / VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4 / 0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

**Note:** 1. See Next Page





### CAPACITANCE (f=1MHz)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	CI1	2.0	4.0	pF
	A0 ~ A12, BA0, BA1, CKE, $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	CI2	2.0	4.0	pF
	LDQM, UDQM	CI3	2.0	4.0	pF
Data input / output capacitance	DQ0 ~ DQ15	CI/O	3.5	6.5	pF

### DC CHARACTERISTICS I (TA= 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	1
Output Leakage Current	ILO	-1	1	uA	2
Output High Voltage	VOH	2.4	-	V	IOH = -4mA
Output Low Voltage	VOL	-	0.4	V	IOL = +4mA

**Note:**

- VIN = 0 to 3.6V, All other balls are not tested under VIN = 0V
- DOUT is disabled, VOUT=0 to 3.6


**DC CHARACTERISTICS II** (TA= 0 to 70°C)

Parameter	Symbol	Test Condition	Speed (MHz)		Unit	Note
			166	133		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA	90	70	mA	1
Precharge Standby Current in Power Down Mode	IDD2P	CKE ≤ VIL(max), tCK = 15ns	2		mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞	2		mA	
Precharge Standby Current in Non Power Down Mode	IDD2N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$ , tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	15		mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	8			
Active Standby Current in Power Down Mode	IDD3P	CKE ≤ VIL(max), tCK = 15ns	5		mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞	5			
Active Standby Current in Non Power Down Mode	IDD3N	CKE ≥ VIH(min), $\overline{CS} \geq VIH(min)$ , tCK = 15ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V	28		mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.	20			
Burst Mode Operating Current	IDD4	tCK ≥ tCK(min), IOL=0mA All banks active	100	80	mA	1
Auto Refresh Current	IDD5	tRC ≥ tRC(min), All banks active	160	140	mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V	Normal	2	mA	3
			Low Power	1		

**Note:** 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.

2. Min. of tRC (Refresh RAS cycle time) is shown at AC CHARACTERISTICS II

3. H57V2562GFR-XXC Series: Normal, H57V2562GFR-XXL Series: Low Power


**AC CHARACTERISTICS I** (AC operating conditions unless otherwise noted)

Parameter		Speed (MHz)	166		133		Unit	Note
			Min	Max	Min	Max		
System Clock Cycle Time	CL = 3	tCK3	6.0	1000	7.5	1000	ns	
	CL = 2	tCK2	-	1000	10	1000	ns	
Clock High Pulse Width		tCHW	2.5	-	2.5	-	ns	1
Clock Low Pulse Width		tCLW	2.5	-	2.5	-	ns	1
Access Time From Clock	CL = 3	tAC3	-	5.4	-	5.4	ns	2
	CL = 2	tAC2	-	-	-	6	ns	2
Data-out Hold Time		tOH	2.0	-	2.5	-	ns	
Data-Input Setup Time		tDS	1.5	-	1.5	-	ns	1
Data-Input Hold Time		tDH	0.8	-	0.8	-	ns	1
Address Setup Time		tAS	1.5	-	1.5	-	ns	1
Address Hold Time		tAH	0.8	-	0.8	-	ns	1
CKE Setup Time		tCKS	1.5	-	1.5	-	ns	1
CKE Hold Time		tCKH	0.8	-	0.8	-	ns	1
Command Setup Time		tCS	1.5	-	1.5	-	ns	1
Command Hold Time		tCH	0.8	-	0.8	-	ns	1
CLK to Data Output in Low-Z Time		tOLZ	1.0	-	1.0	-	ns	
CLK to Data Output in High-Z Time	CL = 3	tOHZ3	2.7	5.4	2.7	5.4	ns	
	CL = 2	tOHZ2	-	-	3	6	ns	

**Note:**

1. Assume  $t_R$  /  $t_F$  (input rise and fall time) is 1ns. If  $t_R$  &  $t_F$  > 1ns, then  $[(t_R+t_F)/2-1]$ ns should be added to the parameter.
2. Access time to be measured with input signals of 1V/ns edge rate, from 0.8V to 0.2V. If  $t_R$  > 1ns, then  $(t_R/2-0.5)$ ns should be added to the parameter.



## AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Speed (MHz)	166		133		Unit	Note
			Min	Max	Min	Max		
RAS Cycle Time	Operation	tRC	60	-	63	-	ns	
	Auto Refresh	tRRC	60	-	63	-	ns	
RAS to CAS Delay		tRCD	18	-	20	-	ns	
RAS Active Time		tRAS	42	100K	42	100K	ns	
RAS Precharge Time		tRP	18	-	20	-	ns	
RAS to RAS Bank Active Delay		tRRD	12	-	15	-	ns	
CAS to CAS Delay		tCCD	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	CLK	
Data-in to Precharge Command		tdPL	2	-	2	-	CLK	
Data-In to Active Command		tdAL	tdPL + tRP					
DQM to Data-Out Hi-Z		tdQZ	2	-	2	-	CLK	
DQM to Data-In Mask		tdQM	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	CLK	
Precharge to Data Output High-Z	CL = 3	tPROZ3	3	-	3	-	CLK	
	CL = 2	tPROZ2	-	-	2	-	CLK	
Power Down Exit Time		tdPE	1	-	1	-	CLK	
Self Refresh Exit Time		tsRE	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	ms	

**Note:** 1. A new command can be given tRC after self refresh exit.

## BASIC FUNCTIONAL DESCRIPTION

### Mode Register

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	OP Code	0	0	CAS Latency			BT	Burst Length		

#### OP Code

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

#### Burst Type

A3	Burst Type
0	Sequential
1	Interleave

#### CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

#### Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3 = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full page	Reserved



## COMMAND TRUTH TABLE

Function	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10 / AP	BA	Note
Mode Register Set	H	X	L	L	L	L	X	Op Code			
No Operation	H	X	L	H	H	H	X	X			
Device Deselect	H	X	H	X	X	X	X	X			
Bank Active	H	X	L	L	H	H	X	Row Address		V	
Read	H	X	L	H	L	H		Col- umn	L	V	
Read with Autoprecharge	H	X	L	H	L	H	X	Col- umn	H	V	
Write	H	X	L	H	L	L	X	Col- umn	L	V	
Write with Autoprecharge	H	X	L	H	L	L	X	Col- umn	H	V	
Precharge All Banks	H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank	H	X	L	L	H	L	X	X	L	V	
Burst stop	H	X	L	H	H	L	X	X			
DQM	H	X	X				V	X			2
Auto Refresh	H	H	L	L	L	H	X	X			
Burst-Read Single-Write	H	X	L	L	L	H	X	A9 Pin High (Other Pins OP code)			
Self Refresh Entry	H	L	L	L	L	H	X	X			
Self Refresh Exit	L	H	H	X	X	X	X	X			1
			L	H	H	H					
Precharge Power Down Entry	H	L	H	X	X	X	X	X			
			L	H	H	H					
Precharge Power Down Exit	L	H	H	X	X	X	X	X			
			L	H	H	H					
Clock Suspend Entry	H	L	H	X	X	X	X	X			
			L	V	V	V					
Clock Suspend Exit	L	H	X				X	X			

Note : 1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.  
 2. see to Next page (DQM TRUTH TABLE)



## DQM TRUTH TABLE

Function	CKEn-1	CKEn	LDQM	UDQM
Data Write/Output enable	H	X	L	L
Data Mask/Output disable	H	X	H	H
Lower byte write/Output enable, Upper byte mask/Output disable	H	X	L	H
Lower byte Mask/Output disable, Upper byte write/Output enable	H	X	H	L

Note 1. H: High Level, L: Low Level, X: Don't Care

2. Write DQM Latency is 0 CLK and Read DQM Latency is 2 CLK



## CURRENT STATE TRUTH TABLE (Sheet 1 of 4)

Current State	Command						Action	Notes	
	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0/BA1	Amax-A0			Description
idle	L	L	L	L		OP CODE	Mode Register Set	Set the Mode Register	
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto or Self Refresh	5
	L	L	H	L	BA	X	Precharge	No Operation	
	L	L	H	H	BA	Row Add.	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4
	L	H	H	H	X	X	No Operation	No Operation	3
	H	X	X	X	X	X	Device Deselect	No Operation or Power Down	3
Row Active	L	L	L	L		OP CODE	Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Precharge	7
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Start Write : optional AP(A10=H)	6
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Start Read : optional AP(A10=H)	6
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L		OP CODE	Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Termination Burst: Start the Precharge	
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Termination Burst: Start Write(optional AP)	8,9
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Termination Burst: Start Read(optional AP)	8
	L	H	H	H	X	X	No Operation	Continue the Burst	





## CURRENT STATE TRUTH TABLE (Sheet 2 of 4)

Current State	Command						Action	Notes	
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0/BA1	Amax-A0			Description
Read	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	Termination Burst: Start the Precharge	10
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Termination Burst: Start Write(optional AP)	8
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Termination Burst: Start Read(optional AP)	8,9
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Read with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	12
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	12
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	



## CURRENT STATE TRUTH TABLE (Sheet 3 of 4)

Current State	Command						Action	Notes	
	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0/BA1	Amax-A0			Description
Precharging	L	L	L	L		OP CODE	Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	No Operation: Bank(s) idle after tRP	
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,12
	L	H	H	H	X	X	No Operation	No Operation: Bank(s) idle after tRP	
	H	X	X	X	X	X	Device Deselect	No Operation: Bank(s) idle after tRP	
Row Activating	L	L	L	L		OP CODE	Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,12
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,11,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,12
	L	H	H	H	X	X	No Operation	No Operation: Row Active after tRCD	
	H	X	X	X	X	X	Device Deselect	No Operation: Row Active after tRCD	
Write Recovering	L	L	L	L		OP CODE	Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	Start Write: Optional AP(A10=H)	
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	Start Read: Optional AP(A10=H)	9
	L	H	H	H	X	X	No Operation	No Operation: Row Active after tDPL	



## CURRENT STATE TRUTH TABLE (Sheet 4 of 4)

Current State	Command						Action	Notes	
	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0/BA1	Amax-A0			Description
Write Recovering	H	X	X	X	X	X	Device Deselect	No Operation: Row Active after tDPL	
Write Recovering with Auto Precharge	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	4,13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	4,12
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	4,12
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	4,9,12
	L	H	H	H	X	X	No Operation	No Operation: Precharge after tDPL	
Refreshing	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	13
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	13
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	13
	L	H	H	H	X	X	No Operation	No Operation: idle after tRC	
Mode Register Accessing	L	L	L	L	OP CODE		Mode Register Set	ILLEGAL	13
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	13
	L	L	H	L	BA	X	Precharge	ILLEGAL	13
	L	L	H	H	BA	Row Add.	Bank Activate	ILLEGAL	13
	L	H	L	L	BA	Col Add. A10	Write/WriteAP	ILLEGAL	13
	L	H	L	H	BA	Col Add. A10	Read/ReadAP	ILLEGAL	13
	L	H	H	H	X	X	No Operation	No Operation: idle after 2 clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation: idle after 2 clock cycles	



---

Note :

1. H: Logic High, L: Logic Low, X: Don't care, BA: Bank Address, AP: Auto Precharge.
2. All entries assume that CKE was active during the preceding clock cycle.
3. If both banks are idle and CKE is inactive, then in power down cycle
4. Illegal to bank in specified states. Function may be legal in the bank indicated by Bank Address, depending on the state of that bank.
5. If both banks are idle and CKE is inactive, then Self Refresh mode.
6. Illegal if tRCD is not satisfied.
7. Illegal if tRAS is not satisfied.
8. Must satisfy burst interrupt condition.
9. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
10. Must mask preceding data which don't satisfy tDPL.
11. Illegal if tRRD is not satisfied
12. Illegal for single bank, but legal for other banks in multi-bank devices.
13. Illegal for all banks.



CKE Enable(CKE) Truth TABLE (Sheet 2 of 1)

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0, BA1	ADDR		
Self Refresh	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Exit Self Refresh with Device Deselect	2
	L	H	L	H	H	H	X	X	Exit Self Refresh with No Operation	2
	L	H	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	L	X	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	X	INVALID	1
	L	H	H	X	X	X	X	X	Power Down mode exit, all banks idle	2
			L	H	H	H	X	X		
	L	H	L	L	X	X	X	X	ILLEGAL	2
				X	X	L	X	X		
	L	L	X	X	X	X	X	X	Maintain Power Down Mode	
All Banks Idle	H	H	H	X	X	X			Refer to the idle State section of the Current State Truth Table	3
	H	H	L	H	X	X				3
	H	H	L	L	H	X				3
	H	H	L	L	L	H	X	X	Auto Refresh	
	H	H	L	L	L	L		OP CODE	Mode Register Set	4
	H	L	H	X	X	X			Refer to the idle State section of the Current State Truth Table	3
	H	L	L	H	X	X				3
	H	L	L	L	H	X				3
	H	L	L	L	L	H	X	X	Entry Self Refresh	4
	H	L	L	L	L	L		OP CODE	Mode Register Set	
L	X	X	X	X	X	X	X	Power Down	4	



## CKE Enable(CKE) Truth TABLE (Sheet 2 of 2)

Current State	CKE		Command						Action	Notes
	Previous Cycle	Current Cycle	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0, BA1	ADDR		
Any State other than listed above	H	H	X	X	X	X	X	X	Refer to operations of the Current State Truth Table	
	H	L	X	X	X	X	X	X	Begin Clock Suspend next cycle	
	L	H	X	X	X	X	X	X	Exit Clock Suspend next cycle	
	L	L	X	X	X	X	X	X	Maintain Clock Suspend	

Note :

1. For the given current state CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. When exiting power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high.
3. The address inputs depend on the command that is issued.
4. The Precharge Power Down mode, the Self Refresh mode, and the Mode Register Set can only be entered from the all banks idle state.
5. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. When exiting deep power down mode, a NOP (or Device Deselect) command is required on the first positive edge of clock after CKE goes high and is maintained for a minimum 200usec.



### PACKAGE INFORMATION

54 Ball FBGA 0.8mm pitch (Size 8.0mm x 8.0mm)

