

## H5N2004DL, H5N2004DS

Silicon N Channel MOS FET  
High Speed Power Switching

REJ03G1103-0200  
(Previous: ADE-208-1372)  
Rev.2.00  
Sep 07, 2005

### Features

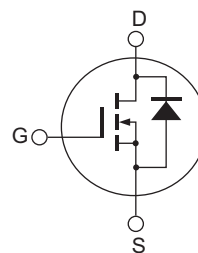
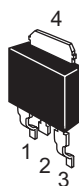
- Low on-resistance:  $R_{DS(on)} = 0.38 \Omega$  typ.
- Low leakage current:  $I_{DSS} = 1 \mu A$  max (at  $V_{DS} = 200 V$ )
- High speed switching:  $t_f = 10 ns$  typ (at  $V_{GS} = 10 V$ ,  $V_{DD} = 100 V$ ,  $I_D = 4 A$ )
- Low gate charge:  $Q_g = 14 nC$  typ (at  $V_{DD} = 160 V$ ,  $V_{GS} = 10 V$ ,  $I_D = 8 A$ )
- Avalanche ratings

### Outline

RENESAS Package code: PRSS0004ZD-B  
(Package name: DPAK (L)-(2) )



RENESAS Package code: PRSS0004ZD-C  
(Package name: DPAK (S) )



1. Gate
2. Drain
3. Source
4. Drain

## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V <sub>DSS</sub>	200	V
Gate to source voltage	V <sub>GSS</sub>	±30	V
Drain current	I <sub>D</sub>	8	A
Drain peak current	I <sub>D (pulse)</sub> <sup>Note 1</sup>	32	A
Body-drain diode reverse drain current	I <sub>DR</sub>	8	A
Body-drain diode reverse drain peak current	I <sub>DR (pulse)</sub> <sup>Note 1</sup>	32	A
Avalanche current	I <sub>AP</sub> <sup>Note 3</sup>	7	A
Channel dissipation	P <sub>ch</sub> <sup>Note 2</sup>	30	W
Channel to case thermal impedance	θ <sub>ch-c</sub>	4.17	°C/W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value at T<sub>c</sub> = 25°C3. T<sub>ch</sub> ≤ 150°C

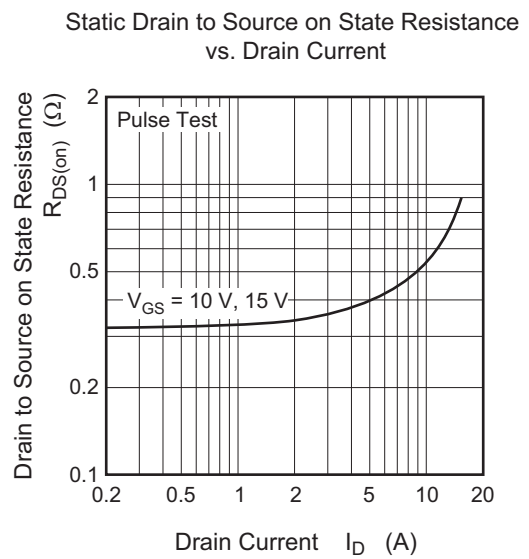
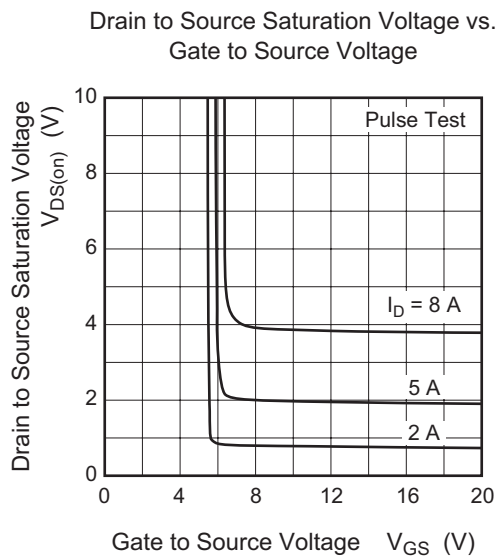
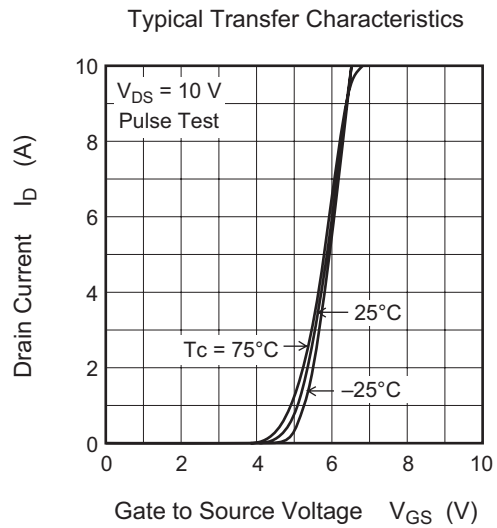
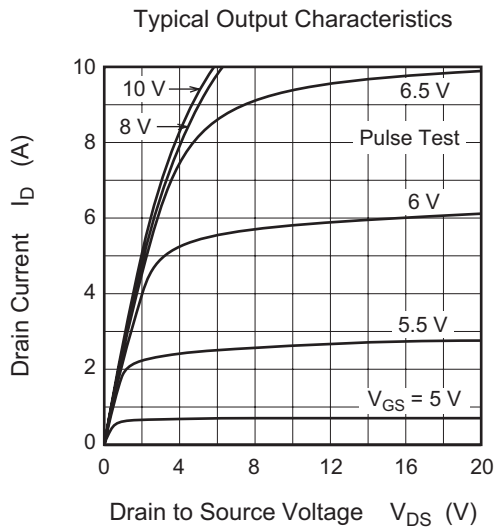
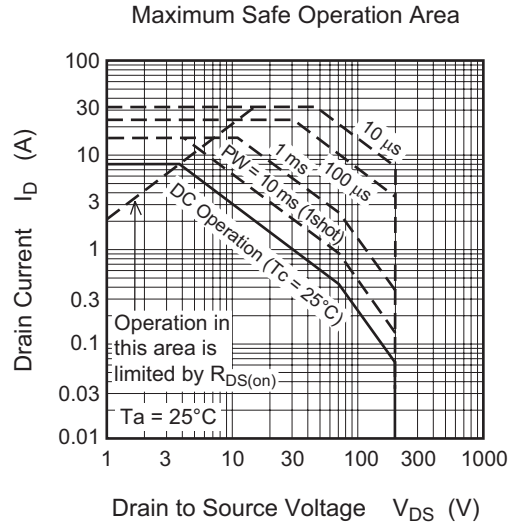
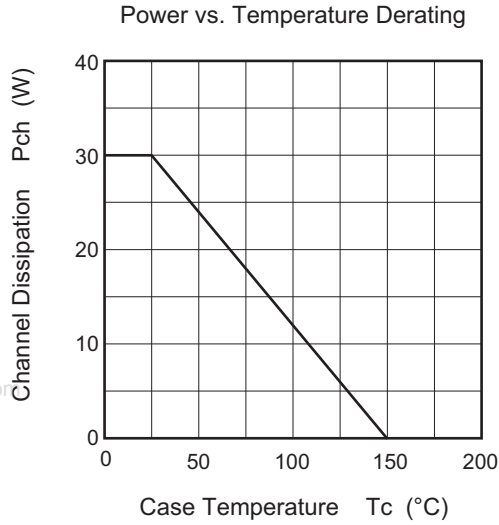
## Electrical Characteristics

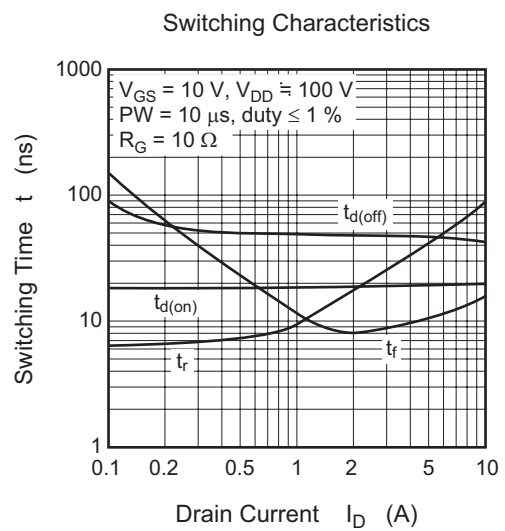
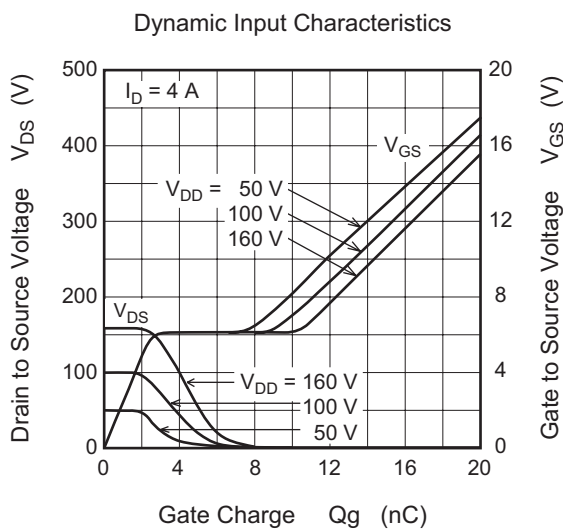
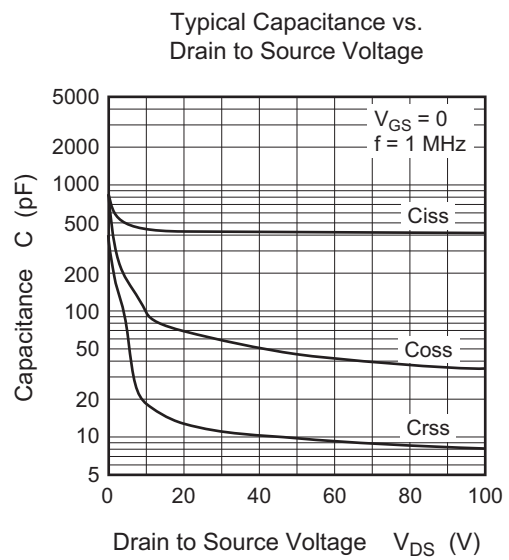
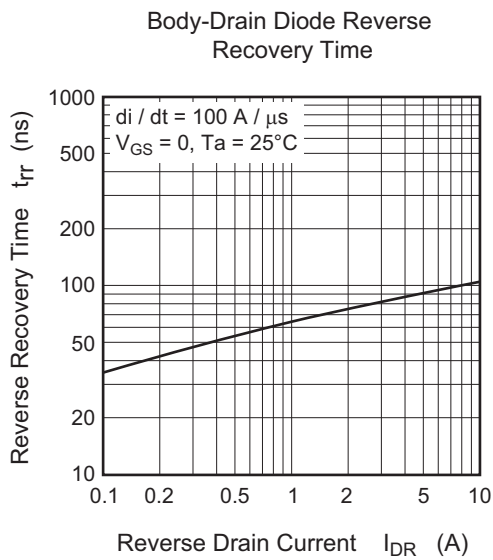
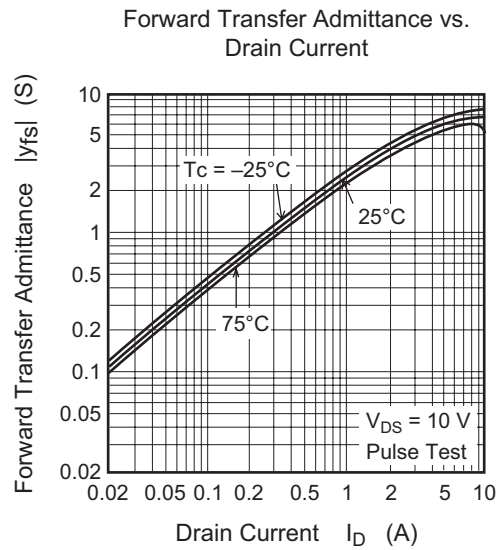
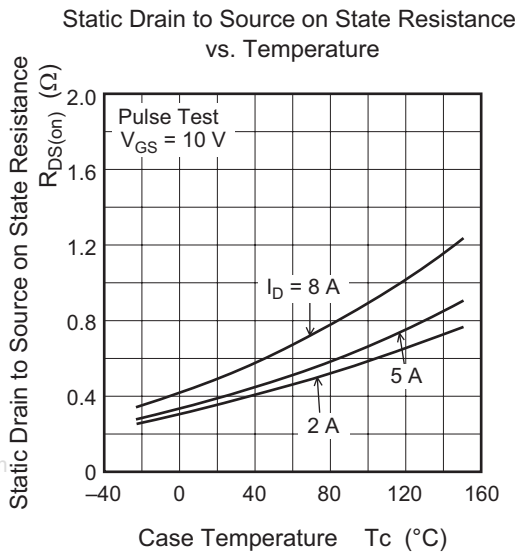
(Ta = 25°C)

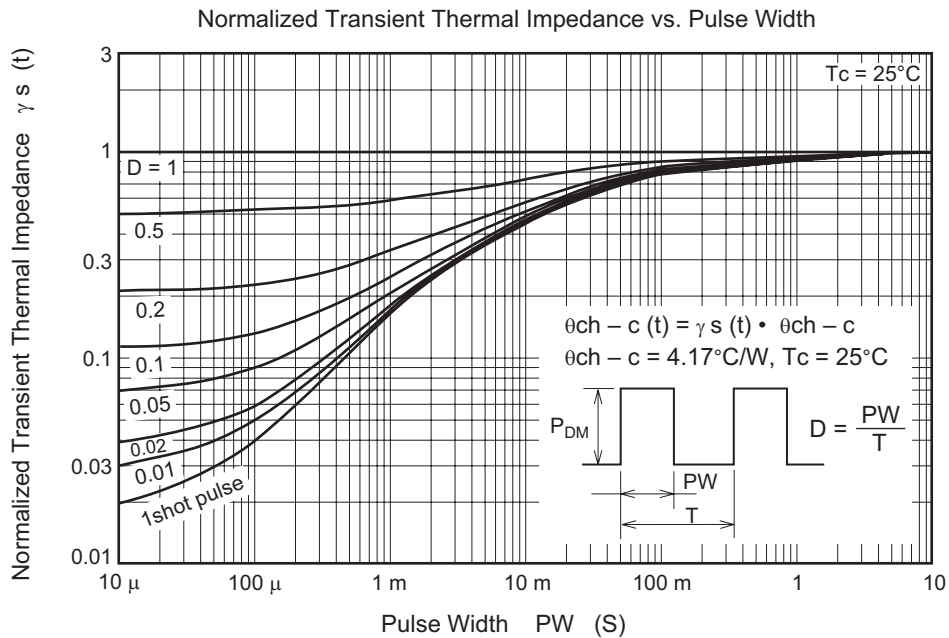
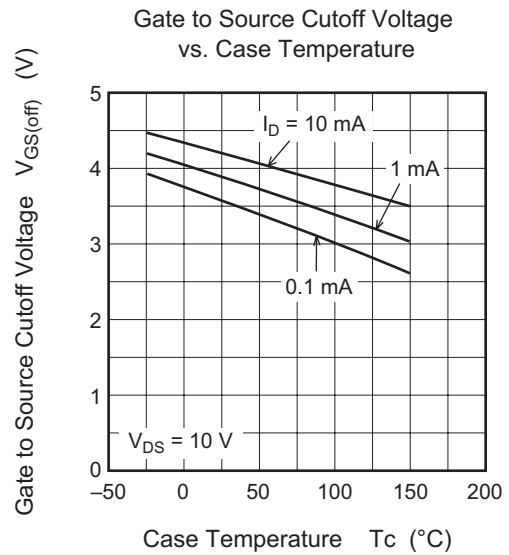
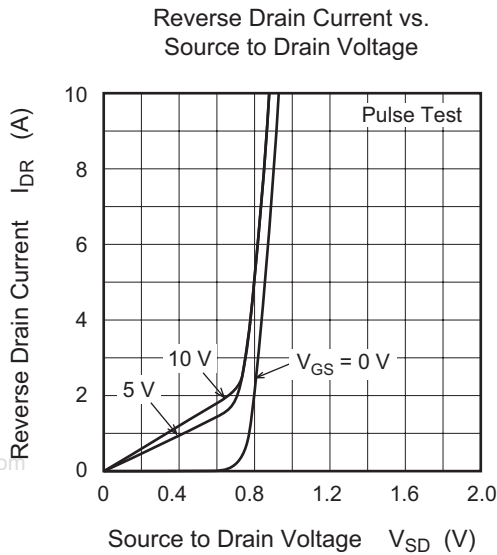
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V <sub>(BR) DSS</sub>	200	—	—	V	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	±0.1	μA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0
Gate to source cutoff voltage	V <sub>GS (off)</sub>	3.0	—	4.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Static drain to source on state resistance	R <sub>DS (on)</sub>	—	0.38	0.48	Ω	I <sub>D</sub> = 4 A, V <sub>GS</sub> = 10 V <sup>Note 4</sup>
Forward transfer admittance	y <sub>fs</sub>	3.3	5.5	—	S	I <sub>D</sub> = 4 A, V <sub>DS</sub> = 10 V <sup>Note 4</sup>
Input capacitance	C <sub>iss</sub>	—	450	—	pF	V <sub>DS</sub> = 25 V
Output capacitance	C <sub>oss</sub>	—	65	—	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	C <sub>rss</sub>	—	13	—	pF	f = 1 MHz
Turn-on delay time	t <sub>d (on)</sub>	—	19	—	ns	I <sub>D</sub> = 4 A
Rise time	t <sub>r</sub>	—	32	—	ns	V <sub>GS</sub> = 10 V
Turn-off delay time	t <sub>d (off)</sub>	—	47	—	ns	R <sub>L</sub> = 25 Ω
Fall time	t <sub>f</sub>	—	10	—	ns	R <sub>g</sub> = 10 Ω
Total gate charge	Q <sub>g</sub>	—	14	—	nC	V <sub>DD</sub> = 160 V
Gate to source charge	Q <sub>gs</sub>	—	2.5	—	nC	V <sub>GS</sub> = 10 V
Gate to drain charge	Q <sub>gd</sub>	—	7.5	—	nC	I <sub>D</sub> = 4 A
Body-drain diode forward voltage	V <sub>DF</sub>	—	0.9	1.4	V	I <sub>F</sub> = 8 A, V <sub>GS</sub> = 0
Body-drain diode reverse recovery time	t <sub>rr</sub>	—	100	—	ns	I <sub>F</sub> = 8 A, V <sub>GS</sub> = 0
Body-drain diode reverse recovery charge	Q <sub>rr</sub>	—	0.4	—	μC	di <sub>F</sub> /dt = 50 A/μs

Note: 4. Pulse test

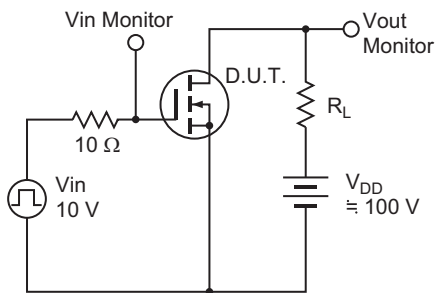
Main Characteristics



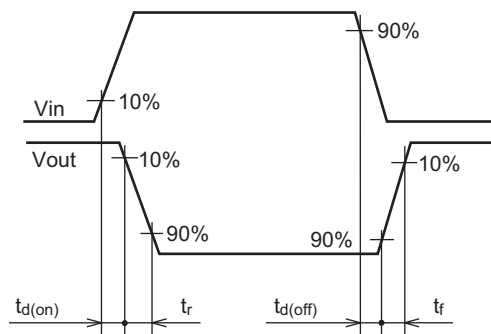




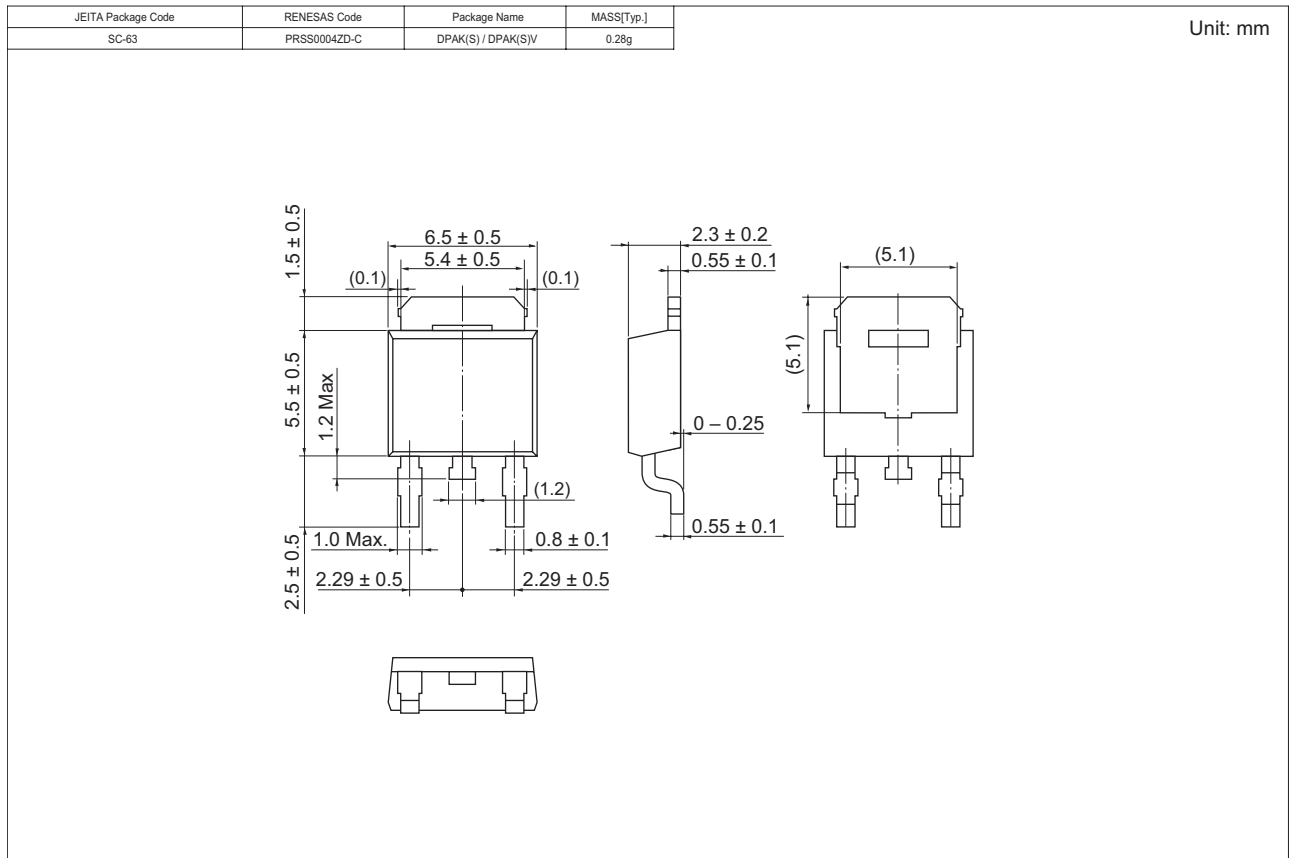
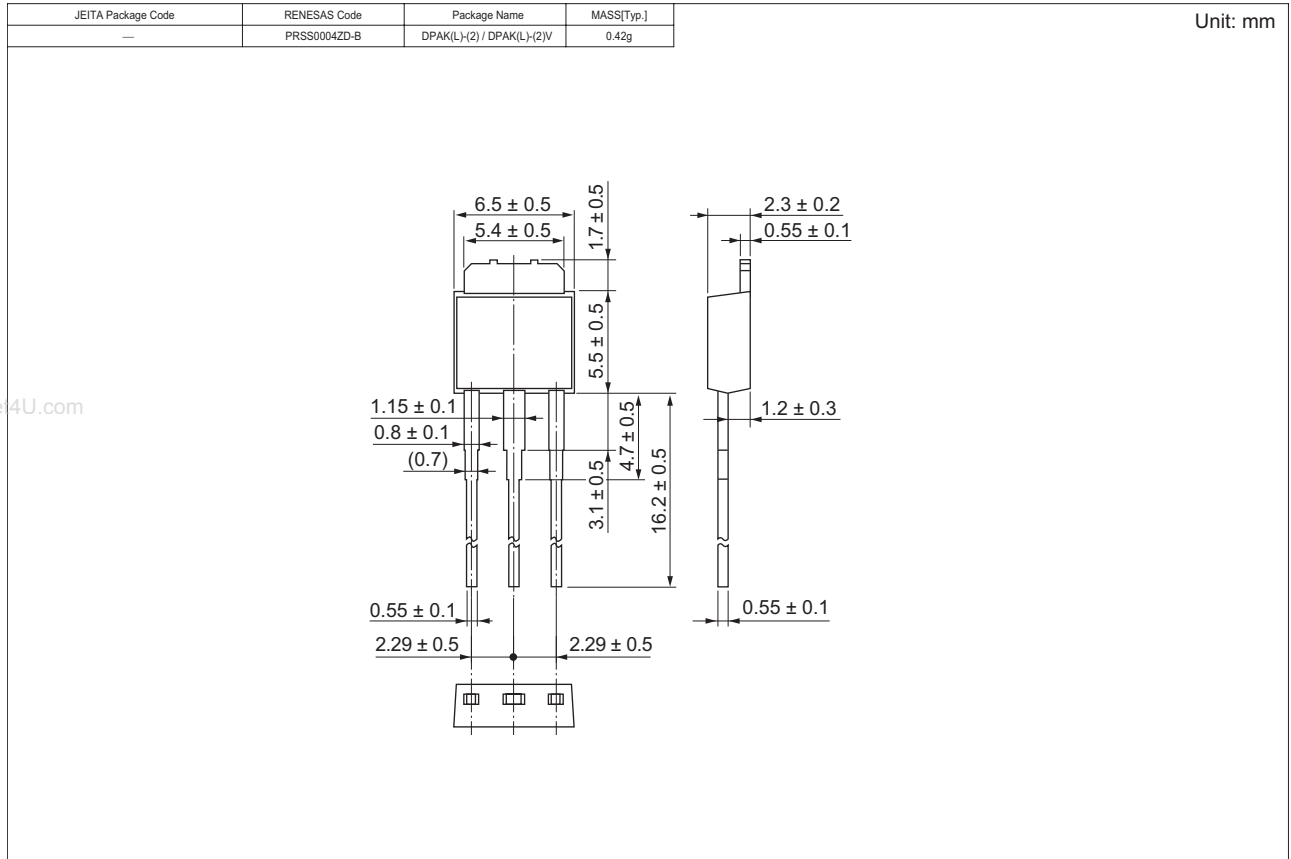
Switching Time Test Circuit



Waveform



Package Dimensions



### Ordering Information

Part Name	Quantity	Shipping Container
H5N2004DL-E	3200 pcs	Box (Sack)
H5N2004DSTL-E	3000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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