H6850 Series

Novel Low Cost Green-Power PWM Controller With Low EMI Technique

Feature

- Low Cost, PWM&PFM&CRM (Cycle Reset Mode)
- Low Start-up Current (about 3μA)
- Low Operating Current (about 1.2mA)
- Current Mode Operation
- Under Voltage Lockout (UVLO)
- Built-in Synchronized Slope Compensation
- Built-in Low EMI Technique
- Programmable PWM Frequency
- Audio Noise Free Operation
- Leading edge Blanking on Sense input
- Constant output power limiting for universal AC input Range
- SOT-23-6 L 、SOP8 and DIP-8 Pb-Free Packaging
- Good Protection Coverage With Auto Self-Recovery
- Compatible with **SG6848 (6849) / SG5701/SG5848/LD7535 (7550) / OB2262 (2263)/OB2278（2279）**

- **Complete Protection with**
  - Soft Clamped GATE output voltage 18.0V
  - VDD over voltage protect 34.0V
  - Cycle-by-cycle current limiting
  - Output SCP (Short circuit Protection)
  - Output OLP (Over Load Protection)
  - High-Voltage CMOS Process with ESD

Applications

- Switching AC/DC Adaptor
- Battery Charger
- Open Frame Switching Power Supply
- Standby Power Supplies
- Set-Top Box Power Supplies
- 384X Replacement

General Description

The H68 50 is a highly integrated low cost current mode PWM controller, which is ideal for small power cur rent mode of of fline AC-DC fly- back converter applic ations. Making use of external resistors, the IC changes the operating frequency and automatically enters the PFM/CRM (Cycle Reset Mode) und er light-load/zer o-load conditions. This can minimize standby power consumption and achieve powe r-saving functions. With a very lo w st art-up current, the H685 0 could use a large value start-up resistor (2MΩ).

Built-in synchronized slo pe compens ation enhances the st ability of the syste m and avoids sub-harmonic oscillation. D ynamic peak current limiting circuit minimizes output power chang e caused by delay time of the system over a universal AC input range.

Leading edge blanking circuit on current sense input could remove the signal glitch due to snubber circuit diode reverse recovery and thus greatly reduces the external component count and system cost in the design. Cycle-by-Cycle current limiting ensures safe operation even during short-circuit.

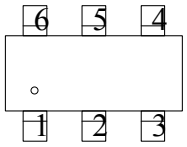
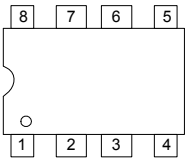
Excellent EMI performance is achieved built-in soft driver and low EMI technique.

The H68 50 offers perfect protection like OVP(Over Voltage Prote ction)、OLP(Over Load Protection) 、 SCP(Short circuit protection)、OTP、Sense Fault Protection and OCP(Over current protection). The H6850's output driver is soft clamped to maximum 18.0V to protect the power MOSFET. H6850 is offered in SOT-23-6L, SOT-8 and DIP-8 packages.

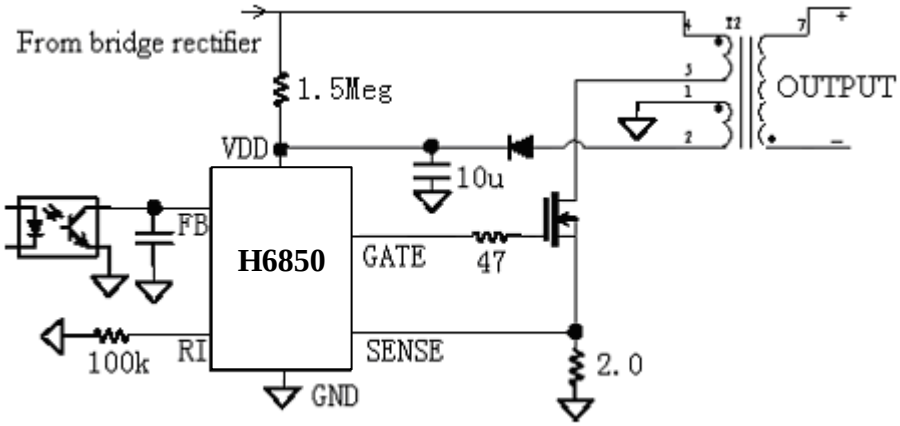
Pin Assignment

Part Number	Description
H6850NF	SOT26, Pb-free,in T/R
H6850S	SOP-8, Pb-free in T/R
H6850P	DIP-8, Pb-free in Tube

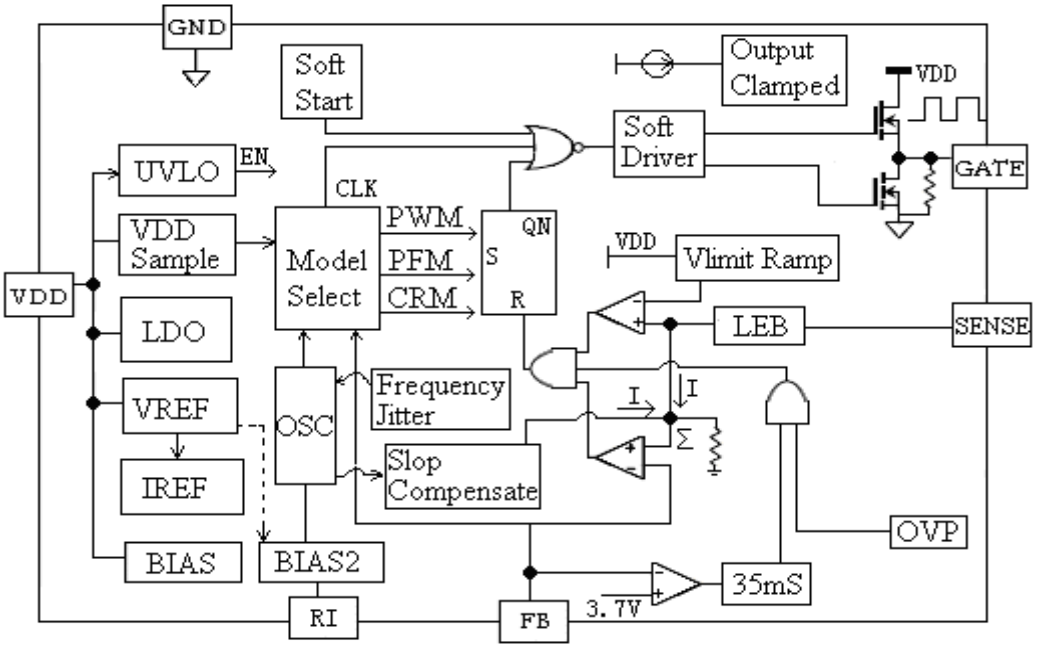
Pin Descriptions

Package	Function		Description
	SOT-26	DIP-8	
 SOT-26	Pin6: GATE	Pin1: GATE	Totem-pole output to drive the external power MOSFET
	Pin5: VDD	Pin2: VDD	Supply voltage pin.
		Pin3: NC	NC Pin.
	Pin4: SENSE	Pin4: SENSE	Current se nse pin, a r esistor connects t o sense the MOSFET current.
 DIP -8(SOP-8)	Pin3: RI	Pin5: RI	This p in is to program the switching freque ncy. By connecting a resistor to ground to set th e switching frequency.
		Pin6: NC	NC Pin
	Pin2: FB	Pin7:FB	Voltage feedback pin. Output current of this pin could controls the PWM duty cycle、OLP and SCP.
	Pin1: GND	Pin8: GND	GND Pin

TYPICAL APPLICATION



Block Diagram



Simplified Internal Circuit Architecture

Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
V_{DD}	Supply voltage Pin Voltage		40	V
I_{OVP}	VDD OVP maximal enter current		20	mA
V_{FB}	Input Voltage to FB Pin		-0.3 to 6V	V
V_{SEN}	Input Voltage to SEN Pin		-0.3 to 6V	V
P_D	Power Dissipation		300	mW
	ESD Capability, HBM Model		2500	V
	ESD Capability, Machine Model		250	V
T_L	Lead Temperature (Soldering)	SOT-23-6L (20S)	220	℃
		DIP-8 (10S)	260	℃
		SOP-8 (10S)	230	℃
T_{STG}	Storage Temperature Range		-55 to + 150	℃

RECOMMENDED OPERATION CONDITION

Symbol	Parameter	Min ~ Max	Unit
VDD	VDD Supply Voltage	10~30	V
RI	RI PIN Resistor Value	100	K ohm
T_{OA}	Operation Ambient Temperature	-20~85	℃
P_{OMAX}	Maximal Output Power	0~80	W
F_{PWM}	Frequency of PWM	30~150	kHz

Electrical Characteristics (Ta=25°C unless otherwise noted, V_{DD} = 16V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD} Pin)						
I_{ST}	Startup Current			3.0	20.0	μA
I_{SS}	Operating Current	V_{FB}=0V		3.0		mA
		V_{FB}=3V		1.2		mA
		V_{FB}=Open		0.8		mA
VDD_{ON}	Turn-on Threshold Voltage		13.0	14.0	15.0	V
VDD_{OFF}	Turn-off Threshold Voltage		7.8	8.8	9.8	V
VDD_{CLAMP}	VDD Clamp Voltage	I_{VDD}=10mA		34.0		V
VDD_{AIS}	Anti Intermission Surge VDD Voltage			9.4		V
Voltage Feedback (FB Pin)						
I_{FB}	Short Circuit Current	V_{FB}=0V		0.7		mA
V_{FB}	Open Loop Voltage	V_{FB}=Open		4.8		V
I_{FB_0D}	Zero Duty Cycle FB current			0.59		mA
I_{PFM}	Enter PFM FB current			0.50		mA
I_{CRM}	Enter CRM FB current			0.55		mA
V_{PFM}	Enter PFM Threshold V_{FB}			1.80		V
V_{CRM}	Enter CRM Threshold V_{FB}			1.40		V
$I_{OLP\&SCP}$	Enter OLP&SCP FB current			170		uA
$V_{OLP\&SCP}$	Enter OLP&SCP FB voltage			3.7		V
$T_{OLP\&SCP}$	OLP&SCP min. delay Time	RI=100K	33	35	50	mS
Current Sensing (SEN Pin)						
V_{TH_L}	SEN Maximum Voltage Level （Dmin=0%）	RI=100K, FB=3.3V		0.80		V
V_{TH_H}	SEN Maximum Voltage Level(Dmax=78%)	RI=100K, FB=3.3V		1.05		V
T_{PD}	Delay to Output	FB=3.3V		75		ns

R_{CS}	Input Impedance			40		KΩ
T_{LEB}	Leading edge blanking time (LEB)	RI=100K		300		nS
Oscillator (RI Pin)						
F_{OSC}	Normal Frequency	RI=100Kohm	60	65	70	KHz
F_{PFM}	PFM Frequency	RI=100Kohm		22		KHZ
DC_{MAX_W}	Maximum Duty Cycle PWM	RI=100Kohm		78		%
DC_{MAX_F}	Maximum Duty Cycle PFM	RI=100Kohm		78		%
ΔF_{TEMP}	Frequency Temp. Stability	-30-100℃		5		%
T_{BLANK}	Leading-Edge Blanking Time			300		nS
F_{JITTER}	Frequency jitter	RI=100Kohm	-4		4	%
GATE Drive Output (GATE Pin)						
V_{OL}	Output Low Level	V_{DD}=16V, I_O=20mA			0.8	V
V_{OH}	Output High Level	V_{DD}=16V, I_O=20mA	10			V
T_{R1}	Rising Time	C_L=500pF		123		ns
T_{F1}	Falling Time	C_L=500pF		71		ns
T_{R2}	Rising Time	C_L=1000pF		248		ns
T_{F2}	Falling Time	C_L=1000pF		116		ns
T_{R3}	Rising Time	C_L=1500pF		343		ns
T_{F3}	Falling Time	C_L=1500pF		153		ns
T_{R4}	Rising Time	C_L=2000pF		508		ns
T_{F4}	Falling Time	C_L=2000pF		209		ns
VG_{CLAMP}	Output Clamp Voltage	VDD=20V		18.0		V
Low EMI technique						
f_{EMI}	Low EMI frequency	RI=100Kohm		65		KHz
Δf_osc	Frequency modulation range /Base frequency	RI=100Kohm	-3		3	%

OPERATION DESCRIPTION

Current Mode

Compared t o voltag e mode contr ol, current mode control has a current feedback loop. When the voltage of the Sense resistor peak current of the primary winding reaches the internal setting value V_{TH}, the register resets and the power MOSFET cuts off. So, to detect and modulate the peak current cycle-by-cycle could control the output of the power supply. The current feedback has a good linear modulation rate and a fast input and output dynamic impact, and avoid the pole that the output filter inductance brings and the two-class system descends to the one-class. So it widens the frequency range and optimizes overload protection and short circuit protection.

Startup Current and Under Voltage Lockout

The startup current of H 6850 is se t to be very l ow so that a large value startup resistor can be used to minimize the power loss. For AC to DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor and a 10uF/25V VDD hold capacitor could be used.

The turn-on and turn-off threshold of the H6850 is designed to 14V/8.8V. During startup, the hold-up capacitor must be charge to 14.0V through the startup resistor. The hysteresis is implemented to prevent the shutdown from the voltage dip during startup.

Internal Bias and OSC Operation

A resistor connected between RI pin and GND pin sets the internal constant current source to charge or discharge the internal fixed capacitor. The charge time and discharge time determines the internal clock speed and the switching frequency. Increasing the resistance will reduce the value of the input current and reduce the switching frequency. The relationship between RI and PWM switching frequency follows the below equation within the RI allowed range.

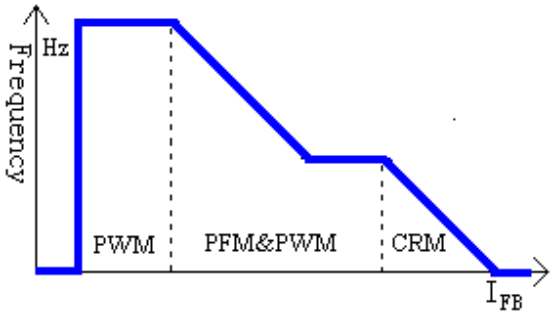
$$F_{OSC} = \frac{6500}{RI(K\Omega)}(kHz)$$

For example, a 100kΩ resistor RI could generate a 20uA constant current and a 65kHz PWM switching frequency. The suggested operating frequency range of H6850 is within 50KHz to 150KHz.

Green Power Operation

The pow er dissip ation of switching mode power supply is very important in zero load o r lig ht load co ndition. The majo r dissipation results from conduction loss、switching loss and consume of the control circuit. However, all of them relates to the switching frequency. There are many difference topologies has been implemented in different chip. The basic operation theory of all these approaches intends to reduce the switching frequency under light-load or no-load condition.

The H6850`s green power function adapts PWM、PFM and CRM combining modulation. When RI resistor is 100kΩ, the PWM frequency is 65kHz in medium or heavy load operation. Through modifying the pulse width, The H6850 could control output voltage. The current of FB pin increases when the load is in light condition and the internal mode controller enters PFM&PWM when the feedback current is over 0.5mA. The operation frequency of oscillator is to descend gradually. When the feedback current is over 0.55mA, the frequency of oscillator is invariable, namely 22kHz.



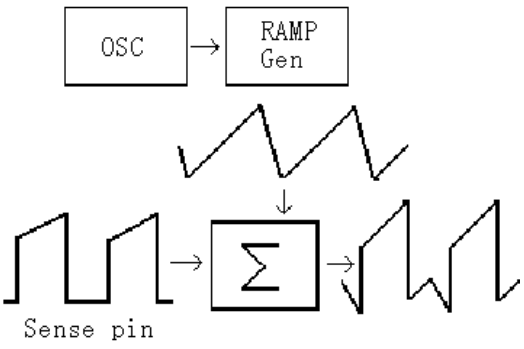
H6850 Green-Power Function

To decrease the standby consumption of the power supply, Chip-Rail introduces the Cycle Reset Mode technology (CRM). If the feedback current is over 0.59mA, mode controller of the H6850 would reset internal register all the time and cut off the GATE pin. While the output voltage is lower than the set value, the register would be set, the GATE pin operate again. So the frequency of the internal OSC is invariable, the register would reset some pulses so that the practical frequency is decreased at the GATE pin.

Internal Synchronized Slop Compensation

Although there are more advantages of the current mode control than conventional voltage mode control, there are still several drawbacks of peak-sensing current-mode converter, especially the open loop instability when it operates in higher than 50% of the duty-cycle. To solve this problem, the H6850 is introduced an internal slope compensation adding voltage ramp to the current sense input voltage for PWM generation. It improves the close loop stability greatly at CCM, prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

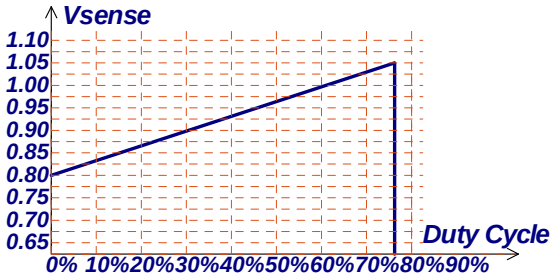
$$V_{SLOP} = 0.33 \times \frac{DUTY}{DUTY_{MAX}} = 0.4389 \times DUTY$$



Slop Compensation

Current Sensing & Dynamic peak limiting

The current flowing by the power MOSFET comes into being a voltage V_{SENSE} on the Sense pin cycl e-by-cycle, which compares to the internal reference volt age, and control s the rever se of the internal register, limits the peak current IMAX of the primary of the transformer . The transforme r energy is $E = \frac{1}{2} \times L \times I_{MAX}^{2}$. So adjusting the R_{SENSE} can set the maximal o utput power of the pow er su pple. The curre nt flowing by the power MOSFET has an extra value ($\Delta I = \frac{V_{IN}}{L_P} \times T_D$) due to the system delay time that is from de tecting the current through the Sense pin to power MOSFET off in the H6850 (Among these, V_{IN} is the primary win ding volt age of the transformer and L_P is the primary wind inductance). V_{IN} ranges from 85V AC to 264V AC. To guarantee the output power is a constant for universal input AC voltage, there is a dynamic peak limit circuit to compensate the system delay T that the system delay brings on.



OLP&SCP

To protect the circuit from being damaged under the over load or short circuit condition, a smart OLP&SCP function is implemented in the H6850. When short circuit or over load occurs in the output end, the feedback cycle would enhance the voltage of FB pin, while the voltage is over 3.7V or the current from FB is below 170uA, the internal detective circuit would send a signal to shut down the GATE and pull down the VDD voltage, then the circuit is restart. To avoid the wrong operation when circuit

starts, the delay time is set. When the RI resistance is 100Kohm , the delay time $T_{OLP\&SCP}$ is between 33m S and 50mS. The relationship between RI and $T_{OLP\&SCP}$ follows the below equation.

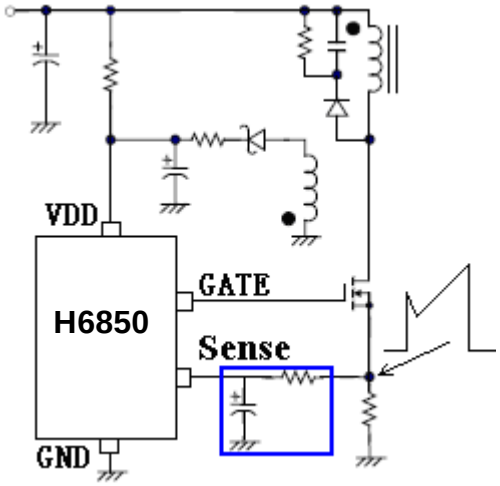
$$\frac{RI \times 2}{6 \times 10^3}(mS) < T_{OLP\&SCP} < \frac{RI \times 3}{6 \times 10^3}(mS)$$

Anti Intermission Surge

When the p ower suppli es change the heavy loa d to light load i mmediately, there could be tow phenomena caused by system delay. They are output voltage overshot and intermission surge. To avoid it, the anti intermission surge is built in the H6850. If it occurs, the FB current is to increase rapidly, the GATE would be cut off for a while, VDD pin voltage descends gradually. When VDD reaches 9.4V, the GATE pin would operate again, which the frequency is 22KHz.

Leading-edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the Sense pin, which would disturb the internal signal from the sampling of the R_{SENSE}. There is a 300nS leading edge blanking time built in to avoid the effect of the turn-on spike, and the power MOSFET cannot be switched off during the moment. So that the conventional external RC filtering on sense input is no longer required.



Over Voltage Protection (OVP)

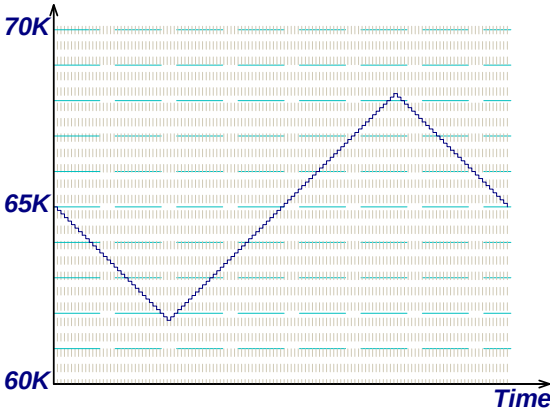
There is a 34V over-voltage protection circuit in the H6850 to improve the credibility and extend the life of the chip. When the VDD voltage is over 34V, the GATE pin is to shutdown immediately and the VDD voltage is to descend rapidly.

GATE Driver & Soft Clamped

The H6850' output designs a totem pole to drive a periphery power MOSFET. The dead time is introduced to minimize the transfixion current during the output operating. The novel soft clamp technology is introduced to protect the periphery power MOSFET from breaking down and current saturation of the Zener.

Low EMI technique

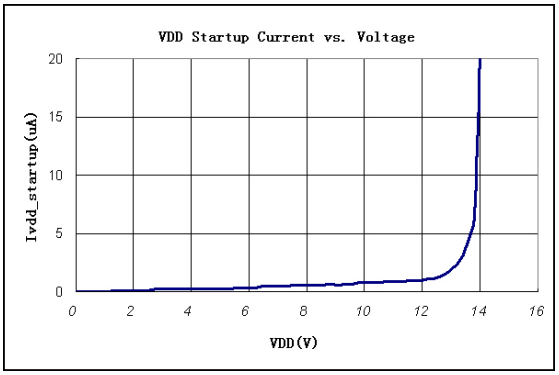
The frequen cy low EMI technique is introduced in the H6850. As following figure, the internal oscillatio n frequency is modulated b y itself. A whole surg e cycle includes 128 pulses and the jittering r anges from -4% to +4%. Thus, the function could minimize the electromagnetic interferer from the power supply module.

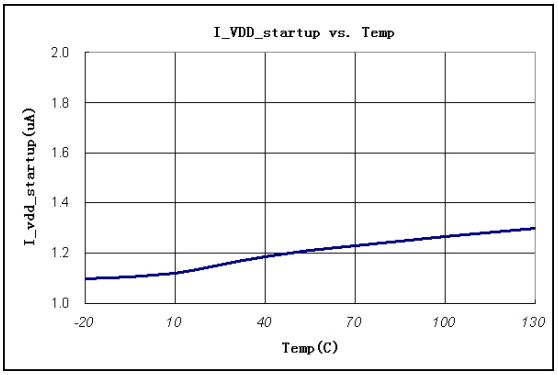


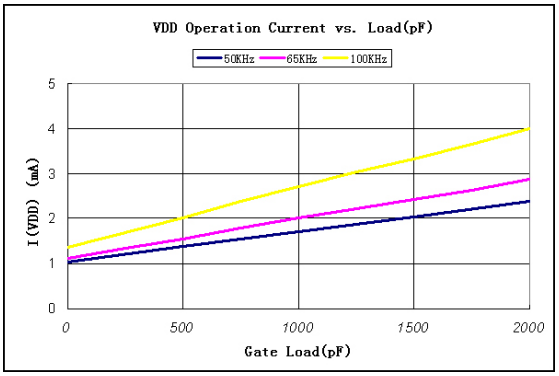
Frequency low EMI

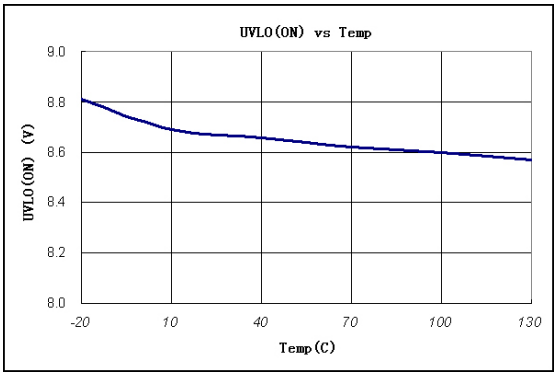
CHARACTERIZATION PLOTS

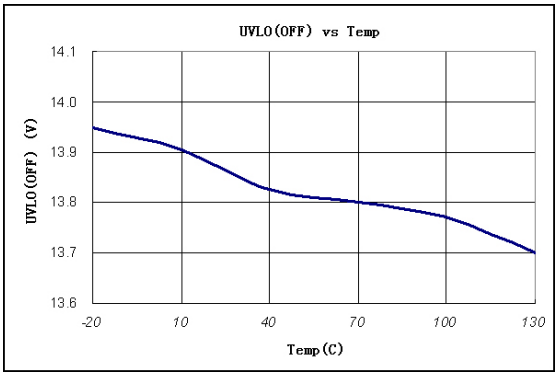
VDD=16V,RI=100Kohm,T_A=25℃ condition applies if not otherwise noted.

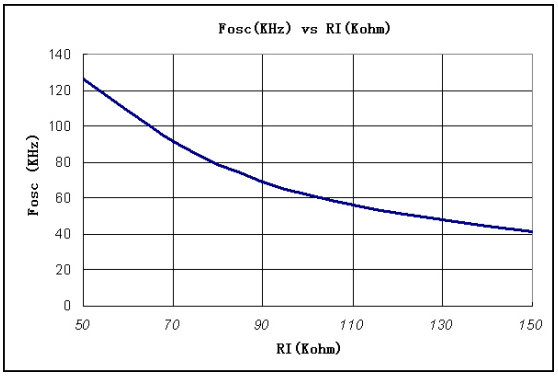


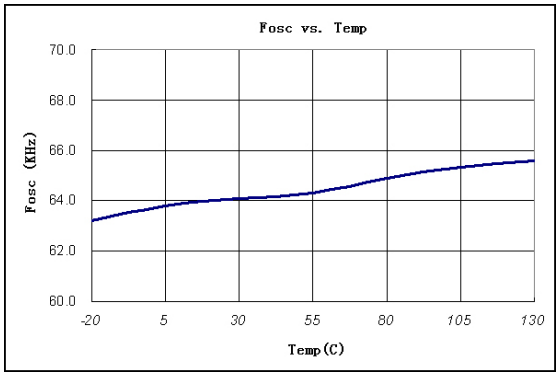


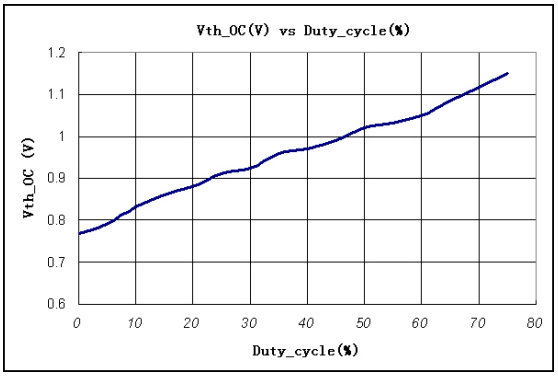






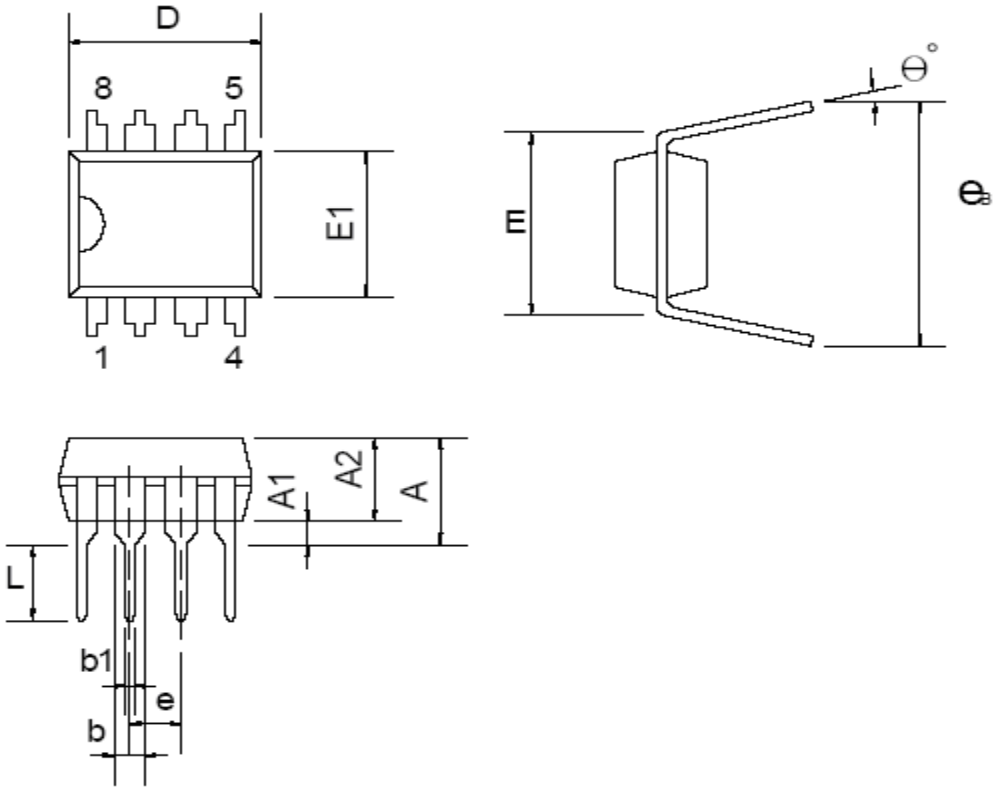



Fosc vs. Temp
70.0
68.0
66.0
64.0
62.0
60.0
Fosc (KHz)
-20
5
30
55
80
105
130
Temp(C)


Vth_OC(V) vs Duty_cycle(%)
1.2
1.1
1
0.9
0.8
0.7
0.6
Vth_OC (V)
0
10
20
30
40
50
60
70
80
Duty_cycle(%)

PACKAGE DEMENSIONS

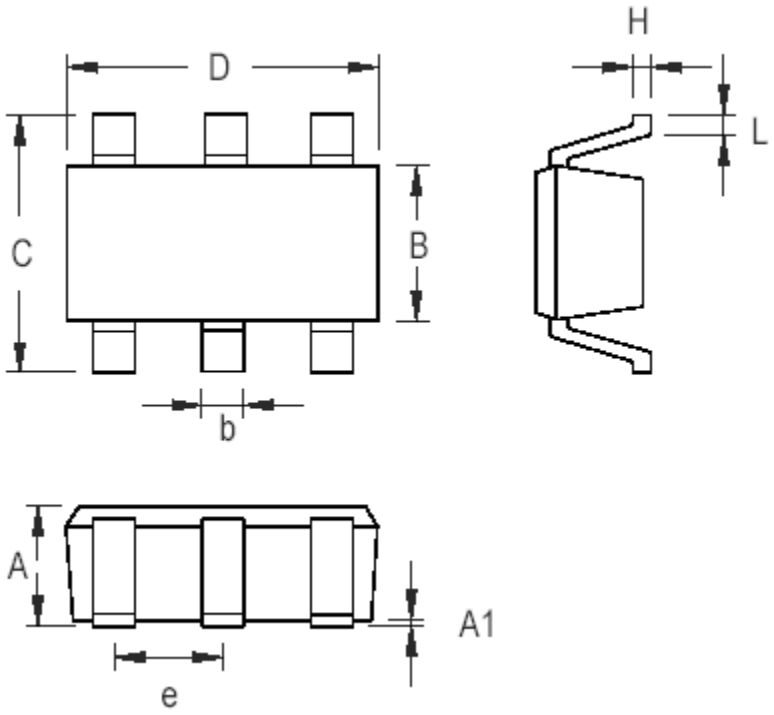
DIP-8L



Dimensions

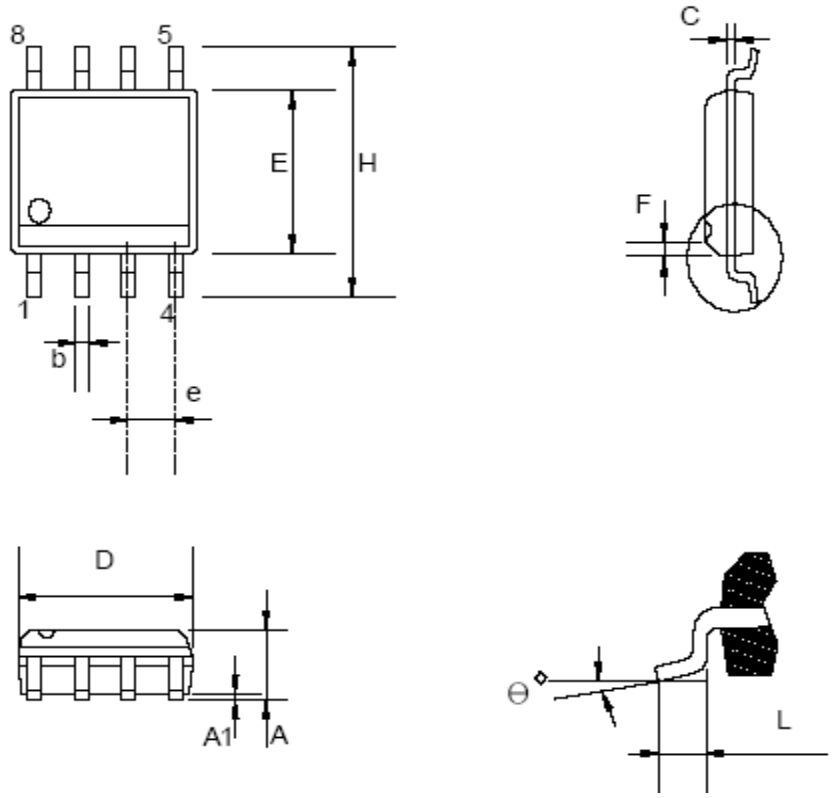
Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

SOT-23-6L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOP-8L



Dimensions DISCLAIMERS

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.752	0.053		0.069
A1	0.101		0.254	0.004		0.010
b		0.406			0.016	
c		0.203			0.008	
D	4.648		4.978	0.183		0.196
E	3.810		3.987	0.150		0.157
e	1.016	1.270	1.524	0.040	0.050	0.060
F		0.381X45°			0.015X45°	
H	5.791		6.197	0.228		0.244
L	0.406		1.270	0.016		0.050
θ°	0°		8°	0°		8°