# H7N0602LD, H7N0602LS, H7N0602LM

## Silicon N Channel MOS FET
## High Speed Power Switching

REJ03G1130-0600
Rev.6.00
Oct 16, 2006

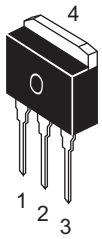


### Features

- Low on-resistance
  $R_{DS\ (on)}$ = 4.1 mΩ typ.
- 4.5 V gate drive devices
- High Speed Switching

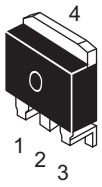
### Outline

RENESAS Package code: PRSS0004AE-A
(Package name: LDPAK (L) )




H7N0602LD

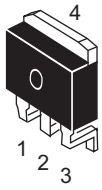
RENESAS Package code: PRSS0004AE-B
(Package name: LDPAK (S)-(1) )



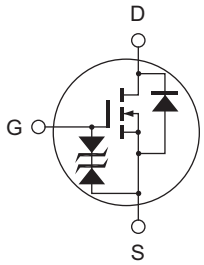

H7N0602LS

1. Gate
2. Drain
3. Source
4. Drain

RENESAS Package code: PRSS0004AE-C
(Package name: LDPAK (S)-(2) )




H7N0602LM



## Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Drain to source voltage | $V_{DSS}$ | 60 | V |
| Gate to source voltage | $V_{GSS}$ | ±20 | V |
| Drain current | $I_D$ | 85 | A |
| Drain peak current | $I_{D\ (pulse)}$ Note 1 | 340 | A |
| Body to drain diode reverse drain current | $I_{DR}$ | 85 | A |
| Avalanche current | $I_{AP}$ Note 3 | 65 | A |
| Avalanche energy | $E_{AR}$ Note 3 | 362 | mJ |
| Channel dissipation | Pch Note 2 | 100 | W |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | –55 to +150 | °C |



Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg ≥ 50 Ω

## Electrical Characteristics

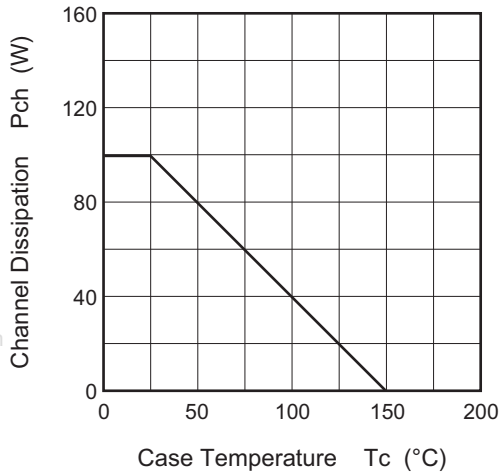
(Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Drain to source breakdown voltage | $V_{(BR)\ DSS}$ | 60 | — | — | V | $I_D$ = 10 mA, $V_{GS}$ = 0 |
| Gate to source breakdown voltage | $V_{(BR)\ GSS}$ | ±20 | — | — | V | $I_G$ = ±100 µA, $V_{DS}$ = 0 |
| Zero gate voltage drain current | $I_{DSS}$ | — | — | 10 | µA | $V_{DS}$ = 60 V, $V_{GS}$ = 0 |
| Gate to source leak current | $I_{GSS}$ | — | — | ±10 | µA | $V_{GS}$ = ±16 V, $V_{DS}$ = 0 |
| Gate to source cutoff voltage | $V_{GS\ (off)}$ | 1.5 | — | 2.5 | V | $V_{DS}$ = 10 V, $I_D$ = 1 mA Note 4 |
| Forward transfer admittance | $\|y_{fs}\|$ | 70 | 120 | — | S | $I_D$ = 45 A, $V_{DS}$ = 10 V Note 4 |
| Static drain to source on state resistance | $R_{DS\ (on)}$ | — | 4.1 | 5.2 | mΩ | $I_D$ = 45 A, $V_{GS}$ = 10 V Note 4 |
| | | — | 6.2 | 9.0 | mΩ | $I_D$ = 45 A, $V_{GS}$ = 4.5 V Note 4 |
| Input capacitance | Ciss | — | 9000 | — | pF | $V_{DS}$ = 10 V |
| Output capacitance | Coss | — | 1000 | — | pF | $V_{GS}$ = 0 |
| Reverse transfer capacitance | Crss | — | 470 | — | pF | f = 1 MHz |
| Total gate charge | Qg | — | 140 | — | nC | $V_{DD}$ = 25 V |
| Gate to source charge | Qgs | — | 30 | — | nC | $V_{GS}$ = 10 V |
| Gate to drain charge | Qgd | — | 30 | — | nC | $I_D$ = 85 A |
| Turn-on delay time | $t_{d\ (on)}$ | — | 55 | — | ns | $V_{GS}$ = 10 V |
| Rise time | $t_r$ | — | 290 | — | ns | $I_D$ = 45 A |
| Turn-off delay time | $t_{d\ (off)}$ | — | 140 | — | ns | $R_L$ = 0.67 Ω |
| Fall time | $t_f$ | — | 50 | — | ns | Rg = 4.7 Ω |
| Body to drain diode forward voltage | $V_{DF}$ | — | 0.95 | — | V | $I_F$ = 85 A, $V_{GS}$ = 0 |
| Body to drain diode reverse recovery time | $t_{rr}$ | — | 45 | — | ns | $I_F$ = 85 A, $V_{GS}$ = 0<br>$di_F/dt$ = 100 A/µs |

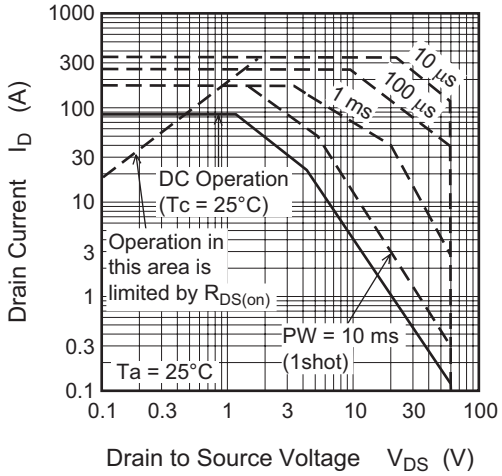
Note: 4. Pulse test

## Main Characteristics

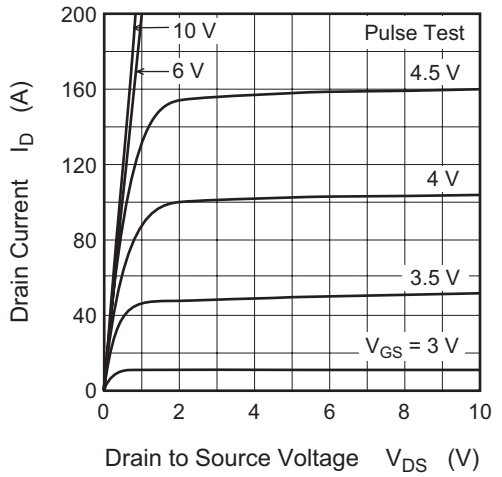
Power vs. Temperature Derating



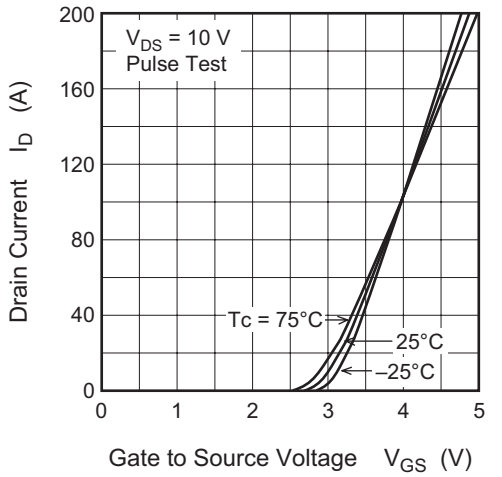

Maximum Safe Operation Area



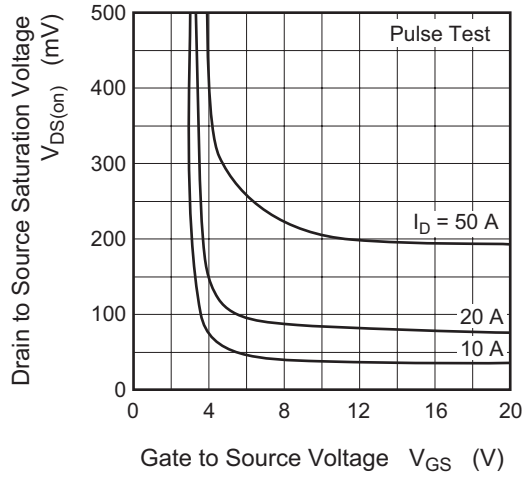

Typical Output Characteristics



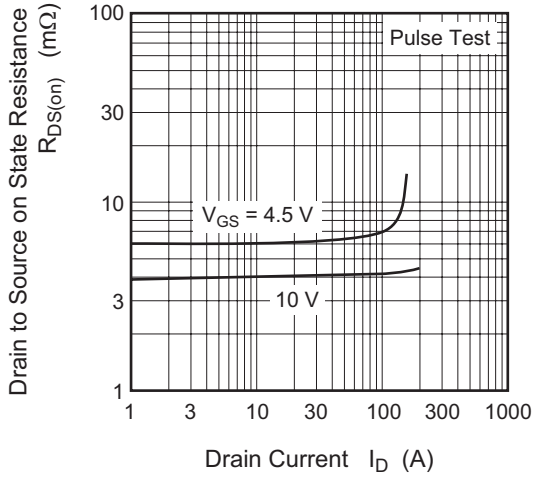

Typical Transfer Characteristics



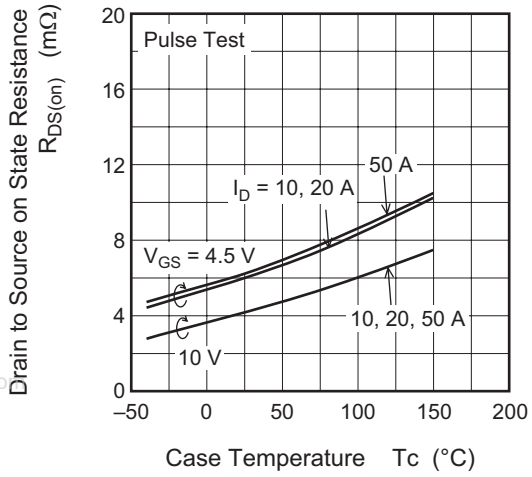

Drain to Source Saturation Voltage vs. Gate to Source Voltage



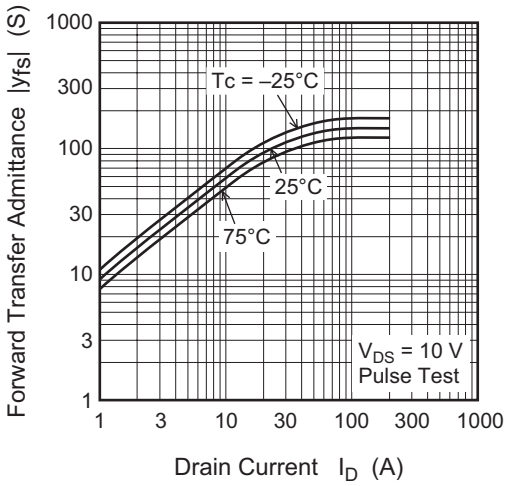

Static Drain to Source on State Resistance vs. Drain Current



Static Drain to Source on State Resistance vs. Temperature

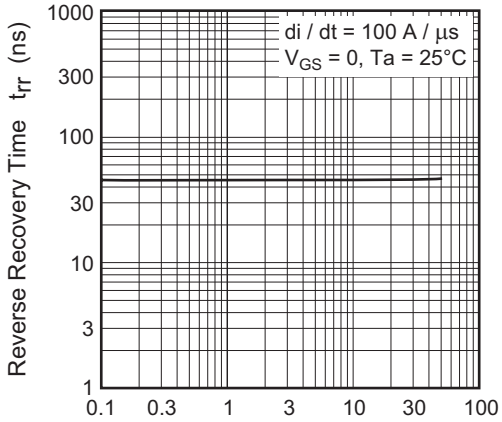



Forward Transfer Admittance vs. Drain Current

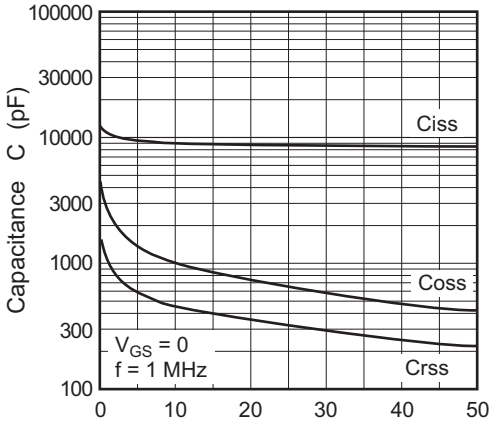




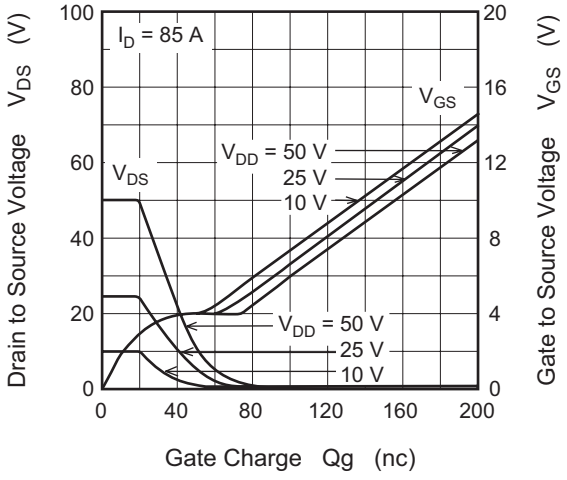

Body to Drain Diode Reverse Recovery Time



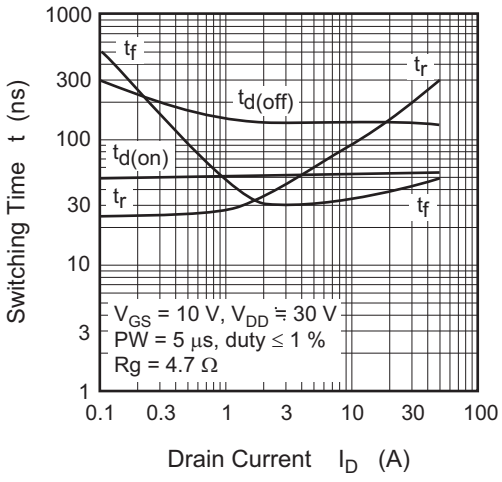

Typical Capacitance vs. Drain to Source Voltage



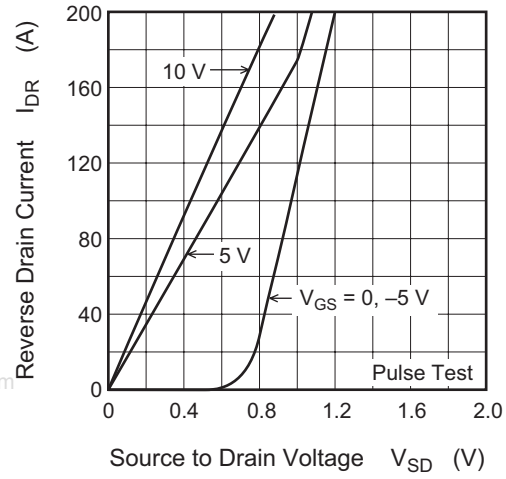

Dynamic Input Characteristics



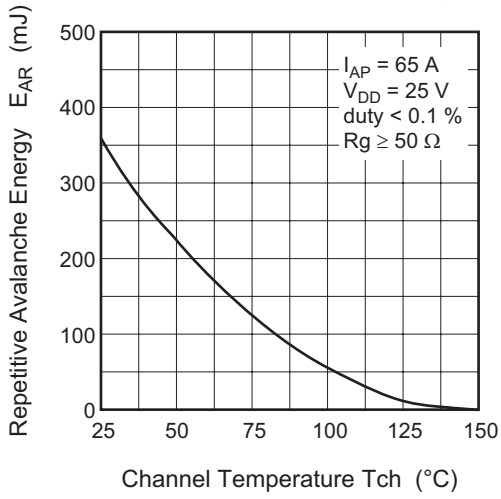

Switching Characteristics



Reverse Drain Current vs. Source to Drain Voltage

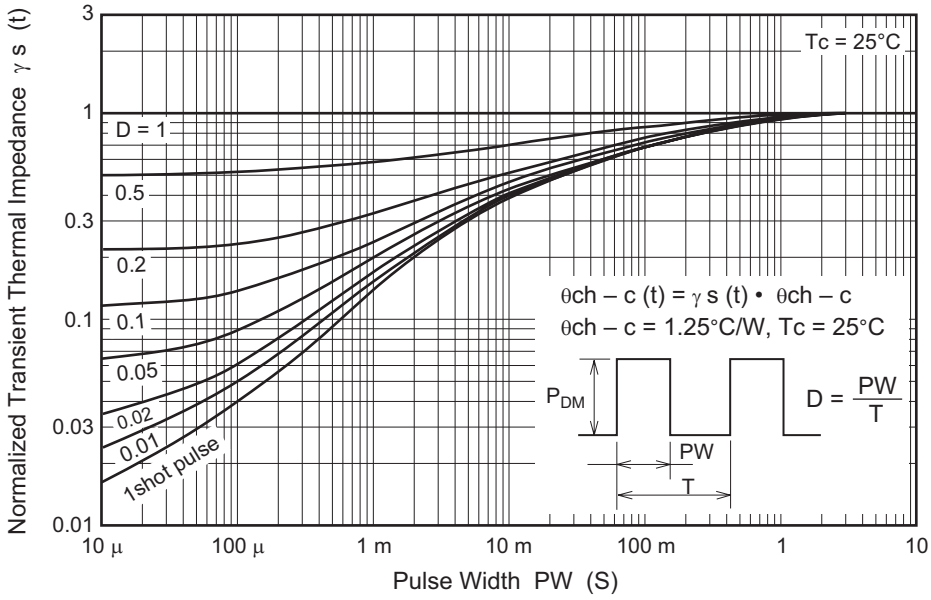



Maximum Avalanche Energy vs. Channel Temperature Derating

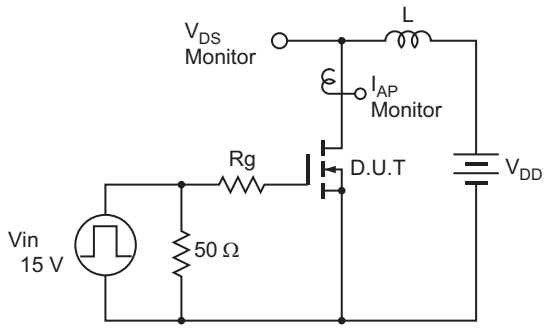





Normalized Transient Thermal Impedance vs. Pulse Width

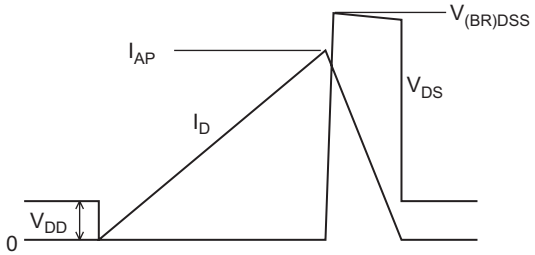



Avalanche Test Circuit

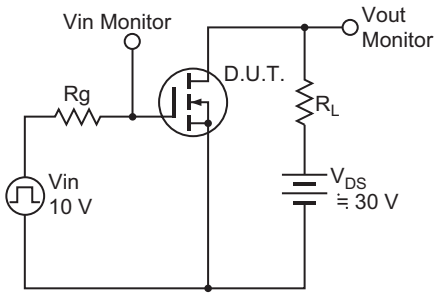



Avalanche Waveform

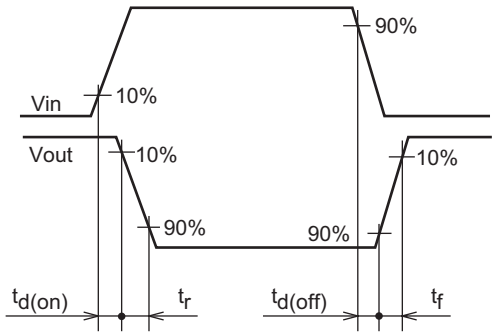
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit



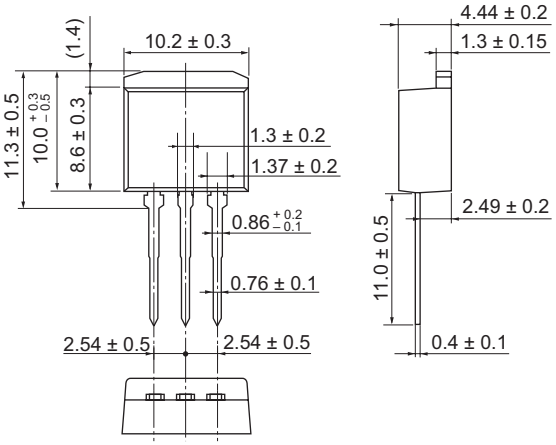

Waveform



## Package Dimensions

| Package Name | JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|---|
| LDPAK(L) | — | PRSS0004AE-A | LDPAK(L) / LDPAK(L)V | 1.40g |

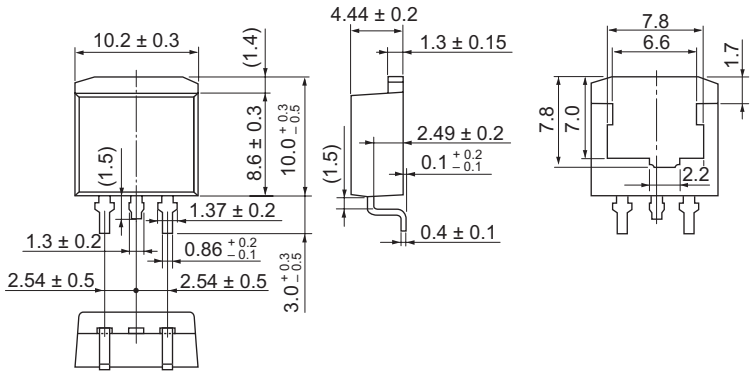
Unit: mm





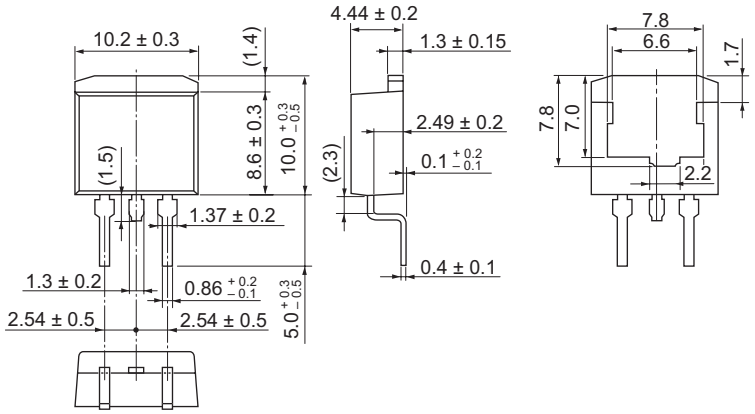

| Package Name | JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|---|
| LDPAK(S)-(1) | SC-83 | PRSS0004AE-B | LDPAK(S)-(1) / LDPAK(S)-(1)V | 1.30g |

Unit: mm



| Package Name | JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|---|
| LDPAK(S)-(2) | — | PRSS0004AE-C | LDPAK(S)-(2) / LDPAK(S)-(2)V | 1.35g |

Unit: mm






## Ordering Information

| Part Name | Quantity | Shipping Container |
|---|---|---|
| H7N0602LD-E | 500 pcs | Box (Conductive Sack) |
| H7N0602LSTL-E | 1000 pcs | Taping |
| H7N0602LMTL-E | 1000 pcs | Taping |

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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