

H7N1005DL, H7N1005DS

Silicon N Channel MOS FET
High Speed Power Switching

REJ03G1736-0100

Rev.1.00

Sep 19, 2008

Features

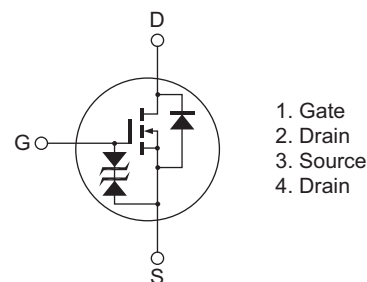
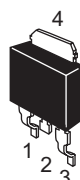
- Low on-resistance
 $R_{DS(on)} = 85 \text{ m}\Omega$ typ.
- Low drive current
- Capable of 4.5 V gate drive

Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK (L)-(2))



RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	12	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	30	A
Body to drain diode reverse drain current	I_{DR}	12	A
Avalanche current	I_{AP} ^{Note 2}	8	A
Avalanche energy	E_{AR} ^{Note 2}	6.4	mJ
Channel dissipation	P_{ch} ^{Note 3}	20	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. Value at $T_c = 25^\circ\text{C}$

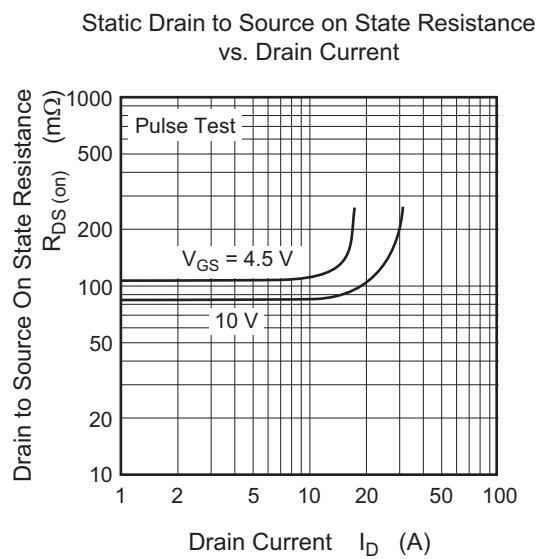
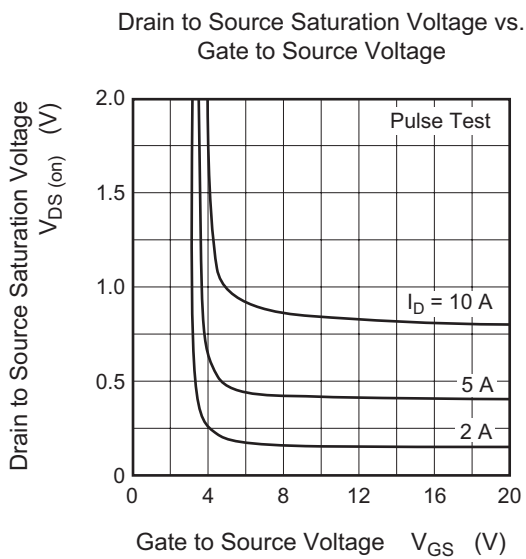
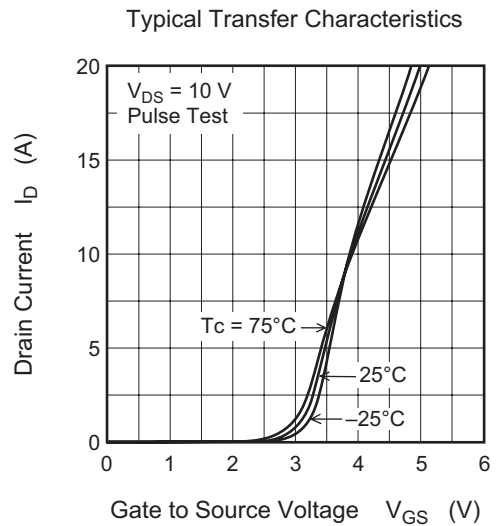
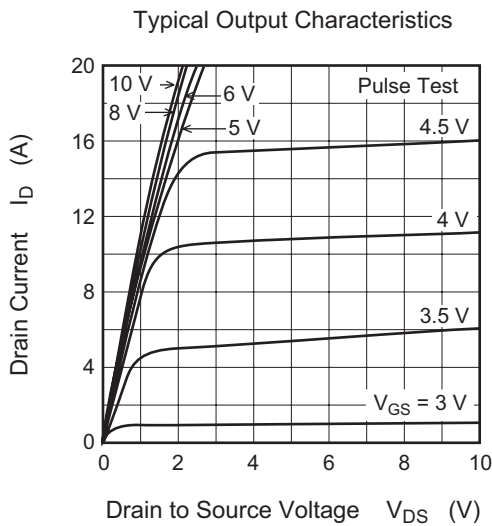
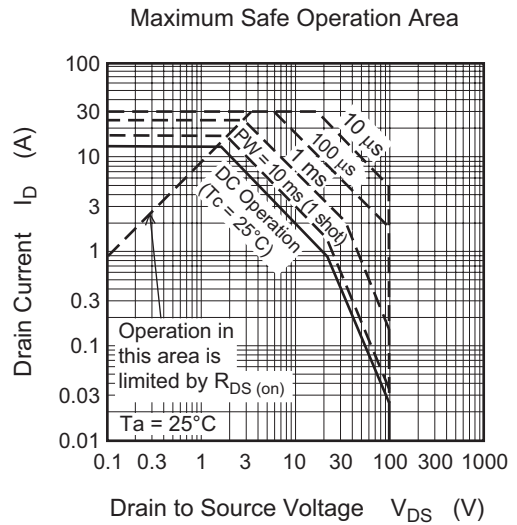
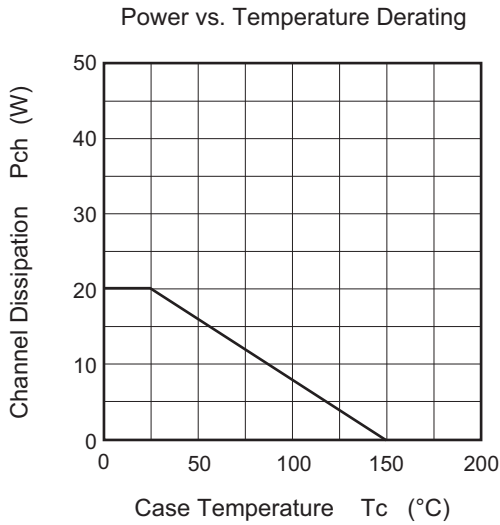
Electrical Characteristics

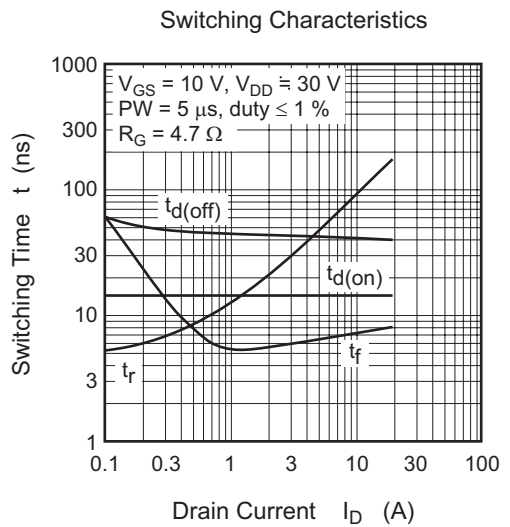
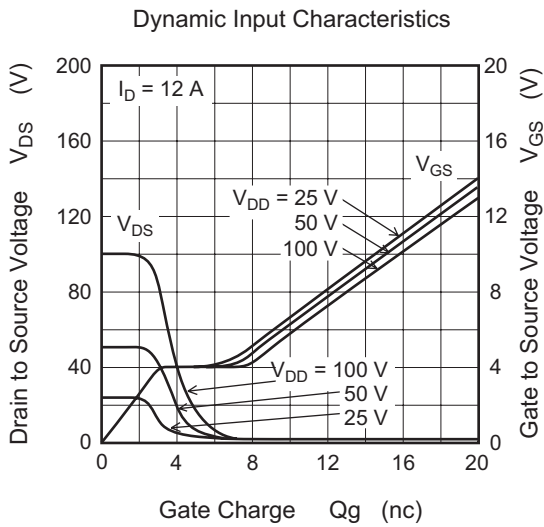
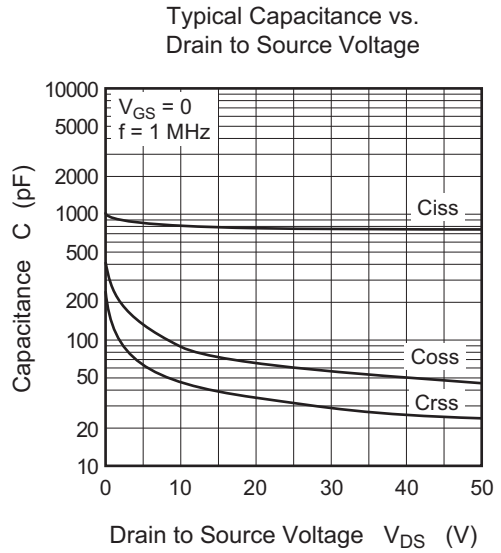
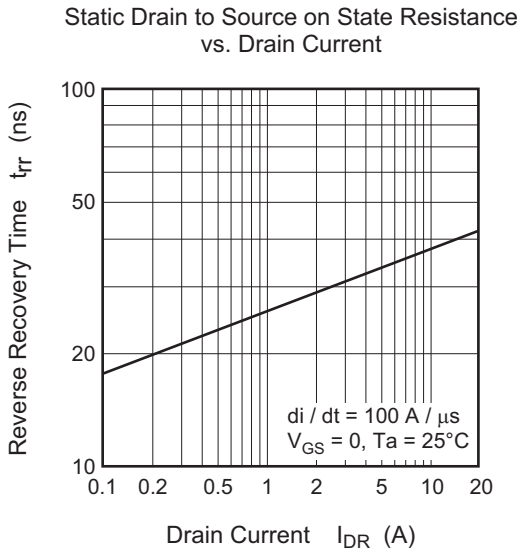
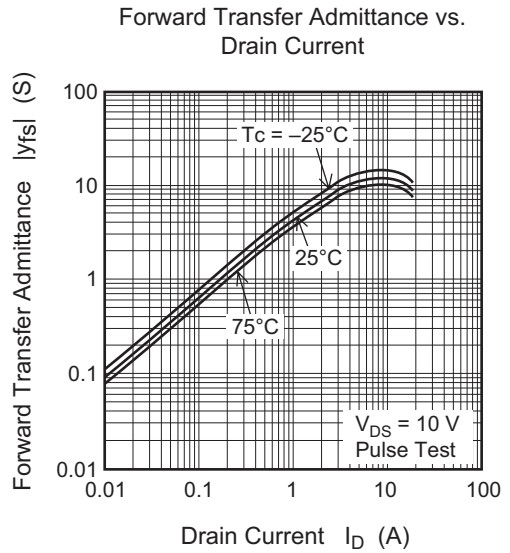
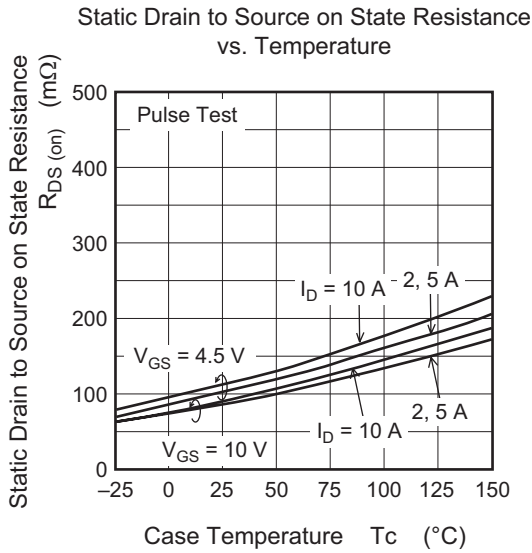
(Ta = 25°C)

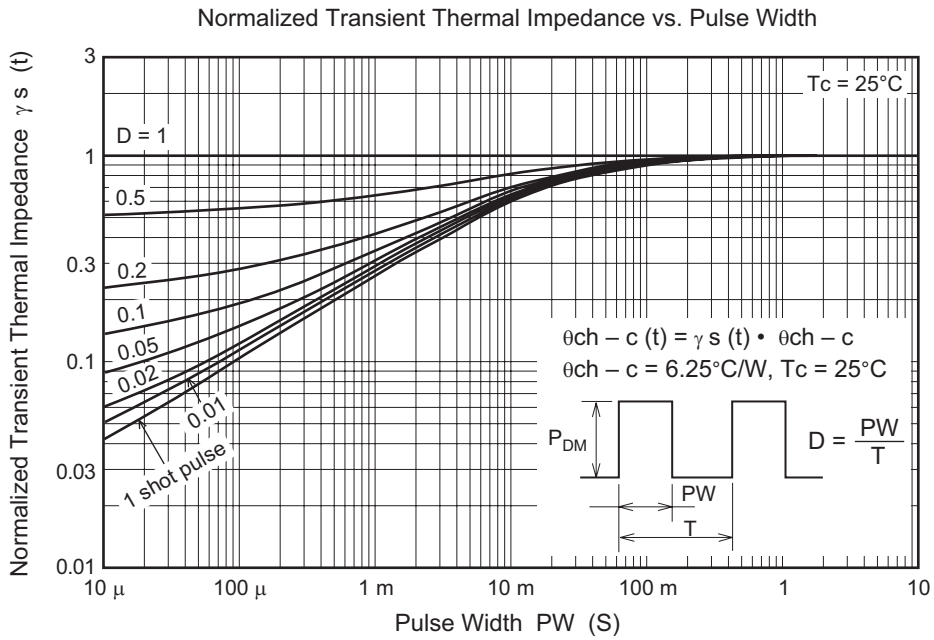
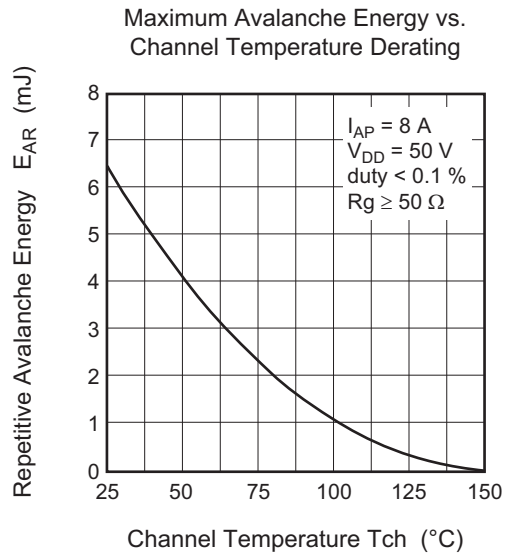
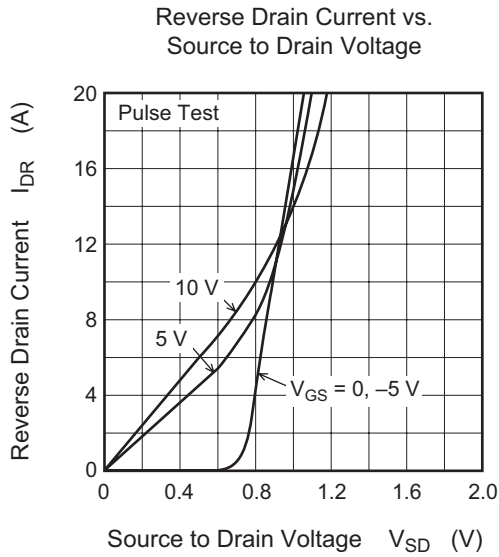
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	2.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Static drain to source on state resistance	$R_{DS(on)}$	—	85	110	$\text{m}\Omega$	$I_D = 6.0 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
		—	105	155	$\text{m}\Omega$	$I_D = 6.0 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	6.5	11	—	S	$I_D = 6.0 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	830	—	pF	$V_{DS} = 10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	90	—	pF	
Reverse transfer capacitance	C_{rss}	—	55	—	pF	
Total gate charge	Q_g	—	15	—	nC	$V_{DD} = 50 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 12 \text{ A}$
Gate to source charge	Q_{gs}	—	3.0	—	nC	
Gate to drain charge	Q_{gd}	—	4.0	—	nC	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 6.0 \text{ A}$ $R_L = 5 \text{ }\Omega$ $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	62	—	ns	
Turn-off delay time	$t_{d(off)}$	—	42	—	ns	
Fall time	t_f	—	6.5	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_F = 12 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	40	—	ns	$I_F = 12 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Note: 4. Pulse test

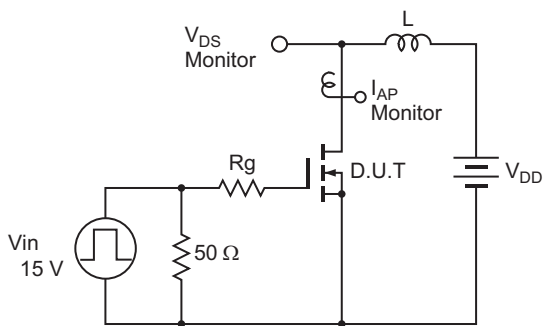
Main Characteristics



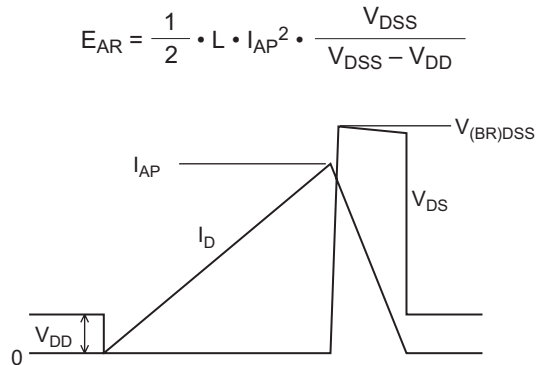


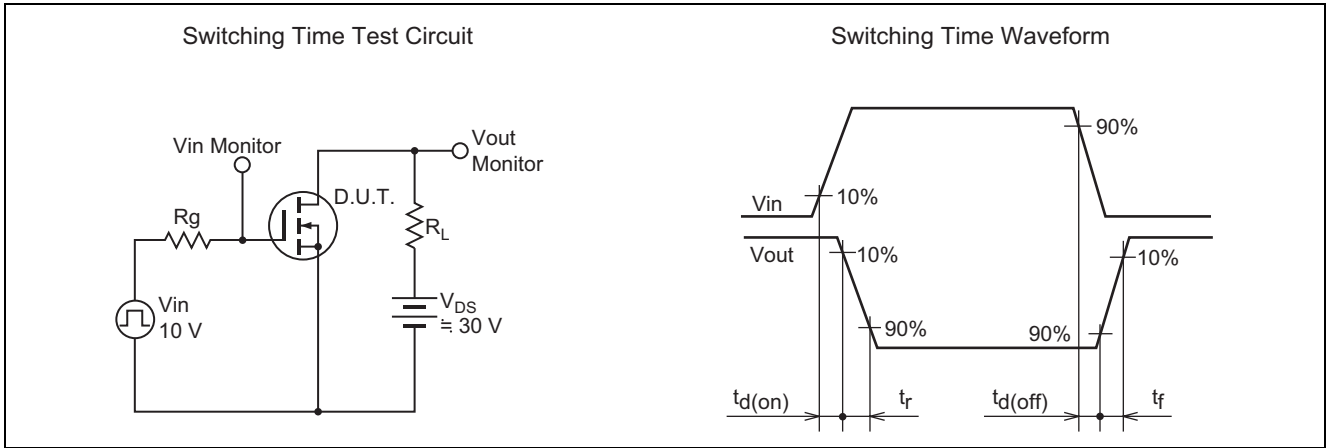


Avalanche Test Circuit

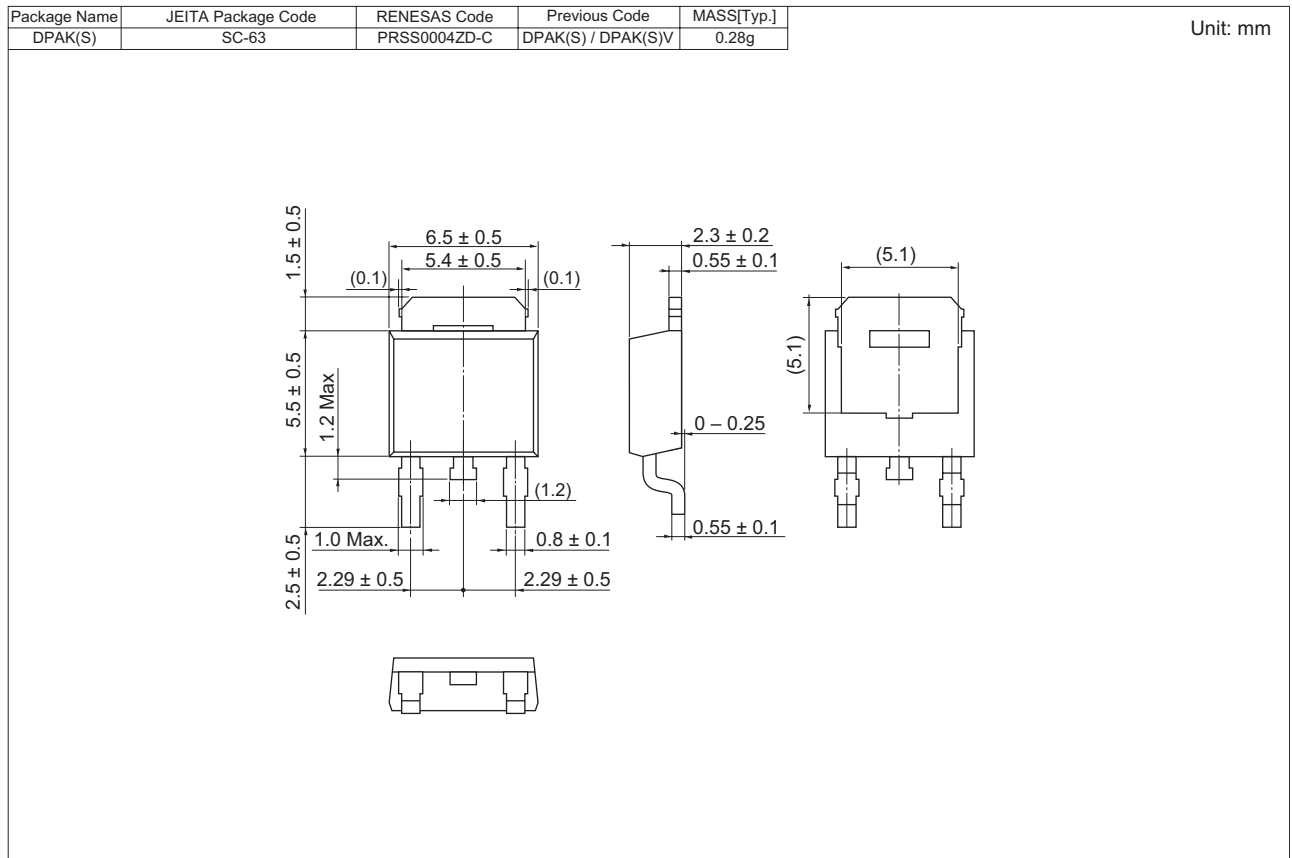
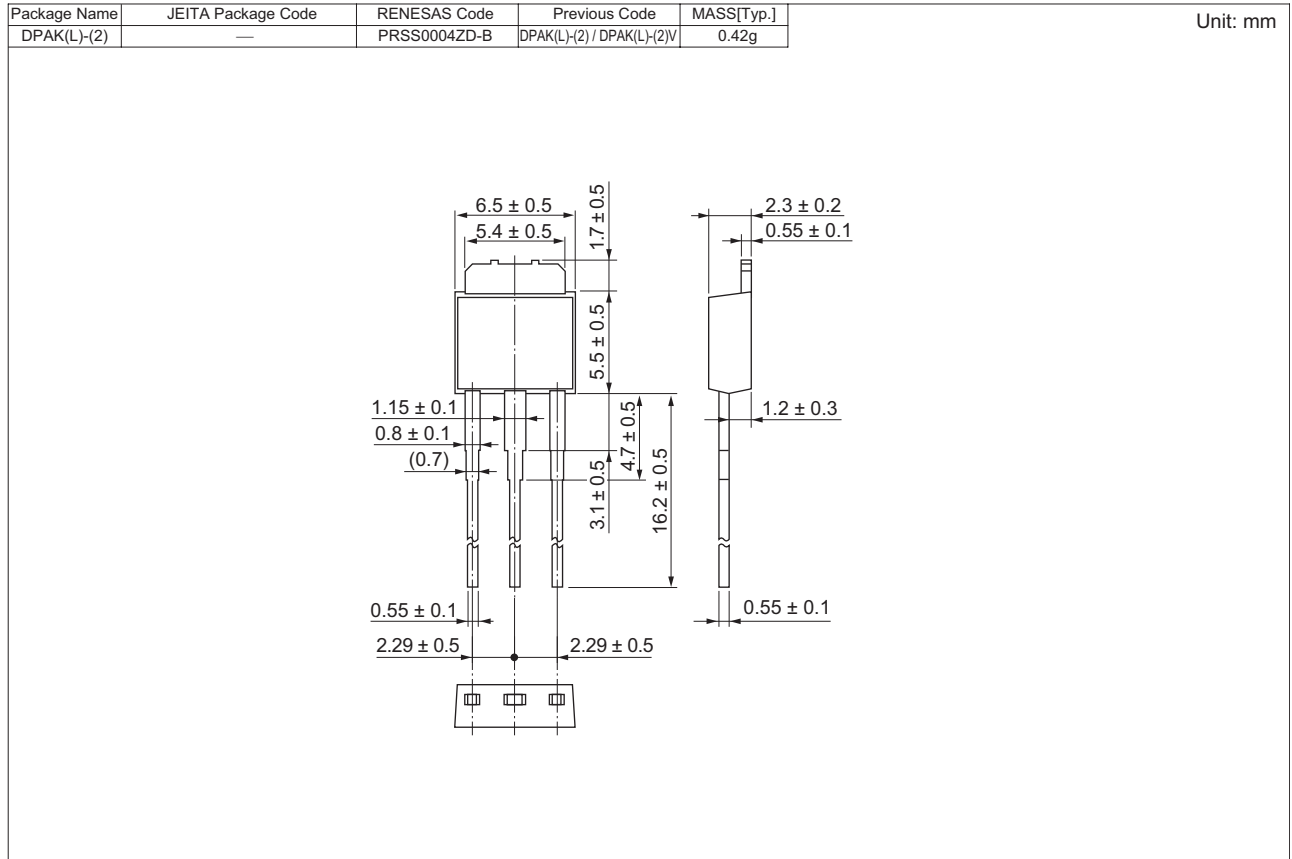


Avalanche Waveform





Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
H7N1005DL-E	3200 pcs	Box (Conductive Sack)
H7N1005DSTL-E	3000 pcs	Taping

Notes:

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