

H7P1002DL, H7P1002DS

Silicon P Channel MOS FET
High Speed Power Switching

REJ03G1601-0100

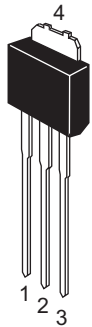
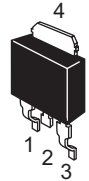
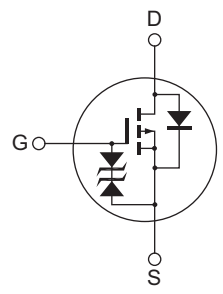
Rev.1.00

Nov 16, 2007

Features

- Low on-resistance
 $R_{DS(on)} = 85 \text{ m}\Omega$ typ.
- Low drive current
- 4.5 V gate drive device can driven from 5 V source

Outline

<p>RENESAS Package code: PRSS0004ZD-B (Package name: DPAK (L)-(2))</p>  <p>H7P0601DL</p>	<p>RENESAS Package code: PRSS0004ZD-C (Package name: DPAK (S))</p>  <p>H7P0601DS</p>	 <p>1. Gate 2. Drain 3. Source 4. Drain</p>
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Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Drain to source voltage	V_{DSS}	-100	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	-15	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-60	A
Body-drain diode reverse drain current	I_{DR}	-15	A
Avalanche current	I_{AP} ^{Note3}	-12	A
Avalanche energy	E_{AR} ^{Note3}	14.4	mJ
Channel dissipation	P_{ch} ^{Note2}	30	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ\text{C}$
 3. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

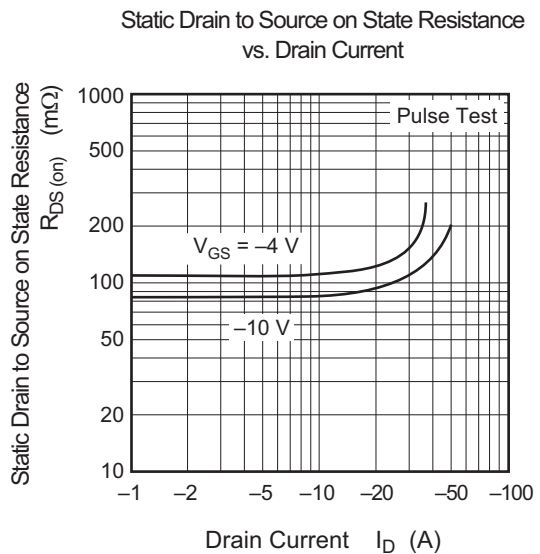
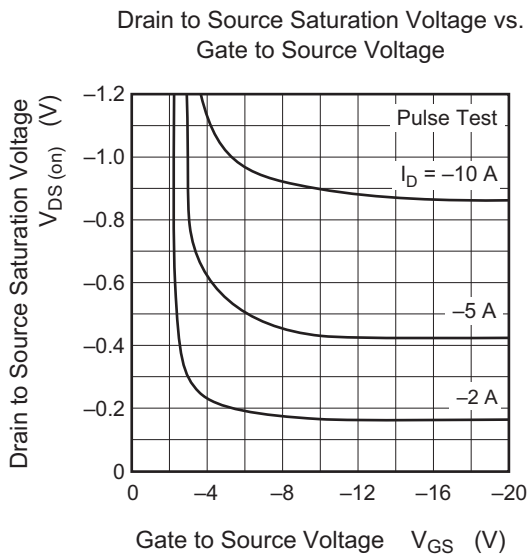
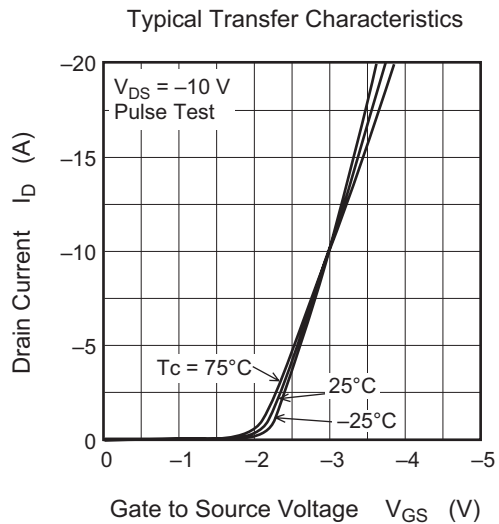
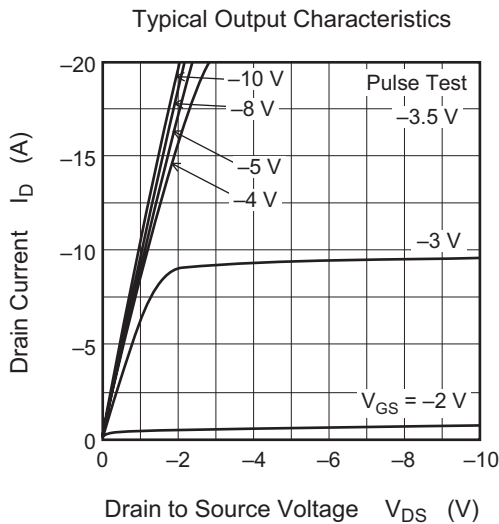
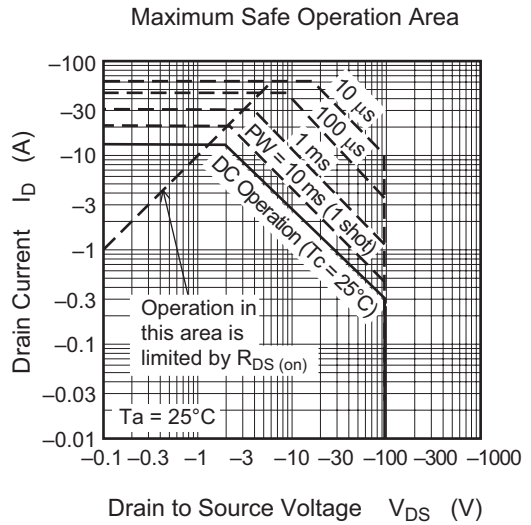
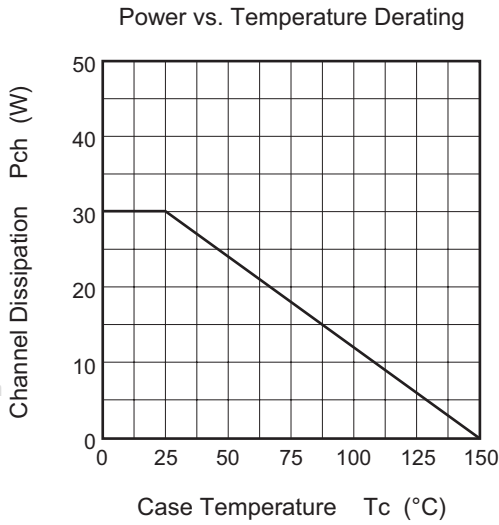
Electrical Characteristics

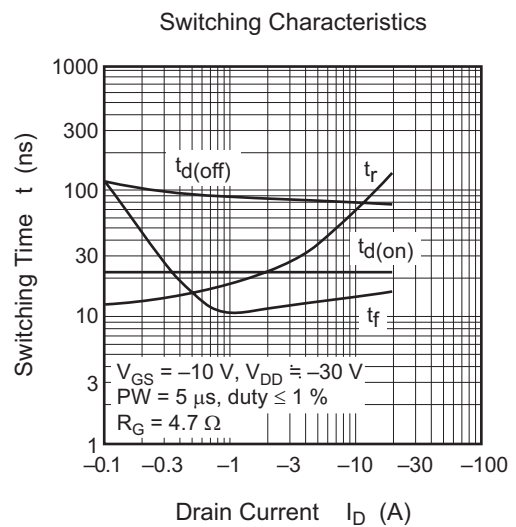
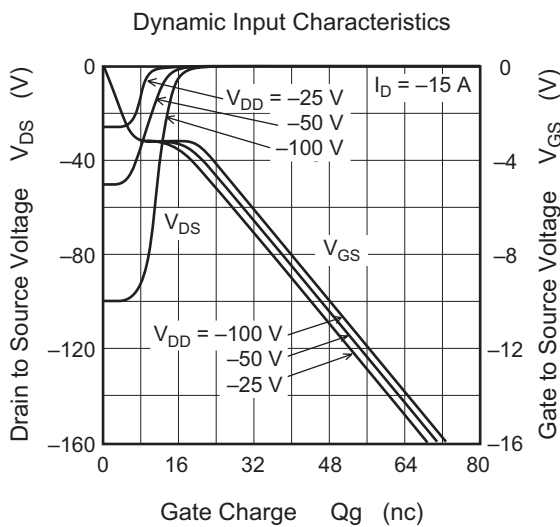
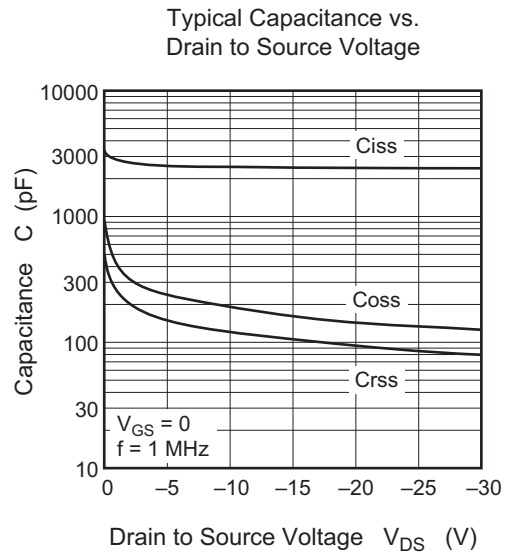
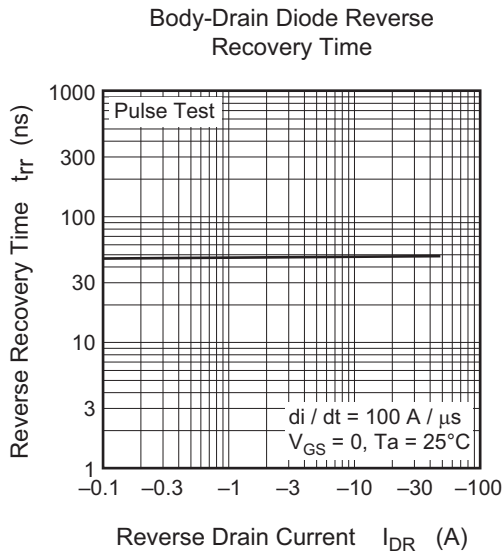
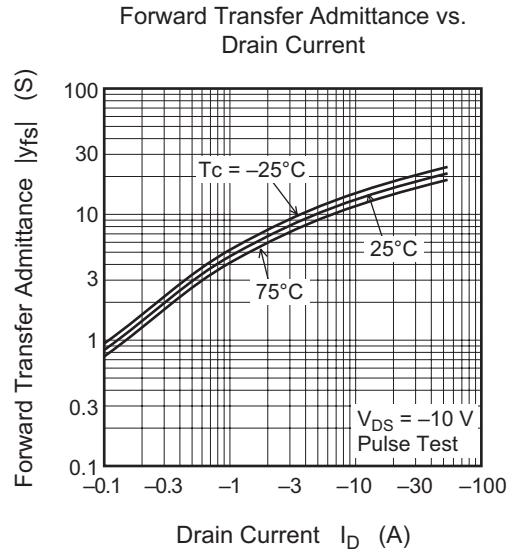
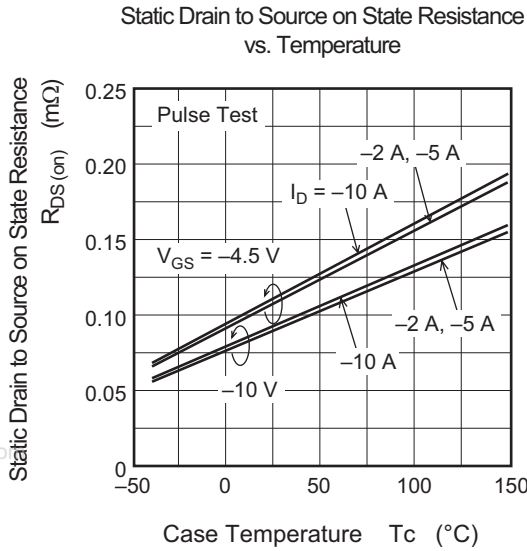
(Ta = 25°C)

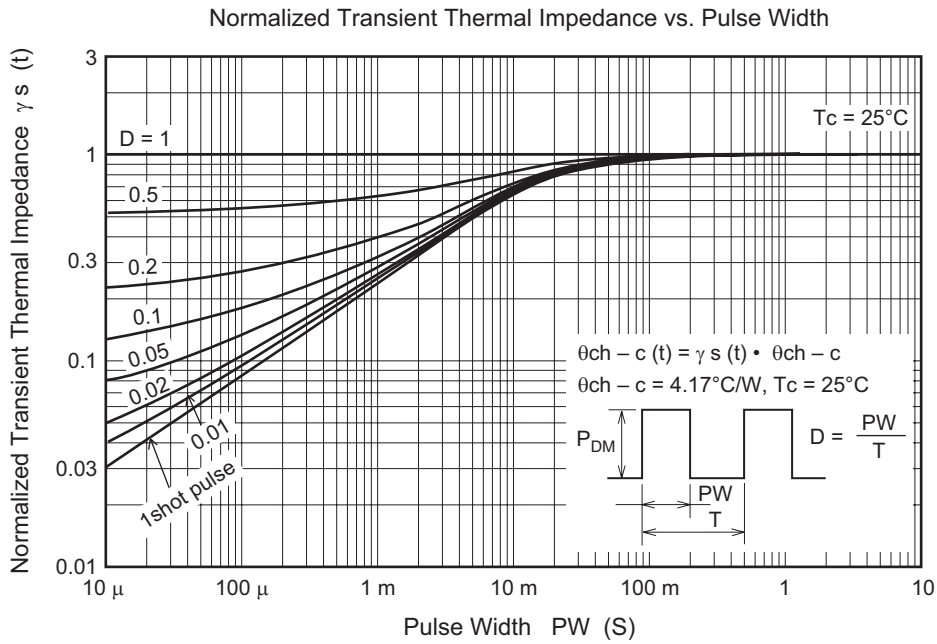
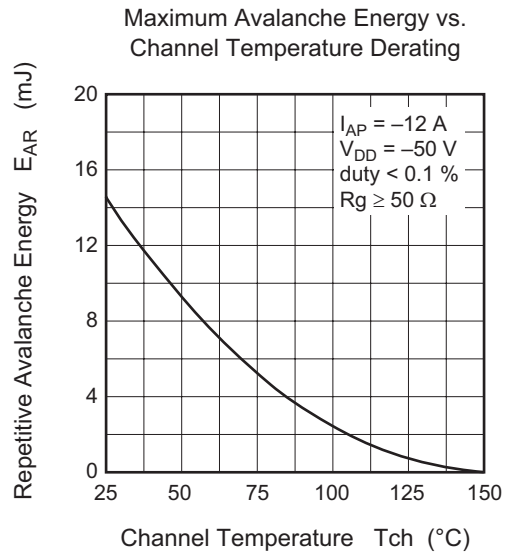
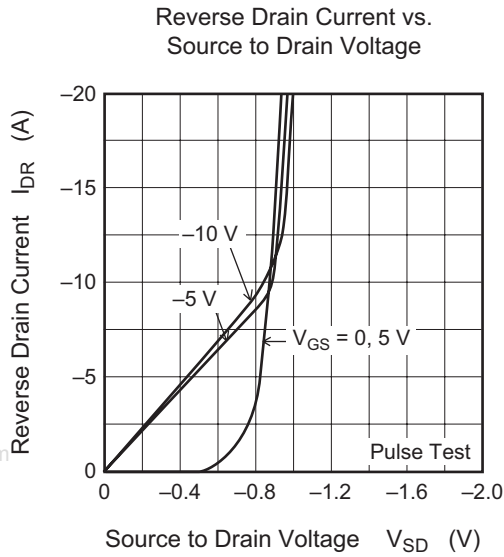
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-100	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -100 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$I_D = -1 \text{ mA}$, $V_{DS} = -10 \text{ V}$ ^{Note4}
Static drain to source on state resistance	$R_{DS(on)}$	—	85	105	m Ω	$I_D = -7.5 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note4}
		—	105	150	m Ω	$I_D = -7.5 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	7.2	12	—	S	$I_D = -7.5 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	2600	—	pF	$V_{DS} = -10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	190	—	pF	
Reverse transfer capacitance	C_{rss}	—	120	—	pF	
Total gate charge	Q_g	—	45	—	nC	$V_{DD} = -50 \text{ V}$
Gate to source charge	Q_{gs}	—	6.5	—	nC	$V_{GS} = -10 \text{ V}$
Gate to drain charge	Q_{gd}	—	9.0	—	nC	$I_D = -15 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	23	—	ns	$V_{GS} = -10 \text{ V}$, $I_D = -7.5 \text{ A}$ $R_L = 4.0 \text{ }\Omega$ $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	45	—	ns	
Turn-off delay time	$t_{d(off)}$	—	80	—	ns	
Fall time	t_f	—	13	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-0.91	—	V	$I_F = -15 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = -15 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Note: 4. Pulse test

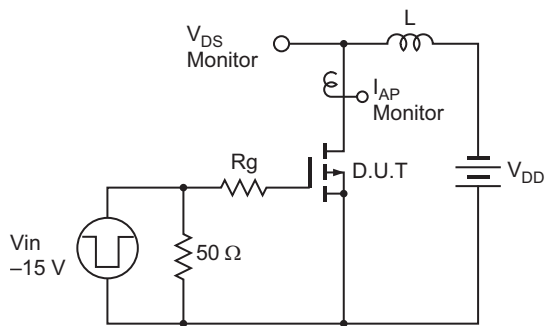
Main Characteristics



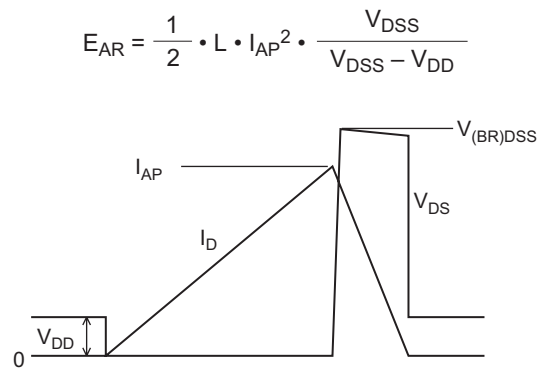


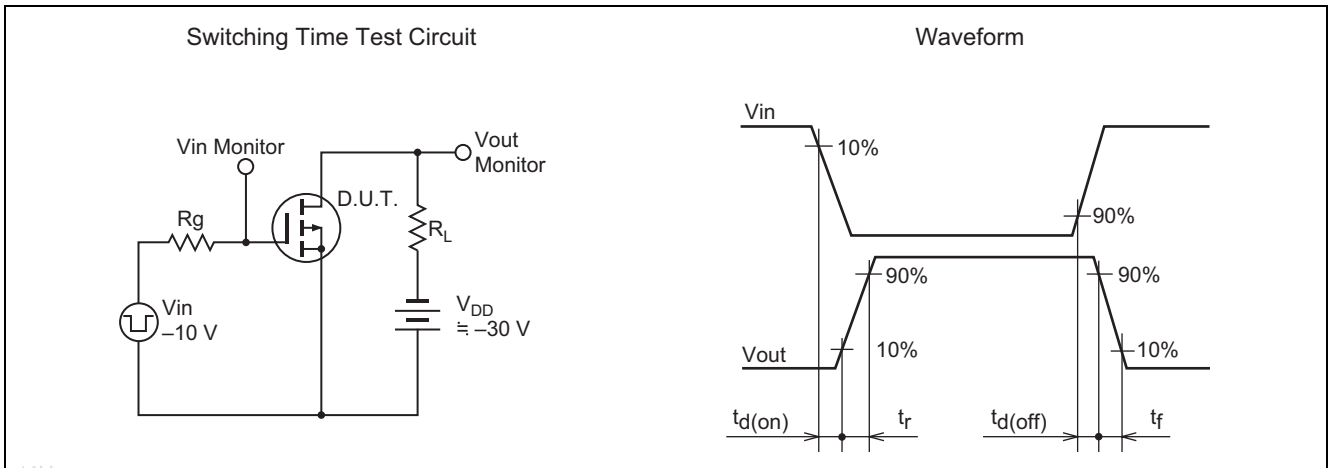


Avalanche Test Circuit



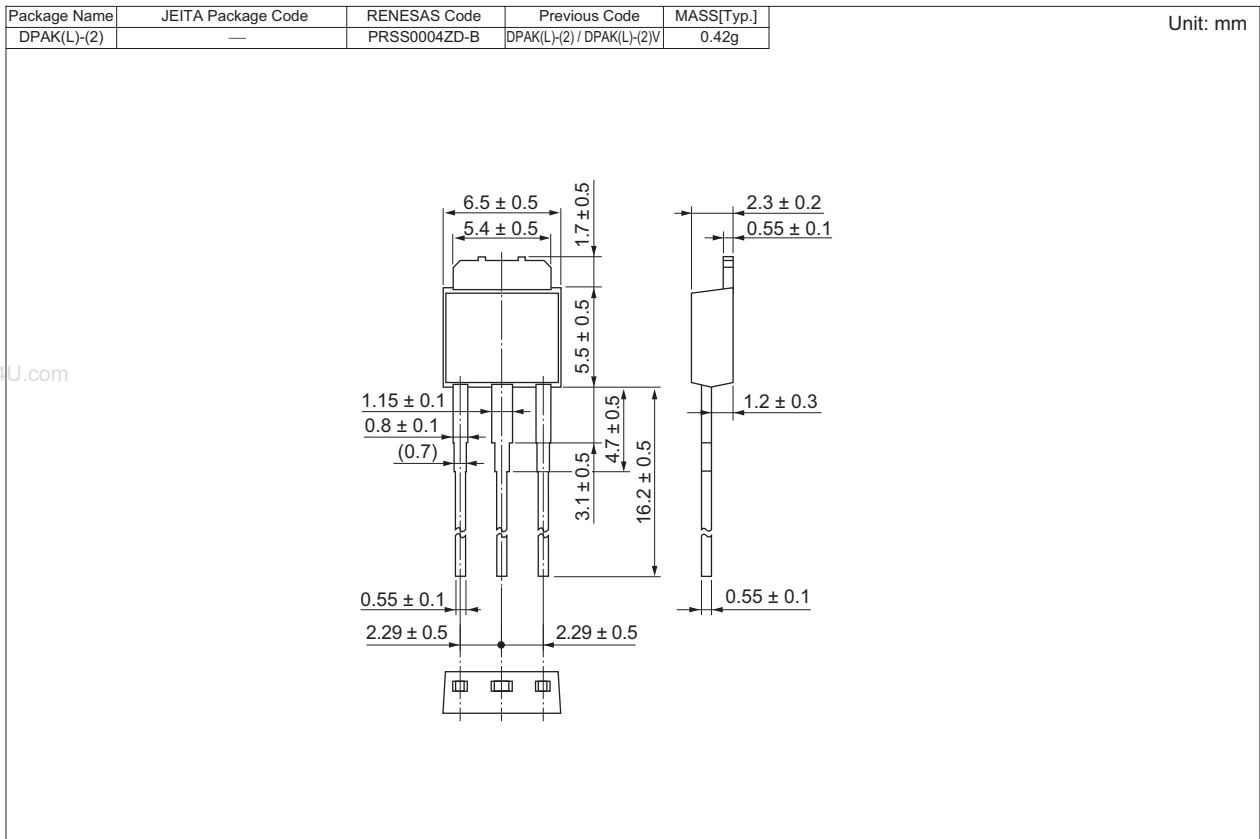
Avalanche Waveform



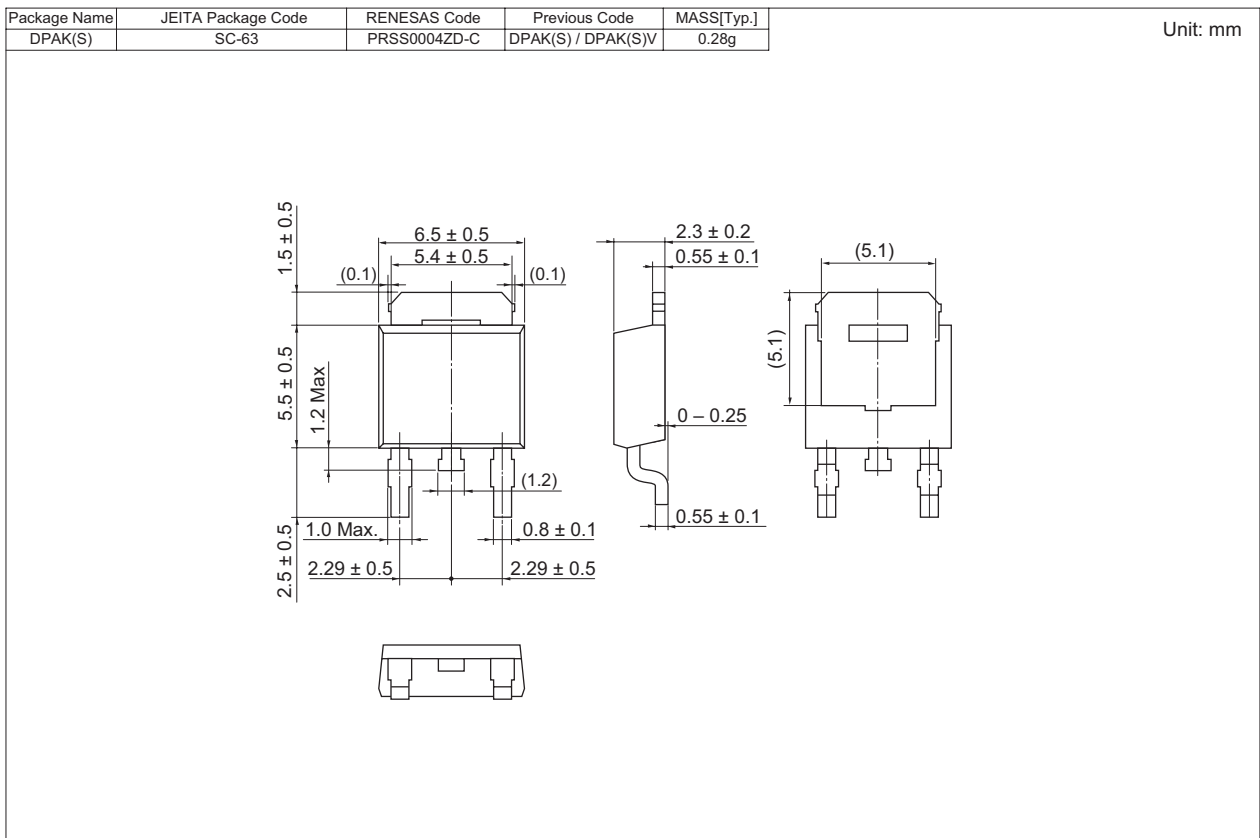


Package Dimensions

• H7P1002DL



• H7P1002DS



Ordering Information

Part No.	Quantity	Shipping Container
H7P1002DL-E	3200 pcs	Hold Box, Radial Taping
H7P1002DSTL-E	3000 pcs	Taping

Notes:

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