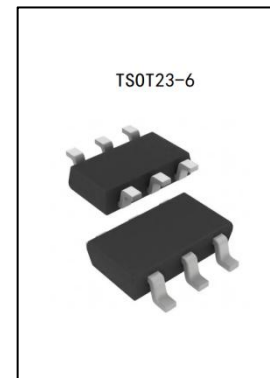


## 18V/2A 800KHz 0.8V/VFB COT BUCK

### H9118

#### General Description

The H9118 is a low EMI signature, synchronous, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution to provide a 2A continuous current over a wide input supply range, with excellent load and line regulation. H9118 achieves low EMI signature with well controlled switching edges. Fault condition protection includes programmable-output over-voltage protection, Constant on time Mode, and thermal shutdown. H9118 requires a minimal number of readily available standard external components. It is available in TSOT23-6 package.



#### Features

- Wide 4.0V to 18V Operating Input Range
- 2.0A Continuous Output Current
- 800KHz Switching Frequency
- Short Protection with Hiccup-Mode
- Built-in Over Current Limit
- Programmable Output Over-Voltage Protection
- DCM Mode for High Efficiency in Light Load
- Integrated internal Soft-Start
- 80mΩ Low RDS(ON) Internal MOSFETs
- Output Adjustable from 0.8V
- 93% Duty cycle Max
- Integrated internal compensation
- Thermal Shutdown
- Available in TSOT23-6 Package
- Constant on time Mode

#### Applications

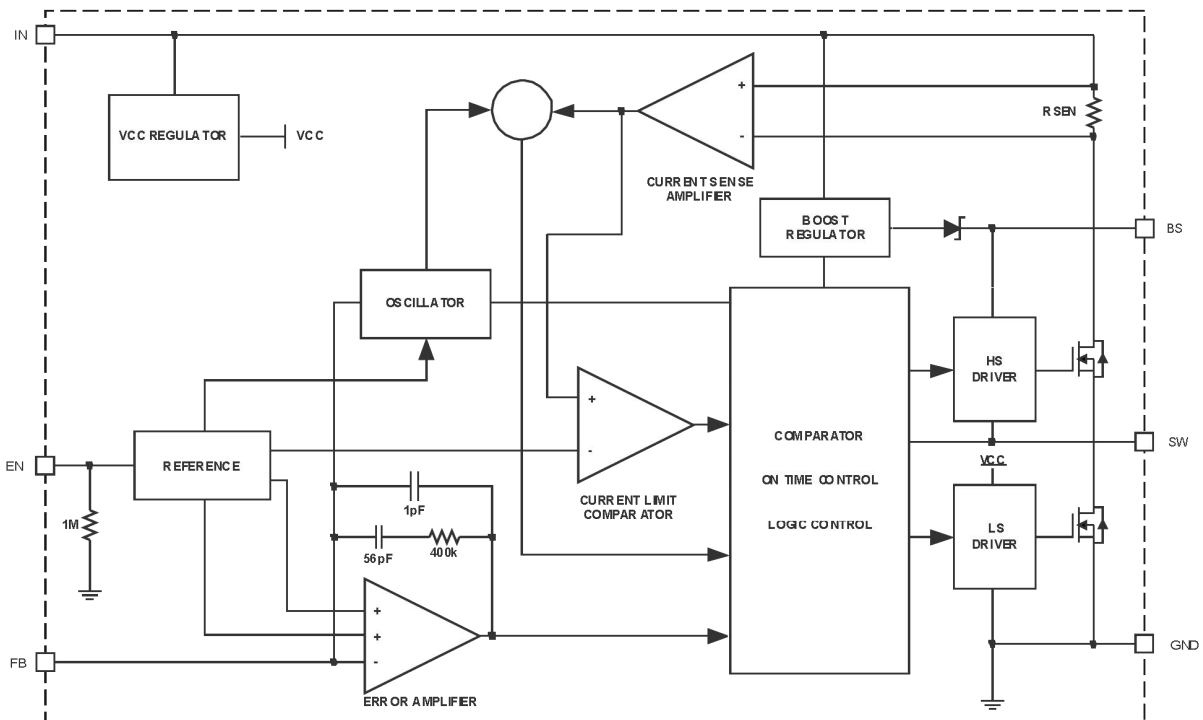
- Automotive Entertainment
- Wireless and DSL Modems
- Computer Entertainment
- Power Supply for Car Chargers

## Order specification

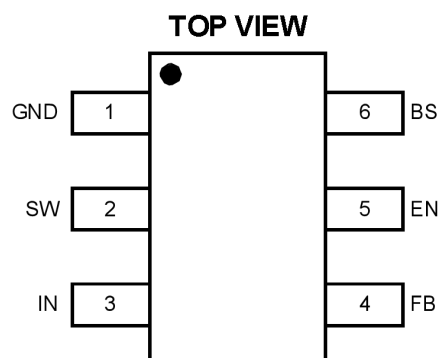
Part No	Description	Package	Devices per reel
H9118	H9118 Buck, 4.0-18V, 2A, 800KHz, VFB 0.8V, DCM, TSOT23-6	TSOT23-6	3000

Note (1): All SIPROIN parts are Pb-Free and adhere to the RoHS directive.

## Block Diagram and Pin Arrangement Diagram



## Pin Assignment



Top Marking: 1821: 21YXX (21: device code, Y=year code, XX = lot number code)

Pin No.	Pin Name	Description
1	GND	Ground Pin
2	SW	Switching Pin
3	VIN	Power Supply Pin
4	FB	Adjustable Version Feedback input. Connect FB to the center point of the external resistor divider
5	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode. Connect 100K resistor to VIN, it can be turned on automatically.
6	BS	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.

### Absolute Maximum Ratings<sup>(1) (2)</sup>

Parameter	Min.	Max.	Unit
V <sub>IN</sub> voltage	-0.3	21	V
EN voltage	-0.3	6.5	V
SW voltage	-0.3	V <sub>IN</sub> +0.5V	V
FB voltage	-0.3	V <sub>IN</sub> +0.5V	V
Power dissipation <sup>(3)</sup>	Internally Limited		
Operating junction temperature, T <sub>J</sub>	-40	150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, T<sub>J(MAX)</sub>, the junction-to-ambient thermal resistance, R<sub>θJA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is calculated using: P<sub>D (MAX)</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>)/R<sub>θJA</sub>. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T<sub>J</sub>=160°C (typical) and disengages at T<sub>J</sub>= 130°C (typical).

## ESD Ratings

Item	Description	Value	Unit
$V_{(ESD-HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD-CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
$I_{LATCH-UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

## Recommended Operating Conditions

Parameter	Min.	Max.	Unit
Operating junction temperature <sup>(1)</sup>	-40	125	°C
Operating temperature range	-40	85	°C
Input voltage $V_{IN}$	4.0	18	V
Output current	0	2.2	A

Note (1): All limits specified at room temperature ( $T_A = 25^\circ\text{C}$ ) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

## Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>	87.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	0.9	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	14.2	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board.

## Electrical Characteristics<sup>(1) (2)</sup>

$V_{IN}=24V$ ,  $T_A=25^{\circ}C$ , unless specified otherwise.

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range		4.0		18	V
Supply Current (Quiescent)	$V_{EN} = 3.0V$ $V_{in}=12V$		230	350	$\mu A$
Supply Current (Shutdown)	$V_{EN} = 0$ or $EN = GND$			5	$\mu A$
Feedback Voltage		790	805	825	mV
High-Side Switch On-Resistance	$I_{SW}=100mA$		120	140	$m\Omega$
Low-Side Switch On-Resistance			80	100	$m\Omega$
Upper Switch Current Limit		2.3			A
Switching Frequency		600	800	1000	KHz
Maximum Duty Cycle	$V_{FB}=90\%$			93	%
Minimum On-Time			35		nS
EN Rising Threshold		1.2			V
EN Falling Threshold				0.4	V
Under-Voltage Lockout Threshold	Wake up $V_{IN}$ Voltage		3.9	4.0	V
	Shutdown $V_{IN}$ Voltage	3.7		3.9	V
	Hysteresis $V_{IN}$ voltage		200		mV
Soft Start	$C_{FF} = 27pF$	1	1.5	2	mS
Thermal Shutdown			160		$^{\circ}C$
Thermal Hysteresis			30		$^{\circ}C$

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

## Functions Description

### Internal Regulator

The H9118 is a constant on time mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 800KHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

### Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference ( $V_{FB}$ ) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external

component counts and simplifies the control loop design.

### **Under-Voltage Lockout (UVLO)**

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

### **Thermal Shutdown**

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 130°C) the chip is enabled again.

### **SS (Power Start)**

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.8V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally fixed to 1.5ms.

### **Over Current Protection and Hiccup**

The H9118 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold. Once a UV is triggered, the H9118 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The H9118 exits the hiccup mode once the over current condition is removed.

### **Startup and Shutdown**

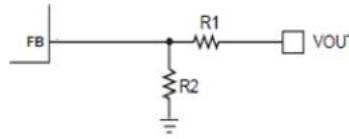
If both  $V_{IN}$  and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low,  $V_{IN}$  low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

## **Applications Information**

### **Setting the Output Voltage**

H9118 external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 10k $\Omega$ -150k $\Omega$  for optimal transient response. R2 is then given by:

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$



V <sub>OUT</sub>	R1	R2	L1	C1	C <sub>IN</sub> (μF)	C <sub>OUT</sub> (μF)	C <sub>FF</sub> Opt.
1.1V	4.2KΩ	11KΩ	1.0-3.3μH	22-100nF	47+0.1	100+0.1	<a href="#">C<sub>FF</sub> Chapter</a>
1.5V	13KΩ	15KΩ	1.0-3.3μH	22-100nF	47+0.1	100+0.1	<a href="#">C<sub>FF</sub> Chapter</a>
3.3V	47KΩ	15KΩ	2.2-6.8μH	22-100nF	47+0.1	100+0.1	<a href="#">C<sub>FF</sub> Chapter</a>
5.0V	68KΩ	13KΩ	2.2-6.8 μH	22-100nF	47+0.1	100+0.1	<a href="#">C<sub>FF</sub> Chapter</a>

All the external components are the suggested values, the final values are based on the application testing results.

### Selecting the Inductor

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the maximum inductor peak current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer. The inductor value can be calculated with:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where  $\Delta I_L$  is the inductor ripple current. Choose inductor ripple current to be approximately 30% to 40% of the maximum load current. The maximum inductor peak current can be estimated as:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency. Larger inductances lead to smaller ripple currents and voltages, but they also have larger physical dimensions, lower saturation currents and higher linear impedance. Therefore, the choice of inductance should be compromised according to the specific application.

### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For a better performance, use ceramic capacitors placed as close to VIN as possible and a 0.1μF input capacitor to filter out high frequency interference is recommended. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

From the above equation, it can be concluded that the input ripple current reaches its maximum

at  $V_{IN}=2V_{OUT}$  where  $I_{CIN} = \frac{I_{OUT}}{2}$ . For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification. The input voltage ripple can be estimate with Equation:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{OSC} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Similarly, when  $V_{IN}=2V_{OUT}$ , input voltage ripple reaches its maximum of

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{OSC} \times C_{IN}}$$

### Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. The output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{OSC} \times C_{OUT}}\right)$$

There are some differences between different types of capacitors. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{OSC}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A larger output capacitor can achieve a better load transient response, but the maximum output capacitor limitation should also be considered in the design application. If the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft-start time and will fail to regulate. The maximum output capacitor value ( $C_{OUT\_MAX}$ ) can be limited approximately with Equation:

$$C_{OUT\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{SS} / V_{OUT}$$

Where  $L_{LIM\_AVG}$  is the average start-up current during the soft-start period, and  $T_{SS}$  is the soft-start time.

On the other hand, special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.



The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , will only vary the capacitance to within  $\pm 15\%$ . The capacitor type X5R has a similar tolerance over a reduced temperature range of  $-55^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Many large value ceramic capacitors, larger than  $1\mu\text{F}$  are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from  $25^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Therefore, X5R or X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below  $25^{\circ}\text{C}$ .

### Feed-Forward Capacitor ( $C_{FF}$ )

H9118 has internal loop compensation, so adding  $C_{FF}$  is optional. Specifically, for specific applications, if necessary, consider whether to add feed-forward capacitors according to the situation.

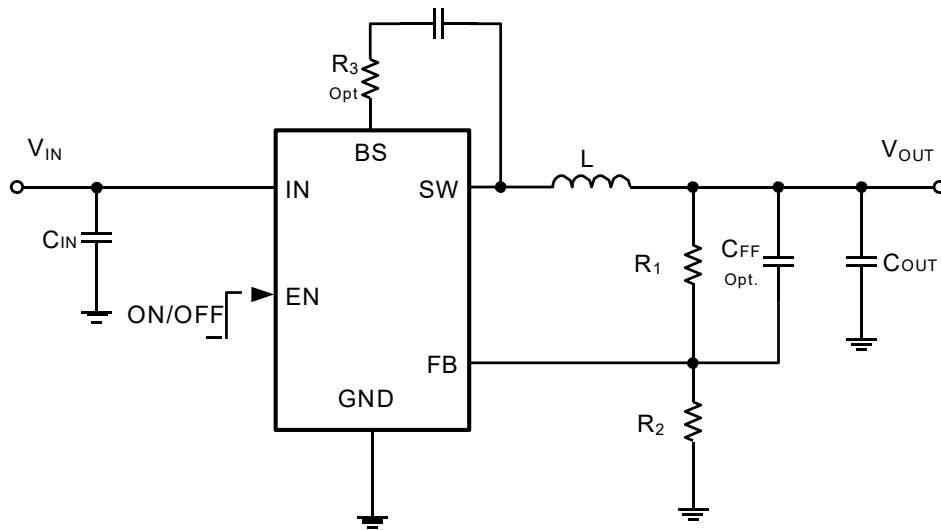
The use of a feed-forward capacitor ( $C_{FF}$ ) in the feedback network is to improve the transient response or higher phase margin. For optimizing the feed-forward capacitor, knowing the cross frequency is the first thing. The cross frequency (or the converter bandwidth) can be determined by using a network analyzer. When getting the cross frequency with no feed-forward capacitor identified, the value of feed-forward capacitor ( $C_{FF}$ ) can be calculated with the following Equation:

$$C_{FF} = \frac{1}{2\pi \times F_{CROSS}} \times \sqrt{\frac{1}{R1} \times \left(\frac{1}{R1} + \frac{1}{R2}\right)}$$

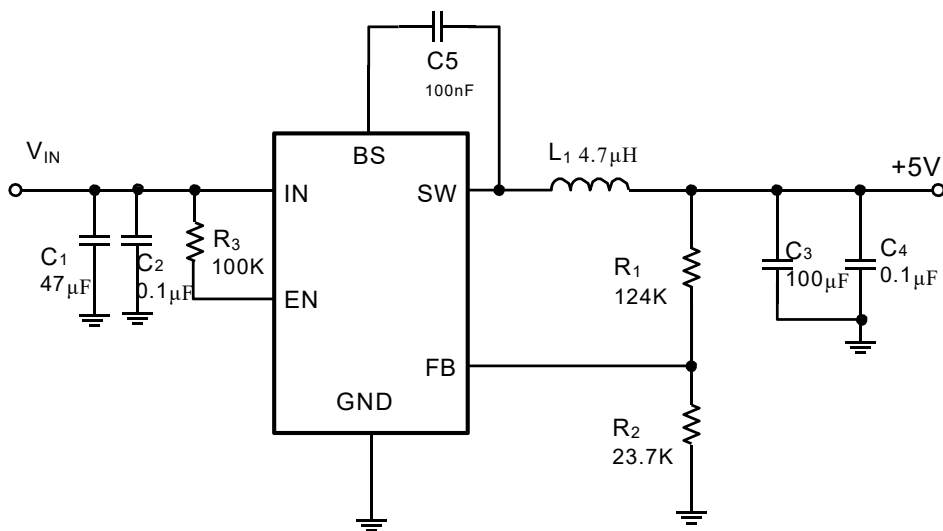
Where  $F_{CROSS}$  is the cross frequency.

To reduce transient ripple, the feed-forward capacitor value can be increased to push the cross frequency to higher region. Although this can improve transient response, it also decreases phase margin and cause more ringing. In the other hand, if more phase margin is desired, the feed-forward capacitor value can be decreased to push the cross frequency to lower region.

## Application Circuits



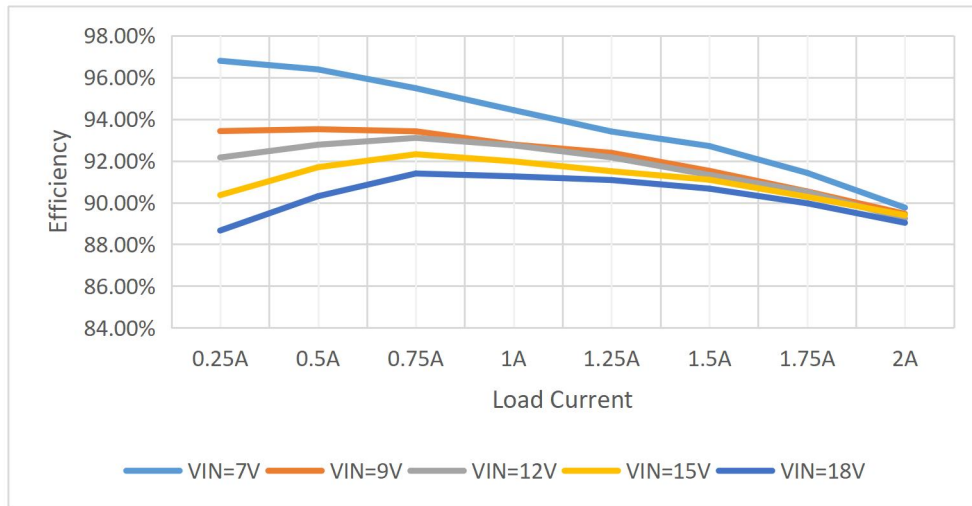
Basic Application Circuit



5V output typical application circuit

## Typical Performance Characteristics

Test Conditions:  $V_{out}=5V$ ,  $L=4.7\mu H$ ,  $C_{IN}=47\mu F$ ,  $C_{OUT}=100\mu F+0.1\mu F$ ,  $T_a=25^\circ C$ , unless otherwise indicated.



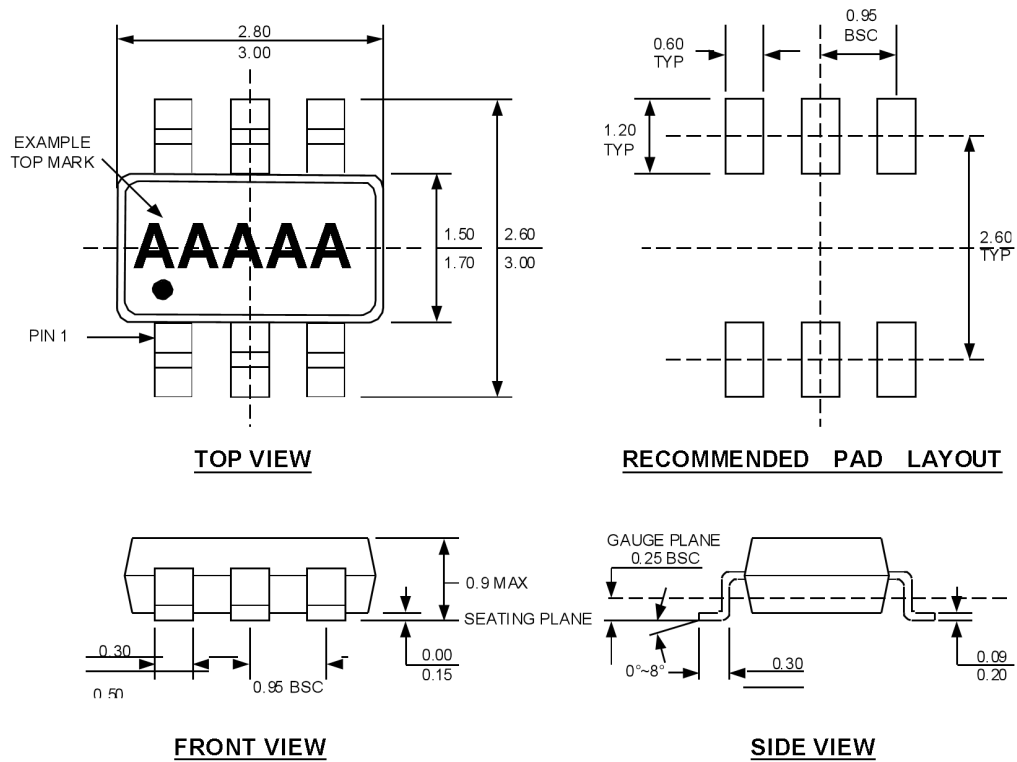
Efficiency vs. Load Current Vout=5V

### PCB Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

1. Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2. Bypass ceramic capacitors are suggested to be put close to the  $V_{IN}$  Pin.
3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4.  $V_{OUT}$ , SW away from sensitive analog areas such as FB.
5. Connect  $V_{IN}$ , SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

## Package Information (TSOT23-6)



**NOTE:**

1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

## Special Instructions

The company reserves the right of final interpretation of this specification.

## Version Change Description

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Version: V1.0	Author: Yang	Time: 2022.8.9
Modify the record:		
1. Re-typesetting the manual and checking some data		

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Version: V1.1	Author: Yang	Time: 2022.11.15
Modify the record:		
1. Updating the general description		

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## Statement

The information in the usage specification is correct at the time of publication, Shanghai Siproin Microelectronics Co. has the right to change and interpret the specification, and reserves the right to modify the product without prior notice. Users can obtain the latest version information from our official website or other effective channels before confirmation, and verify whether the relevant information is complete and up to date.

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