CI-MCP Specification

4GB eNAND Flash(x8)
+ 4Gb Mobile DDR (x32)

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Document Title

CI-MCP

4GB(x8) eNAND Flash / 4Gb (x32) Mobile DDR

Revision History

Revision No.	History	Draft Date	Remark
0.1	- Initial Draft	Nov. 2012	Preliminary
0.2	- Updated DC and AC CHARACTERISTICS	Nov. 2012	Preliminary

FEATURES

[CI-MCP]

● Operation Temperature
- (-25)^{o}C ~ 85^{o}C

● Package
- 153-ball FBGA - 11.5x13.0mm^{2}, 1.0t, 0.5mm pitch
- Lead & Halogen Free

[e-NAND]

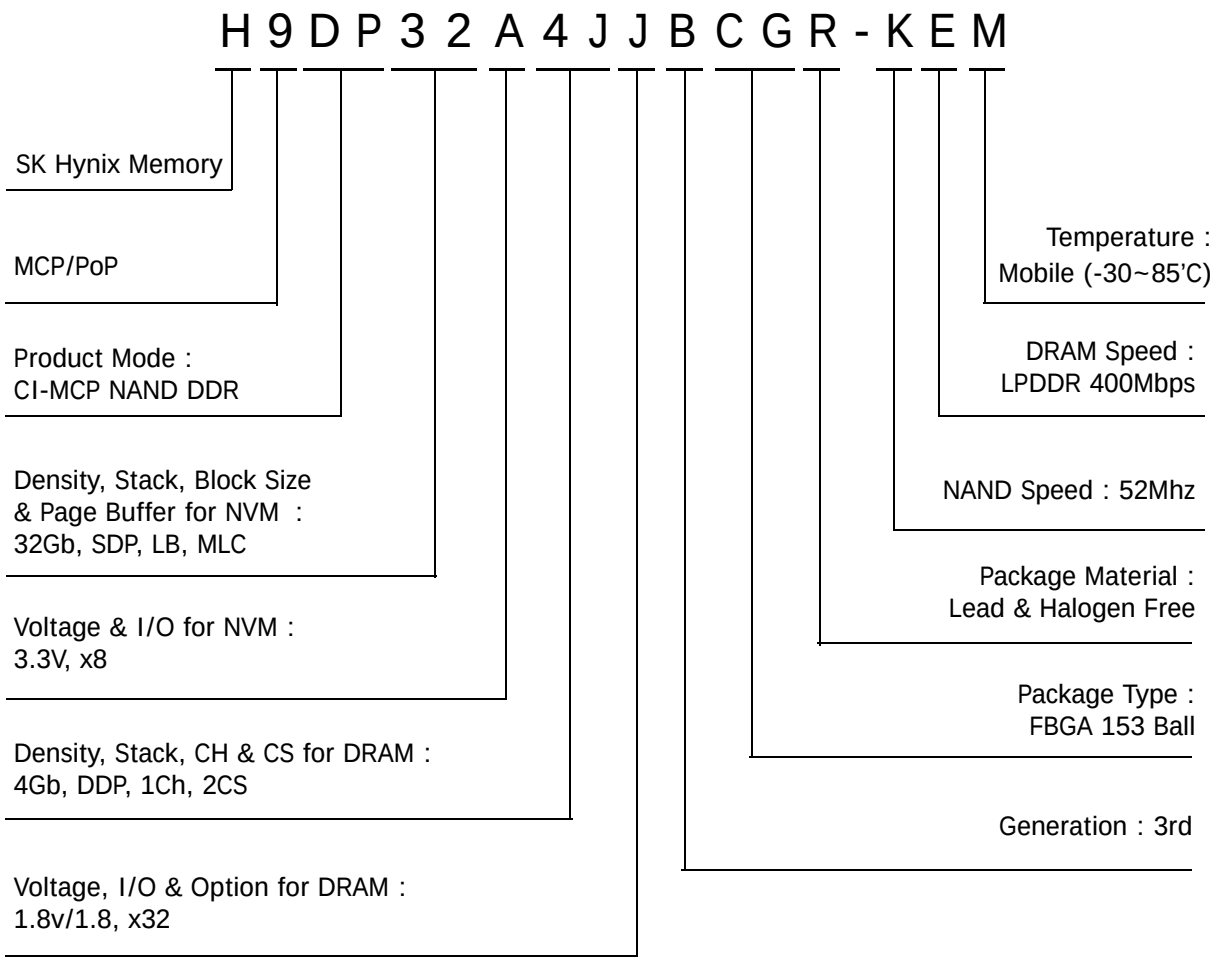
● Packaged NAND flash memory with MultiMediaCard interface
● e-NAND system specification, compliant with V4.41
● Full backward compatibility with previous e-NAND system specification
● Bus mode
  - High-speed eMMC protocol.
  - Three different data bus widths: 1 bit, 4 bits,8 bits.
  - Data transfer rate: up to 104Mbyte/s
  - DDR mode supported
● Operating voltage range:
  - V_{CCQ} = 3.3/1.8V
  - V_{CC} = 3.3V
● Error free memory access
  - Internal error correction code
  - Internal enhanced data management algorithm (Wear levelling, Bad block management, Garbage collection)
  - Possibility for the host to make sudden power failure safe-update operations for data content
● Security
  - Password protection of data
  - Secure Erase
  - Secure Trim
  - Secure bad block management
  - Write Protection
● Boot
  - Nomal / Alternative boot sequence method
● Power saving
  - Enhanced power saving method by introducing sleep functionality
● Partition management with enhanced storage.
● Hardware reset supported

[DDR SDRAM]

● Double Data Rate architecture
  - two data transfer per clock cycle
● x32 bus width
● Supply Voltage
  - VDD / VDDQ = 1.7 - 1.95 V
● Memory Cell Array
  - 16Mb x 4Bank x 32 I/O
● Bidirectional data strobe (DQS)
● Input data mask signal (DQM)
● Input Clock
  - Differential Clock Inputs (CK, /CK)
● MRS, EMRS
  - JEDEC Standard guaranteed
● CAS Latency
  - Programmable CAS latency 2 or 3 supported
● Burst Length
  - Programmable burst length 2 / 4 / 8 with both sequential and interleave mode

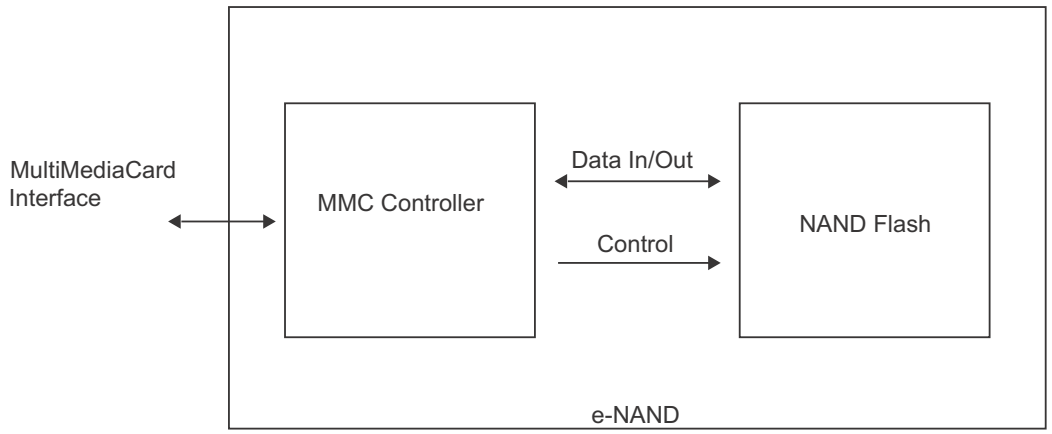
ORDERING INFORMATION

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
H9DP32A4JJBCGR-KEM	e-NAND mobile DDR	3.3V 1.8V	4GB (x8) 4Gb (x32)	52MHz DDR 400	153Ball FBGA (Lead & Halogen Free)

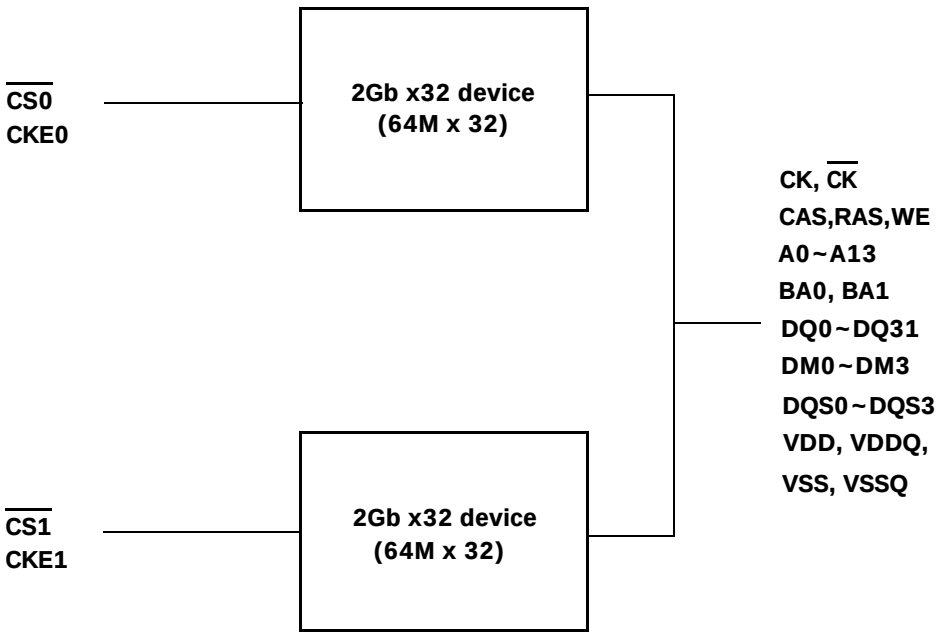


Functional Block Diagram

e-NAND Block Diagram

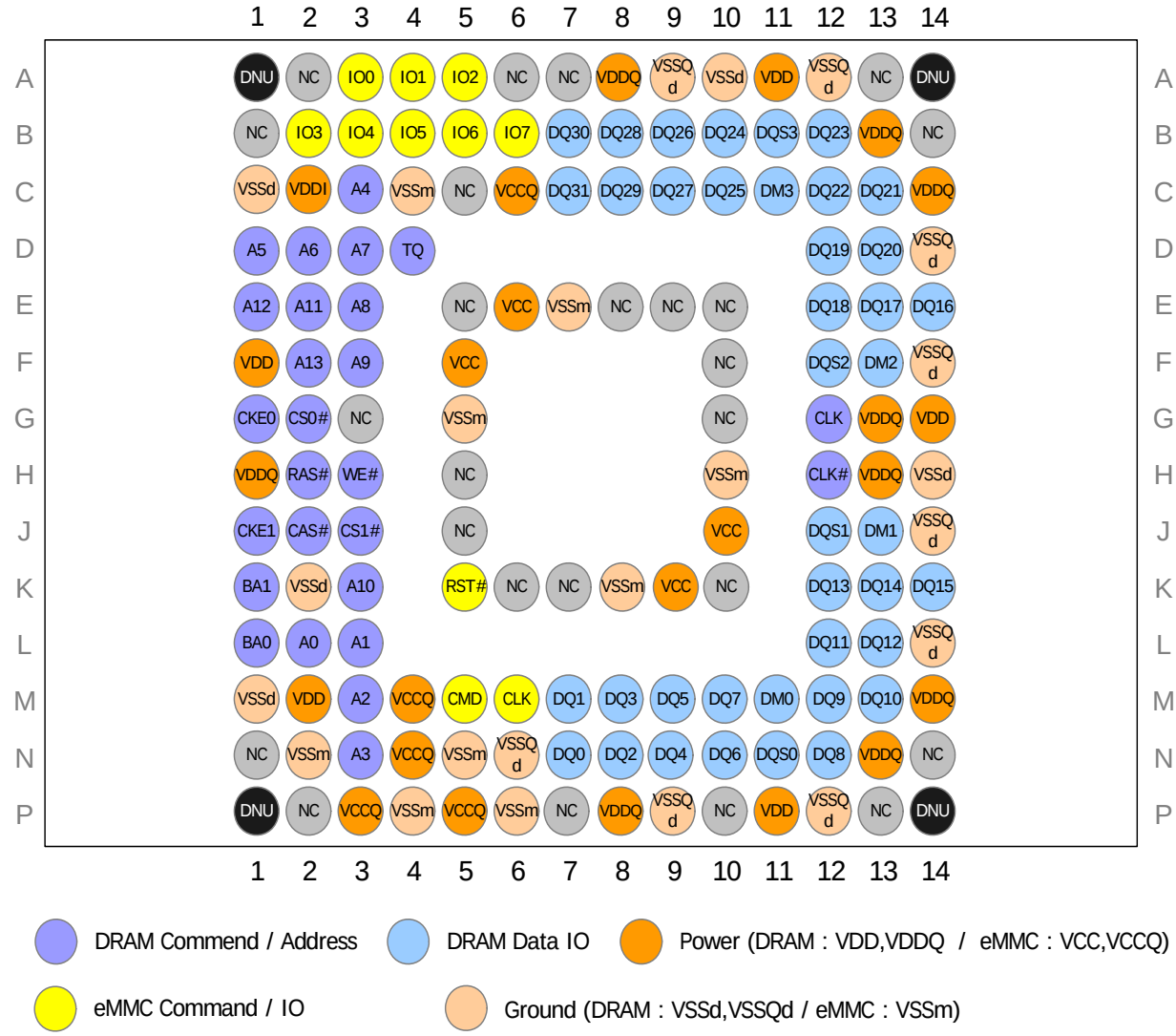


DRAM Block Diagram



Note
1. Total current consumption is dependent to user operating conditions. AC and DC Characteristics shown in this specification are based on a single die. See the section of “DC Parameters and Operating Conditions”

Ball ASSIGNMENT



Top View
153ball 11.5x13 CI-MCP
(e-NAND X8 + Mobile DDR X32)

Pin Description

SYMBOL	DESCRIPTION

< 4GB (x8) e-NAND Flash >

I/O0 ~ I/O7	Data Input / Output
CMD	Command / Response
CLK	Clock Input
RST#	Reset Signal
VSS	Flash Memory Supply Voltage Ground
VCCQ	Core Supply Voltage
VCC	Flash Memory Supply Voltage
VDDI	Should be connected to external capacitance for Internal power stability

< 4Gb (64Mb x32 2CS) mobile DDR >

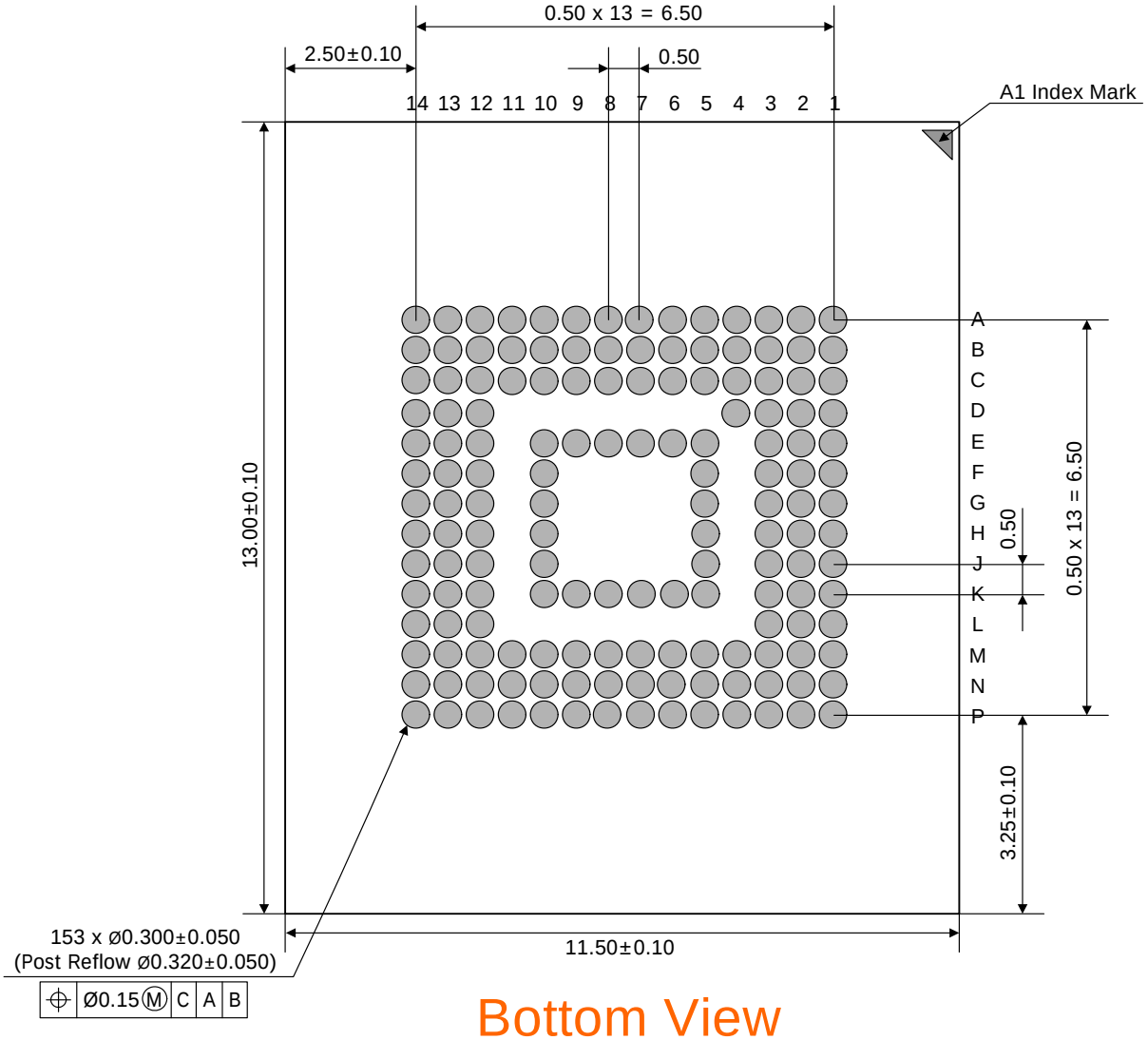
CLK, CLK#	Differential Clock Inputs
CKE0, CKE1	Clock Enable
CS0#, CS1#	Chip Select
RAS#, CAS#, WE#	Command Inputs
BA0, BA1	Bank Address Inputs
A0 ~ A13	Address Inputs
DQ0 ~ DQ31	Data Bus
DQM0~DQM3	Input Data Mask
DQS0~DQS3	Data Strobe
VDD	Power Supply
VSS	Ground
VDDQ	I/O Power Supply
VSSQ	I/O Ground
TQ	Temperature Sensor Output

< Common >

DNU	Do Not Use
NC	No Connection

PACKAGE INFORMATION

153 Ball 0.5mm pitch 11.5mm x 13.0mm FBGA *[t = 1.0mm max]*



4GB(x8) e-NAND Flash

1. Description

The SK hynix e-NAND is an embedded flash memory storage solution. The SK hynix e-NAND was developed for universal low cost data storage and communication media. The SK hynix e-NAND is fully compatible with MMC bus and host.

The SK hynix e-NAND communications are made through an advanced 13-pin bus, and it can be either 1-bit, 4-bit, or 8-bit in width. The SK hynix e-NAND operates in high-speed mode at clock frequencies equal or higher than 20MHz as defined in the MMC JEDEC standard. The communication protocol is defined in this MMC JEDEC standard.

The SK hynix e-NAND is designed to cover a wide area of applications such as smart phones, cameras, organizers, PDA, digital recorders, MP3 players, pagers, electronic toys, etc. Features are mainly high speed performance, low power consumption, low cost and high density.

To meet the requirements of embedded high density storage media and mobile applications, the SK hynix e-NAND supports 3.3V for V_{CC}, and 3.3V/1.8V for V_{CCQ}. The address argument for the SK hynix e-NAND is consistent with the sector (512-byte sectors) instead of the byte. This means that the SK hynix e-NAND is not capable to support backward compatibility for devices with the condition of the density with lower than 2 Gigabytes. If the SK hynix e-NAND receives the byte addressing type, then the SK hynix e-NAND will change its state to inactive.

The SK hynix e-NAND has the built-in intelligent controller which manages interface protocols, data storage and retrieval, wear leveling, bad block management, garbage collection, and internal ECC. The SK hynix e-NAND protects the data contents from the host sudden power off failure by safe-update operations with reliable write features. The device supports a boot operation with enhance area and sleep/awake commands. In particular, the host power regulator for V_{CC} can minimize the power consumption during the sleep state.

1.1 e-NAND standard specification

The SK hynix e-NAND device is fully compatible with the JEDEC Standard Specification No. JESD84-A441. This data sheet describes the key and specific features of the SK hynix e-NAND. Any additional interface related information, the device to a host system, and all other practical methods for card detection/access can be found in the proper section of the JEDEC Standard Specification.

2. e-NAND Features

2.1 Bus Modes

• **Boot mode**

e-NAND will be in boot mode after power cycle, reception of CMD0 with argument of 0xF0F0F0F0 or assertion of hardware reset signal.

• **Identification Mode**

e-NAND will be in identification mode when boot operation mode is finished or if host does not support a boot operation mode. e-NAND will be in this mode until the SET_RELATIVE_ADDR command (CMD3) is received.

• **Interrupt Mode**

e-NAND does not support Interrupt Mode.

• **Data Transfer Mode**

e-NAND will enter Data Transfer Mode once RCA is assigned to it. The host will enter Data Transfer Mode after identifying e-NAND on the bus.

• **Inactive Mode**

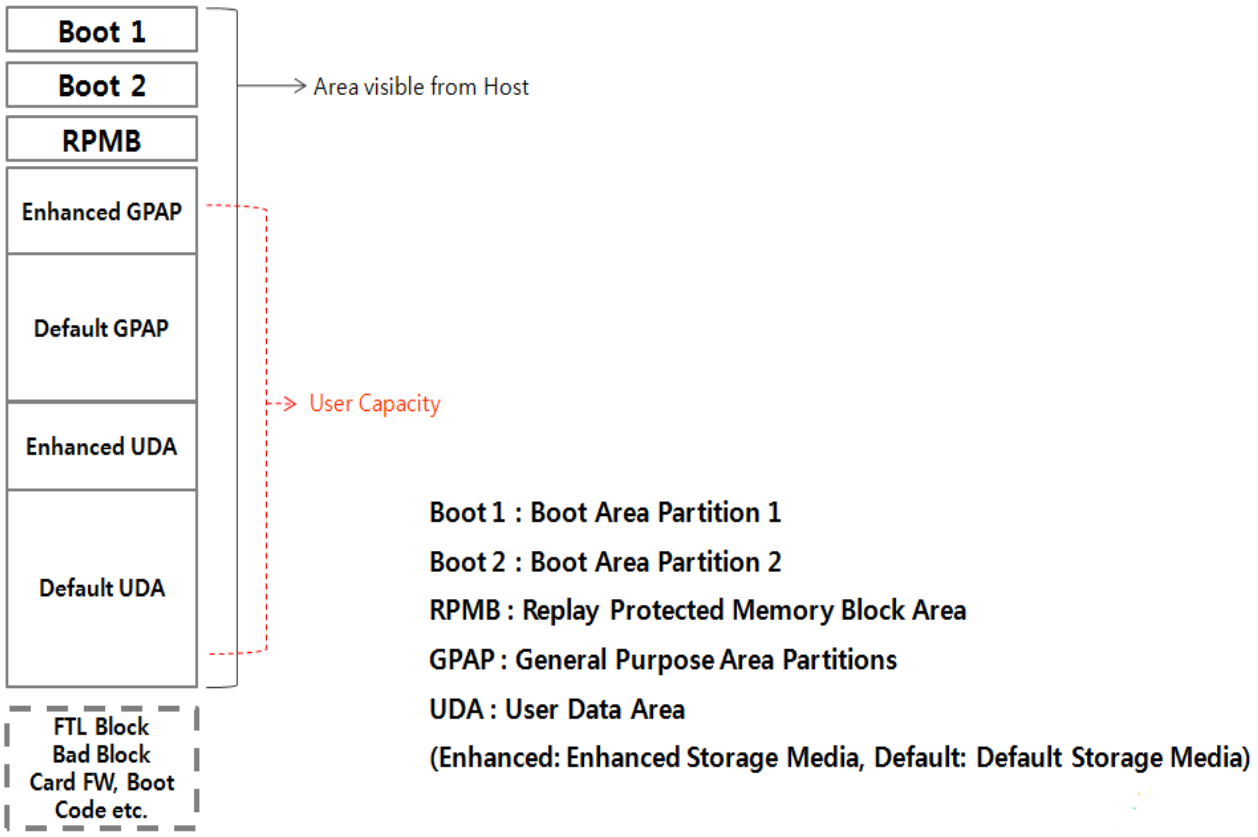
e-NAND will enter to inactive mode when e-NAND is operating invalid voltage range or access mode. Also e-NAND can be set to inactive mode by Go_INACTIVE_STATE command (CMD15). e-NAND can change from inactive mode to Pre-idle state by reset.

Table 2: Bus modes overview

e-NAND state	Operation mode	Bus mode
Inactive state	Inactive mode	Open-drain
Pre-Idle state	Boot mode	
Pre-Boot state		
Idle state	Identification mode	
Ready state		
Identification state		
Stand-by state	Data transfer mode	Push-pull
Sleep state		
Transfer state		
Bus-Test state		
Sending-data state		
Receive-data state		
Programming state		
Disconnect state		
Boot state	Boot mode	

2.2 Partition

Figure 14: Partition diagram



	Boot size	RPMB size
4GB	2MB	2MB

2.3 Boot Operation

Figure 15: e-NAND state diagram (Boot Mode)

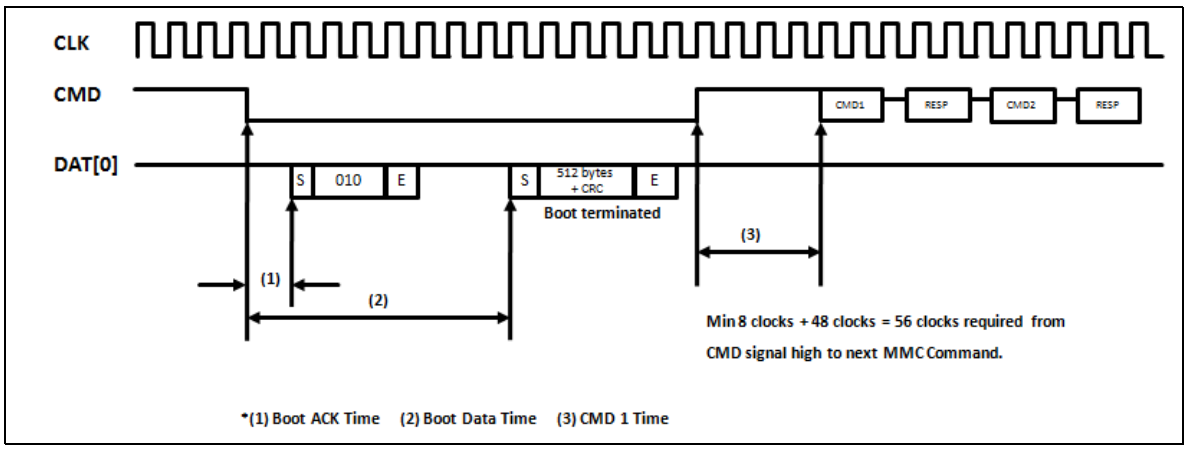
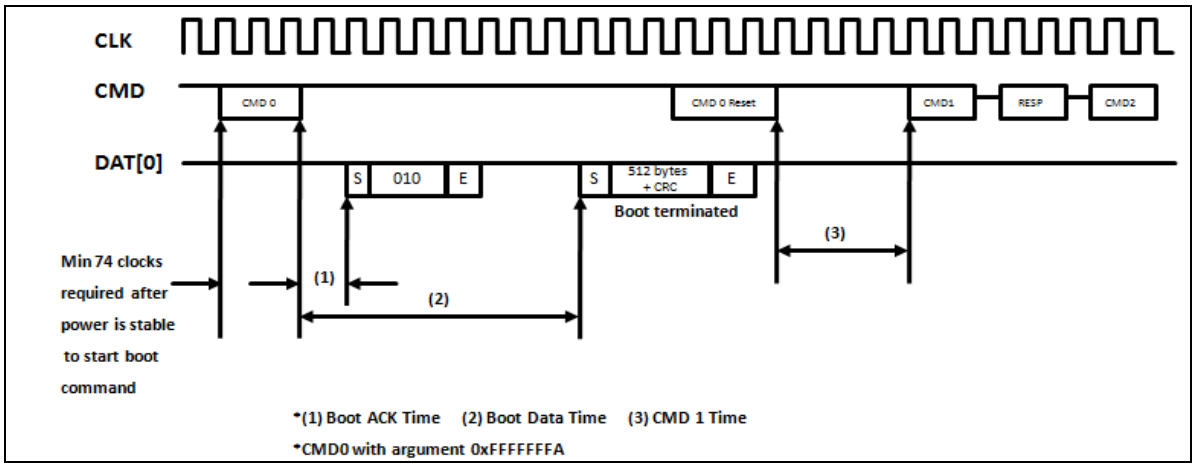


Figure 16: e-NAND state diagram (Alternative Boot Mode)



Timing Factor	
(1) Boot ACK Time	50 ms
(2) Boot Data Time	1000 ms
(3) Initialization Time	1000 ms

2.4 Power Modes

2.4.1 e-NAND power-up guidelines

e-NAND power-up must adhere to the following guidelines:

• When power-up is initiated, either V_{CC} or V_{CCQ} can be ramped up first, or both can be ramped up simultaneously.

• After power up, e-NAND enters the pre-idle state. The power up time of each supply voltage should be less than the specified tPRU (tPRUH, tPRUL or tPRUV) for the appropriate voltage range.

• If e-NAND does not support boot mode or its BOOT_PARTITION_ENABLE bit is cleared, e-NAND moves immediately to the idle state. While in the idle state, e-NAND ignores all bus transactions until receive CMD1. If e-NAND supports only standard v4.2 or earlier versions, the device enters the idle state immediately after power-up. e-NAND begins boot operation with the argument of 0xFFFFFFFA. If a boot acknowledge is finished, e-NAND shall send acknowledge pattern “010” to the host within the specified time. After boot operation is terminated, e-NAND enters the idle state and shall be ready for CMD1 operation. If e-NAND receives CMD1 in the pre-boot state, it begins to respond to the command and moves to the card identification mode.

• When e-NAND initiated by alternative boot command(CMD0 with arg=0xFFFFFFFA), all the data will be read from the boot partition and then e-NAND automatically goes to idle state. But hosts are still required to issue CMD0 with arg=0x0000000000 in order to complete a boot mode properly and move to the idle state. While in the idle state, e-NAND ignores all bus transactions until it receives CMD1.

• CMD1 is a special synchronization command which is used to negotiate the operation voltage range and to pull the device until it is out of its power-up sequence. In addition to the operation voltage profile of the device, the response to CMD1 contains a busy flag indicating that the device is still working on its power-up procedure and is not ready for identification. This bit informs the host that the device is not ready, and the host must wait until this bit is cleared. The device must complete its initialization within 200ms of the first CMD1 issued with a valid OCR range.

• If e-NAND device was successfully partitioned during the previous power up session (bit 0 of EXT_CSD byte [155] PARTITION_SETTING_COMPLETE successfully set) then the initialization delay is (instead of 200ms) calculated from INI_TIMEOUT_PA (EXT_CSD byte [241]). This timeout applies only for the very first initialization after successful paritioning. For all the consecutive initialization 200ms time out will be applied.

• The bus master moves the device out of the idle state. Because the power-up time and the supply ramp-up time depend on the application parameters such as the bus length and the power supply unit, the host must ensure that power is built up to the operating level (the same level that will be specified in CMD1) before CMD1 is transmitted.

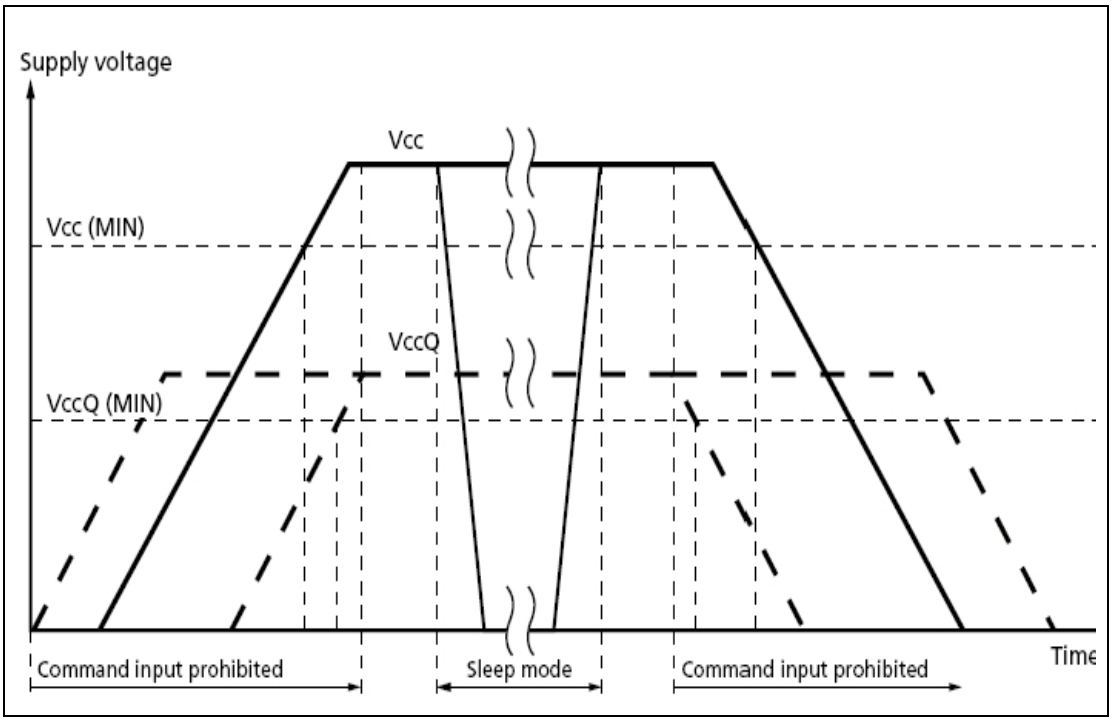
• After power-up, the host starts the clock and sends the initializing sequence on the CMD line. The sequence length can be as long as: 1ms, 74 clocks, the supply ramp-up time, or the boot operation period. An additional 10 clocks (beyond the 64 clocks of the power-up sequence) are provided to eliminate power-up synchronization problems.

• Every bus master must implement CMD1.

2.4.2 e-NAND Power Cycling

The master can execute any sequence of V_{CC} and V_{CCQ} power-up/power-down. However, the master must not issue any commands until V_{CC} and V_{CCQ} are stable with each operating voltage range. After the slave enters sleep mode, the master can power-down V_{CC} to reduce power consumption. It is necessary for the slave to be ramped up to V_{CC} before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit.

Figure 17: e-NAND power cycle



If V_{CC} or V_{CCQ} are below 0.5 V for longer than 1 ms, the slave shall always return to the pre-idle state, and perform the appropriate boot behavior. The slave will behaves as in a standard power up condition once the voltages have returned to their functional ranges. An exception to the this behavior is if the device is in sleep state, in which the voltage on V_{CC} is not monitored.

2.4.3 Leakage

Table 3: General operation conditions

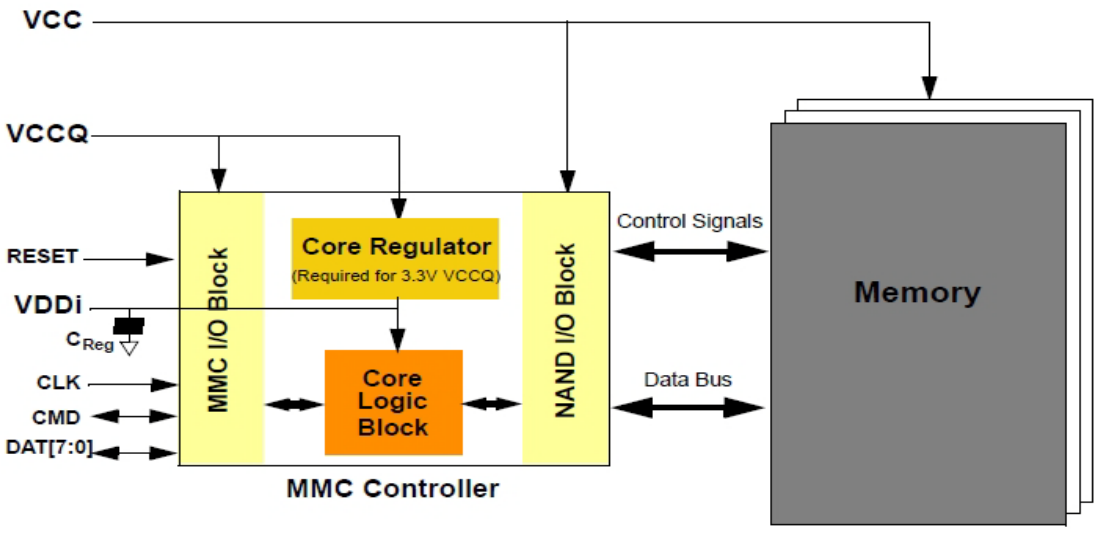
Parameter		Symbol	Min	Max.	Unit	Remark
Peak voltage on lines	Card		-0.5	V_{DD}+0.5	V	
	BGA		-0.5	VccQ+0.5	V	
All inputs						
Input leakage current (before initialization sequenceand/or the internalpull up resistors connected)			-100	100	μA	
Input leakage current (after initialization sequence and the internal pull up resistors disconnected)			-2	2	μA	
All outputs						
Output leakage current (before initialization sequence)			-100	100	μA	
Output leakage current (after initialization sequence)			-2	2	μA	

• NOTE 1. Initialization sequence is defined in JEDEC Section 12.3 on page 161

2.4.4 Power Supply

In e-NAND, V_{CC} is used for the NAND core voltage; V_{CCQ} is for the controller core, NAND interface and e-NAND interface voltage shown in Figure 18. A C_{REG} capacitor must be connected to the V_{DDi} terminal to stabilize regulator output on the system.

Figure 18: e-NAND internal power diagram



e-NAND supports one or more combinations of V_{CC} and V_{CCQ} as shown in Table 4.
The available voltage configuration is shown in Table 5.

Table 4: e-NAND power supply voltage

Parameter	Symbol	Min	Max.	Unit	Remark
Supply voltage (NAND)	V_{CC}	2.7	3.6	V	
		1.7	1.95	V	**Not support**
Supply voltage (I/O)	V_{CCQ}	2.7	3.6	V	
		1.65	1.95	V	
Supply power-up for 3.3V	tPRUH		35	ms	
Supply power-up for 3.3V	tPRUL		25	ms	
Supply power-up for 3.3V	tPRUV		20	ms	

- **NAND I/O Voltage: 1.8V for HS NAND**

Table 5: e-NAND voltage combinations

		V_{CCQ}	
		1.65V ~ 1.95V	**2.7V ~ 3.6V**
V_{CC}	**2.7V–3.6V**	Valid	Valid
	1.7V–1.95V	NOT VALID	NOT VALID

2.4.5 Operation Current

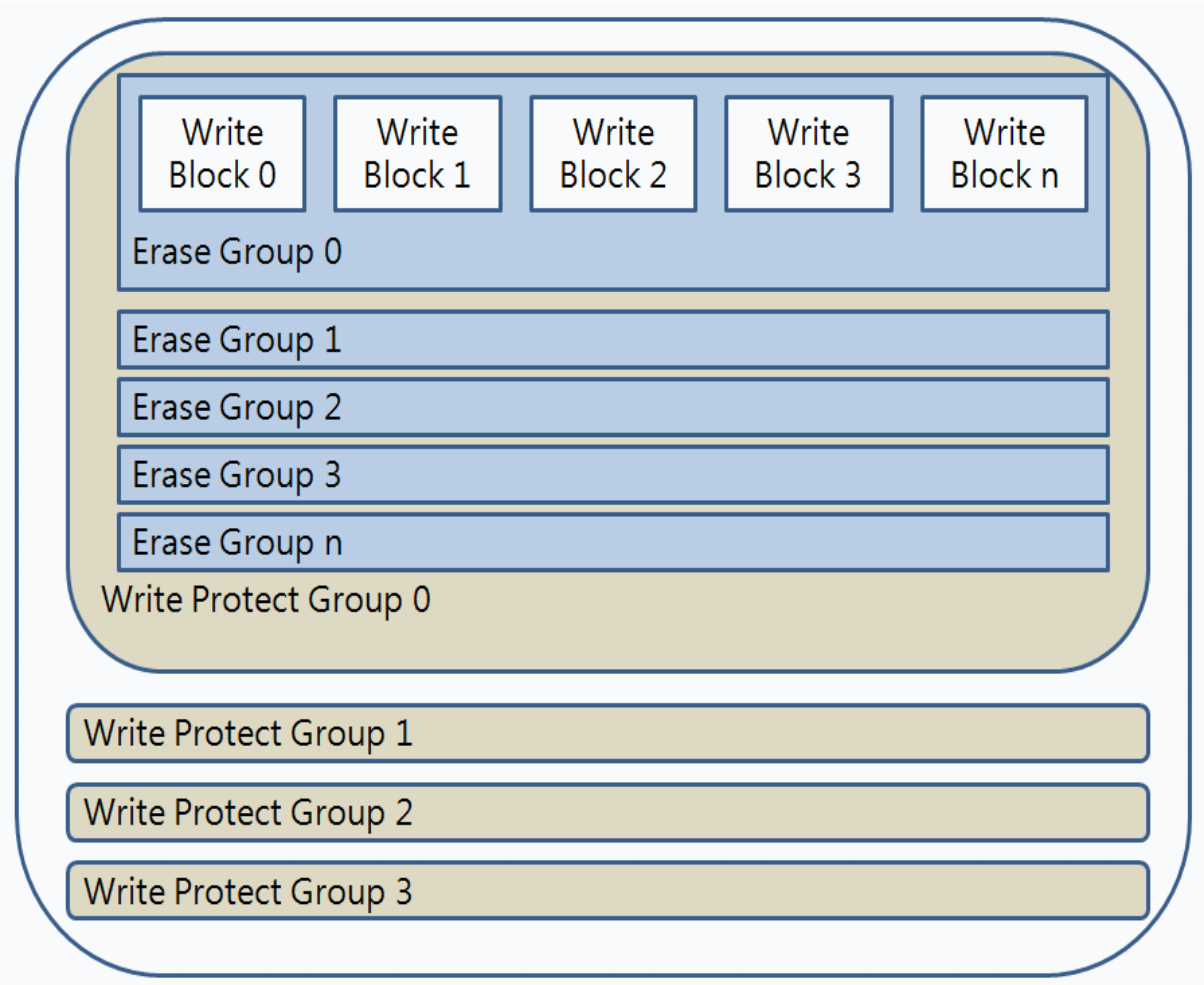
Table 6: e-NAND operation current

Mode	Density	V_{CC}	V_{CCQ}
RMS	4GB	50mA	100mA

2.4.6 Low Power Mode

TBD

2.5 Erase Write Protect Group Size



	Erase group size		Write protect group size
	ERASE_GROUP_DEF=0	ERASE_GROUP_DEF=1	
4GB	512KB	512KB	4MB

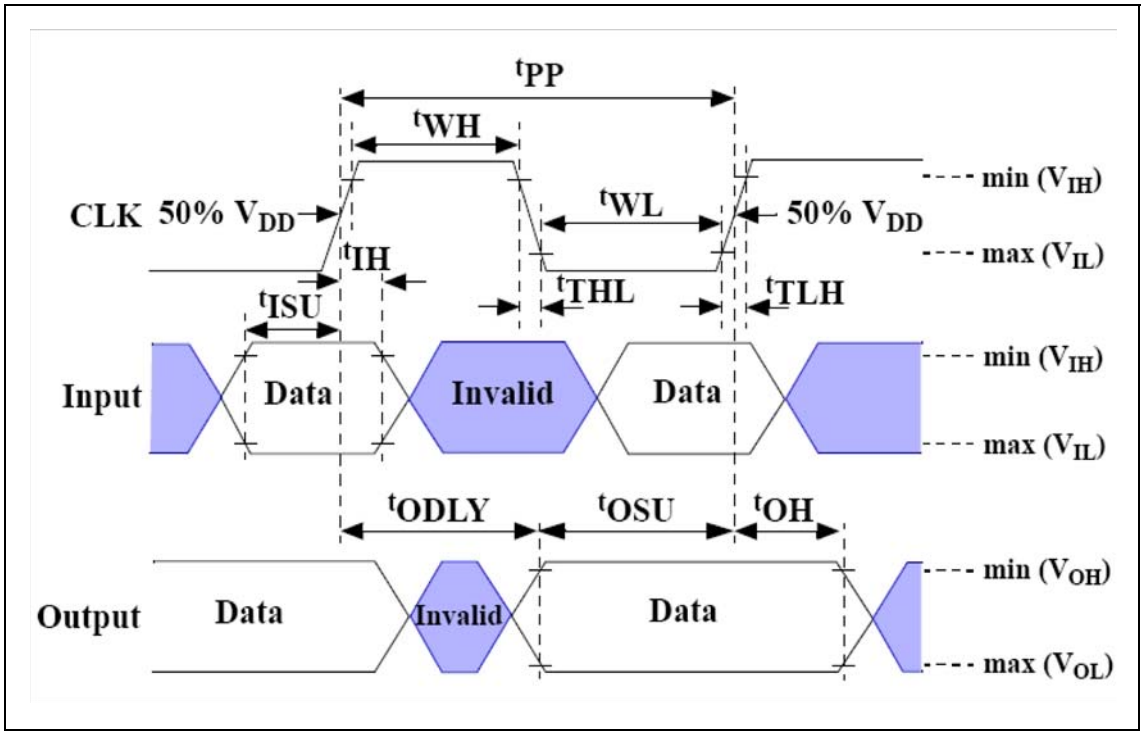
2.6 Timings

2.6.1 Time Out

Timing parameter	Value
Read timeout	100 ms
Write timeout	350 ms
Erase timeout	600 ms
Force erase timeout	3 min
Trim timeout	300 ms
Partition switching time out (after init)	30 ms

2.6.2 Bus Timing

Figure 19: Timing diagram: data input/output



Data must always be sampled on the rising edge of the clock.

Table 7: High-speed e-NAND interface timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	f_{PP}	0	52[3]	MHz	C_L ≤30 pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20KHz
Clock high time	t_{WH}	6.5		ns	C_L ≤ 30 pF
Clock low time	t_{WL}	6.5		ns	C_L ≤ 30 pF
Clock rise time[4]	t_{TLH}		3	ns	C_L ≤ 30 pF
Clock fall time	t_{THL}		3	ns	C_L ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L ≤ 30 pF
Input hold time	t_{IH}	3		ns	C_L ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t_{ODLY}		13.7	ns	C_L ≤ 30 pF
Output hold time	t_{OH}	2.5		ns	C_L ≤ 30 pF
Signal rise time[5]	t_{rise}		3	ns	C_L ≤ 30 pF
Signal fall time	t_{fall}		3	ns	C_L ≤ 30 pF

- NOTE 1. CLK timing is measured at 50% of V_{DD}.
- NOTE 2. e-NAND shall support the full frequency range from 0-26Mhz, or 0-52MHz
- NOTE 3. Card can operate as high-speed card interface timing at 26 MHz clock frequency.
- NOTE 4. CLK rising and falling times are measured by min (V_{IH}) and max (V_{IL}).
- NOTE 5. Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).

Table 8: Backward-compatible e-NAND interface timing

Parameter	Symbol	Min	Max	Unit	Remark(1)
Clock CLK(2)					
Clock frequency Data Transfer Mode (PP)(3)	f_{PP}	0	26	MHz	CL ≤ 30 pF
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	
Clock high time	t_{WH}	10		ns	CL ≤ 30 pF
Clock low time	t_{WL}	10		ns	CL ≤ 30 pF
Clock rise time(4)	t_{TLH}		10	ns	CL ≤ 30 pF
Clock fall time	t_{THL}		10	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	CL ≤ 30 pF
Input hold time	t_{IH}	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time	t_{OSU}	11.7		ns	CL ≤ 30 pF
Output hold time	t_{OH}	8.3		ns	CL ≤ 30 pF

- NOTE 1. e-NAND must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed timing by the host sending the SWITCH command (CMD6) with the argument for high speed interface select.
- NOTE 2. CLK timing is measured at 50% of V_{DD}.
- NOTE 3. For compatibility with cards that support the v4.2 standard or earlier, host should not use > 20 MHz before switching to high-speed interface timing.
- NOTE 4. CLK rising and falling times are measured by min (V_{IH}) and max (V_{IL}).
- NOTE 5. t_{OSU} and t_{OH} are defined as values from clock rising edge. However, there may be cards or devices which utilize clock falling edge to output data in backward compatibility mode.

  Therefore, it is recommended for hosts to either to set t_{WL} value as long as possible within the range which will not go over t_{CK}-t_{OH}(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices.

  In this case, each device which utilizes clock falling edge might show the correlation either between t_{WL} and t_{OSU} or between t_{CK} and t_{OSU} for the device in its own datasheet as a note or its' application notes.

2.6.3 Bus Timing for DAT Signals During 2X Data Rate Operation

These timings apply to the DAT[7:0] signals only when the device is configured for dual data mode operation. In dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in eMMC JEDEC spec. section 11.5, therefore there is no timing change for the CMD signal.

Figure 20: Timing diagram: data input/output in dual data rate mode

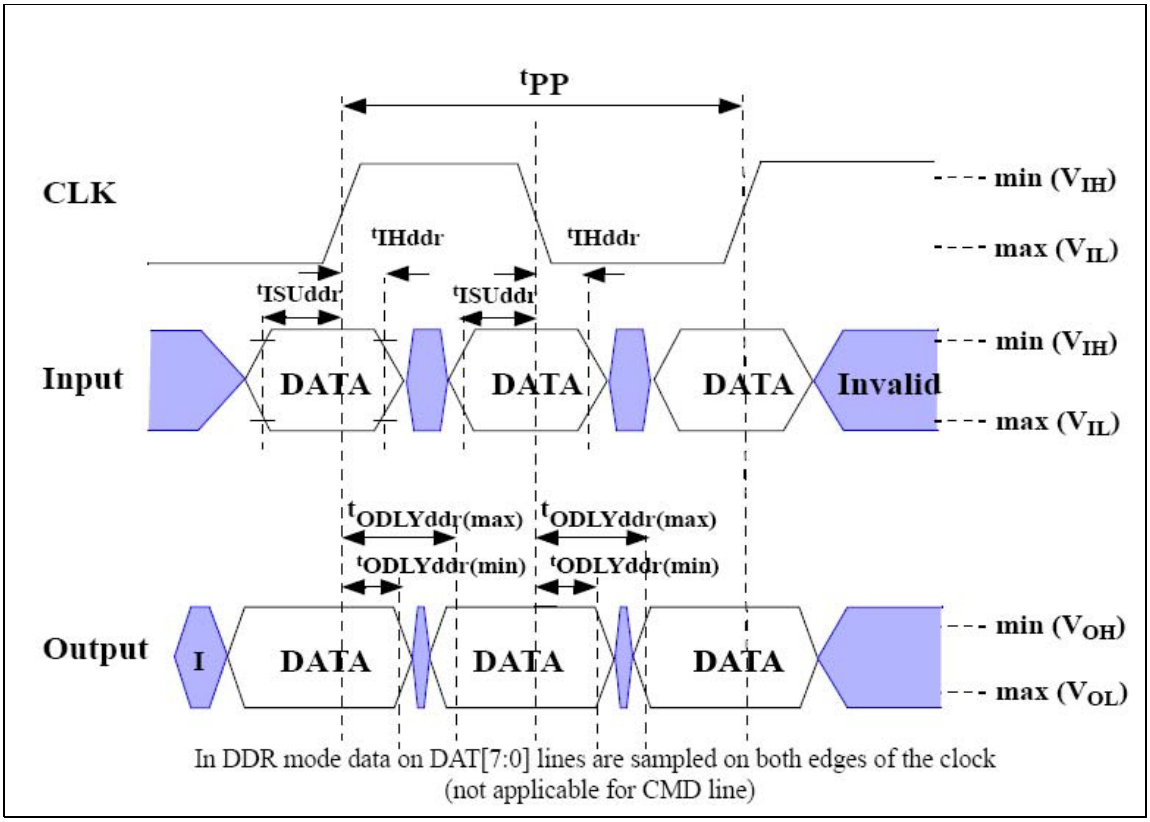


Table 9: Dual data rate interface timings

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK(1)					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Inputs DAT (referenced to CLK-DDR mode)					
Input set-up time	t_{ISUDDR}	2.5		ns	C_L ≤ 20 pF
Input hold time	t_{IHDDR}	2.5		ns	C_L ≤ 20 pF
Outputs DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	$t_{ODLYDDR}$	1.5	7	ns	C_L ≤ 20 pF
Signal rise time(all signal)(2)	t_{RISE}		2	ns	C_L ≤ 20 pF
Signal fall time (all signal)	t_{FALL}		2	ns	C_L ≤20 pF

- NOTE 1. CLK timing is measured at 50% of V_{DD}.
- NOTE 2. Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL})

3. Commands

3.1 Command Classes

The command set of e-NAND is divided into several classes. Each class supports a subset of e-NAND functions.
The supported e-NAND command Classes are coded as a parameter in the eMMC specific data (CSD) register, providing the host with information on how to access the e-NAND.

Table 14: Supported eMMC command classes

e-NAND command class	Class description	Support commands																						
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	23	24	25
Class 0	basic	+	+	+	+	+	+	+	+	+	+	+		+	+	+	+				+				
Class 1	stream read												+												
Class 2	block read																	+	+	+			+		
Class 3	stream write																					+			
Class 4	block write																	+					+	+	+
Class 5	erase																								
Class 6	write protection																								
Class 7	lock eMMC																	+							
Class 8	application specific																								
Class 9	I/O mode																								
Class 10-11	reserved																								

e-NAND command class	Class description	Support commands														Note
		26	27	28	29	30	31	35	36	38	39	40	42	55	56	
Class 0	basic															
Class 1	stream read															**Not Support**
Class 2	block read															
Class 3	stream write															**Not Support**
Class 4	block write	+	+													
Class 5	erase							+	+	+						
Class 6	write protection			+	+	+	+									
Class 7	lock eMMC												+			
Class 8	application specific													+	+	**Not Support**
Class 9	I/O mode										+	+				**Not Support**
Class 10-11	reserved															

3.2 Detailed Command Description

The following tables define in detail all e-NAND commands.

Table 15: Basic command (class 0 and class 1)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD0	bc	[31:0] 00000000	-	GO_IDLE_STATE	Resets e-NAND to idle state
	bc	[31:0] F0F0F0F0	-	GO_PRE_IDLE_STATE	Resets e-NAND to pre-idle state
	-	[31:0] FFFFFFFA	-	BOOT_INITIATION	Inititiate alternative boot operation
CMD1	bcr	[31:0] OCR with-out busy	R3	SEND_OP_COND	Asks e-NAND, in idle state, to send its Operating Conditions Register contents in the response on the CMD line.
CMD2	bcr	[31:0] stuff bits	R2	ALL_SEND_CID	Asks e-NAND to send its CID number on the CMD line
CMD3	ac	[31:16] RCA [15:0] stuff bits	R1	SET_RELATIVE_ADDR	Assigns relative address to e-NAND
CMD4	bc	[31:16] DSR [15:0] stuff bits	-	SET_DSR	Programs the DSR of e-NAND
CMD5	ac	[31:16] RCA [15] Sleep/Awake [14:0] stuff bits	R1b	SLEEP_AWAKE	Toggles the card between Sleep state and Standby state.
CMD6	ac	[31:26] Set to 0 [25:24] Access [23:16] Index [15:8] Value [7:3] Set to 0 [2:0] Cmd Set	R1b	SWITCH	Switches the mode of operation of e-NAND the EXT_CSD registers.
CMD7	ac	[31:16] RCA [15:0] stuff bits	R1/ R1b(1)	SELECT/DESELECT_CARD	Command toggles e-NAND between the stand-by and transfer states or between the programming and disconnect states. In both cases e-NAND is selected by its own relative address and gets deselected by any other address; address 0 deselects e-NAND.
CMD8	adtc	[31:0] stuff bits	R1	SEND_EXT_CSD	e-NAND sends its EXT_CSD register as a block of data.
CMD9	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CSD	e-NAND sends its card-specific data (CSD) on the CMD line.
CMD10	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CID	e-NAND sends its card identification (CID) on CMD the line.
CMD11	adtd	[31:0]data address	R1	READ_DAT_UNTIL_STOP	The response to CMD11 will be undefined.
CMD12	ac	[31:16]RCA(2) [15:1]stuff bits [0]HPI	R1/ R1b(3)	STOP_TRANSMISSION	Forces e-NAND to stop transmission.If HPI flag is set the device shall interrupt itsin-ternal operations in a well defined timing.

Table 16: Basic commands and read-stream command (class 0 and class 1) (continued)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD13	bc	[31:16] RCA [15:1] stuff bits [0] HPI	R1	SEND_OP_COND	e-NAND sends its status register. e-NAND does not support HPI by CMD13.
CMD14	adtc	[31:0] stuff bits	R1	BUSTEST_R	A host reads the reversed bus testing data pattern from e-NAND.
CMD15	ac	[31:16] RCA [15:0] stuff bits	-	GO_INACTIVE_STATE	Sets e-NAND to inactive state
CMD19	adtc	[31:0] stuff bits	R1	BUSTEST_W	A host sends the bus test data pattern to e-NAND.

- NOTE 1. R1 while selecting from Stand-By State to Transfer State; R1b while selecting from Disconnected State to Programming State.
- NOTE 2. RCA in CMD12 is used only if HPI bit is set. The argument does not imply any RCA check on the device side.
- NOTE 3. R1 for read cases and R1b for write cases.

Table 17: Block-oriented read commands (class 2)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	Sets the block length (in bytes) for all following block commands (read and write). Default block length is specified in the CSD.
CMD17	adtc	[31:0] data address(1)	R1	READ_SINGLE_BLOCK	Reads a block of the size selected by the SET_BLOCKLEN command.
CMD18	adtc	[31:0] data address(1)	R1	READ_MULTIPLE_ BLOCK	Continuously transfers data blocks from e-NAND to host until interrupted by a stop command, or the requested number of data blocks is transmitted

- NOTE 1. Data address for e-NAND is a 32bit sector (512B) address.

Table 18: Stream write commands (class 3)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD20	adtc	[31:0] data address	R1	WRITE_DAT_UNTIL_STOP	The response to CMD20 will be defined.
CMD21 CMD22	reserved				

Table 19: Block-oriented write commands (class 4)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD23	ac	[31] Reliable Write Request [30:16] set to 0 [15:0] number of blocks	R1	SET_BLOCK_COUNT	Defines the number of blocks (read/ write) and the reliable writer parame-ter (write) for a block read or write command.
CMD24	adtc	[31:0] data address(1)	R1	WRITE_BLOCK	Writes a block of the size selected by the SET_BLOCKLEN command.
CMD25	adtc	[31:0] data address(1)	R1	WRITE_MULTIPLE_BLOCK	Continuously writes blocks of data until a STOP_TRANSMISSION follows or the requested number of block received.
CMD26	adtc	[31:0] stuff bits	R1	PROGRAM_CID	Programming of the card identification register.This command shall be issued only once. e-NAND contains hardware to prevent this operation after the first programming. Normally this command is reserved for the manufacturer.
CMD27	adtc	[31:0] stuff bits	R1	PROGRAM_CSD	Programming of the programmable bits of the CSD.

- NOTE 1. Data address for e-NAND is a 32bit sector (512B) address.

Table 20: Block-oriented write protection commands (class 6)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command Description
CMD28	ac	[31:0] data address(1)	R1b	SET_BLOCK_COUNT	If e-NAND has write protection fea-tures, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE or HC_WP_GRP_SIZE).
CMD29	ac	[31:0] data address(1)	R1b	CLR_WRITE_PROT	If e-NAND provides write protection fea-tures, this command clears the write protec-tion bit of the addressed group.
CMD30	adtc	[31:0] write protect data address	R1	SEND_WRITE_PROT	If e-NAND provides write protection fea-tures, this command asks e-NAND to send the status of the write protec-tion bits.(2)
CMD31	adtc	[31:0] write protect data address	R1	SEND_WRITE_PROT_TYPE	This command sends the type of write pro-tection that is set for the different write pro-tection groups.(3)

- NOTE 1. Data address for e-NAND is a 32bit sector (512B) address.
- NOTE 2. 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data lines. The last (least significant) bit of the protection bits corresponds to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding write protection bits shall be set to zero.
- NOTE 3. 64 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data lines. Each set of two protection bits shows the type of protection set for each of the write protection groups. The definition of the different bit settings are shown below. The last (least significant) two bits of the protection bits correspond to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding write protection bits shall be set to zero.

  “00” Write protection group not protected
  “01” Write protection group is protected by temporary write protection
  “10” Write protection group is protected by power-on write protection
  “11” Write protection group is protected by permanent write protection

Table 21: Erase commands (class 5)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD32 ... CMD34	Reserved. These command indexes cannot be used in order to maintain backwards compatibility with older versions of the MultiMediaCards				
CMD35	ac	[31:0] data address(1),(2)	R1	ERASE_GROUP_START	Sets the address of the first erase group within a range to be selected for erase
CMD36	ac	[31:0] data address(1),(2)	R1	ERASE_GROUP_END	Sets the address of the last erase group within a continuous range to be selected for erase
CMD37	Reserved. This command index cannot be used in order to maintain backwards compatibility with older versions of the MultiMediaCards				
CMD38	ac	[31] Secure request [30:16] set to 0 [15] Force garbage collect request [14:1] set to 0 [0]Identify Write block for Erase	R1b	ERASE	Erases all previously selected write blocks according to argument bits.

- NOTE 1. Data address for e-NAND is a 32bit sector (512B) address.
- NOTE 2. e-NAND will ignore all LSB's below the Erase Group size, effectively rounding the address down to the Erase Group boundary.

Table 22: I/O mode commands (class 9)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD39	ac	[31:16] RCA [15:15] register write flag [14:8] register address [7:0] register dat	R4	FAST_IO	Used to write and read 8 bit (register) data fields. The command addresses a Device and a register and provides the data for sriting if the write flag is set. The R4 response contains data read from the addressed register if the write flag is cleared to 0. This command accesses application dependent registers which are not defined in th eMMC standard.
CMD40	bcr	[31:0] stuff bits	R5	GO_IRQ_STATE	Sets the system into interrupt mode
CMD41	reserved				

Table 23: Lock eMMC commands (class 7)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD42	adtc	[31:16] stuff bits	R1	LOCK_UNLOCK	Used to set/reset the password or lock/unlock the card. The size of the data block is set by the SET_BLOCK_LEN command.
CMD43 ... CMD54	reserved				

Table 24: Application-specific commands (class 8)

CMD INDEX	Type	Argument	Resp	Abbreviation	Command description
CMD55	ac	[31:16] RCA [15:0] stuff bits	R1	APP_CMD	Indicates to the Device that the next command is an application sp**ecific command rather than a standard command.**
CMD56	adtc	[31:1] stuff bits. [0]: RD/WR(1)	R1	GEN_CMD	Used either to transfer a data block to the Device or to get a data block from the Device for general purpose / application specific commands. The size of the data block shall be set by the SET_BLOCK_LEN command.
CMD57 ... CMD59	reserved				
CMD60 ... CMD63	reserved for manufacturer				

- NOTE 1. RD/WR: “1” the host gets a block of data from e-NAND. “0” the host sends block of data to e-NAND.

4. Device Registers

There are six different registers within the device interface:

- Operation Conditions Register (OCR)
- Card Identification Register (CID)
- Card Specific Data Register (CSD)
- Relative Card Address Register (RCA)
- DSR (Driver Stage Register)
- Extended Card Specific Data Register (EXT_CSD).

These registers are used for the serial data communication and can be accessed only using the corresponding commands . (refer to section 8 of the JEDEC Standard Specification No. JESD84-A441)

e-NAND has a status register to provide information about the device current state and completion codes for the last host command.

4.1 Operation Conditions Register (OCR)

The 32-bit operation conditions register (OCR) stores the V_{DD} voltage profile of e-NAND and the access mode indication. In addition, this register includes a status information bit. This status bit is set if e-NAND power up procedure has been finished. The OCR register shall be implemented by e-NAND.

Table 25: OCR register definition

OCR bit	Description	e-NAND
[6:0]	Reserved	000 0000b
[7]	1.70 - 1.95V	0b
[14:8]	2.0 - 2.6	000 0000b
[23:15]	2.7 - 3.6 (High V_{CCQ} range)	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access mode	10b
[31]	(card power up status bit ((busy)[1]	

- NOTE 1. This bit is set to LOW if the card has not finished the power up routine

4.2 Card Identification (CID) Register

The Card IDentification (CID) register is 128 bits wide. It contains e-NAND identification information used during e-NAND identification phase (e-NAND protocol). Every individual flash or I/O e-NAND shall have a unique identification number. Table 26 lists these identifiers. The structure of the CID register is defined in the following sections., refer to section 8.2 of the JEDEC Standard Specification No. JESD84-A441.

Table 26 : Card identification (CID) fields

Name	Field	Width	CID slice	CID value	Remark
Manufacturer ID	MID	8	[127:120]	90h	
Reserved		6	[119:114]		
Card/BGA	CBX	2	[113:112]	01h	BGA
OEM/application ID	OID	8	[111:104]	4ah	
Product name	PNM	48	[103:56]	0x483447316404	
Product revision	PRV	8	[55:48]		Not Fixed
Product serial number	PSN	32	[47:16]		Not Fixed
Manufacturing date	MDT	8	[15:8]		Not Fixed
CRC7 checksum	CRC	7	[7:1]		Not Fixed
Not used, always '1'	Reserved	1	[0:0]	1	

4.3 Card Specific Data Register (CSD)

The Card Specific Data (CSD) register provides information on how to access e-NAND contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the CSD Registry entries in the Table 27 below is coded as follows:

- ***R:*** Read only. W: One time programmable and not readable. R/W: One time programmable and readable.
- ***W/E:*** Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- ***R/W/E:*** Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
- ***R/W/C_P:*** Writable after value cleared by power failure and HW/rest assertion (the value not cleared by CMD0 reset) and readable.
- ***R/W/E_P:*** Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
- ***W/E_P:*** Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

For details, refer to section 8.3 of the JEDEC Standard Specification No. JESD84-A441.

Table 27: CSD fields

Name	Field	Width	Cell type	CSD slice	CSD value	Remark
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h	
System specification version	SPEC_VERS	4	R	[125:122]	4h	
Reserved		2	R	[121:120]		
Data read access-time 1	TAAC	8	R	[119:112]	27	
Data read access-time 2in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h	
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h	
Card command classes	CCC	12	R	[95:84]	f5h	
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h	
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h	
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h	
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h	
DSR implemented	DSR_IMP	1	R	[76:76]	0h	
Reserved		2	R	[75:74]		
Device size	C_SIZE	12	R	[73:62]	fffh	
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	7h	
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	7h	
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	7h	
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	7h	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h	
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1fh	
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1fh	
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	7h	
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h	
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h	
Write speed factor	R2W_FACTOR	3	R	[28:26]	2	

Table 27: CSD fields (continued)

Name	Field	Width	Cell type	CSD slice	CSD value	Remark
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h	
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h	
Reserved		4	R	[20:17]		
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h	
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h	
Copy flag (OTP)	COPY	1	R/W	[14:14]	1h	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h	
File format	FILE_FORMAT	2	R/W	[11:10]	0h	
ECC code	ECC	2	R/W/E	[9:8]	0h	
CRC	CRC	7	R/W/E	[7:1]	0	
Reserved		1		[0:0]		

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

4.4 Extended CSD Register

The Extended CSD register defines e-NAND properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines e-NAND capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration e-NAND is working in. These modes can be changed by the host by means of the SWITCH command.

For details, refer to section 8.4 of the JEDEC Standard Specification No. JESD84-A441.

Table 28: Extended CSD

Name	Field	CSD slice	Cell Type	EXT_CSD Value	Remark
Properties segment					
Reserved		[511:505]			
Supported command sets	S_CMD_SET	[504]	R	1h	Allocated by MMCA
HPI features	HPI_FEATURES	[503]	R	3h	Bit[1]=1: HPI mechanism implementation based on CMD12 Bit[1]=0: HPI mechanism implementation based on CMD13 Bit[0]=1: HPI mechanism support Bit[0]=0: HPI mechanism not supported (default)
Background operations support	BKOPS_SUPPORT	[502]	R	1h	Background operation are supported
Reserved		[501:247]			
Background operations status	BKOPS_STATUS	[246]	R	0h	Outstanding: No operations required
Number of correctly programmed sectors	CORRECTLY_PRG_ SECTORS_NUM	[245:242]	R	0h	Number of correctly programmed sectors = [245]*224+[244]*216+[243]*28+[242]
1st initialization time after partitioning	INI_TIMEOUT_AP	[241]	R	0ah	100ms*10=1000ms
Reserved		[240]			
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_ 52_360	[239]	R	0h	MAX RMS Current=100mA, MAX Peak Current=200mA
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_ 52_195	[238]	R	0h	MAX RMS Current=65mA, MAX Peak Current=130mA
Reserved		[237:236]			
Minimum write performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_ 8_52	[235]	R	0h	For cards not reaching the 4.8MB/s value
Minimum read performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_ R_8_52	[234]	R	0h	For cards not reaching the 4.8MB/s value
Reserved		[233]			
TRIM multiplier	TRIM_MULT	[232]	R	1h	TRIM Timeout = 300ms*1=300ms
Secure feature support	SEC_FEATURE_ SUPPORT	[231]	R	15h	Bit[4]=1: Card supports the secure and insecure trim operations Bit[2]=1: Card supports the automatic secure purge operation on retired defective portions of the array Bit[0]=1: Secure purge operations are supported Bit[0,2,4]=0: Not support each feature Bit[1,3,5,6,7]=Reserved

Name	Field	CSD slice	Cell Type	EXT_CSD Value	Remark
Secure erase multiplier	SEC_ERASE_MULT	[230]	R	0ah	Secure Erase Timeout=300ms*2*10=6000ms
Secure TRIM multiplier	SEC_TRIM_MULT	[229]	R	0ah	Secure Erase Timeout=300ms*2*10=6000ms
Boot information	BOOT_INFO	[228]	R	5h	Bit[2]=1 : Device supports high speed timing duing boot Bit[1]=1 : Device supports dual data rate duing boot Bit[0]=1 : Device supports alternate boot method Bit[0,1,2]=0 : Not supports each feature Bit[7:3]=Reserved
Reserved		[227]			
Boot partition size	BOOT_SIZE_MULTI	[226]	R	10h	Boot Partition Size = 128KB*16=2048KB
Access size	ACC_SIZE	[225]	R	7h	Super-Page Size = 512*2^(7-1)=32768 Bytes
High-capacity erase unit size	HC_ERASE_GRP_SIZE	[224]	R	1h	Erase Unit Size = 512KB*1=512KB
High_capacity erase timeout	ERASE_TIMEOUT_MULT	[223]	R	2h	Erase Timeout=300ms*2=600ms
Reliable write sector count	REL_WR_SEC_C	[222]	R	1h	1 sector supported for reliable write feature
High-capacity write protect group size	HC_WP_GRP_SIZE	[221]	R	8h	8 high-capacity erase unit size
Sleep current(VCC)	S_C_VCC	[220]	R	7h	Sleep Curent @ Vcc = 1uA*2^7=128uA
Sleep current(VCCQ)	S_C_VCCQ	[219]	R	7h	Sleep Curent @ Vccq = 1uA*2^7=128uA
Reserved		[218]			
Sleep/awake timeout	S_A_TIMEOUT	[217]	R	13h	Sleep/Awake Timeout=100ns*2^19=52428800ns
Reserved		[216]			
Sector count	SEC_COUNT	[215:212]	R	738000h	TBD
Reserved		[211]			
Minimum write performance for 8bit at52MHz	MIN_PERF_W_8_52	[210]	R	8h	Class A: 2.4MB/s and is the next allowed value (16*150KB/s)
Minimum read performance for 8bit at 52MHz	MIN_PERF_R_8_52	[209]	R	8h	Class A: 2.4MB/s and is the next allowed value (16*150KB/s)
Minimum write performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	[208]	R	8h	Class A: 2.4MB/s and is the next allowed value (16*150KB/s)
Minimum read performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	[207]	R	8h	Class A: 2.4MB/s and is the next allowed value (16*150KB/s)
Minimum write performance for 4bit at 26MHz	MIN_PERF_W_4_26	[206]	R	8h	Class A: 2.4MB/s and is the next allowed value (16*150KB/s)

Name	Field	CSD Slice	Cell Type	EXT_CSD Value	Remark
Minimum read performance for 4bit at 26MHz	MIN_PERF_R_4_26	[205]	R	8h	Class A: 2.4MB/s and is the next allowed value (16*150KB/s)
Reserved		[204]			
Power class for 26MHz at 3.6V	PWR_CL_26_360	[203]	R	0h	MAX RMS Current = 100mA, MAX Peak Current = 200mA
Power class for 52MHz at 3.6V	PWR_CL_52_360	[202]	R	0h	MAX RMS Current = 100mA, MAX Peak Current = 200mA
Power class for 26MHz at 1.95V	PWR_CL_26_195	[201]	R	0h	MAX RMS Current = 65mA, MAX Peak Current = 130mA
Power class for 52MHz at 1.95V	PWR_CL_52_195	[200]	R	0h	MAX RMS Current = 65mA, MAX Peak Current = 130mA
Partition switching timing	PARTITION_ SWITCH_TIME	[199]	R	3h	Maximum partition switch timeout = 10ms*2=20ms
Out-of-interrupt busy timing	OUT_OF_INTERRUPT _TIME	[198]	R	2h	Maximum out-of-interrupt timeout = 10ms*2=20ms
Reserved		[197]			
Card type	CARD_TYPE	[196]	R	7h	Bit[3]=1 : High-Speed Dual Data Rate MultimediaCard @ 52MHz - 1.2V I/O Bit[2]=1 : High-Speed Dual Data Rate MultimediaCard @ 52MHz - 1.8V or 3V I/O Bit[1]=1 : High-Speed MultimediaCard @ 52MHz - at rated device voltage(s) Bit[0]=1 : High-Speed MultimediaCard @ 26MHz - at rated device voltage(s) Bit[7:4] : Reserved
Reserved		[195]			
CSD structure version	CARD_STRUCTURE	[194]	R	2h	Version 4.1 - 4.2 - 4.3 - 4.4
Reserved		[193]			
Extended CSD revision	EXT_CSD_REV	[192]	R	5h	Revision 1.5 (for MMC v4.41)
Modes Segment					
Command set	CMD_SET	[191]	R/W/E_P	0h	Currently active command set. It can be 1 by host.
Reserved		[190]			
Command set revision	CMD_SET_REV	[189]	R	0h	See EXT_CSD in spec. It does not have a fixed rule.
Reserved		[188]			
Power class	POWER_CLASS	[187]	R/W/E_P	0h	See EXT_CSD in spec.
Reserved		[186]			
High-speed interface timing	HS_TIMING	[185]	R/W/E_P	1h	It depends on Host I/F speed. Default is 0, but it can be 1 by host.
Reserved		[184]			
Bus width mode	BUS_WIDTH	[183]	W/E_P	2h	Partition switch timeout = 10ms*2=20ms

Name	Field	CSD Slice	Cell Type	EXT_CSD Value	Remark
Reserved		[182]			
Erased memory content	ERASED_MEM_CONT	[181]	R	0h	Erased memory range shall be '0'
Reserved		[180]			
Partition configuration	PARTITION_CONFIG	[179]	R/W/E & R/WE_P	0h	See EXT_CSD in spec
Boot config protection	BOOT_CONFIG_PROT	[178]	R/W & R/W/C_P	0h	See EXT_CSD in spec
Boot bus width	BOOT_BUS_WIDTH	[177]	R/W/E	0h	See EXT_CSD in spec
Reserved		[176]	TBD		
High-density erase group definition	ERASE_GROUP_DEF	[175]	R/W/E_P	0h	Use old erase group size and write protect group size definition (default)
Reserved		[174]	TBD		
Boot area write protection register	BOOT_WP	[173]	R/W & R/W/C_P	0h	Bit[6]=0 : Master is permitted to set B_PWR_WP_EN (bit0) Bit[4]=0 : Master is permitted to set B_PERM_WP_EN (bit2) Bit[2]=0 : Boot Region is not permanently write protected Bit[0]=0 : Boot Region is not power-on write protected
Reserved		[172]	TBD		
User area write protection register	USER_WP	[171]	R/W,R/W/C_P & R/W/E_P	0h	See EXT_CSD in spec
Reserved		[170]	TBD		
FW configuration	FW_CONFIG	[169]	R/W	0h	FW updates enabled
RPMB Size	RPMB_SIZE_MULT	[168]	R	10h	RPMB Partition Size=128KB*16=2048KB
Write reliability setting register	WR_REL_SET	[167]	R/W	1fh	Write Data Reliability Partition FALSE
Write reliability parameter register	WR_REL_PARAM	[166]	R	5h	Bit[2]=1 : The device supports the enhanced definition of reliable write Bit[2]=0 : The device supports the previous definition of reliable write Bit[0]=1 : All the WR_DATA_REL parameters in the WR_REL_SET registers are R/W Bit[0]=0 : All the WR_DATA_REL parameters in the WR_REL_SET registers are read only bits
Sanitize start	SANITIZE_START	[165]	W/E_P	0h	-
Manually start background operations	BKOPS_START	[164]	W/E_P	0h	Writing any value to this field shall manually start BKOPs.
Enable background operations handshake	BKOPS_EN	[163]	R/W	0h	Host does not support BKOPs handling and is not expected to write to BKOPS_START field
H/W reset function	RST_n_FUNCTION	[162]	R/W	0h	RST_n signal is temporarily disabled (default)
HPI management	HPI_MGMT	[161]	R/W/E_P	0h	HPI mechanism not activated by the host (default)
Max enhanced area size	MAX_ENH_SIZE_MULT	[159:157]	R	00015e	Max Enhanced Area=2867200KBytes=5734400sectors

Name	Field	CSD Slice	Cell Type	EXT_CSD Value	Remark
Paritioning setting	PARTITION_SETTING_COMPLETED	[155]	R/W	0h	NOT PARTITION_SETTING_COMPLETED
Partitioning support	PARTITIONING_SUPPORT	[160]	R	3h	Bit[1]=1 : Device can have enhanced technological features in partitions and user data area Bit[1]=0 : Device can not have enhanced technological features in partitions and user data area Bit[0]=1 : Device supports partitioning features Bit[0]=0 : Device does not support partitioning features
Partitions attribute	PARTITIONS_ATTRIBUTE	[156]	R/W	0h	Bit[7:5] : Reserved Bit[4]=1 : Set Enhanced attribute in General Purpose partition 4 Bit[4]=1 : Set Enhanced attribute in General Purpose partition 4 Bit[3]=1 : Set Enhanced attribute in General Purpose partition 3 Bit[2]=1 : Set Enhanced attribute in General Purpose partition 2 Bit[1]=1 : Set Enhanced attribute in General Purpose partition 1
General purpose partition size	GP_SIZE_MULT	[154:143]	R/W	0h	See EXT_CSD in spec
Enhanced user data area size	ENH_SIZE_MULT	[142:140]	R/W	0h	See EXT_CSD in spec
Enhanced user data start address	ENH_START_ADDR	[139:136]	R/W	0h	See EXT_CSD in spec & See EXT_CSD.txt
Reserved		[135]			
Bad Block management mode	SEC_BAD_BLK_MGMNT	[134]	R/W	0h	(Default) Feature Disabled
Reserved		[133:0]			

4.5 RCA (Relative Card Address)

The writable 16-bit relative card address (RCA) register carries the card address assigned by the host during the ca identification. This address is used for the addressed host-card communication after the card identification procedure. Tl default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7

4.6 DSR (Driver Stage Register)

Not support.

5. Connection Guide

Figure 22: Connection Guide Drawing

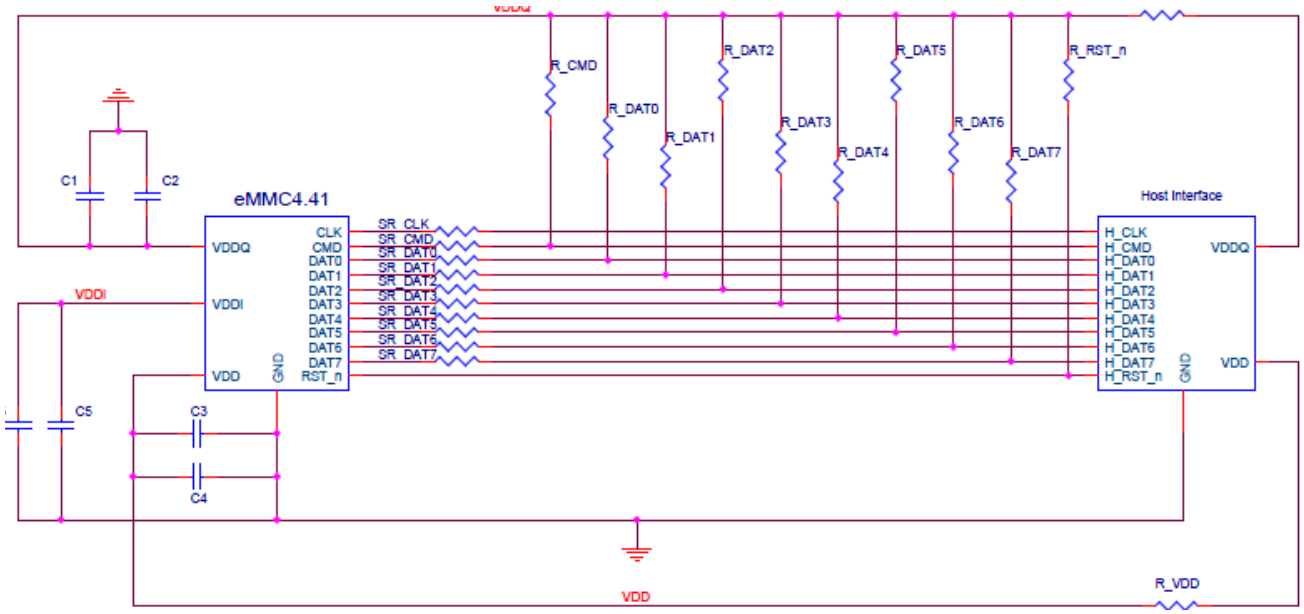


Table 29: Connection Guide Specification

Parameter	Symbol	Min	Max	Recommend	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	100	10	kohm	Pull-up resistance should be put on CMD line to prevent bus floating.
Pull-up resistance for DAT0	R_{DAT}	10	100	50	kohm	Pull-up resistance should be put on DAT line to prevent bus floating.
Pull-up resistance for RST_n	R_{RST_n}	10	100	TBD	kohm	It is not necessary to put pull-up resistance on RSTn line if host does not use H/W reset. (Extended CSD register [162] = 0b)
Serial resistance on CLDm	R_CLK	0	50	27	ohm	To reduce overshooting/undershooting and ringing.
V_{CCQ} Capacitor value	C1 & C2	2+0.2	TBD	2+0.2	uF	Coupling cap should be connected with V_{CCQ} and V_{SSQm} as closely possible.
V_{CC} Capacitor value(≤8GB)	C3 & C4	4.7+0.2	TBD	4.7+0.2	uF	Coupling cap should be connected with Vcc and Vssm as closely possible.
V_{CC} Capacitor value(>8GB)					uF	
V_{DDi} capacitor value	C5 & C6	1+0.2	TBD	1+0.2	uF	Coupling cap should be connected with V_{DDi} and Vssm as closely possible.

2Gb (64Mbx32) Mobile DDR B-Die

DESCRIPTION

The SK hynix mobile DDR SDRAMs is 2,147,483,648-bit CMOS Low Power Double Data Rate Synchronous DRAM (Mobile DDR SDRAM), ideally suited for mobile applications which use the battery such as PDAs, 2.5G and 3G cellular phones with internet access and multimedia capabilities, mini-notebook, hand-held PCs. It is organized as 4banks of 16,777,216x32.

The SK hynix mobile DDR SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2*n* prefetch architecture with an interface designed to transfer two data per clock cycle at the I/O pins.

The SK hynix mobile DDR SDRAM offers fully synchronous operations referenced to both rising and falling edges of the clock. While all address and control inputs are latched on the rising edges of the CK (Mobile DDR SDRAM operates from a differential clock*: the crossing of CK going HIGH and* $\overline{CK}$ *going LOW is referred to as the positive edge of CK*), data, data strobe and data mask inputs are sampled on both rising and falling edges of it (*Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK*). The data paths are internally pipelined and 2-bit prefetched to achieve high bandwidth. All input voltage levels are compatible with LVCMOS.

Read and write accesses to the Low Power DDR SDRAM (Mobile DDR SDRAM) are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The SK hynix mobile DDR SDRAM provides for programmable read or write bursts of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDRAM, the pipelined and multibank architecture of Low Power DDR SDRAM (Mobile DDR SDRAM) allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation times.

The SK hynix mobile DDR SDRAM also provides for special programmable Self Refresh options which are Partial Array Self Refresh (full, half and quarter array) and Temperature Compensated Self Refresh.

A burst of Read or Write cycles in progress can be interrupted and replaced by a new burst Read or Write command on any cycle (this pipelined design is not restricted by a 2N rule). Only Read bursts in progress with auto precharge disabled can be terminated by a burst terminate command. Burst Terminate command is undefined and should not be used for Read with Autoprecharge enabled and for Write bursts.

The SK hynix mobile DDR SDRAM has the special Low Power function of Auto TCSR (Temperature Compensated Self Refresh) to reduce self refresh current consumption. Since an internal temperature sensor is implemented, it enables to automatically adjust refresh rate according to temperature without external EMRS command.

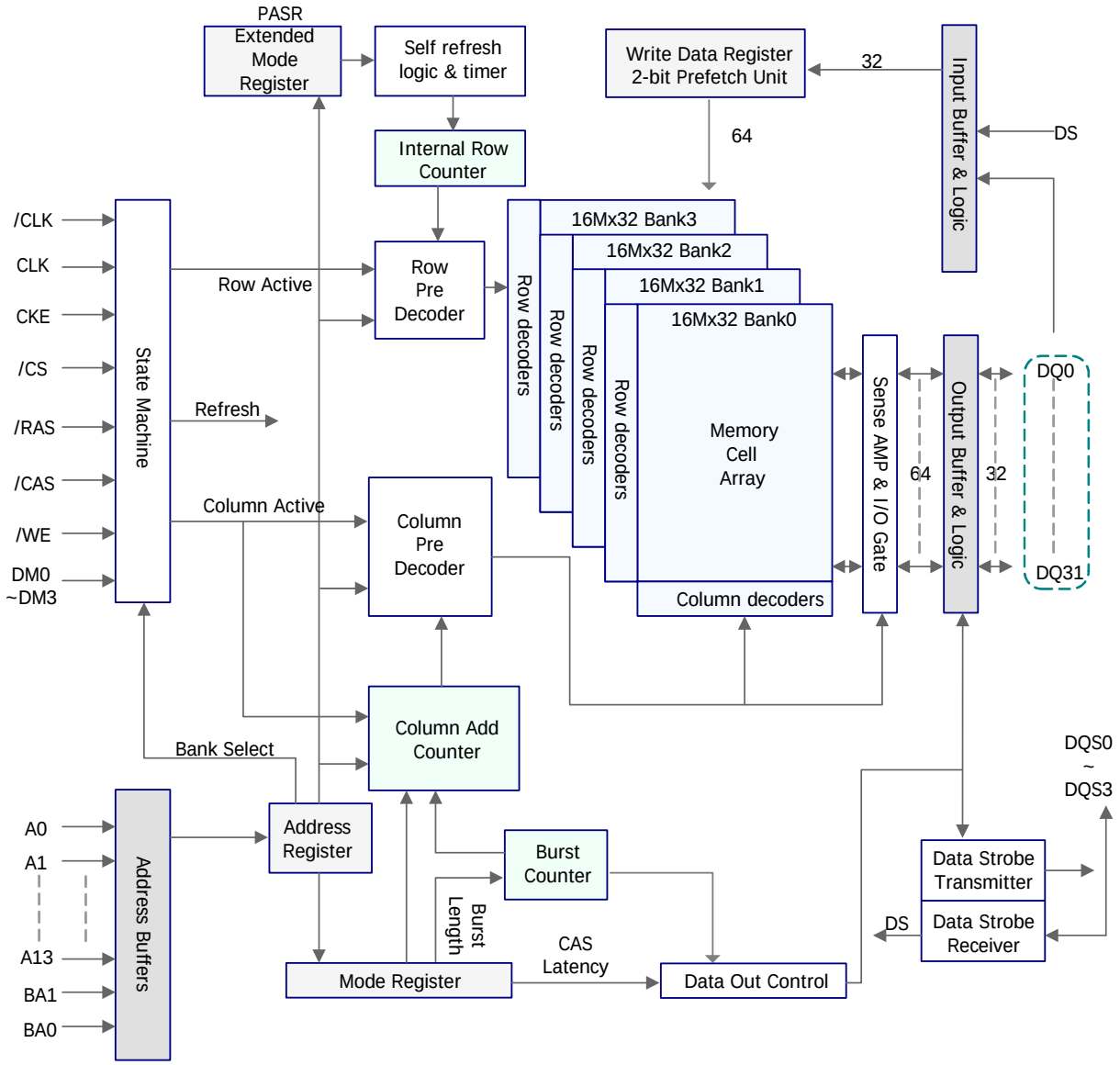
All inputs are LVCMOS compatible. Devices will have a V_{DD} and V_{DDQ} supply of 1.8V (nominal).

Mobile DDR SDRAM PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CK, $\overline{CK}$	INPUT	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	INPUT	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously.
$\overline{CS}$	INPUT	Chip Select: $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	INPUT	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered
BA0, BA1	INPUT	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is to be loaded during a MODE REGISTER SET command (MRS, EMRS).
A0 ~ A13	INPUT	Address inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during a MODE REGISTER SET command. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. Row Address: A0 ~ A13 Column Address: A0 ~ A9 Auto-precharge flag: A10
DQ0 ~ DQ31	I/O	Data Bus: data input / output pin
DM0 ~ DM3	INPUT	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled. HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Data Mask pins include dummy loading internally, to match the DQ and DQS loading. For x32 devices, DM0 corresponds to the data on DQ0-DQ7, DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, and DM3 corresponds to the data on DQ24-DQ31.
DQS0 ~ DQS3	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, center-aligned with write data. Used to capture write data. For x32 device, DQS0 corresponds to the data on DQ0-DQ7, DQS1 corresponds to the data on DQ8-DQ15, DQS2 corresponds to the data on DQ16-DQ23, and DQS3 corresponds to the data on DQ24-DQ31.
V_{DD}	SUPPLY	Power supply
V_{SS}	SUPPLY	Ground
V_{DDQ}	SUPPLY	I/O Power supply
V_{SSQ}	SUPPLY	I/O Ground
NC	-	No Connect: No internal electrical connection is present.

FUNCTIONAL BLOCK DIAGRAM

16Mbit x 4banks x 32 I/O Mobile DDR SDRAM



REGISTER DEFINITION I

Mode Register Set (MRS) for Mobile DDR SDRAM

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	0	CAS Latency			BT	Burst Length		

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Reserved	Reserved

REGISTER DEFINITION II

Extended Mode Register Set (EMRS) for Mobile DDR SDRAM

BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	DS			0	0	PASR		

DS (Drive Strength)

A7	A6	A5	Drive Strength
0	0	0	Full (Default)
0	0	1	Half
0	1	0	Quarter
0	1	1	Octant
1	0	0	Three-Quarters

PASR (Partial Array Self Refresh)

A2	A1	A0	Self Refresh Coverage
0	0	0	All Banks (Default)
0	0	1	Half of Total Bank (BA1=0)
0	1	0	Quarter of Total Bank (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

COMMAND TRUTH TABLE

Function	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10 / AP	ADDR	Note
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (Select Bank and activate Row)	L	L	H	H	V	Row	Row	
READ (Select bank and column and start read burst)	L	H	L	H	V	L	Col	
READ with AP (Read Burst with Autoprecharge)	L	H	L	H	V	H	Col	3
WRITE (Select bank and column and start write burst)	L	H	L	L	V	L	Col	
WRITE with AP (Write Burst with Autoprecharge)	L	H	L	L	V	H	Col	3
BURST TERMINATE	L	H	H	L	X	X	X	4, 5
PRECHARGE (Deactivate Row in selected bank)	L	L	H	L	V	L	X	6
PRECHARGE ALL (Deactivate rows in all Banks)	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	7,8,9
MODE REGISTER SET	L	L	L	L	V	Op code		10

DM TRUTH TABLE

Function	DM	DQ	Note
Write Enable	L	Valid	11
Write Inhibit	H	X	11

Note:
1. All states and sequences not shown are illegal or reserved.
2. DESLECT and NOP are functionally interchangeable.
3. Autoprecharge is non-persistent. A10 High enables Autoprecharge, while A10 Low disables Autoprecharge
4. Burst Terminate applies to only Read bursts with auto precharge disabled. This command is undefined and should not be used for Read with Autoprecharge enabled, and for Write bursts.
5. This command is BURST TERMINATE if CKE is High.
6. If A10 is low, bank address determines which bank is to be precharged. If A10 is high, all banks are precharged and BA0-BA1 are don't care.
7. This command is AUTO REFRESH if CKE is High, and SELF REFRESH if CKE is low.
8. All address inputs and I/O are "don't care" except for CKE. Internal refresh counters control Bank and Row addressing.
9. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10. BA0 and BA1 value select among MRS, EMRS.
11. Used to mask write data, provided coincident with the corresponding data.
12. CKE is HIGH for all commands shown except SELF REFRESH.

CKE TRUTH TABLE

CKEn-1	CKEn	Current State	COMMAND*n*	ACTION*n*	Note
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5,6,8
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5,7,9
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh entry	
H	H	See the other Truth Tables			

Note:
1. CKEn is the logic state of CKE at clock edge *n*; CKE*n*-1 was the state of CKE at the previous clock edge.
2. Current state is the state of LP DDR immediately prior to clock edge *n*.
3. COMMAND*n* is the command registered at clock edge n, and ACTION*n* is the result of COMMAND*n*.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (t_{XP}) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (t_{XSR}) should elapse before a command other than NOP or DESELECT is issued.
8. The clock must toggle at least one time during the t_{XP} period.
9. The clock must toggle at least once during the t_{XSR} time.

CURRENT STATE BANK*n* TRUTH TABLE (COMMAND TO BANK *n*)

Current State	Command					Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	L	L	H	H	ACTIVE	Select and activate row	
	L	L	L	H	AUTO REFRESH	Auto refresh	10
	L	L	L	L	MODE REGISTER SET	Mode register set	10
	L	L	H	H	PRECHARGE	No action if bank is idle	
Row Active	L	H	L	H	READ	Select Column & start read burst	
	L	H	L	L	WRITE	Select Column & start write burst	
	L	L	H	L	PRECHARGE	Deactivate Row in bank (or banks)	4
Read (without Auto precharge)	L	H	L	H	READ	Truncate Read & start new Read burst	5,6
	L	H	L	L	WRITE	Truncate Read & start new Write burst	5,6,13
	L	L	H	L	PRECHARGE	Truncate Read, start Precharge	
	L	H	H	L	BURST TERMINATE	Burst terminate	11
Write (without Auto precharge)	L	H	L	H	READ	Truncate Write & start new Read burst	5,6,12
	L	H	L	L	WRITE	Truncate Write & start new Write burst	5,6
	L	L	H	L	PRECHARGE	Truncate Write, start Precharge	12

Note:
1. The table applies when both CKE*n*-1 and CKE*n* are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE Burst with auto precharge is enabled.
6. The new Read or Write command could be auto precharge enabled or auto precharge disabled.
7. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met.
   No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
   Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank.
   DESELECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring

during these states. Allowable commands to the other bank are determined by its current state and Truth Table3, and according to Truth Table 4.
Precharging: Starts with the registration of a PRECHARGE command and ends when t_{RP} is met.
Once t_{RP} is met, the bank will be in the idle state.
Row Activating: Starts with registration of an ACTIVE command and ends when t_{RCD} is met.
Once t_{RCD} is met, the bank will be in the "row active" state.
Read with AP Enabled: Starts with the registration of the READ command with AUTO PRECHARGE enabled and ends when t_{RP} has been met. Once t_{RP} has been met, the bank will be in the idle state.
Write with AP Enabled: Starts with registration of a WRITE command with AUTO PRECHARGE enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

9. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied to each positive clock edge during these states.
Refreshing: Starts with registration of an AUTO REFRESH command and ends when t_{RFC} is met.
Once t_{RFC} is met, the LP DDR will be in an "all banks idle" state.
Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met.
Once t_{MRD} is met, the LP DDR will be in an "all banks idle" state.
Precharging All: Starts with the registration of a PRECHARGE ALL command and ends when t_{RP} is met.
Once t_{RP} is met, the bank will be in the idle state.
10. Not bank-specific; requires that all banks are idle and no bursts are in progress.
11. Not bank-specific. BURST TERMINATE affects the most recent READ burst, regardless of bank.
12. Requires appropriate DM masking.
13. A WRITE command may be applied after the completion of the READ burst; otherwise, a Burst terminate must be used to end the READ prior to asserting a WRITE command.

CURRENT STATE BANK*n* TRUTH TABLE (COMMAND TO BANK *m*)

Current State	Command					Action	Notes
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous Operation	
	L	H	H	H	NOP	Continue previous Operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Pre-charging	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge dis-abled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8
	L	H	L	L	WRITE	Start WRITE burst	8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge dis-abled	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	8,9
	L	H	L	L	WRITE	Start WRITE burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto precharge	L	L	H	H	ACTIVE	Activate Row	
	L	H	L	H	READ	Start READ burst	5,8
	L	H	L	L	WRITE	Start WRITE burst	5,8
	L	L	H	L	PRECHARGE	Precharge	

Note:
1. The table applies when both CKE*n*-1 and CKE*n* are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. Current State Definitions:

Idle: The bank has been precharged, and tRP has been met.
Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
Read: A READ burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.
Write: a WRITE burst has been initiated, with AUTO PRECHARGE disabled, and has not yet terminated or been terminated.

5. Read with AP enabled and Write with AP enabled: The read with Autoprecharge enabled or Write with Autoprecharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with Auto precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period, of the Read with Autoprecharge enabled or Write with Autoprecharge enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
6. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
7. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
8. READs or WRITEs listed in the Command column include READs and WRITEs with AUTO PRECHARGE enabled and READs and WRITEs with AUTO PRECHARGE disabled.
9. Requires appropriate DM masking.
10. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Operating Case Temperature	TC	-30 ~ 85	°C
Storage Temperature	TSTG	-55 ~ 150	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.3 ~ VDDQ+0.3	V
Voltage on VDD relative to VSS	VDD	-0.3 ~ 2.7	V
Voltage on VDDQ relative to VSS	VDDQ	-0.3 ~ 2.7	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	0.7	W

AC and DC OPERATING CONDITIONS

OPERATING CONDITION

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	VDD	1.7	1.8	1.95	V	1
I/O Supply Voltage	VDDQ	1.7	1.8	1.95	V	1
Operating Case Temperature	TC	-30		85	°C	

CLOCK INPUTS (CK, $\overline{CK}$)

Parameter	Symbol	Min	Max	Unit	Note
DC Input Voltage	VIN	-0.3	VDDQ+0.3	V	
DC Input Differential Voltage	VID(DC)	0.4*VDDQ	VDDQ+0.6	V	2
AC Input Differential Voltage	VID(AC)	0.6*VDDQ	VDDQ+0.6	V	2
AC Differential Crosspoint Voltage	VIX	0.4*VDDQ	0.6*VDDQ	V	3

Address And Command Inputs(A0~An, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)

Parameter	Symbol	Min	Max	Unit	Note
Input High Voltage	VIH	0.8*VDDQ	VDDQ+0.3	V	
Input Low Voltage	VIL	-0.3	0.2*VDDQ	V	

Data Inputs (DQ, DM, DQS)

Parameter	Symbol	Min	Max	Unit	Note
DC Input High Voltage	VIHD(DC)	0.7*VDDQ	VDDQ+0.3	V	
DC Input Low Voltage	VILD(DC)	-0.3	0.3*VDDQ	V	
AC Input High Voltage	VIHD(AC)	0.8*VDDQ	VDDQ+0.3	V	
AC Input Low Voltage	VILD(AC)	-0.3	0.2*VDDQ	V	

Data Outputs (DQ, DQS)

Parameter	Symbol	Min	Max	Unit	Note
DC Output High Voltage (IOH = -0.1mA)	VOH	0.9*VDDQ	-	V	
DC Output Low Voltage (IOL = 0.1mA)	VOL	-	0.1*VDDQ	V	

Leakage Current

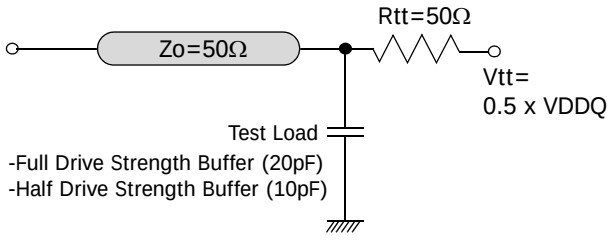
Parameter	Symbol	Min	Max	Unit	Note
Input Leakage Current	ILI	-1	1	uA	4
Output Leakage Current	ILO	-1.5	1.5	uA	5

Note:
1. All voltages are referenced to VSS = 0V and VSSQ must be same potential and VDDQ must not exceed the level of VDD.
2. VID(DC) and VID(AC) are the magnitude of the difference between the input level on CK and the input level on CK.
3. The value of VIX is expected to be 0.5*VDDQ and must track variations in the DC level of the same.
4. VIN = 0 to 1.8V. All other pins are not tested under VIN=0V.
5. DOUT is disabled. VOUT= 0 to 1.95V.

AC OPERATING TEST CONDITION

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	VIH / VIL	0.8*VDDQ/0.2*VDDQ	V	
Input Timing Measurement Reference Level Voltage	Vtrip	0.5*VDDQ	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level Voltage	Voutref	0.5*VDDQ	V	
Output Load Capacitance for Access Time Measurement	CL		pF	1

Note: 1. The circuit shown on the right represents the timing load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production (generally a coaxial transmission line terminated at the tester electronics). For the half strength driver with a nominal 10pF load parameters tAC and tQH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design and characterization. Use of IBIS or other simulation tools for system design validation is suggested.



Input / Output Capacitance

Parameter	Symbol	Speed		Unit	Note
		Min	Max		
Input capacitance, CK, $\overline{CK}$	CCK	1.5	3.5	pF	
Input capacitance, all other input-only pins	CI	1.5	3.0	pF	
Input/output capacitance, DQ, DM, DQS	CIO	2.0	4.5	pF	4

Note:
1. These values are guaranteed by design and are tested on a sample base only.
2. These capacitance values are for single monolithic devices only. Multiple die packages will have parallel capacitive loads.
3. Input capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. VDD, VDDQ are applied and all other pins (except the pin under test) floating. DQ's should be in high impedance state. This may be achieved by pulling CKE to low level.
4. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS and DM in the system.

Mobile DDR OUTPUT SLEW RATE CHARACTERRISTICS

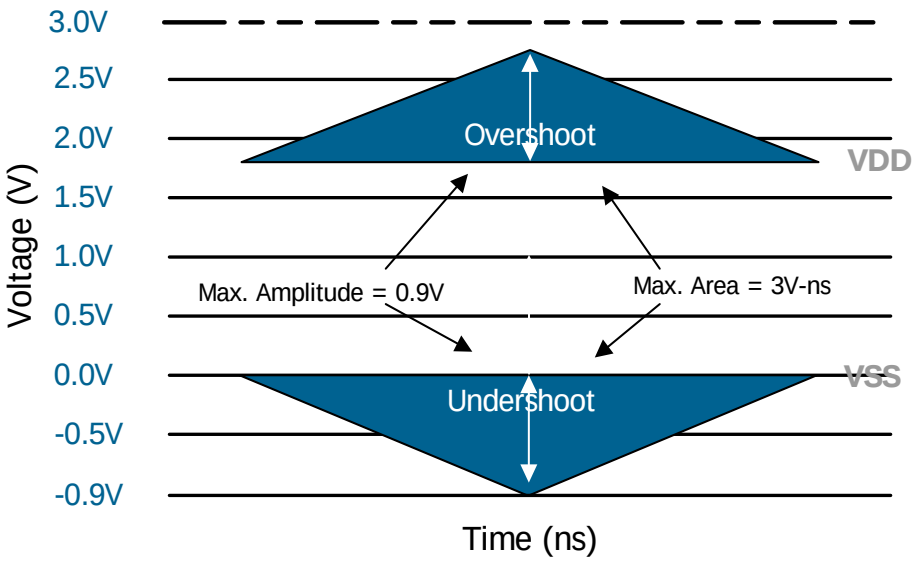
Parameter	Min	Max	Unit	Note
Pull-up and Pull-Down Slew Rate for Full Strength Driver	0.7	2.5	V/ns	1, 2
Pull-up and Pull-Down Slew Rate for Half Strength Driver	0.3	1.0	V/ns	1, 2
Output Slew Rate Matching ratio (Pull-up to Pull-down)	0.7	1.4	-	3

Note:
1. Measured with a test load of 20pF connected to VSSQ
2. Output slew rate for rising edge is measured between VILD(DC) to VIHD(AC) and for falling edge between VIHD(DC) to VILD(AC)
3. The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

Mobile DDR AC OVERSHOOT / UNDERSHOOT SPECIFICATION

Parameter	Specification
Maximum peak amplitude allowed for overshoot	0.9V
Maximum peak amplitude allowed for undershoot	0.9V
The area between overshoot signal and VDD must be less than or equal to	3V-ns
The area between undershoot signal and GND must be less than or equal to	3V-ns

Note:
1. This specification is intended for devices with no clamp protection and is guaranteed by design.



DC CHARACTERISTICS (Symbols)

Parameter	Symbol
Operating one bank active-precharge current	IDD0
Precharge power-down standby current	IDD2P
Precharge power-down standby current with clock stop	IDD2PS
Precharge non power-down standby current	IDD2N
Precharge non power-down standby current with clock stop	IDD2NS
Active power-down standby current	IDD3P
Active power-down standby current with clock stop	IDD3PS
Active non power-down standby current	IDD3N
Active non power-down standby current with clock stop	IDD3NS
Operating burst read current	IDD4R
Operating burst write current	IDD4W
Auto Refresh Current	IDD5
Self Refresh Current	IDD6

DC CHARACTERISTICS

Symbol	Test Condition	Max					Unit	Note
		DDR 400	DDR 370	DDR 333	DDR 266	DDR 200		
IDD0	tRC = tRC(min); tCK = tCK(min); CKE is HIGH; CS is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE	75	70	65	60	55	mA	1
IDD2P	all banks idle; CKE is LOW; CS is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	0.9					mA	
IDD2PS	all banks idle; CKE is LOW; CS is HIGH; CK = LOW; CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	0.9					mA	
IDD2N	all banks idle; CKE is HIGH; CS is HIGH, tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	7					mA	
IDD2NS	all banks idle; CKE is HIGH; CS is HIGH; CK = LOW; CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	5						
IDD3P	one bank active; CKE is LOW; CS is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	5					mA	
IDD3PS	one bank active; CKE is LOW; CS is HIGH; CK = LOW; CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	4						
IDD3N	one bank active; CKE is HIGH; CS is HIGH; tCK = tCK(min); address and control inputs are SWITCHING; data bus inputs are STABLE	10					mA	
IDD3NS	one bank active; CKE is HIGH; CS is HIGH; CK = LOW; CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	8					mA	
IDD4R	one bank active; BL=4; CL=3; tCK=tCK(min); continuous read bursts; IOUT=0mA; address inputs are SWITCHING, 50% data change each burst transfer	100	95	90	80	70	mA	1
IDD4W	one bank active; BL=4; tCK=tCK(min); continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer	90	85	80	70	60	mA	
IDD5	tRC=tRFC; tCK=tCK(min); burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	150					mA	tRFC= 138ns
IDD6	CKE is LOW; CK=LOW; CK=HIGH; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE	See Next Page					uA	2

Note:
1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is 1V/ns
3. Definitions for IDD:
   LOW is defined as VIN £ 0.1 * VDDQ
   HIGH is defined as VIN ³ 0.9 * VDDQ
   STABLE is defined as inputs stable at a HIGH or LOW level
   SWITCHING is defined as
   - address and command: inputs changing between HIGH and LOW once per two clock cycles
   - data bus inputs: DQ changing between HIGH and LOW once per clock cycle
     DM and DQS are STABLE
4. All IDD values are guaranteed by full range of operating voltage and temperature.
   VDD, VDDQ = 1.7V ~ 1.95V. Temperature = -30oC ~ +85oC

DC CHARACTERISTICS - IDD6

Temp. (°C)	Memory Array			Unit
	4 Banks	2 Banks	1 Bank	
45	TBD	TBD	TBD	uA
85	2000	1400	1200	uA

Note:

1. Related numerical values in this 45°C are examples for reference sample value only.
2. With a on-chip temperature sensor, auto temperature compensated self refresh will automatically adjust the interval of self-refresh operation according to case temperature variations.
3. IDD6 85°C are guaranteed. IDD6 45°C are typical value.

AC CHARACTERISTICS (Symbols)

Parameter		Symbol	Unit
DQ Output Access Time (from CK, $\overline{CK}$)		tAC	ns
DQS Output Access Time (from CK, $\overline{CK}$)		tDQSCK	ns
Clock High-level Width		tCH	tCK
Clock Low-level Width		tCL	tCK
Clock Half Period		tHP	ns
System Clock Cycle Time	CL = 3	tCK3	ns
	CL = 2	tCK2	ns
DQ and DM Input Setup Time		tDS	ns
DQ and DM Input Hold Time		tDH	ns
DQ and DM Input Pulse Width		tDIPW	ns
Address and Control Input Setup Time		tIS	ns
Address and Control Input Hold Time		tIH	ns
Address and Control Input Pulse Width		tIPW	ns
DQ & DQS Low-impedance time from CK, $\overline{CK}$		tLZ	ns
DQ & DQS High-impedance time from CK, $\overline{CK}$		tHZ	ns
DQS - DQ Skew		tDQSQ	ns
DQ / DQS output hold time from DQS		tQH	ns
Data Hold Skew Factor		tQHS	ns
Write Command to 1st DQS Latching Transition		tDQSS	tCK
DQS Input High-Level Width		tDQSH	tCK
DQS Input Low-Level Width		tDQSL	tCK
DQS Falling Edge of CK Setup Time		tDSS	tCK
DQS Falling Edge Hold Time from CK		tDSH	tCK
MODE REGISTER SET Command Period		tMRD	tCK
Write Preamble Setup Time		tWPRES	ns
Write Postamble		tWPST	tCK
Write Preamble		tWPRE	tCK
Read Preamble	CL = 3	tRPRE3	tCK
	CL = 2	tRPRE2	tCK
Read Postamble		tRPST	tCK
ACTIVE to PRECHARGE Command Period		tRAS	ns
ACTIVE to ACTIVE Command Period		tRC	ns
AUTO REFRESH to ACTIVE/AUTO REFRESH Command Period		tRFC	ns
ACTIVE to READ or WRITE Delay		tRCD	ns
PRECHARGE Command Period		tRP	ns
ACTIVE Bank *A* to ACTIVE Bank *B* Delay		tRRD	ns
WRITE Recovery Time		tWR	ns
Auto Precharge Write Recovery + Precharge Time		tDAL	tCK
Internal Write to Read Command Delay		tWTR	tCK
Self Refresh Exit to next valid Command Delay		tXSR	ns
Exit Power Down to next valid Command Delay		tXP	ns
CKE *min*. Pulse Width (High and Low)		tCKE	tCK
Average Periodic Refresh Interval		tREFI	us
Refresh Period		tREF	ms

AC CHARACTERISTICS (AC operating conditions unless otherwise noted) (Sheet 1 of 2)

Symbol	DDR400		DDR370		DDR333		DDR266		DDR200		Unit	Note
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tAC	2.0	5.0	2.0	5.0	2.0	5.0	2.5	6.0	2.5	7.0	ns	
tDQSCK	2.0	5.0	2.0	5.0	2.0	5.0	2.5	6.0	2.5	7.0	ns	
tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
tHP	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	tCL, tCH (Min)	-	ns	1,2
tCK3	5	-	5.4	-	6.0	-	7.5	-	10	-	ns	3
tCK2	12		12		12		12	-	15	-	ns	
tDS	0.48		0.54		0.6		0.8		1.1		ns	4,5,6
tDH	0.48		0.54		0.6		0.8		1.1		ns	4,5,6
tDIPW	1.8	-	1.8	-	1.8	-	1.8	-	2.2	-	ns	7
tIS	0.9		1.0		1.1		1.3		1.5		ns	6,8,9
tIH	0.9		1.0		1.1		1.3		1.5		ns	6,8,9
tIPW	2.3	-	2.3	-	2.3	-	2.6	-	3.0	-	ns	7
tLZ	1.0	-	1.0	-	1.0	-	1.0	-	1.0	-	ns	10
tHZ		5.0		5.0		5.0		6.0		7.0	ns	10
tDQSQ		0.4		0.45		0.5		0.6		0.7	ns	11
tQH	tHP - tQHS		tHP - tQHS		tHP - tQHS		tHP - tQHS		tHP - tQHS		ns	2
tQHS		0.5		0.5		0.65		0.75		1.0	ns	2
tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
tDQSH	0.4		0.4		0.4		0.4		0.4		tCK	
tDQSL	0.4		0.4		0.4		0.4		0.4		tCK	
tDSS	0.2		0.2		0.2		0.2		0.2		tCK	
tDSH	0.2		0.2		0.2		0.2		0.2		tCK	
tMRD	2	-	2	-	2	-	2	-	2	-	tCK	
tWPRES	0	-	0	-	0	-	0	-	0	-	ns	12
tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	13
tWPRE	0.25	-	0.25	-	0.25	-	0.25	-	0.25	-	tCK	
tRPRE3	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	14
tRPRE2	0.5	1.1	0.5	1.1	0.5	1.1	0.5	1.1	0.5	1.1	tCK	14
tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
tRAS	40	70,000	42	70,000	42	70,000	45	70,000	50	70,000	ns	
tRC	tRAS +tRP	-	tRAS +tRP	-	tRAS +tRP	-	tRAS +tRP	-	tRAS +tRP	-	ns	
tRFC	90	-	90	-	90	-	90	-	90	-	ns	
tRCD	15	-	16.2	-	18	-	22.5	-	30	-	ns	15
tRP	15	-	16.2	-	18	-	22.5	-	30	-	ns	15
tRRD	10	-	10.8	-	12	-	15	-	15	-	ns	
tWR	15	-	15	-	15	-	15	-	15	-	ns	
tDAL	(tWR/tCK) + (tRP/tCK)										tCK	16
tWTR	2	-	2	-	1	-	1	-	1	-	tCK	

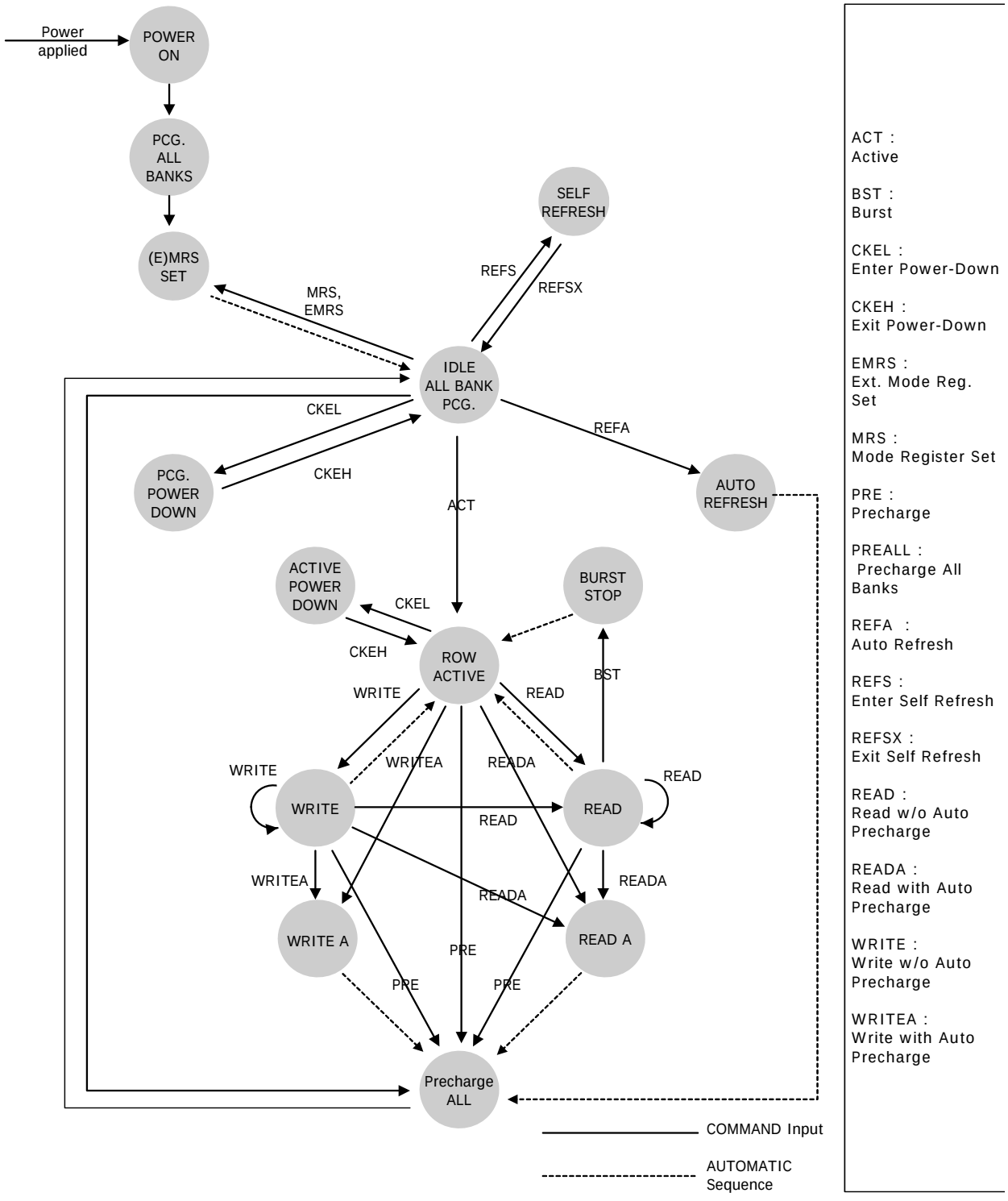
AC CHARACTERISTICS (AC operating conditions unless otherwise noted) (Sheet 2 of 2)

Symbol	DDR400		DDR370		DDR333		DDR266		DDR200		Unit	Note
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
tXSR	120	-	120	-	120	-	120	-	120	-	ns	
tXP	1CLK	-	1CLK	-	1CLK	-	1CLK	-	1CLK	-	ns	19
tCKE	1	-	1	-	1	-	1	-	1	-	tCK	
tREFI	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	us	17
tREF	-	64	-	64	-	64	-	64	-	64	ms	

Note:
1. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)
2. tQH = tHP - tQHS, where tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCL, tCH). tQHS accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
3. The only time that the clock frequency is allowed to change is during clock stop, power-down or self-refresh modes.
4. The transition time for DQ, DM and DQS inputs is measured between VIL(DC) to VIH(AC) for rising input signals, and VIH(DC) to VIL(AC) for falling input signals.
5. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.
6. Input slew rate ³ 1.0 V/ns.
7. These parameters guarantee device timing but they are not necessarily tested on each device.
8. The transition time for address and command inputs is measured between VIH and VIL.
9. A CK/CK differential slew rate of 2.0 V/ns is assumed for this parameter.
10. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).
11. tDQSQ consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
12. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
13. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
14. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
15. Speed bin (CL-tRCD-tRP) = 3-3-3 for DDR400, DDR200, DDR266, DDR333 and DDR 370
16. In case of above 33MHz (tCK=30ns) condition, tDAL should be minimum of 3*tCK.
    tDAL = (tWR/tCK) + (tRP/tCK): for each of the terms above, if not already an integer, round to the next higher integer.
17. A maximum of eight Refresh commands can be posted to any given Low Power DDR SDRAM (Mobile DDR SDRAM), meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8*tREFI.
18. All AC parameters are guaranteed by full range of operating voltage and temperature.
    VDD, VDDQ = 1.7V ~ 1.95V. Temperature = -30oC ~ 85oC
19. There must be at least one clock pulse during the tXP period. Please refer to the 'Power Down Mode' Section.

Mobile DDR SDRAM OPERATION

State Diagram



DESELECT

The DESELECT function ($\overline{CS}$ = High) prevents new commands from being executed by the Mobile DDR SDRAM. The Mobile DDR SDRAM is effectively deselected. Operations already in progress are not affected.

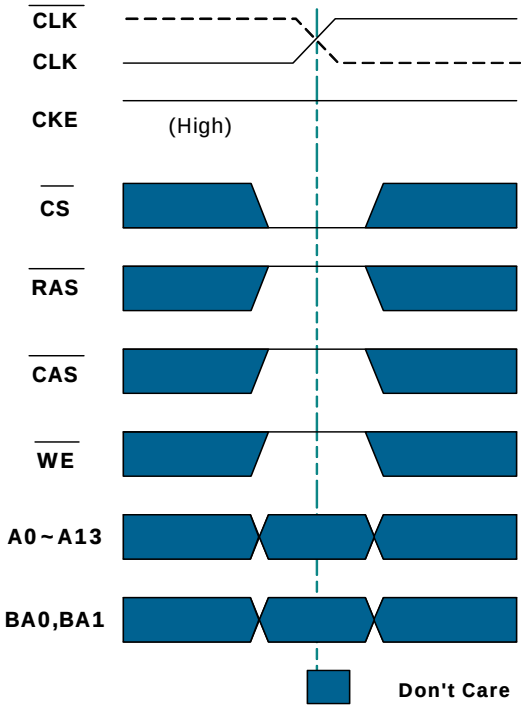
NO OPERATION

The NO OPERATION (NOP) command is used to perform a NOP to a Mobile DDR SDRAM that is selected ($\overline{CS}$ = Low). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected. (see to next figure)

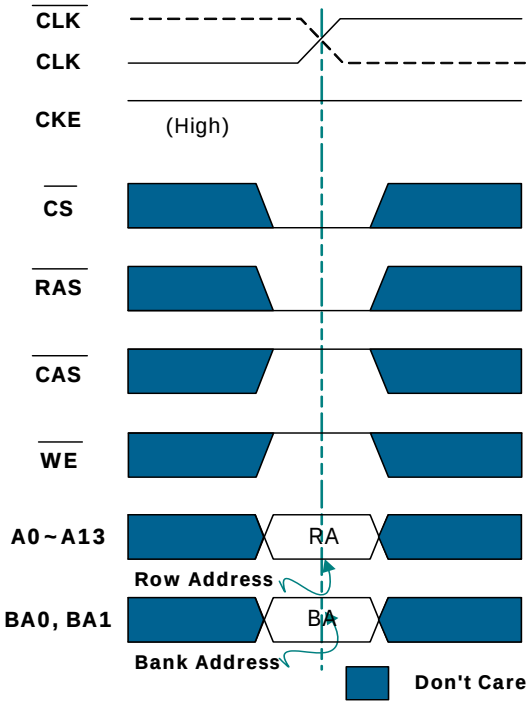
ACTIVE

The Active command is used to activate a row in a particular bank for a subsequent Read or Write access. The value of the BA0,BA1 inputs selects the bank, and the address provided on A0-A13 selects the row. (see to next figure)

Before any READ or WRITE commands can be issued to a bank within the Mobile DDR SDRAM, a row in that bank must be opened. This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.
The row remains active until a PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command is issued to the bank.
A PRECHARGE (or READ with AUTO PRECHARGE or WRITE with AUTO PRECHARGE) command must be issued before opening a different row in the same bank.



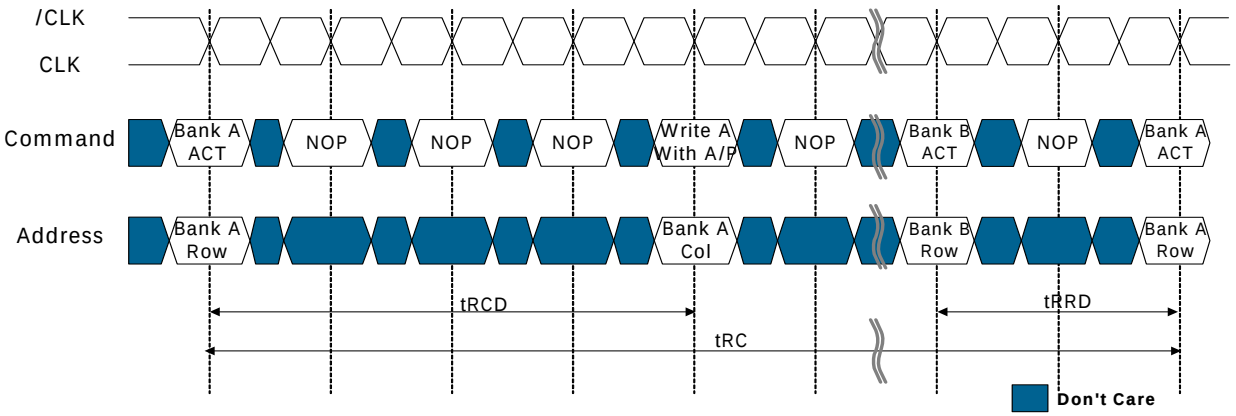
NOP Command



ACTIVE Command

Once a row is Open (with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (*MIN*) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been closed (precharge). The minimum time interval between successive ACTIVE commands to the same bank is defined by tRC.
A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by tRRD.



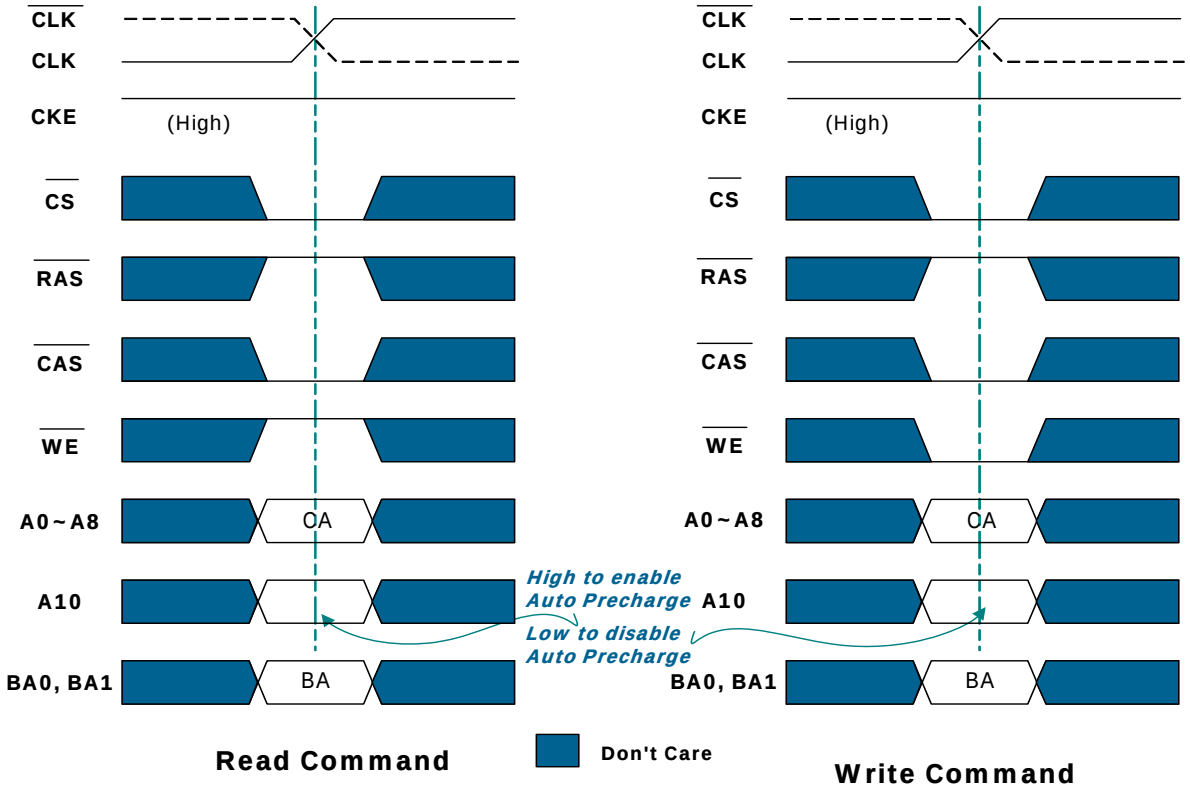
Once a row is Open(with an ACTIVE command) a READ or WRITE command may be issued to that row, subject to the tRCD specification. tRCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered.

READ / WRITE COMMAND

The READ command is used to initiate a Burst Read to an active row. The value of BA0 and BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent access. The valid data-out elements will be available CAS latency after the READ command is issued. The Mobile DDR drives the DQS during read operations. The initial low state of the DQS is known as the read preamble and the last data-out element is coincident with the read postamble. DQS is edge-aligned with read data. Upon completion of a burst, assuming no new READ commands have been initiated, the I/O's will go high-Z.

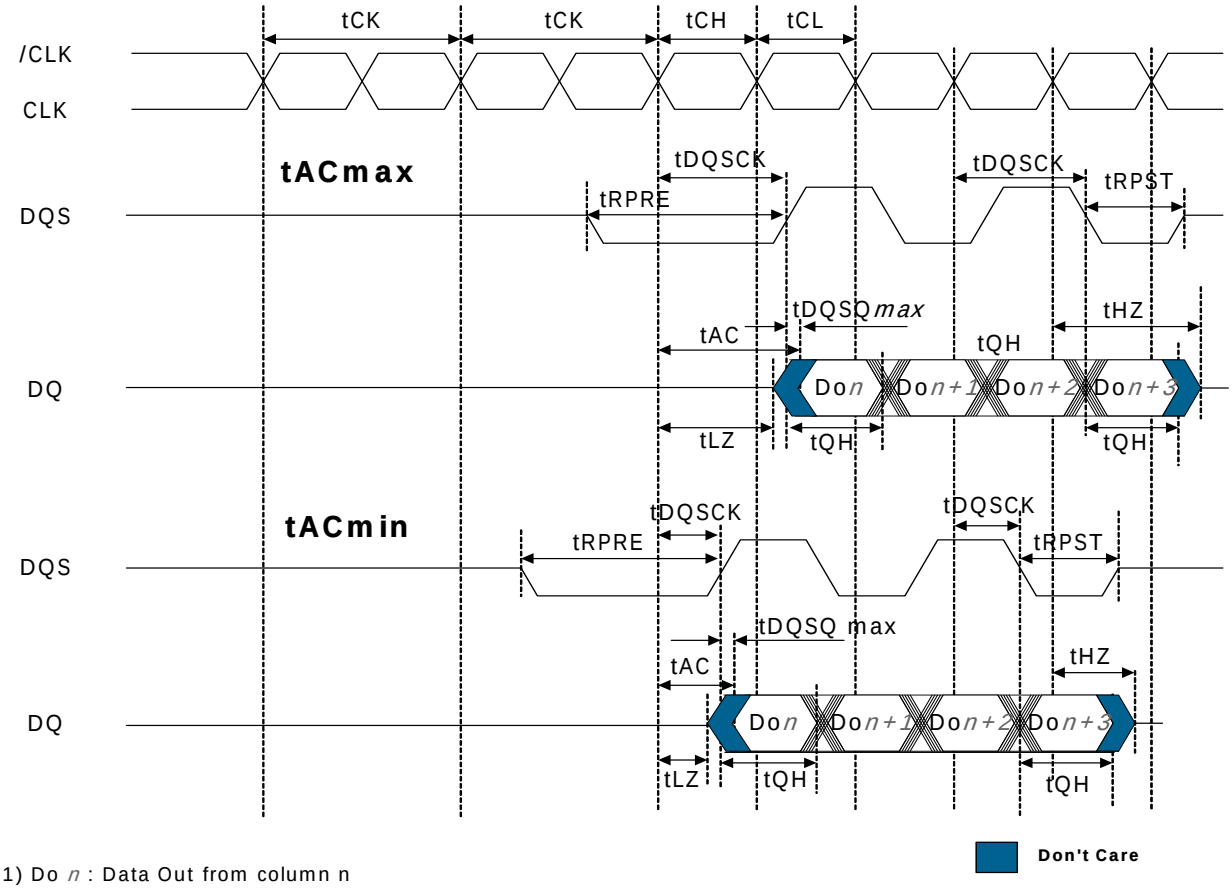
The WRITE command is used to initiate a Burst Write access to an active row. The value of BA0, BA1 selects the bank and address inputs select the starting column location.
The value of A10 determines whether or not auto precharge is used.If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent access. Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered low, the corresponding data will be written to the memory; if the DM signal is registered high, the corresponding data-inputs will be ignored, and a write will not be executed to that byte/column location. The memory controller drives the DQS during write operations. The initial low state of the DQS is known as the write preamble and the low state following the last data-in element is write postamble. Upon completion of a burst, assuming no new commands have been initiated, the I/O's will stay high-Z and any additional input data will be ignored.

When READ or WRITE command issues, the A0~A8 (column address) are provided if only 2KBytes page size as shown below figure. If the page size is 4KBytes, the A0~A9 (column address) are provided.



READ

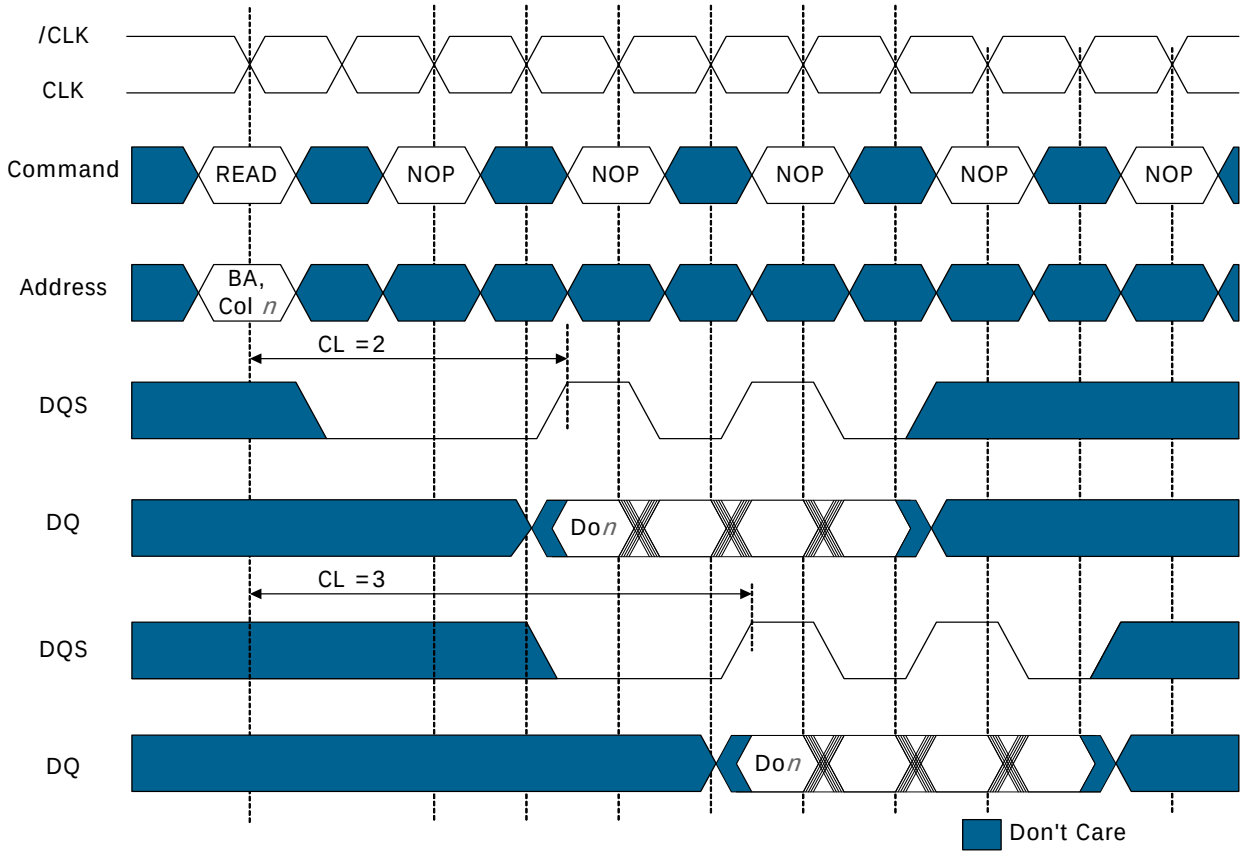
The basic Read timing parameters for DQ are shown next figure (Basic Read Timing Parameters). They apply to all Read operations. During Read bursts, DQS is driven by the Mobile DDR SDRAM along with the output data. The initial Low state of the DQS is known as the read preamble; the Low state coincident with last data-out element is known as the read postamble.



1) Do *n* : Data Out from column n
2) All DQ are vaild tAC after the CK edge
   All DQ are vaild tDQSQ after the DQS edge, regardless of tAC

Basic Read Timing Parameters

The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. This is shown in next figure with a CAS latency of 2 and 3.
Upon completion of a read burst, assuming no other READ command has been initiated, the DQ will go to High-Z.

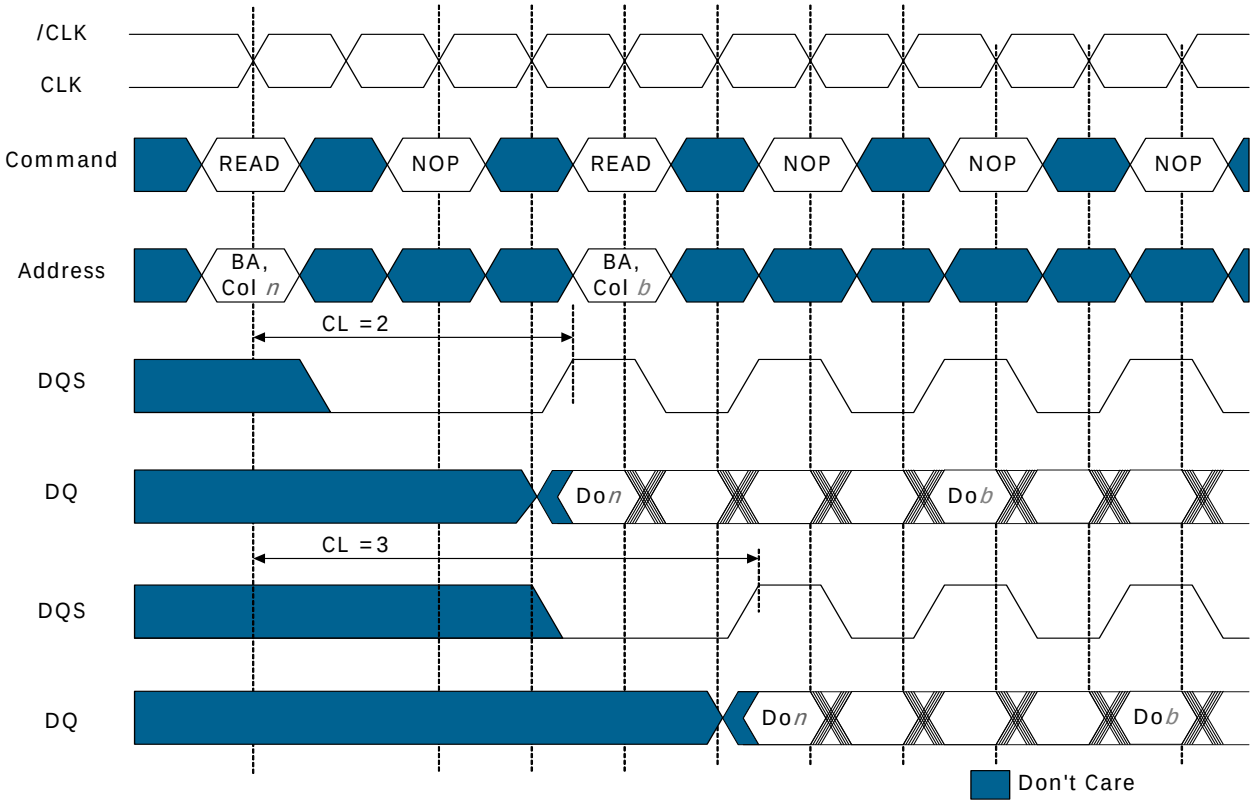


1) Do*n* : Data out from column n
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 4; 3 subseqnent elements of Data Out appear in the programmed order following Do *n*
4) Shown with nominal tAC, tDQSCK and tDQSQ

Read Burst Showing CAS Latency

READ to READ

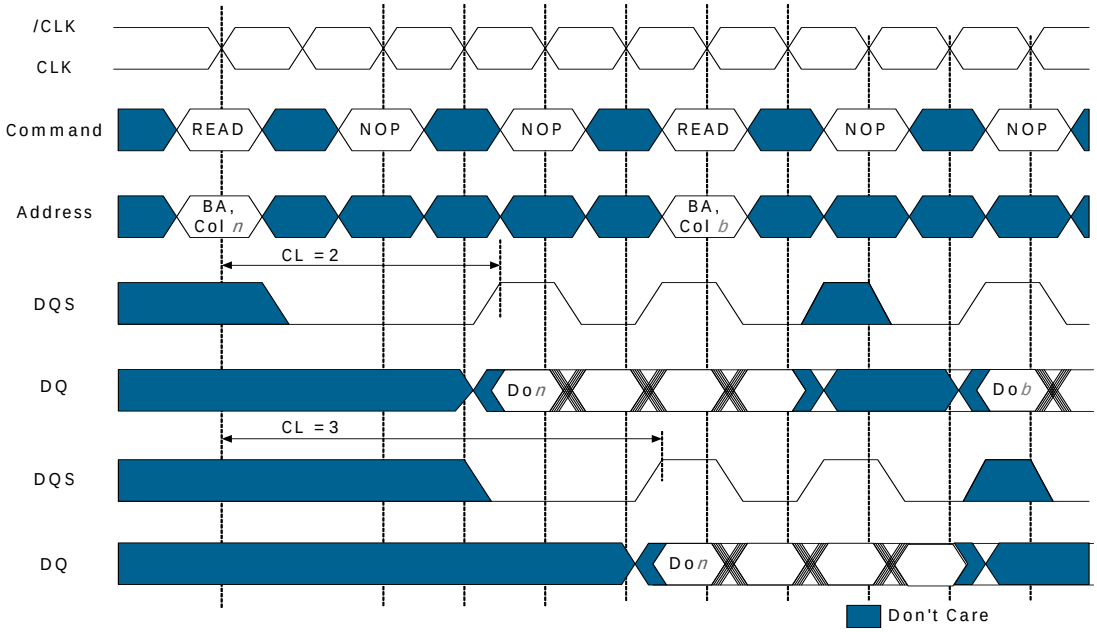
Data from a read burst may be concatenated or truncated by a subsequent READ command. The first data from the new burst follows either the last element of a completed burst or the last desired element of a longer burst that is being truncated. The new READ command should be issued X cycles after the first READ command, where X equals the number of desired data-out element pairs (pairs are required by the 2n prefetch architecture).



1) Do*n* (or *b*): Data out from column n (or column b)
2) BA, Col *n (b)* = Bank A, Column n (b)
3) Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
4) Read bursts are to an active row in any bank
5) Shown with nominal tAC, tDQSCK and tDQSQ

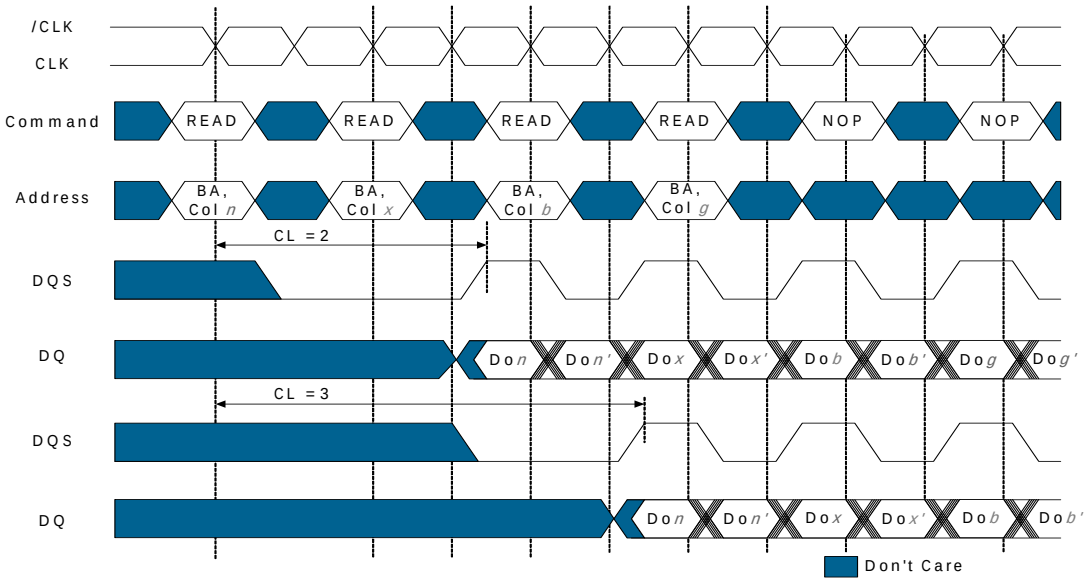
Consecutive Read Bursts

A READ command can be initiated on any clock cycle following a previous READ command. Non-consecutive Reads are shown in the first figure of next page. Random read accesses within a page or pages can be performed as shown in second figure of next page.



1) Do*n* (or *b*): Data out from column n (or column b)
2) BA, Col *n* (*b*) = Bank A, Column n (b)
3) Burst Length = 4; 3 subsequent elements of Data Out appear in the programmed order following Do *n* (*b*)
4) Shown with nominal tAC, tDQSCK and tDQSQ

Non-Consecutive Read Bursts

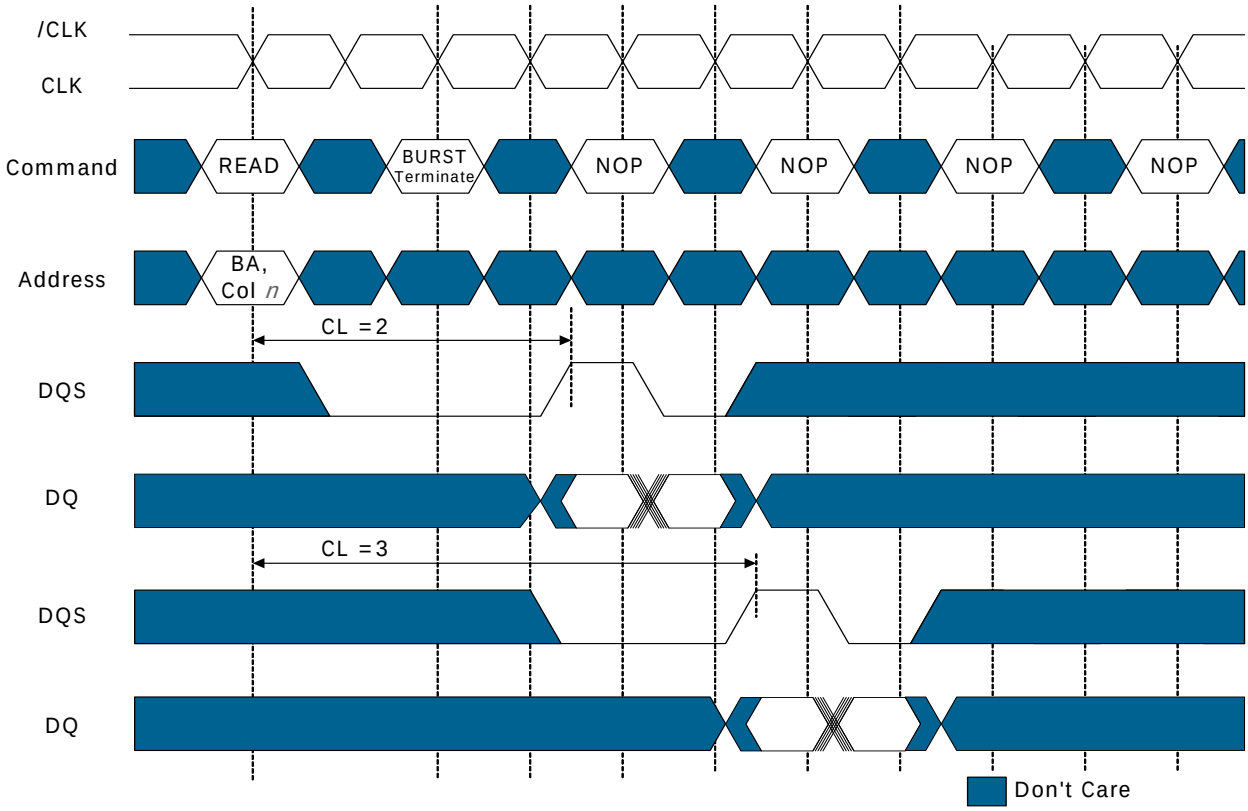


1) Do*n*, etc: Data out from column n, etc
n', x', etc : Data Out elements, accoding to the programmd burst order
2) BA, Col *n* = Bank A, Column n
3) Burst Length = 2, 4 or 8 in cases shown (if burst of 4 or 8, the burst is interrupted)
4) Read are to active rows in any banks

Random Read Bursts

READ BURST TERMINATE

Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued X cycles after the READ command where X equals the desired data-out element pairs.

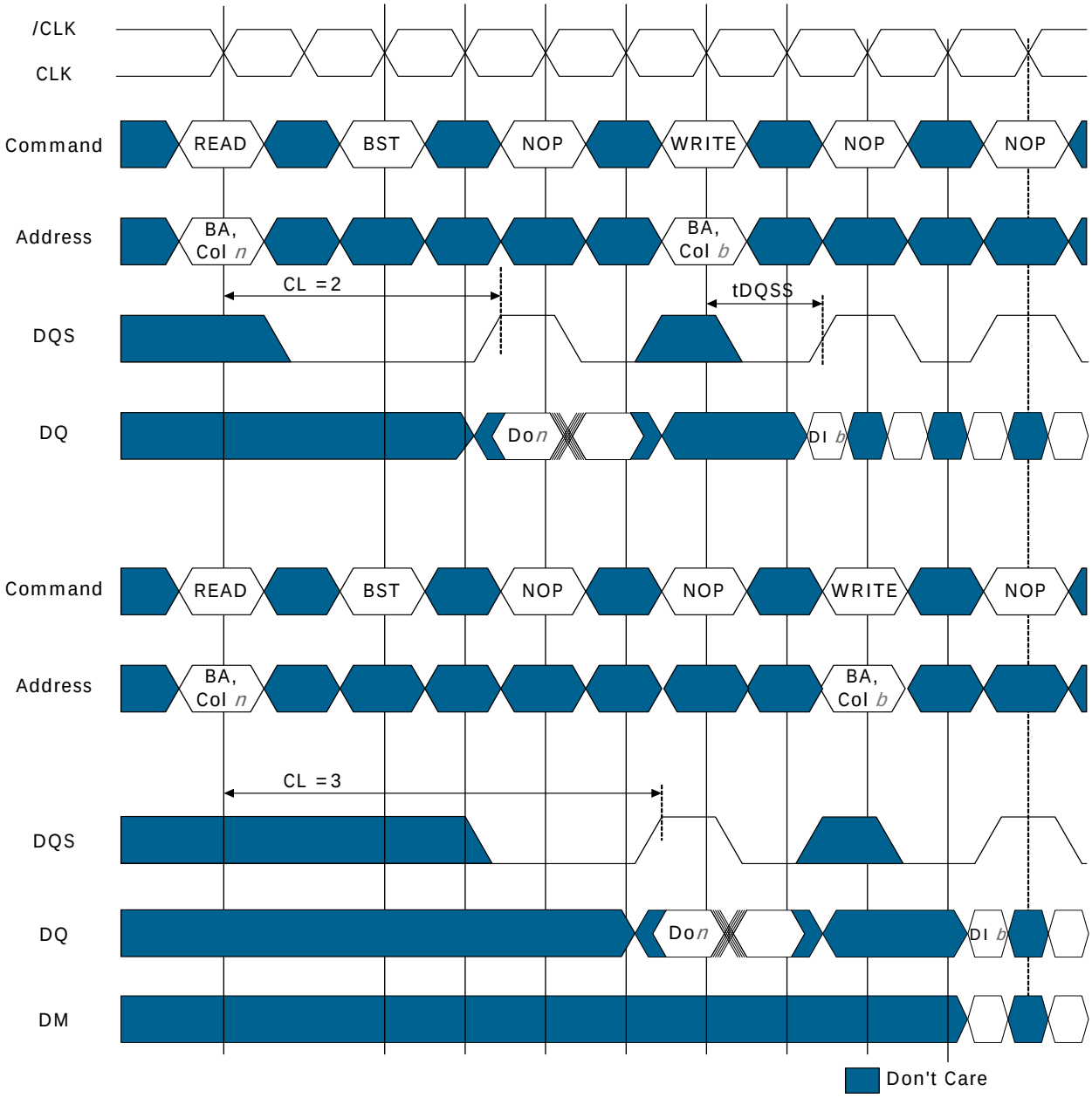


1) Do*n* : Data out from column n
2) BA, Col *n* = Bank A, Column n
3) Cases shown are bursts of 4 or 8 terminated after 2 data elements
4) Shown with nominal tAC, tDQSCK and tDQSQ

Terminating a Read Burst

READ to WRITE

Data from READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in next fig. for the case of nominal tDQSS.

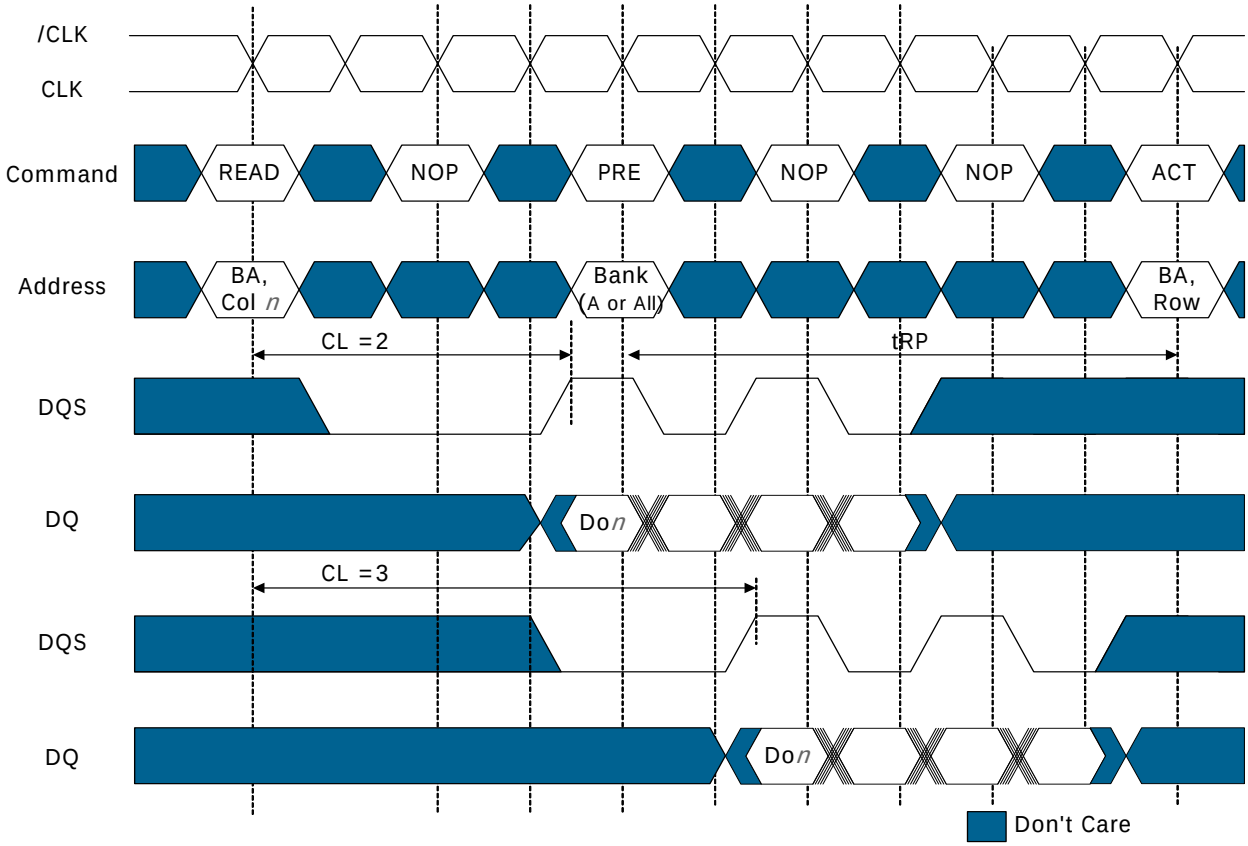


1) DO *n* = Data Out from column n; DI b = Data In to column b
2) Burst length = 4 or 8 in the cases shown; if the burst length is 2, the BST command can be ommitted
3) Shown with nominal tAC, tDQSCK and tDQSQ

Read to Write

READ to PRECHARGE

A Read burst may be followed by or truncated with a PRECHARGE command to the same bank (provided Auto Precharge was not activated). The PRECHARGE command should be issued X cycles after the READ command, where X equal the number of desired data-out element pairs.
Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data-out elements.In the case of a Read being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from Read burst with Auto Precharge enabled.
The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. The advantage of the PRECHARGE command is that it can be used to truncate bursts.

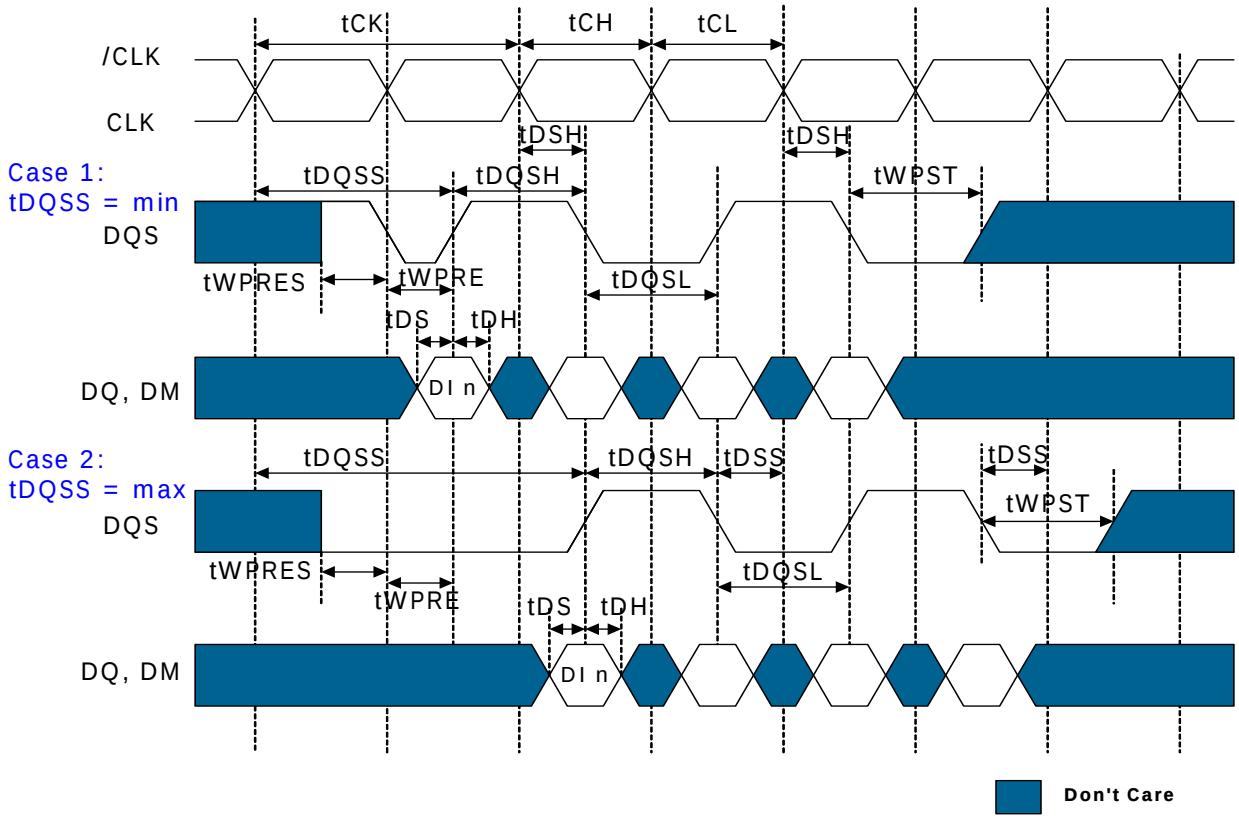


1) DO *n* = Data Out from column n
2) Cases shown are either uninterrupted burst of 4, or interrupted bursts of 8
3) Shown with nominal tAC, tDQSCK and tDQSQ
4) Precharge may be applied at (BL / 2) tCK after the READ command.
5) Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
6) The ACTIVE command may be applied if tRC has been met.

READ to PRECHARGE

Write

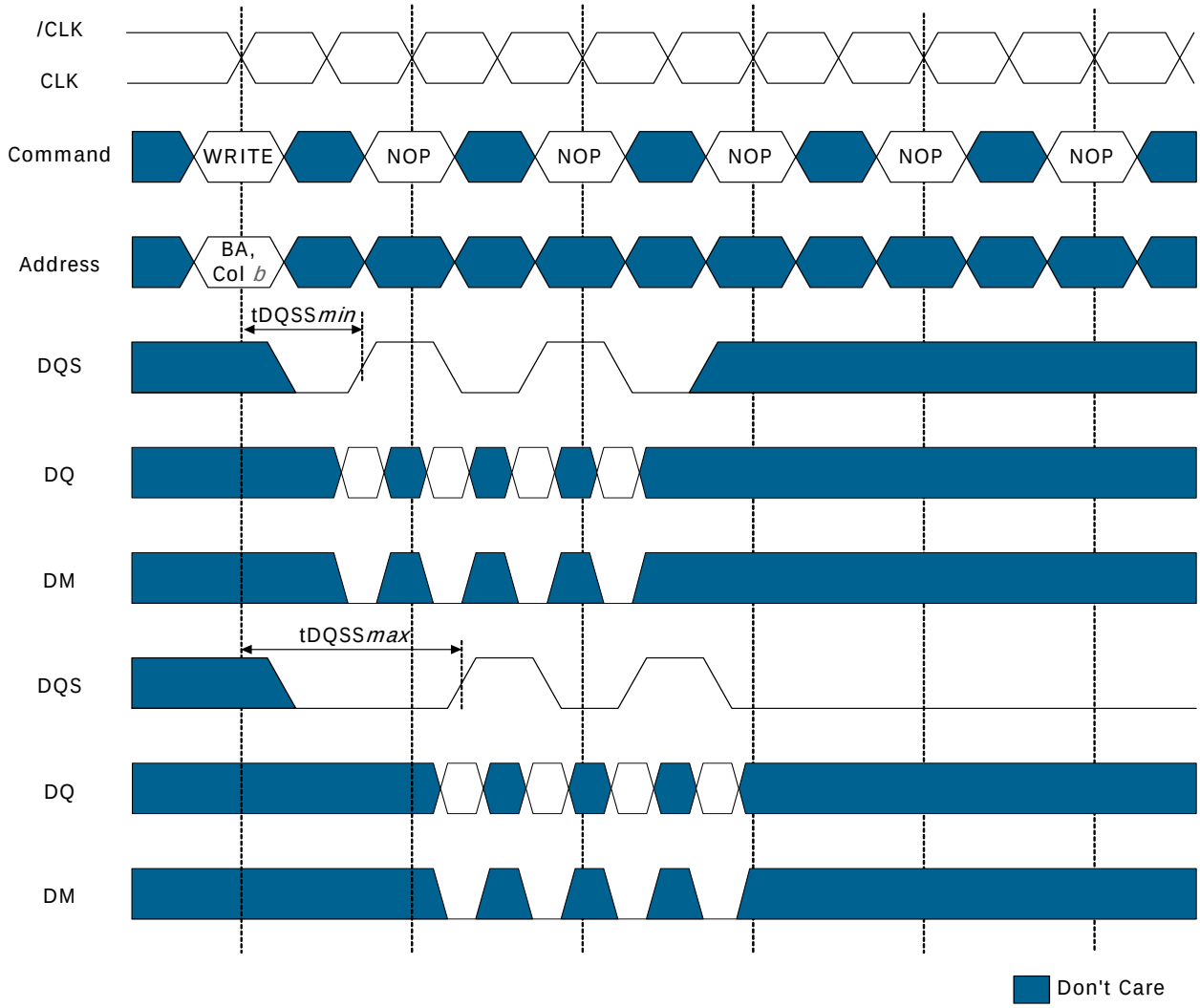
Input data appearing on the data bus, is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered Low, the corresponding data will be written to the memory; if the DM signal is registered High, the corresponding data inputs will be ignored, and a write will not be executed to that byte / column location.
Basic Write timing parameters for DQ are shown in Figure; they apply to all Write operations.



1) DI n: Data in for column n
2) 3 subsequent elements of Data in are applied in the programmed order following DI n
3) tDQSS : each rising edge of DQS must fall within the +/-25 (percentage) window of the corresponding positive clock edge

Basic Write Timing Parameters

During Write bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and the subsequent data elements will be registered on successive edges of DQS. The Low state of DQS between the WRITE command and the first rising edge is called the write preamble, and the Low state on DQS following the last data-in element is called the write postamble.
The time between the WRITE command and the first corresponding rising edge of DQS (t_{DQSS}) is specified with a relatively wide range - from 75% to 125% of a clock cycle. Next fig. shows the two extremes of t_{DQSS} for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain high-Z and any additional input data will be ignored.

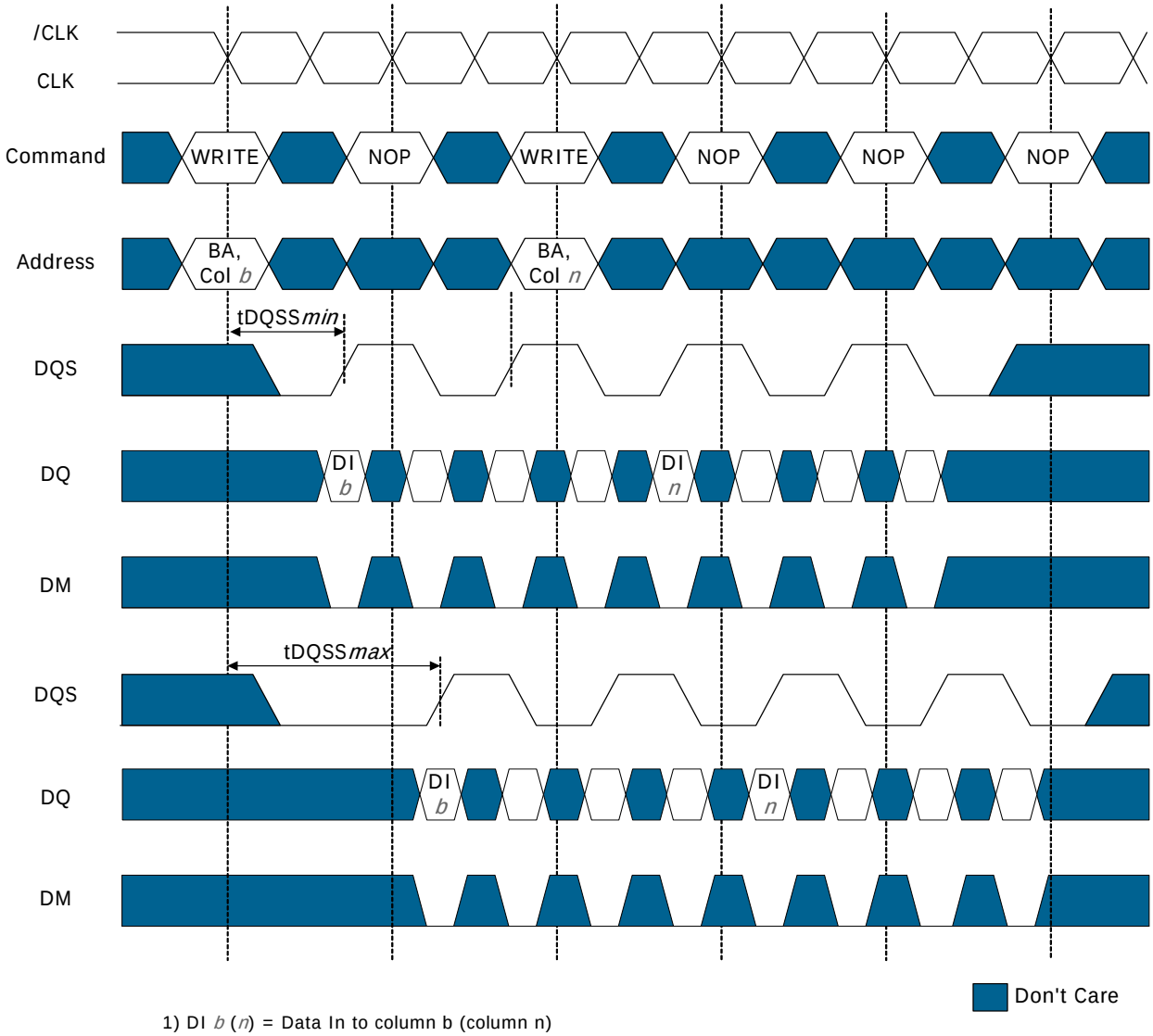


1) DI b = Data In to column b
2) 3 subsequent elements of Data In are applied in the programmed order following DI b
3) A non-interrupted burst of 4 is shown
4) A10 is low with the WRITE command (Auto Precharge is disabled)

Write Burst (min. and max. tDQSS)

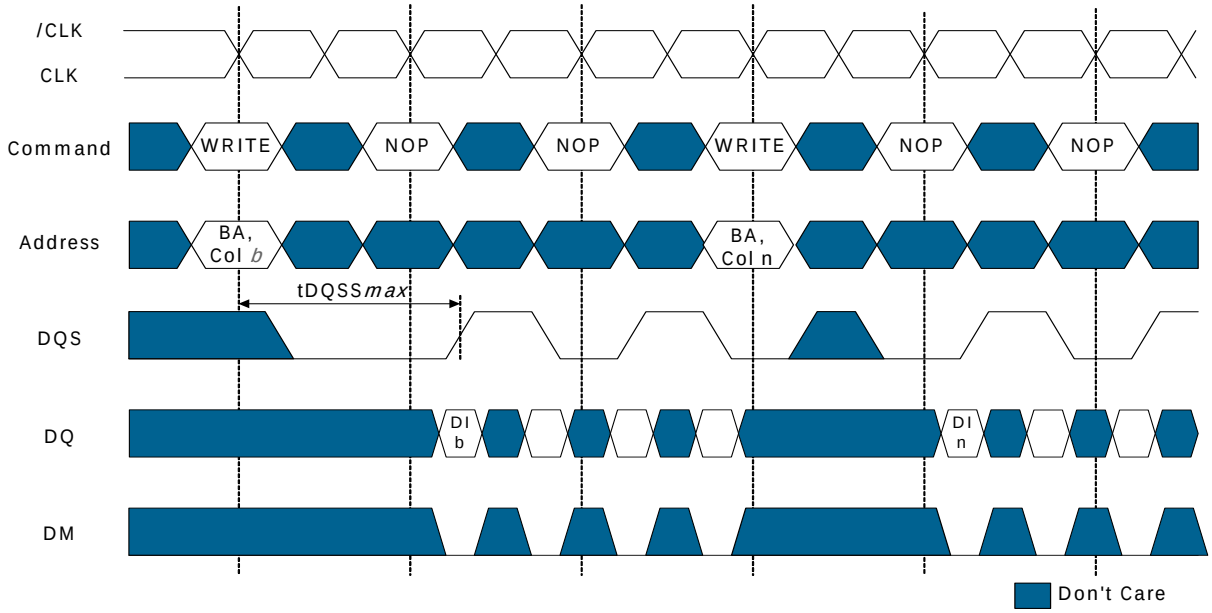
WRITE to WRITE

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data, can be maintained. The new WRITE command can be issued on any positive edge of the clock following the previous WRITE command.The first data-in element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued X cycles after the first WRITE command, where X equals the number of desired data-in element pairs.



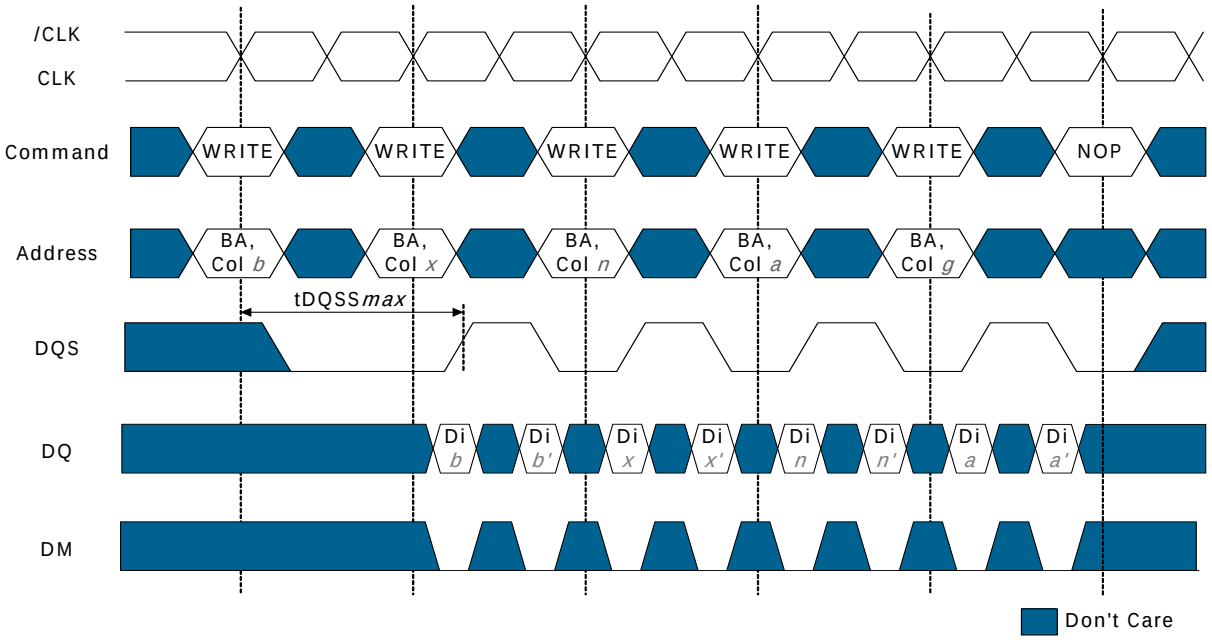
1) DI *b* (*n*) = Data In to column b (column n)
2) 3 subsequent elements of Data In are applied in the programmed order following DI b.
   3 subsequent elements of Data In are applied in the programmed order following DI n.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank

Concatenated Write Bursts



1) DI *b* (*n*) = Data In to column b (or column n).
2) 3 subsequent elements of Data In are applied in the programmed order following DI *b*.
   3 subsequent elements of Data In are applied in the programmed order following DI *n*.
3) Non-interrupted bursts of 4 are shown.
4) Each WRITE command may be to any active bank and may be to the same or different devices.

Non-Concatenated Write Bursts

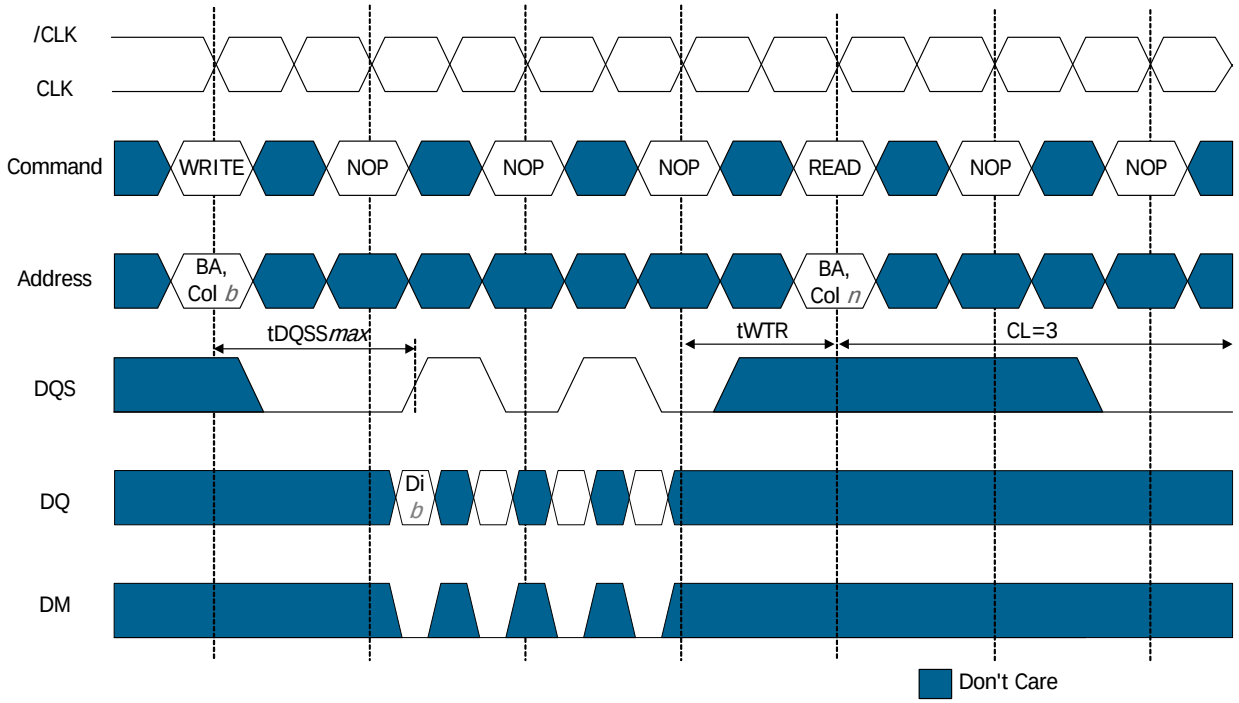


1) DI b etc. = Data In to column b, etc.
   ; b', etc. = the next Data In following DI b, etc. according to the programmed burst order
2) Programmed burst length = 2, 4 or 8 in cases shown. If burst of 4 or 8, burst would be truncated.
3) Each WRITE command may be to any active bank and may be to the same or different devices.

Random Write Cycles

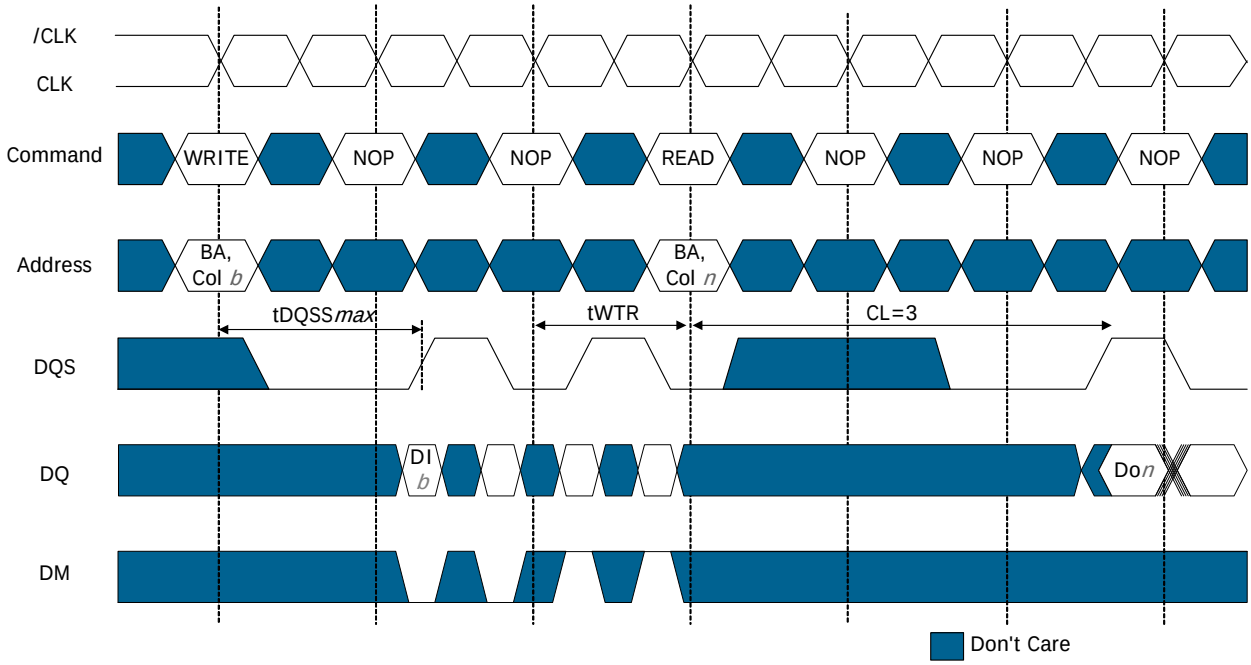
WRITE to READ

Data for any Write burst may be followed by a subsequent READ command. To follow a Write without truncating the write burst, tWTR should be met as shown in Figure.



1) DI *b* = Data In to column b . 3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted burst of 4 is shown.
3) tWTR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Data for any Write burst may be truncated by a subsequent READ command as shown in Figure. Note that the only data-in pairs that are registered prior to the tWTR period are written to the internal array, and any subsequent data-in must be masked with DM.

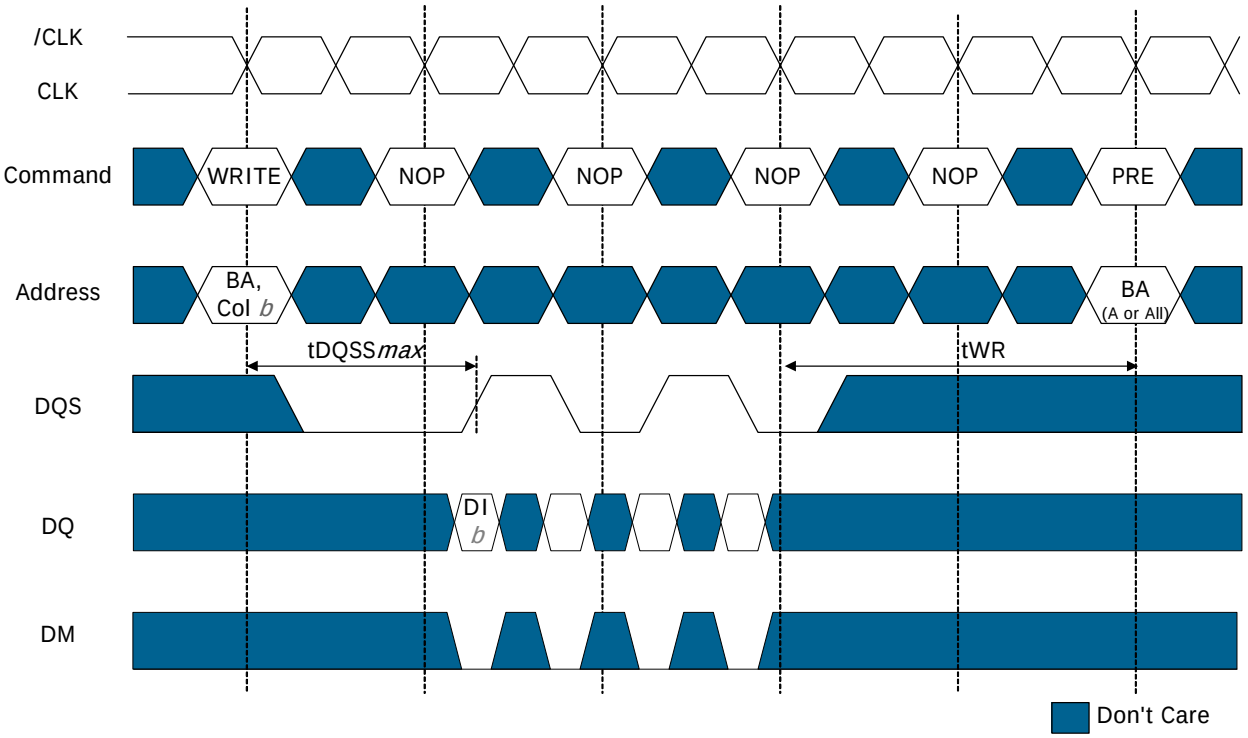


1) DI *b* = Data In to column b. DO *n* = Data Out from column n.
2) An interrupted burst of 4 is shown, 2 data elements are written.
   3 subsequent elements of Data In are applied in the programmed order following DI b.
3) tWTR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Interrupting Write to Read

WRITE to PRECHARGE

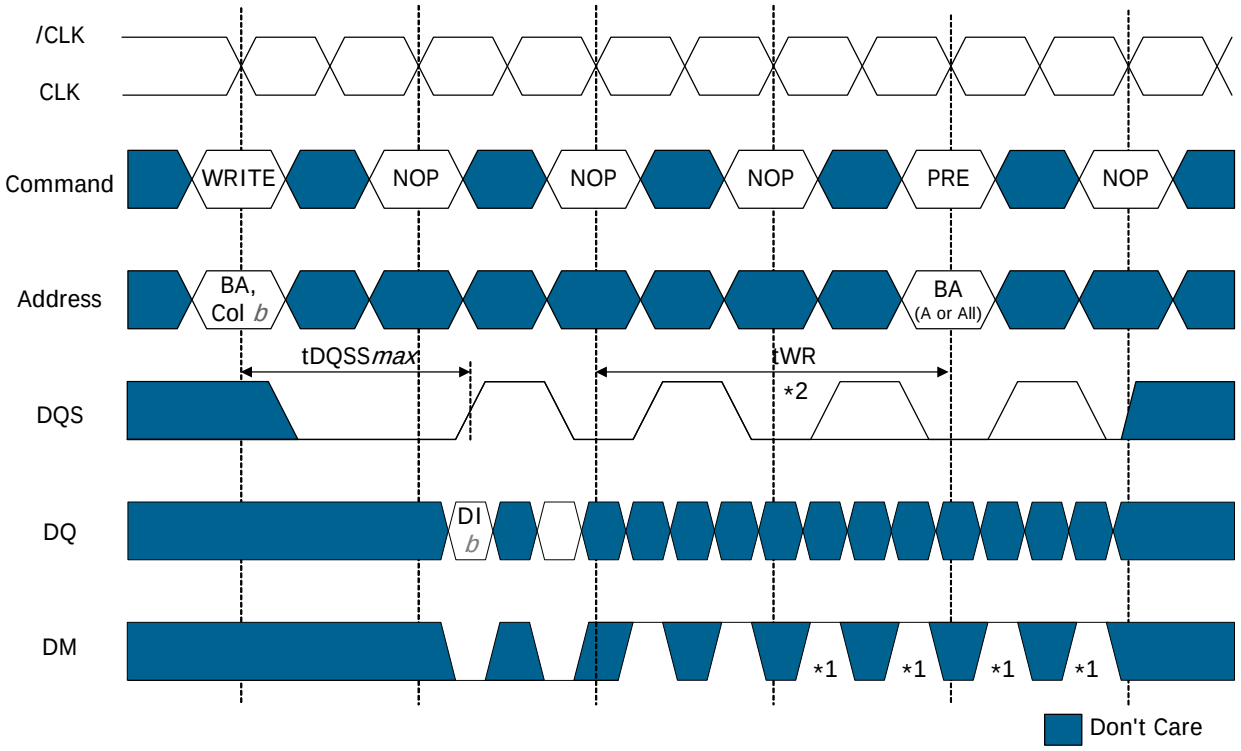
Data for any WRITE burst may be followed by a subsequent PRECHARGE command to the same bank (provided Auto Precharge was not activated). To follow a WRITE without truncating the WRITE burst, tWR should be met as shown in Fig.



1) DI b (n) = Data In to column b (column n)
   3 subsequent elements of Data In are applied in the programmed order following DI b.
2) A non-interrupted bursts of 4 are shown.
3) tWR is referenced from the positive clock edge after the last Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)

Non-Interrupting Write to Precharge

Data for any WRITE burst may be truncated by a subsequent PRECHARGE command as shown in Figure.
Note that only data-in pairs that are registered prior to the tWR period are written to the internal array, and any subsequent data-in should be masked with DM, as shown in next Fig. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

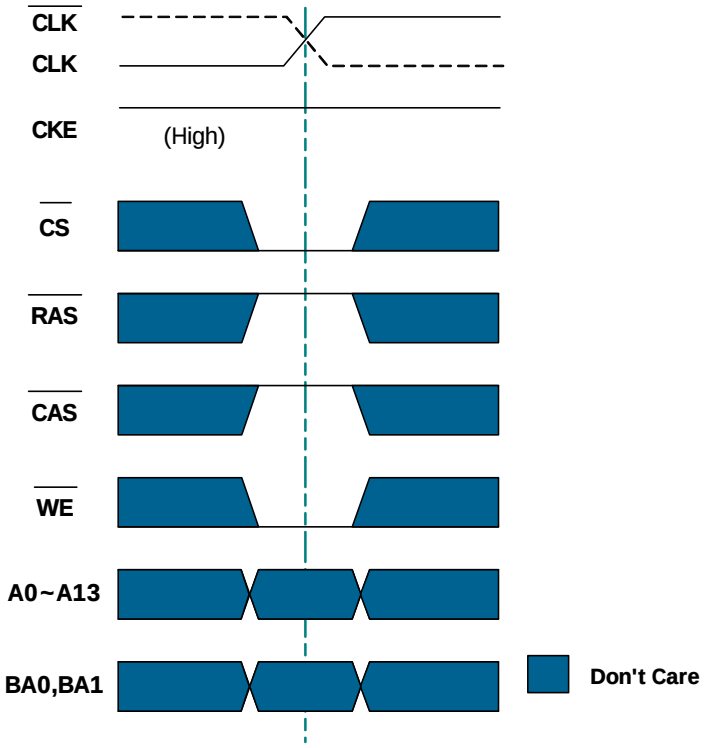


1) DI b = Data In to column b .
2) An interrupted burst of 4 or 8 is shown, 2 data elements are written.
3) tWR is referenced from the positive clock edge after the last desired Data In pair.
4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
5) *1 = can be Don't Care for programmed burst length of 4
6) *2 = for programmed burst length of 4, DQS becomes Don't Care at this point

Interrupting Write to Precharge

BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this datasheet. Note the BURST TERMINATE command is not bank specific. This command should not be used to terminate write bursts.

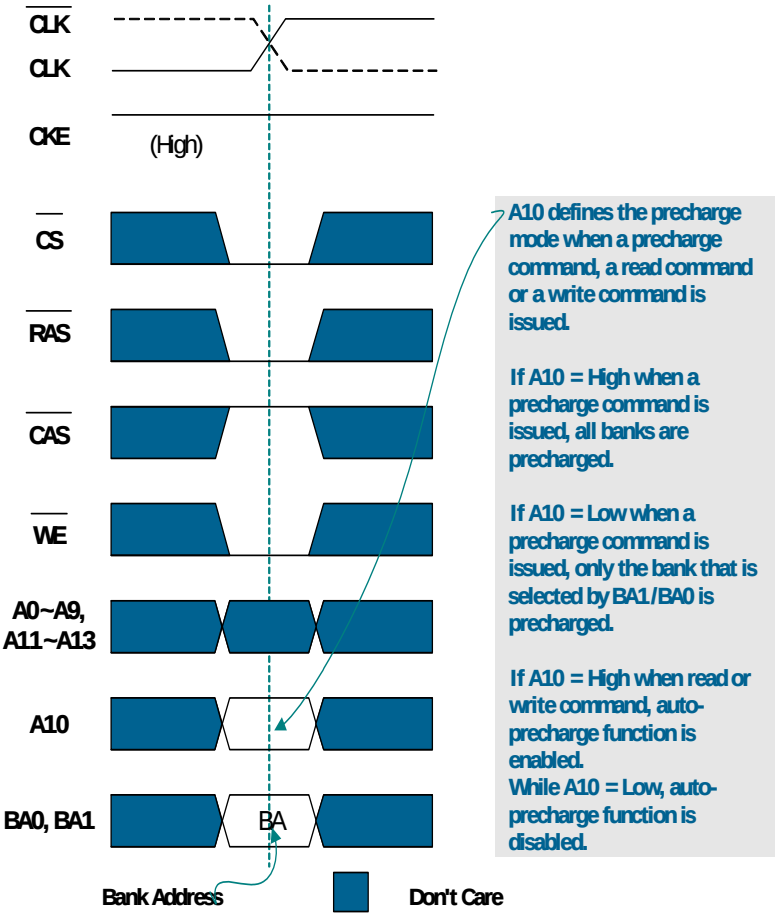


BURST TERMINATE COMMAND

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. Another command to the same bank (or banks) being precharged must not be issued until the precharge time (tRP) is completed.

If one bank is to be precharged, the particular bank address needs to be specified. If all banks are to be precharged, A10 should be set high along with the PRECHARGE command. If A10 is high, BA0 and BA1 are ignored. A PRECHARGE command will be treated as a NOP if there is no open row in that bank, or if the previously open row is already in the process of precharging.



PRECHARGE command

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command.

This is accomplished by using A10 (A10=high), to enable auto precharge in conjunction with a specific Read or Write command. This precharges the bank/row after the Read or Write burst is complete.

Auto precharge is non persistent, so it should be enabled with a Read or Write command each time auto precharge is desired. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst.

The user must not issue another command to the same bank until the precharge time (tRP) is completed.

AUTO REFRESH AND SELF REFRESH

Mobile DDR devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode:

- AUTO REFRESH

This command is used during normal operation of the Mobile DDR. It is non persistent, so must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller.The Mobile DDR requires AUTO REFRESH commands at an average periodic interval of tREFI.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given Mobile DDR, and the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 8*tREFI.

- SELF REFRESH

This state retains data in the Mobile DDR, even if the rest of the system is powered down (even without external clocking). Note refresh interval timing while in Self Refresh mode is scheduled internally in the Mobile DDR and may vary and may not meet tREFI time.

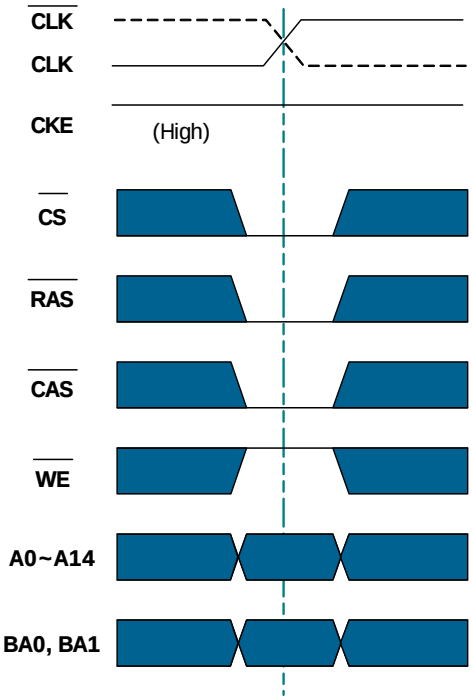
"Don't Care" except CKE, which must remain low. An internal refresh cycle is scheduled on Self Refresh entry. The procedure for exiting Self Refresh mode requires a series of commands. First clock must be stable before CKE going high. NOP commands should be issued for the duration of the refresh exit time (tXSR), because time is required for the completion of any internal refresh in progress.

The use of SELF REFRESH mode introduces the possibility that an internally timed event can be missed when CKE is raised for exit from self refresh mode. Upon exit from SELF REFRESH an extra AUTO REFRESH command is recommended. In the self refresh mode, two additional power-saving options exist. They are Temperature Compensated Self Refresh and Partial Array Self Refresh and are described in the Extended Mode Register section.

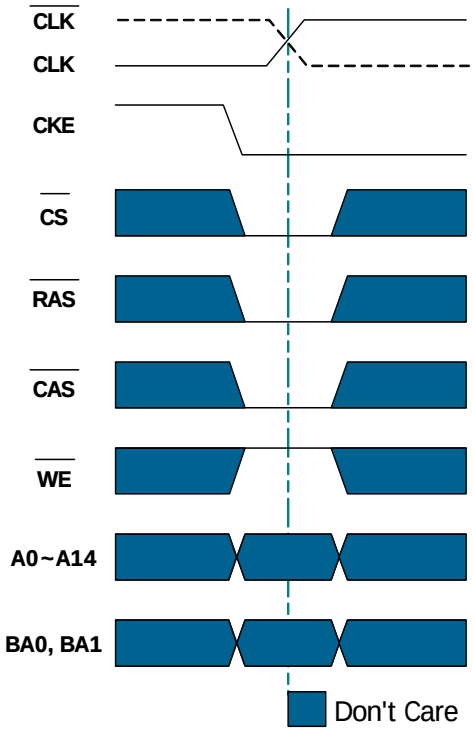
The Self Refresh command is used to retain cell data in the Mobile SDRAM. In the Self Refresh mode, the Mobile SDRAM operates refresh cycle asynchronously.

The Self Refresh command is initiated like an Auto Refresh command except CKE is disabled (Low). The Mobile DDR can accomplish an special Self Refresh operation by the specific modes (PASR) programmed in extended mode registers. The Mobile DDR can control the refresh rate automatically by the temperature value of Auto TCSR (Temperature Compensated Self Refresh) to reduce self refresh current and select the memory array to be refreshed by the value of PASR (Partial Array Self Refresh). The Mobile DDR can reduce the self refresh current(IDD6) by using these two modes.

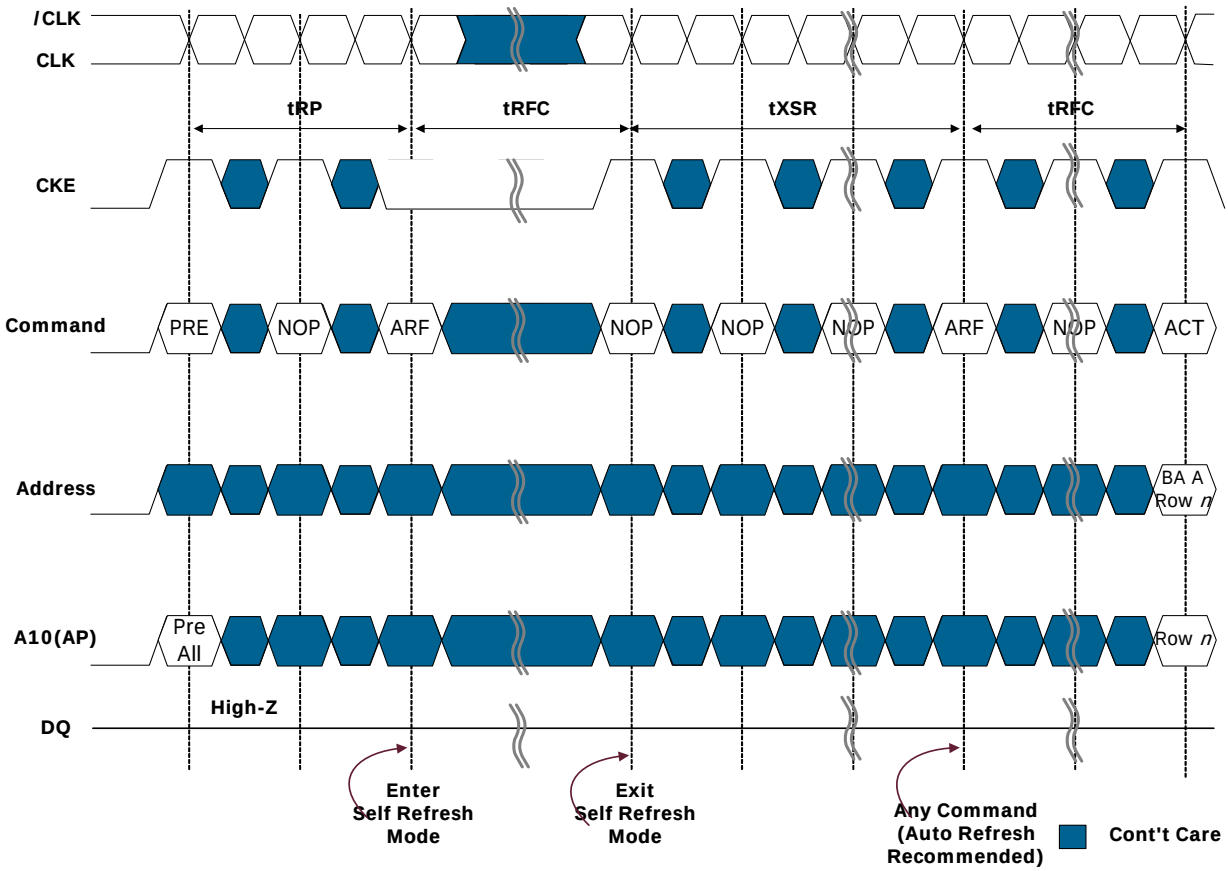
The figure of next page shows in case of 2KByte page size. If the page size is 4KByte, A0~A13 are provided.



Auto Refresh Command



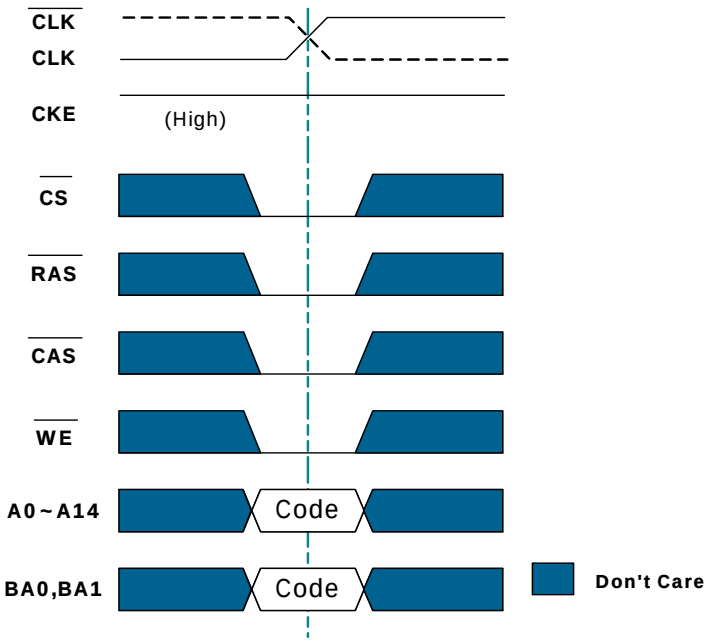
Self Refresh Command



SELF REFRESH ENTRY AND EXIT

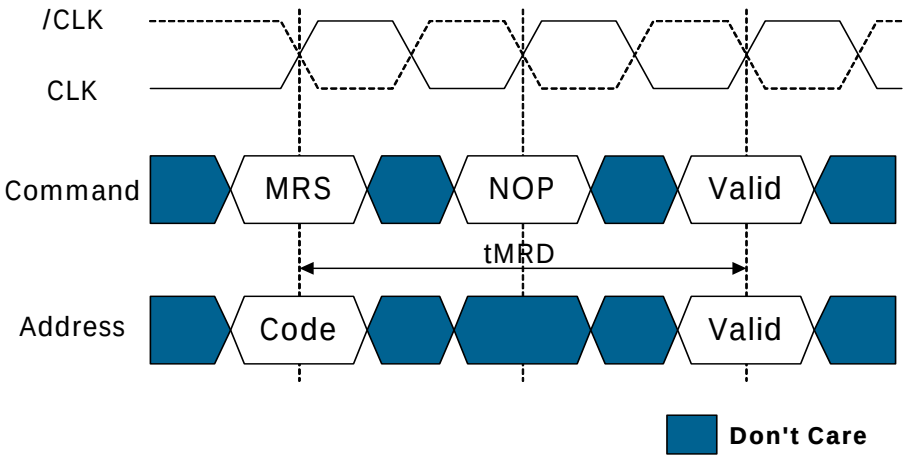
MODE REGISTER SET

The Mode Register and the Extended Mode Register are loaded via the address bits. BA0 and BA1 are used to select among the Mode Register, the Extended Mode Register and Status Register. See the Mode Register description in the register definition section. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.
The below figure shows in case of 2KByte page size. If the page size is 4KByte, A0~A13 are provided.



MODE REGISTER SET COMMAND

(A14 is used as 2Kbytes Reduced page)

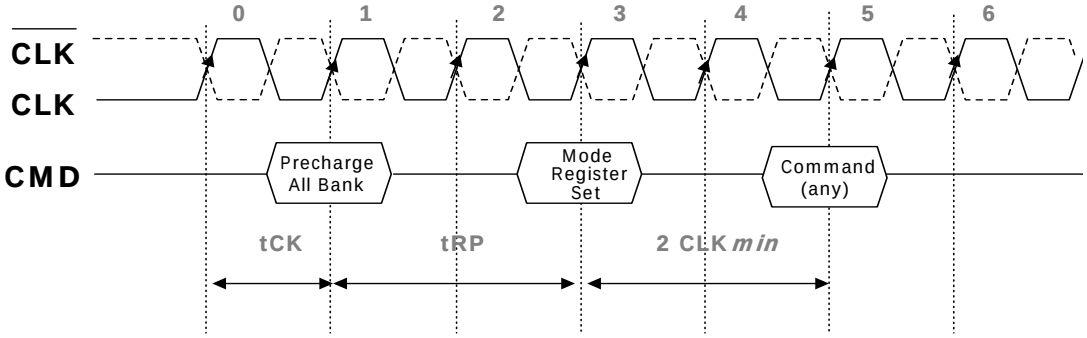


Code = Mode Register / Extended Mode Register selection
(BA0, BA1) and op-code (A0 - An)

tMRD DEFINITION

Mode Register

The mode register contains the specific mode of operation of the Mobile DDR SDRAM. This register includes the selection of a burst length(2, 4 or 8), a cas latency(2 or 3), a burst type. The mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of mode register set command.



Mode Register Set

BURST LENGTH

Read and write accesses to the Mobile DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Page10. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4 or 8 locations are available for both the sequential and the interleaved burst types.

BURST TYPE

Accesses within a given burst may be programmed to be either sequential or interleaved.

CAS LATENCY

The CAS latency is the delay between the registration of a READ command and the availability of the first piece of output data. If a READ command is registered at a clock edge *n* and the latency is 3 clocks, the first data element will be valid at *n* + 2tCK + tAC. If a READ command is registered at a clock edge *n* and the latency is 2 clocks, the first data element will be valid at *n* + tCK + tAC.

Extended Mode Register

The Extended Mode Register contains the specific features of self refresh operation of the Mobile DDR SDRAM.

The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=0) and will retain the stored information until it is reprogrammed, or the device loses power. The Extended Mode Register should be loaded when all Banks are idle and no bursts are in progress, and subsequent operation should only be initiated after tMRD. Violating these requirements will result in unspecified operation.

The Extended Mode Register is written by asserting low on CS, RAS, CAS, WE and high on BA0. The state of address pins A0 ~ A14 (or A13 which depends on page size) and BA1 in the same cycle as CS, RAS, CAS and WE going low are written in the extended mode register. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

This register includes the selection of partial array to be refreshed (full array, half array, quarter array, etc.). The extended mode register set must be done before any activate command after the power up sequence. Any contents of the mode register be altered by re-programming the mode register through the execution of extended mode register set command.

PARTIAL ARRAY SELF REFRESH (PASR)

With PASR, the self refresh may be restricted to a variable portion of the total array. The whole array (default), 1/2 array and 1/4 array could be selected.

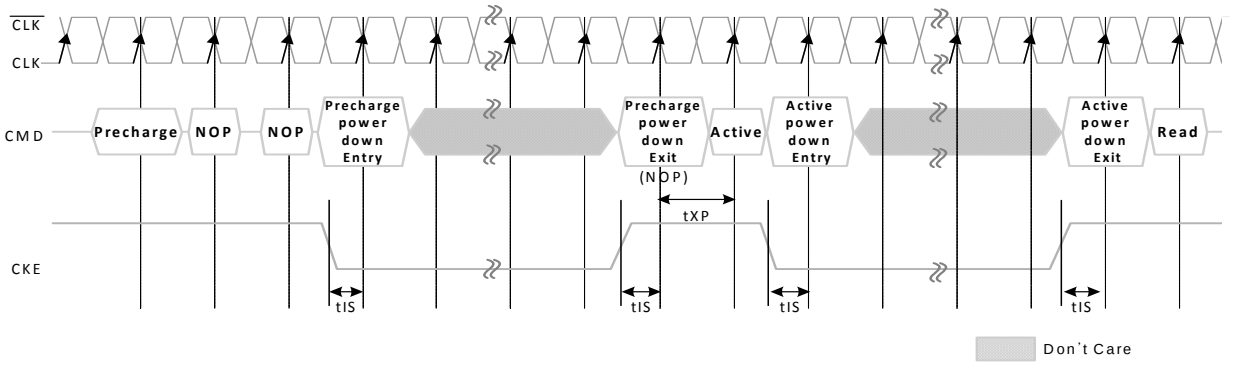
DRIVE STRENGTH (DS)

The drive strength could be set to full or half via address bits A5 and A6. The half drive strength is intended for lighter loads or point-to-point environments.

POWER DOWN

Power down occurs if CKE is set low coincident with Device Deselect or NOP command and when no accesses are in progress. If power down occurs when all banks are idle, it is Precharge Power Down.
If Power down occurs when one or more banks are Active, it is referred to as Active power down. The device cannot stay in this mode for longer than the refresh requirements of the device, without losing data. The power down state is exited by setting CKE high while issuing a Device Deselect or NOP command.
A valid command can be issued after tXP. For Clock stop during power down mode, please refer to the Clock Stop sub-section in Operation section of this datasheet.

NOTE: This case shows CKE low coincident with NO OPERATION.
Alternately POWER DOWN entry can be achieved with CKE low coincident with Device DESELECT.

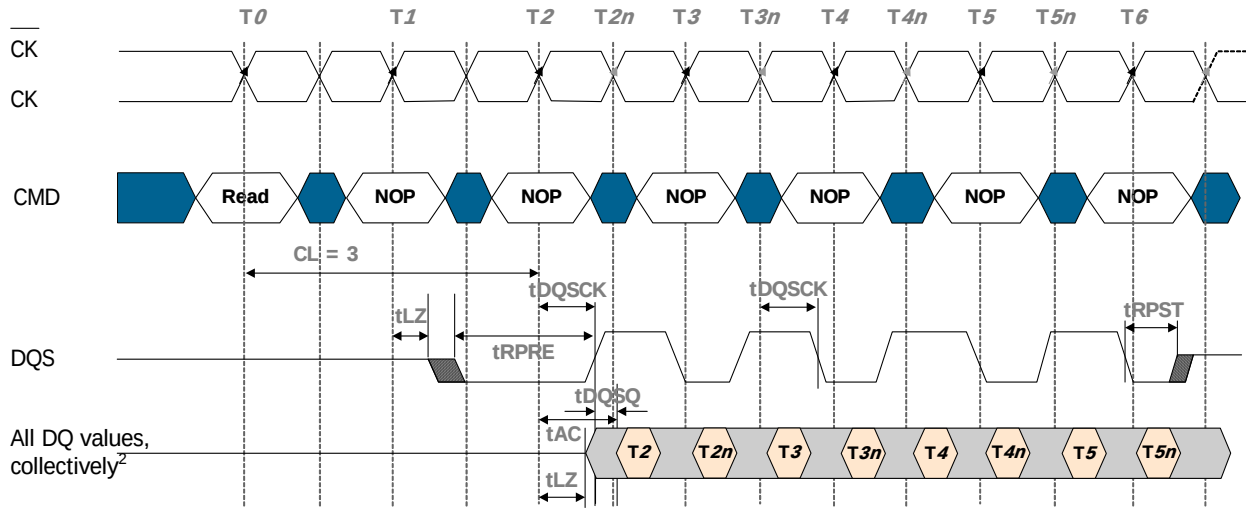


Mobile DDR SDRAM Power-Down Entry and Exit Timing

CAS LATENCY DEFINITION

CAS latency definition of Mobile DDR SDRAM must be must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation.

CAS latency definition: with CL = 3 the first data element is valid at (2 * tCK + tAC) after the clock at which the READ command was registered (See Figure 2)



CAS LATENCY DEFINITION

NOTE

1. DQ transitioning after DQS transition define tDQSQ window.
2. All DQ must transition by tDQSQ after DQS transitions, regardless of tAC.
3. tAC is the DQ output window relative to CK, and is the long term component of DQ skew.

Clock Stop Mode

Clock stop mode is a feature supported by Mobile DDR SDRAM devices. It reduces clock-related power consumption during idle periods of the device.

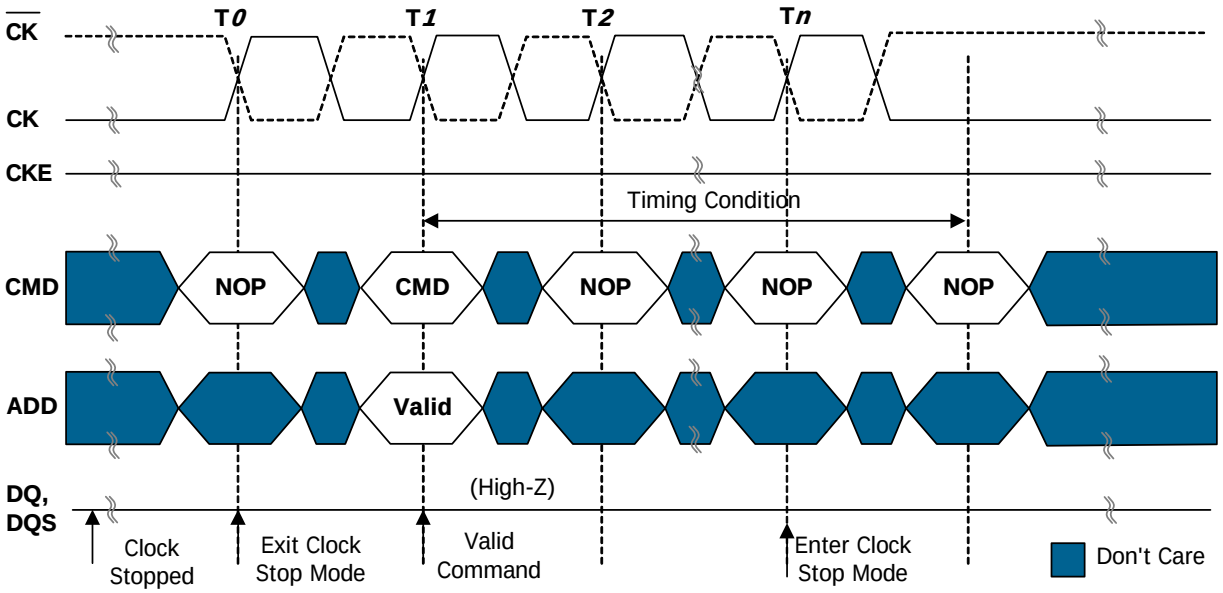
Conditions: the Mobile DDR SDRAM supports clock stop in case:

- The last access command (ACTIVE, READ, WRITE, PRECHARGE, AUTO REFRESH or MODE REGISTER SET) has executed to completion, including any data-out during read bursts; the number of required clock pulses per access command depends on the device's AC timing parameters and the clock frequency;
- The related timing condition (tRCD, tWR, tRP, tRFC, tMRD) has been met;
- CKE is held HIGH.

When all conditions have been met, the device is either in "idle" or "row active" state, and clock stop mode may be entered with CK held LOW and $\overline{CK}$ held HIGH. Clock stop mode is exited when the clock is restarted. NOPs command have to be issued for at least one clock cycle before the next access command may be applied. Additional clock pulses might be required depending on the system characteristics.

Figure1 illustrates the clock stop mode:

- Initially the device is in clock stop mode;
- The clock is restarted with the rising edge of T0 and a NOP on the command inputs;
- With T*1* a valid access command is latched; this command is followed by NOP commands in order to allow for clock stop as soon as this access command has completed;
- T*n* is the last clock pulse required by the access command latched with T*1.*
- The timing condition of this access command is met with the completion of T*n*; therefore Tn is the last clock pulse required by this command and the clock is then stopped.



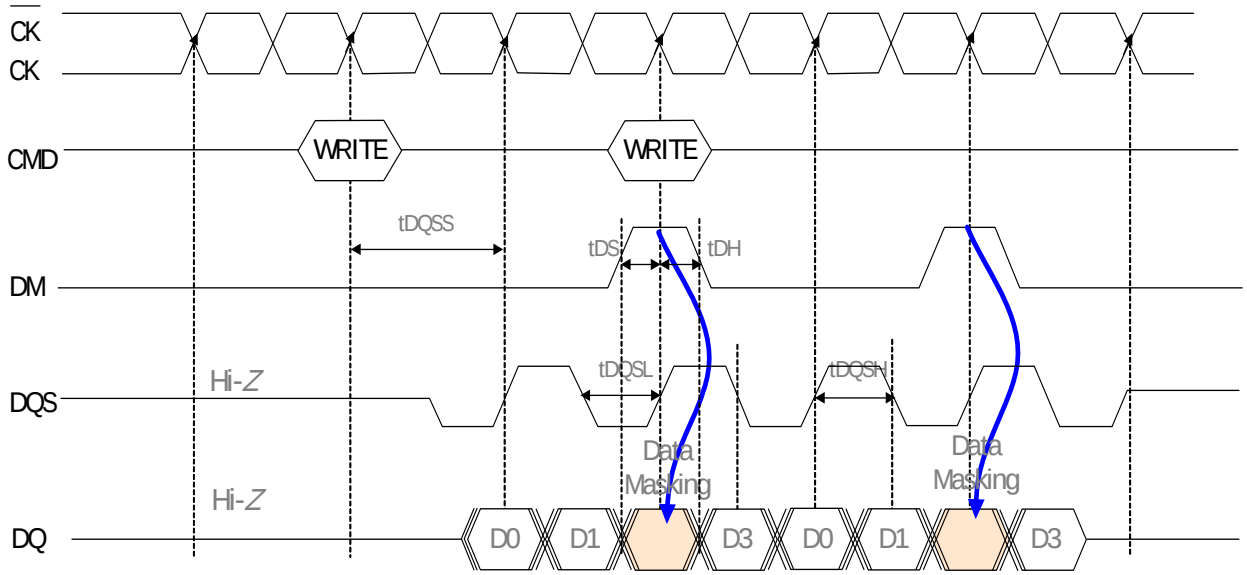
Clock Stop Mode

Data mask[1,2)

Mobile DDR SDRAM uses a DQ write mask enable signal (DM) which masks write data.
Data masking is only available in the write cycle for Mobile DDR SDRAM. Data masking is available during write, but data masking during read is not available.
DM command masks burst write data with reference to data strobe signal and it is not related with read data. DM command can be initiated at both the rising edge and the falling edge of the DQS. DM latency for write operation is zero.
For x32 data I/O, Mobile DDR SDRAM is equipped with DM0, DM1, DM2 and DM3 which control DQ0~DQ7, DQ8~DQ15, DQ16~DQ23 and DQ24~DQ31 respectively.

Note:
1) Mobile SDR SDRAM can mask both read and write data, but the read mask is not supported by Mobile DDR SDRAM.
2) Differences in Functions and Specifications (next table)

Item	Mobile DDR SDRAM	Mobile SDR SDRAM
Data mask	Write mask only	Write mask/Read mask



Data Masking (Write cycle: BL=4)

POWER-UP AND INITIALIZATION SEQUENCES

Mobile DDR SDRAM must be powered up and initialized in a predefined manner. Operations procedures other thank those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below.

- Step1: Provide power, the device core power (V_{DD}) and the device I/O power (V_{DDQ}) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that V_{DD} and V_{DDQ} are from the same power source. Also assert and hold CLOCK ENABLE (CKE) to a LVCMOS logic high level.

- Step 2: Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.

- Step 3: There must be at least 200us of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus.

- Step 4: Issue a PRECHARGE ALL command.

- Step 5: Provide NOPs or DESELECT commands for at least t_{RP} time.

- Step 6: Issue an AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time. Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least t_{RFC} time.
  Note as part of the initialization sequence there must be two auto refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.

- Step 7: Using the MRS command, load the base mode register. Set the desired operating modes.

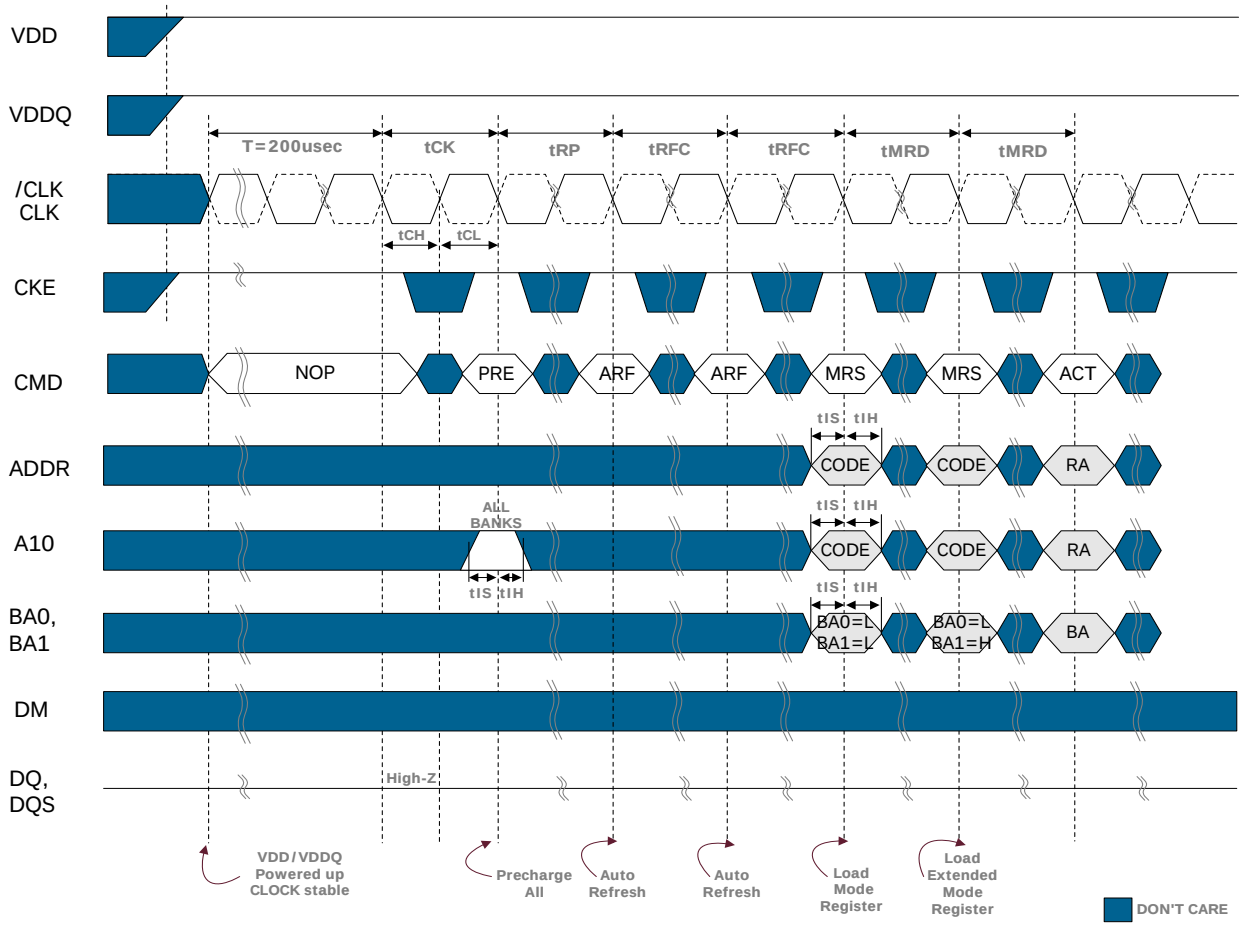
- Step 8: Provide NOPs or DESELECT commands for at least t_{MRD} time.

- Step 9: Using the MRS command, program the extended mode register for the desired operating modes. Note the order of the base and extended mode register programming is not important.

- Step 10: Provide NOP or DESELCT commands for at least t_{MRD} time.

- Step 11: The DRAM has been properly initialized and is ready for any valid command.

The Initialization flow sequence is below.



Initialization Waveform Sequence