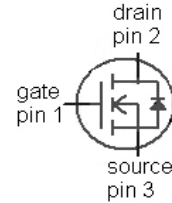


**OptiMOS<sup>®</sup> 2 Power-Transistor**
**Features**

- Ideal for high-frequency dc/dc converters
- Qualified according to JEDEC<sup>1)</sup> for target application
- N-channel, logic level
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Superior thermal resistance
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant

**Product Summary**

$V_{DS}$	25	V
$R_{DS(on),max}$ (SMD version)	9.2	mΩ
$I_D$	30	A



Type	IPDH9N03LA G	IP9N03LA G
<b>Package</b>	PG-TO252-3-11	PG-TO251-3-11
<b>Marking</b>	H9N03LA	H9N03LA

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C=25\text{ °C}^{2)}$	30	A
		$T_C=100\text{ °C}$	30	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}^{3)}$	210	
Avalanche energy, single pulse	$E_{AS}$	$I_D=30\text{ A}, R_{GS}=25\text{ }\Omega$	80	mJ
Reverse diode $dv/dt$	$dv/dt$	$I_D=30\text{ A}, V_{DS}=20\text{ V},$ $di/dt=200\text{ A}/\mu\text{s},$ $T_{j,max}=175\text{ °C}$	6	kV/ $\mu\text{s}$
Gate source voltage <sup>4)</sup>	$V_{GS}$		$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	52	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - case	$R_{thJC}$		-	-	2.9	K/W
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	75	
		6 cm <sup>2</sup> cooling area <sup>5)</sup>	-	-	50	

**Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=20\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=15\text{ A}$	-	13.5	16.8	m $\Omega$
		$V_{GS}=4.5\text{ V}, I_D=15\text{ A},$ (PG-TO252-3-11)	-	13.3	16.6	
		$V_{GS}=10\text{ V}, I_D=30\text{ A}$	-	7.9	9.4	
		$V_{GS}=10\text{ V}, I_D=30\text{ A},$ (PG-TO252-3-11)	-	7.7	9.2	
Gate resistance	$R_G$		-	1	-	$\Omega$
Transconductance	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max},$ $I_D=30\text{ A}$	21	42	-	S

<sup>1)</sup> J-STD20 and JESD22

<sup>2)</sup> Current is limited by bondwire; with an  $R_{thJC}=2.9\text{ K/W}$  the chip is able to carry 56 A.

<sup>3)</sup> See figure 3

<sup>4)</sup>  $T_{j,max}=150\text{ °C}$  and duty cycle  $D<0.25$  for  $V_{GS}<-5\text{ V}$ 
<sup>5)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V}, f=1\text{ MHz}$	-	1000	1350	pF
Output capacitance	$C_{oss}$		-	400	520	
Reverse transfer capacitance	$C_{rss}$		-	50	78	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V}, I_D=15\text{ A}, R_G=2.7\ \Omega$	-	4.1	6.1	ns
Rise time	$t_r$		-	4.0	6.0	
Turn-off delay time	$t_{d(off)}$		-	16	23	
Fall time	$t_f$		-	2.8	4.2	

**Gate Charge Characteristics<sup>6)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=15\text{ V}, I_D=15\text{ A}, V_{GS}=0\text{ to }5\text{ V}$	-	3.7	4.9	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.8	2.4	
Gate to drain charge	$Q_{gd}$		-	2.6	3.9	
Switching charge	$Q_{sw}$		-	4.5	6.4	
Gate charge total	$Q_g$		-	9	12	
Gate plateau voltage	$V_{plateau}$		-	3.3	-	
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V}, V_{GS}=0\text{ to }5\text{ V}$	-	7.9	10.5	nC
Output charge	$Q_{oss}$	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	9.4	12	

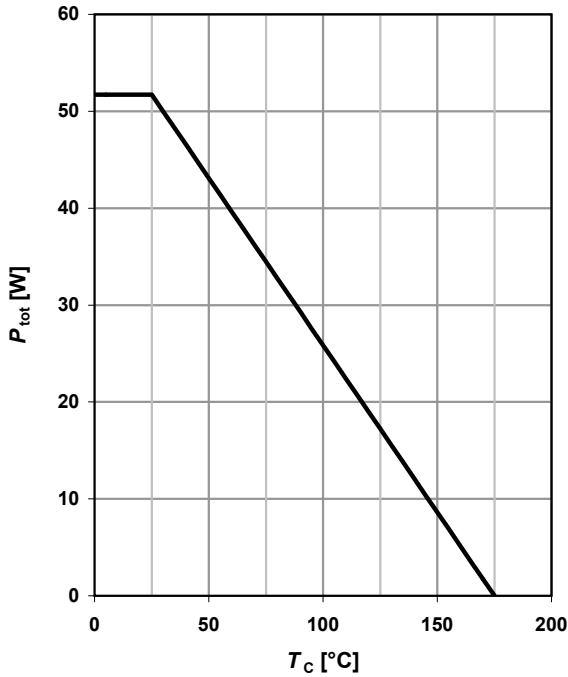
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	30	A
Diode pulse current	$I_{S,pulse}$		-	-	210	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=30\text{ A}, T_j=25\text{ }^\circ\text{C}$	-	0.91	1.2	V
Reverse recovery charge	$Q_{rr}$	$V_R=15\text{ V}, I_F=I_S, di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

<sup>6)</sup> See figure 16 for gate charge parameter definition

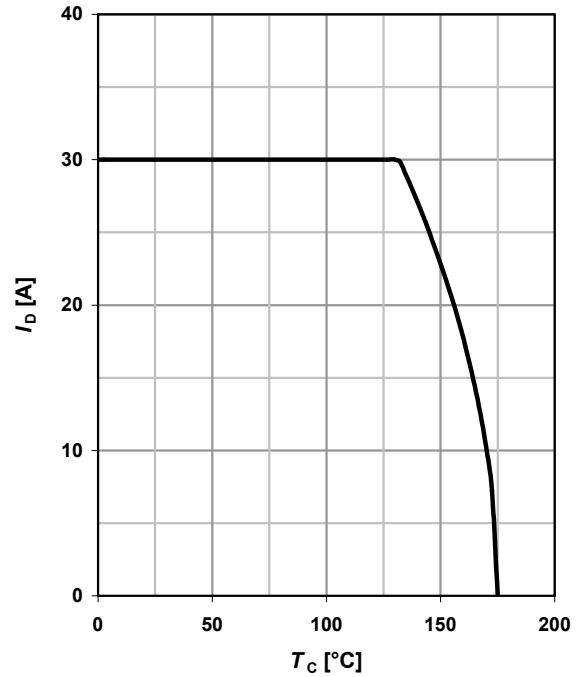
**1 Power dissipation**

$$P_{tot} = f(T_C)$$



**2 Drain current**

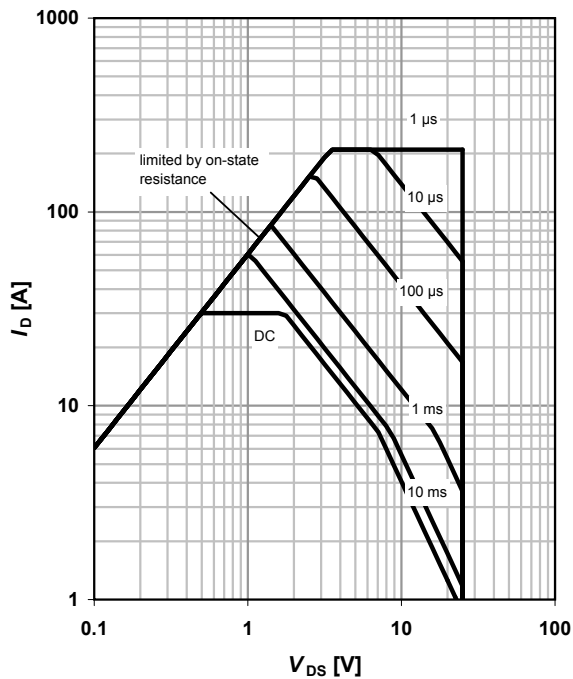
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



**3 Safe operating area**

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

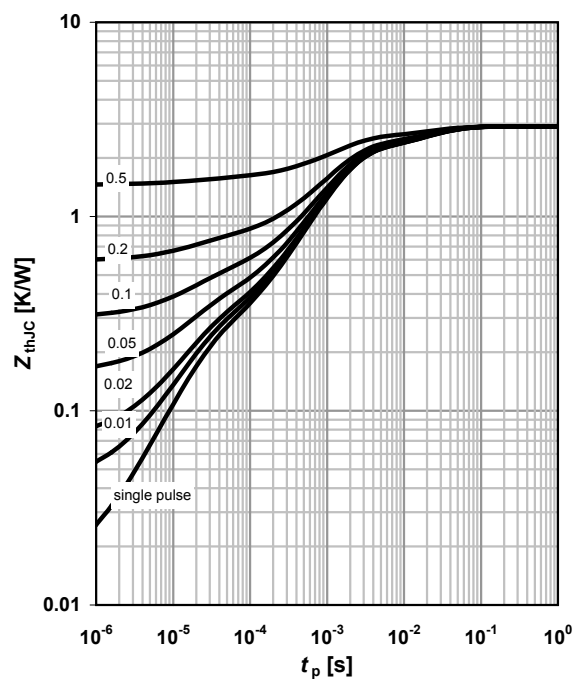
parameter:  $t_p$



**4 Max. transient thermal impedance**

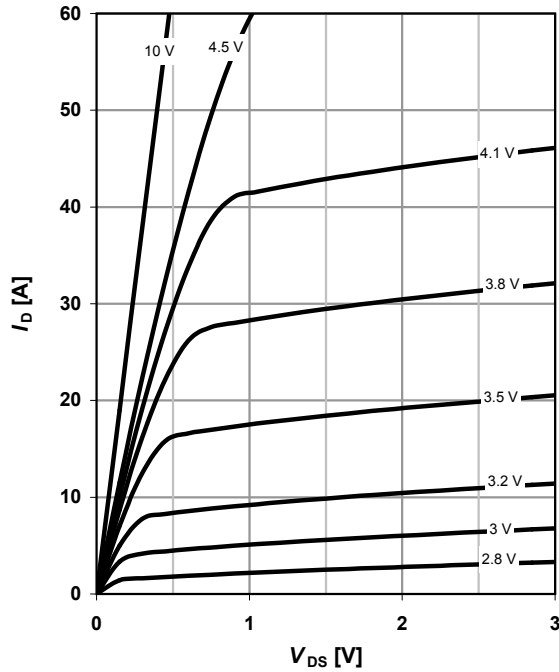
$$Z_{thJC} = f(t_p)$$

parameter:  $D = t_p / T$

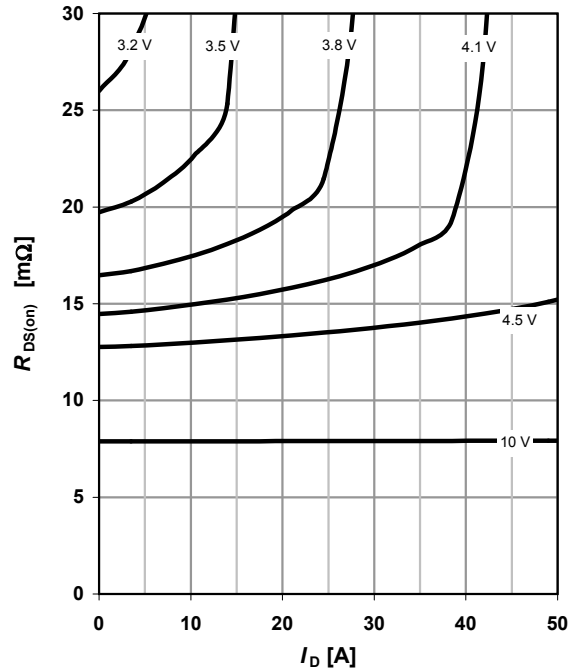


**5 Typ. output characteristics**

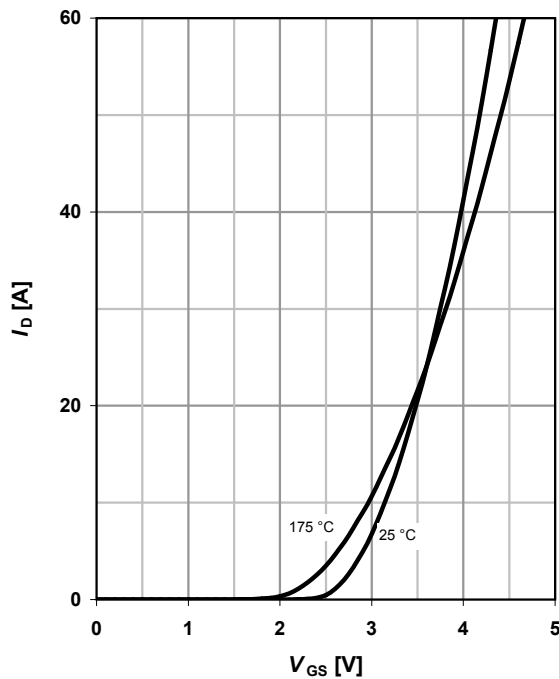
$$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$$

 parameter:  $V_{GS}$ 

**6 Typ. drain-source on resistance**

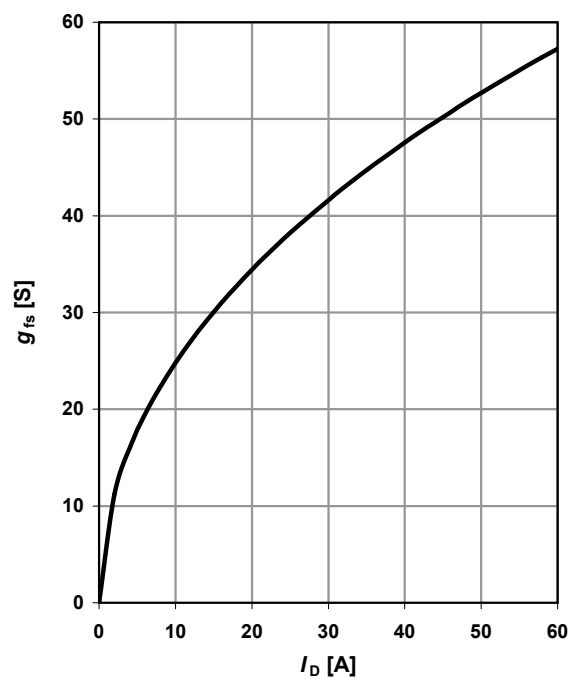
$$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$$

 parameter:  $V_{GS}$ 

**7 Typ. transfer characteristics**

$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

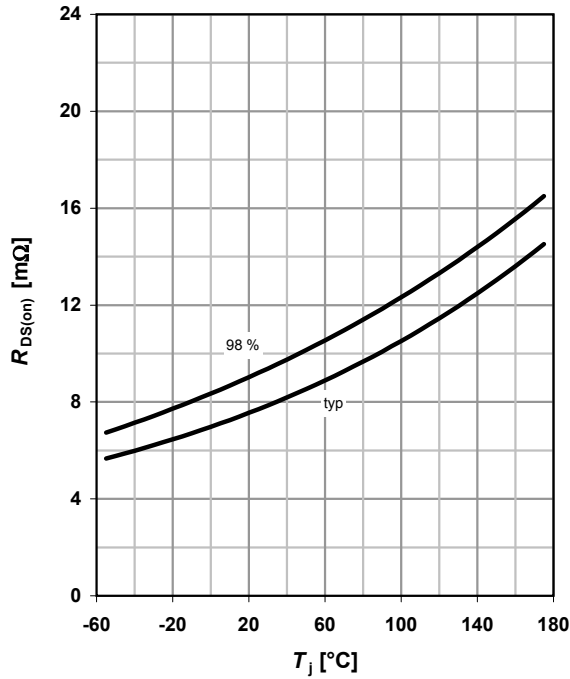
 parameter:  $T_j$ 

**8 Typ. forward transconductance**

$$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$$



**9 Drain-source on-state resistance**

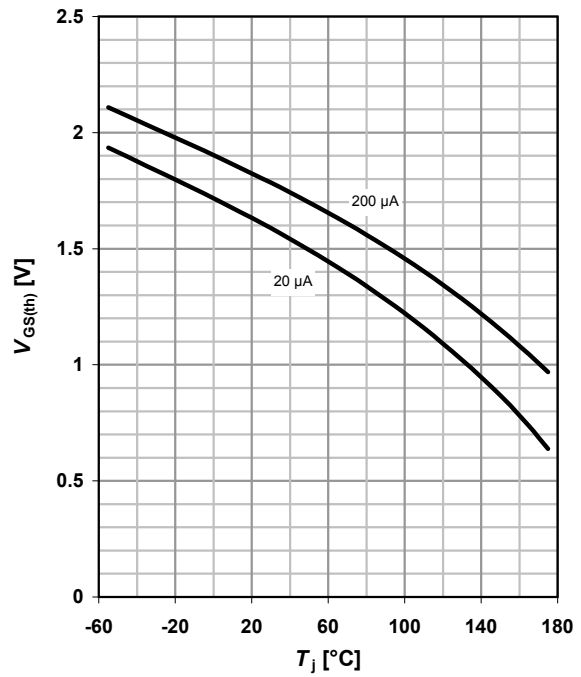
$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$



**10 Typ. gate threshold voltage**

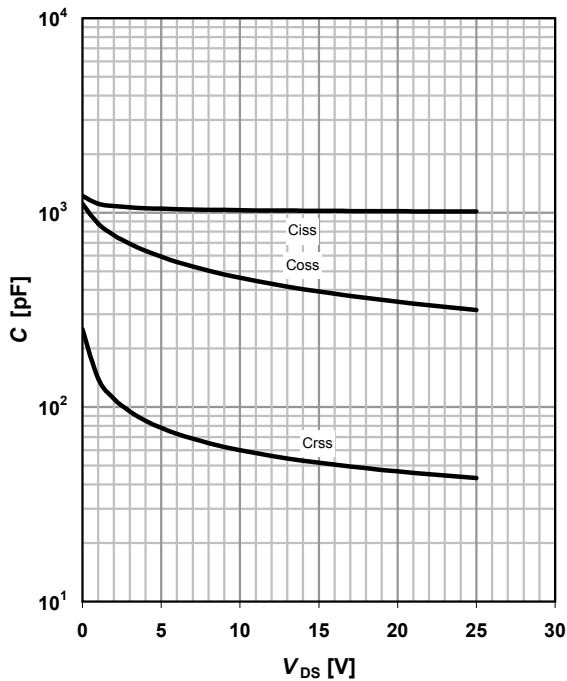
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $I_D$



**11 Typ. capacitances**

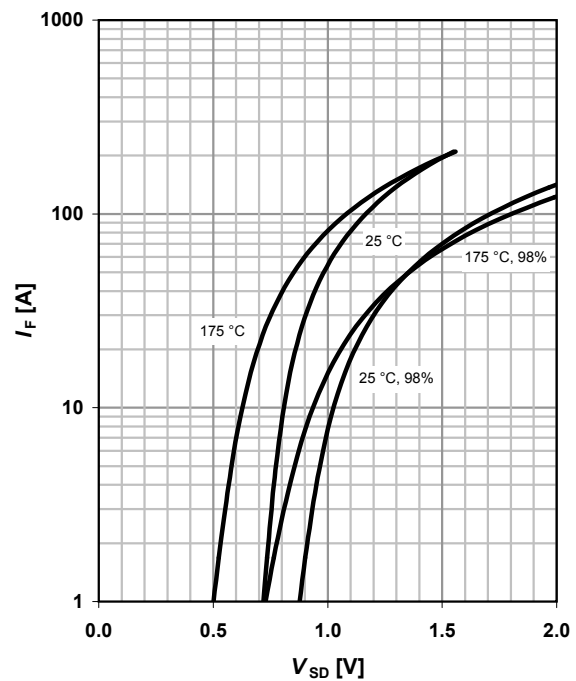
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F = f(V_{SD})$

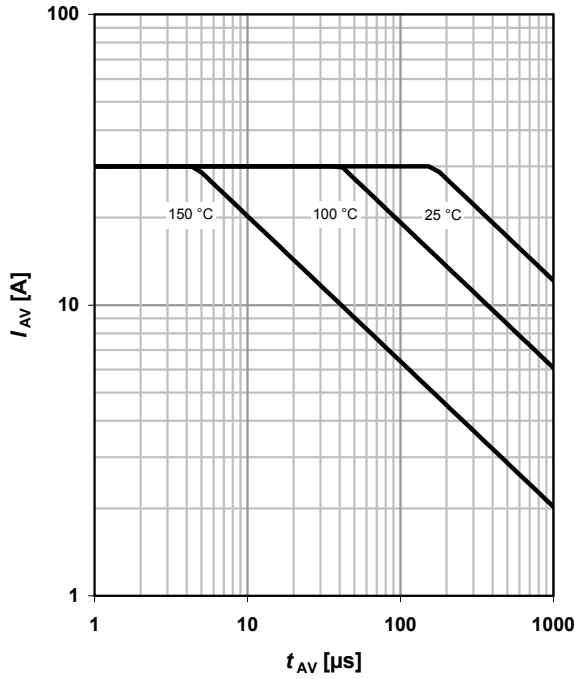
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

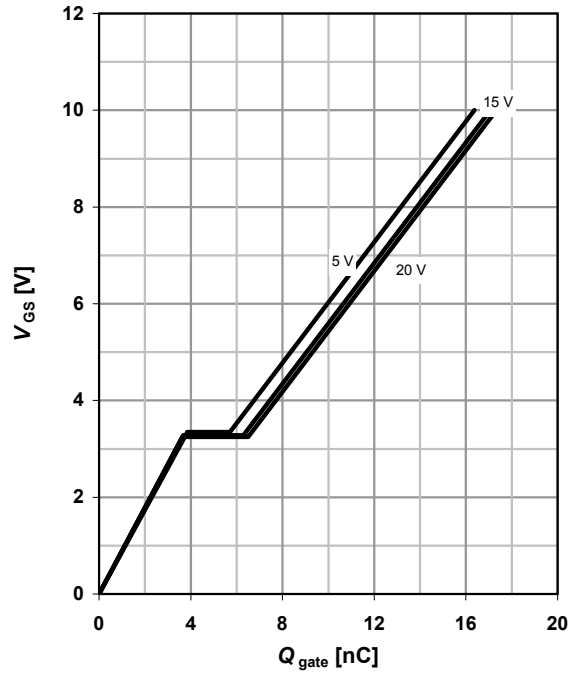
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

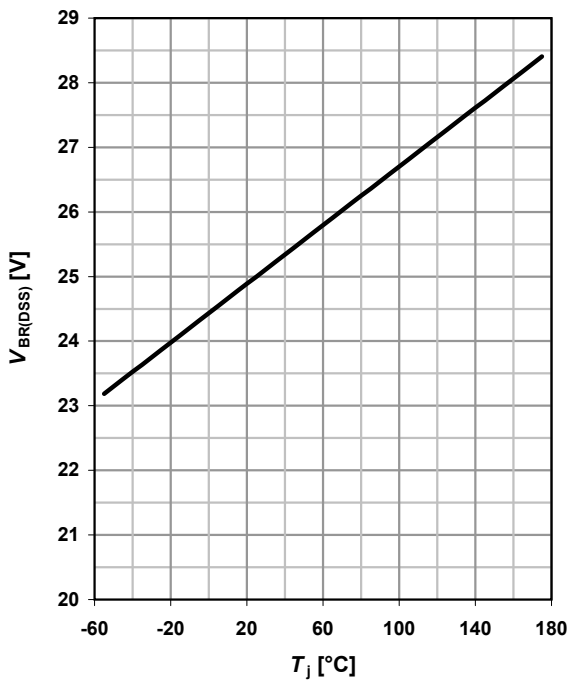
$V_{GS}=f(Q_{gate}); I_D=15 \text{ A pulsed}$

parameter:  $V_{DD}$



**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

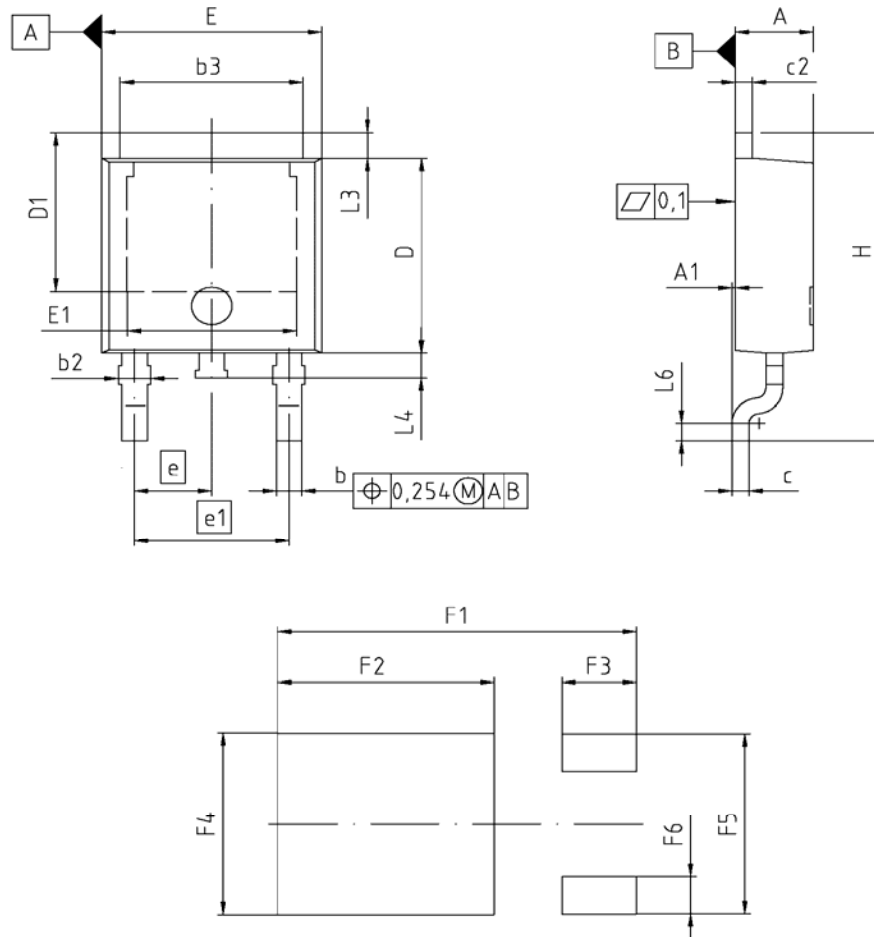


**16 Gate charge waveforms**



## Package Outline

## PG-T0252-3-11



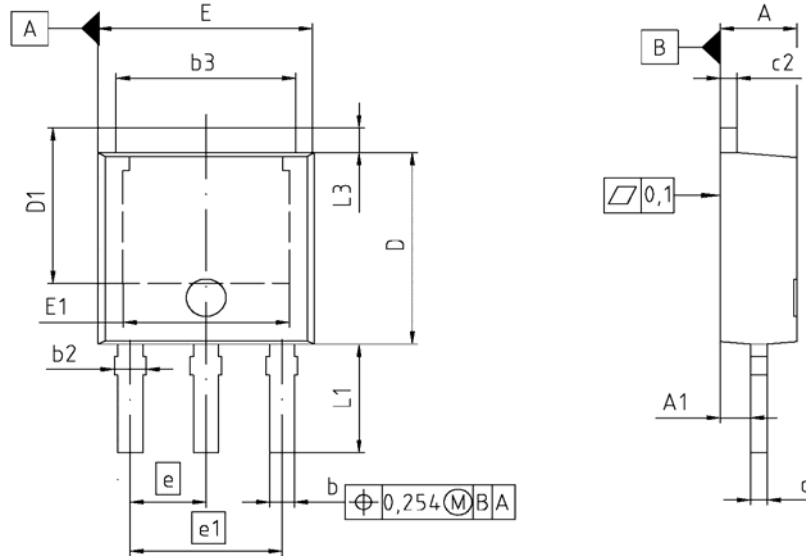
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.159	2.413	0.085	0.095
A1	0.000	0.150	0.000	0.006
b	0.635	0.889	0.025	0.035
b2	0.650	1.150	0.026	0.045
b3	5.004	5.500	0.197	0.217
c	0.457	0.580	0.018	0.023
c2	0.460	0.980	0.018	0.039
D	5.969	6.223	0.235	0.245
D1	5.020	5.842	0.198	0.230
E	6.400	6.731	0.252	0.265
E1	4.850	5.207	0.191	0.205
e	2.286		0.090	
e1	4.572		0.180	
N	3		3	
H	9.400	10.480	0.370	0.413
L3	0.900	1.143	0.035	0.045
L4	0.584	0.950	0.023	0.037
L6	0.510	0.686	0.020	0.027
F1	10.500	10.700	0.413	0.421
F2	6.300	6.500	0.248	0.256
F3	2.100	2.300	0.083	0.091
F4	5.700	5.900	0.224	0.232
F5	5.660	5.860	0.222	0.231
F6	1.100	1.300	0.043	0.051

<b>REFERENCE</b> JEDEC TO252
<b>SCALE</b> 0 2.0 4mm
<b>EUROPEAN PROJECTION</b> 
<b>ISSUE DATE</b> 21-09-2005
<b>FILE</b> TO252_1



## Package Outline

## PG-TO251-3-11



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.184	2.388	0.086	0.094
A1	0.000	0.150	0.000	0.006
b	0.635	0.889	0.025	0.035
b2	0.650	1.150	0.025	0.045
b3	5.004	5.500	0.197	0.217
c	0.460	0.580	0.018	0.023
c2	0.460	0.980	0.018	0.039
D	5.969	6.223	0.235	0.245
D1	5.020	5.320	0.198	0.209
E	6.400	6.731	0.252	0.265
E1	4.900	5.100	0.193	0.201
e	2.286		0.090	
e1	4.572		0.180	
N	3		3	
L1	3.400	3.600	0.134	0.142
L3	0.900	1.118	0.035	0.044

<b>REFERENCE</b> ..
<b>SCALE</b> 0 2.0 4mm
<b>EUROPEAN PROJECTION</b> 
<b>ISSUE DATE</b> 20-07-2005
<b>FILE</b> TO251_2

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