DATASHEET

HA-2400/883

PRAM Four-Channel Programmable Operational Amplifier

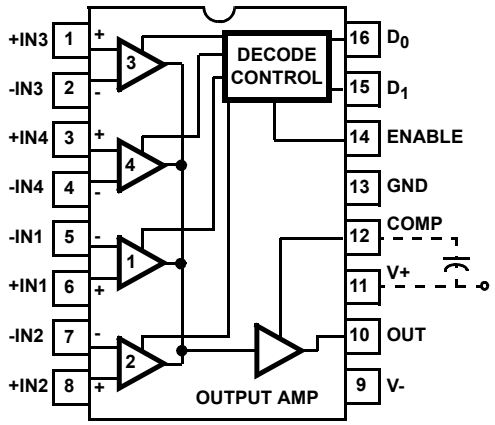
FN3926
Rev 0.00
April 9, 2012

HA-2400/883 is a four-channel programmable amplifier providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

Each channel of the HA-2400/883 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection and mathematical function designs. With 20V/µs slew rate, 20MHz gain bandwidth and low input bias currents makes this device an ideal building block for signal generators, active filters and data acquisition designs. Programmability, coupled with 9mV typical offset voltage and 50nA offset current, makes these amplifiers outstanding components for signal conditioning circuits.

Pin Configuration

HA1-2400/883
(CERDIP)
TOP VIEW)



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	None

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Digital Programmability
- High Slew Rate
  - Uncompensated . . . . . 20V/µs Min
  - Compensated . . . . . 6V/µs Min
- Wide Gain Bandwidth
  - Uncompensated . . . . . 20MHz Min
  - Compensated . . . . . 4MHz Min
- High Gain 50kV/V
- Low Offset Current 50nA
- Single Capacitor Compensation for Unity Gain
- DTL/TTL Compatible Inputs

Applications

- Single Selection/Multiplexing
- Op Amp Gain Stage
- Frequency Oscillator
- Filter Characteristics
- Add-Subtract Functions
- Integrator Characteristics
- Comparator Levels

Ordering Information

PART #	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA1-2400/883	HA1-2400/883	-55 to +125	16 Ld CERDIP	F16.3

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 45V
Differential Input Voltage . . . . . $\pm V_{SUPPLY}$
Voltage at Either Input Terminal . . . . . V+ to V-
Digital Input Voltage. . . . . -0.76V to +10V
Peak Output Current (Short Circuit Protected) . . . . . I_{SC} < ±33mA)
ESD Rating . . . . . <2000V

Recommended Operating Conditions

Temperature Range . . . . . -55°C to +125°C
Supply Voltage . . . . . +15V
Negative Supply Voltage . . . . . -15V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CerDIP Package (Note 1).	91	25

Internal Power Dissipation
Package Power Dissipation Limit at +75°C for $T_J \leq +175°C$
CerDIP Package 1.11W
Package Power Dissipation Derating Factor Above +75°C
CerDIP Package . . . . . 11.1mW/°C
Junction Temperature (T_J) . . . . . +175°C
Storage Temperature Range. . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = +15V, V- = -15V, R_S = 100Ω , R_L = 500kΩ, V_O = 0V, unless otherwise specified. Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4V, limits apply to each of the four channels, when addressed.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP (°C)	MIN	MAX	UNITS
Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25	-9	9	mV
			2, 3	+125, -55	-11	11	mV
Input Bias Current	$+I_B$	V_{CM} = 0V, $+R_S$ = 100kΩ, $-R_S$ = 100Ω	1	+25	-200	200	nA
			2, 3	+125, -55	-400	400	nA
	$-I_B$	V_{CM} = 0V, $+R_S$ = 100Ω, $-R_S$ = 100kΩ	1	+25	-200	200	nA
			2, 3	+125, -55	-400	400	nA
Input Offset Current	I_{IO}	V_{CM} = 0V, $+R_S$ = 100kΩ, $-R_S$ = 100kΩ	1	+25	-50	50	nA
			2, 3	+125, -55	-100	100	nA
Common Mode Range	+CMR	V+ = +6V, V- = -24V, V_{OUT} = -9V	1	+25	9	-	V
			2, 3	+125, -55	9	-	V
	-CMR	V+ = +24V, V- = -6V, V_{OUT} = +9V	1	+25	-	-9	V
			2, 3	+125, -55	-	-9	V
Large Signal Voltage Gain	A_V	V_{OUT} = -10V to +10V, R_L = 2kΩ	4	+25	50	-	kV/V
			5, 6	+125, -55	25	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +5V, V+ = +10V, V- = -20V, V_{OUT} = -5V	1	+25	80	-	dB
			2, 3	+125, -55	80	-	dB
	-CMRR	ΔV_{CM} = -5V, V+ = +20V, V- = -10V, V_{OUT} = +5V	1	+25	80	-	dB
			2, 3	+125, -55	80	-	dB
Output Voltage Swing	$+V_{OUT}$	R_L = 2kΩ	4	+25	10	-	V
			5, 6	+125, -55	10	-	V
	$-V_{OUT}$	R_L = 2kΩ	4	+25	-	-10	V
			5, 6	+125, -55	-	-10	V
Output Current	$+I_{OUT}$	V_{OUT} = +10V	4	+25	10	-	mA
	$-I_{OUT}$	V_{OUT} = -10V	4	+25	-	-10	mA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V+ = +15V, V- = -15V, R_S = 100Ω , R_L = 500kΩ, V_O = 0V, unless otherwise specified. Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4V, limits apply to each of the four channels, when addressed.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP (°C)	MIN	MAX	UNITS
Supply Current	$+I_{CC}$	V_{OUT} = 0V	1	+25	-	6	mA
			2, 3	+125, -55	-	7	mA
	$-I_{CC}$	V_{OUT} = 0V	1	+25	-6	-	mA
			2, 3	+125, -55	-7	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_{SUP} = ±5V V+ = +20V, V- = -15V V+ = +10V, V- = -15V	1	+25	74	-	dB
			2, 3	+125, -55	74	-	dB
	-PSRR	ΔV_{SUP} = ±5V V+ = +15V, V- = -20V V+ = +15V, V- = -10V	1	+25	74	-	dB
			2, 3	+125, -55	74	-	dB
Crosstalk	C_T	V_{IN} = ±10V	1	+25	-80	-	dB
Digital Logic Current	I_{IL}	V_{IL} = 0V	1	+25	-	1.5	mA
			2, 3	+125, -55	-	1.5	mA
	I_{IH}	V_{IH} = 5.0V	1	+25	-	1	µA
			2, 3	+125, -55	-	1	µA

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V+ = +15V, V- = -15V, R_L = 2kΩ , C_{LOAD} = 50pF, unless otherwise specified. Digital Inputs: V_{IL} = +0.5V, V_{IH} = +2.4V, limits apply to each of the four channels, when addressed.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMP (°C)	MIN	MAX	UNITS
Slew Rate (Note 2)	$+SR_1$	V_{OUT} = -5V to +5V	7	+25	6	-	V/µs
	$-SR_1$	V_{OUT} = +5V to -5V	7	+25	6	-	V/µs
Rise and Fall Time	t_{R1}	V_{OUT} = 0 to +200mV	7	+25	-	45	ns
	t_{F1}	V_{OUT} = 0 to -200mV	7	+25	-	45	ns
Overshoot	$+OS_1$	V_{OUT} = 0 to +200mV	7	+25	-	40	%
	$-OS_1$	V_{OUT} = 0 to -200mV	7	+25	-	40	%

NOTES:

2. A_V = +1, C_{COMP} = 15pF.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V+ = +15V, V- = -15V, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP (°C)	MIN	MAX	UNITS
Unity Gain Bandwidth	$UGBW_1$	A_V = +1V, C_{COMP} = 15pF, R_L = 2kΩ, C_L = 50pF	3	+25	4	-	MHz
Gain Bandwidth Product	$GBWP_2$	A_V = +10V, C_{COMP} = 0pF, R_L = 2kΩ, C_L = 50pF	3	+25	20	-	MHz
Full Power Bandwidth$_1$	$FPBW_1$	R_L = 2kΩ, A_V = +1V, V_O = ±10V, C_L = 50pF, C_{COMP} = 15pF	3, 4	+25	95	-	kHz
Full Power Bandwidth$_2$	$FPBW_2$	R_L = 2kΩ, A_V = +10V, V_O = ±10V, C_L = 50pF, C_{COMP} = 0pF	3, 4	+25	300	-	kHz
Settling Time	T_{SET1}	A_V = +1V, C_{COMP} = 15pF, R_L = 2kΩ, C_L = 50pF, V_O = $10V_{P-P}$, to 0.1% F.V., Logic Control = +5.0V	3	+25	-	2.5	µs

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Characterized at: V+ = +15V, V- = -15V, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMP (°C)	MIN	MAX	UNITS
Slew Rate (Note 5)	$+SR_2$	V_{OUT} = -5V to +5V, R_L = 2kΩ, C_L = 50pF, A_V = +10V, C_{COMP} = 0pF	3	+25	20	-	V/µs
	$-SR_2$	V_{OUT} = +5V to -5V, R_L = 2kΩ, C_L = 50pF, A_V = +10V, C_{COMP} = 0pF	3	+25	20	-	V/µs
Output Delay	T_{DEL}	R_L = 2kΩ, C_L = 50pF, C_{COMP} = 15pF, V_{IN} = +5V	3	+25	-	250	ns
Minimum Closed Loop Stability	CLS_1	R_L = 2kΩ, C_L = 50pF, C_{COMP} = 15pF	3	+25	1	-	V/V
	CLS_2	R_L = 2kΩ, C_L = 50pF, C_{COMP} = 0pF	3	+25	10	-	V/V

NOTES:

3. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
4. FPBW = Slew Rate/($2\pi V_{PEAK}$).
5. A_V = +10, C_{COMP} = 0pF.

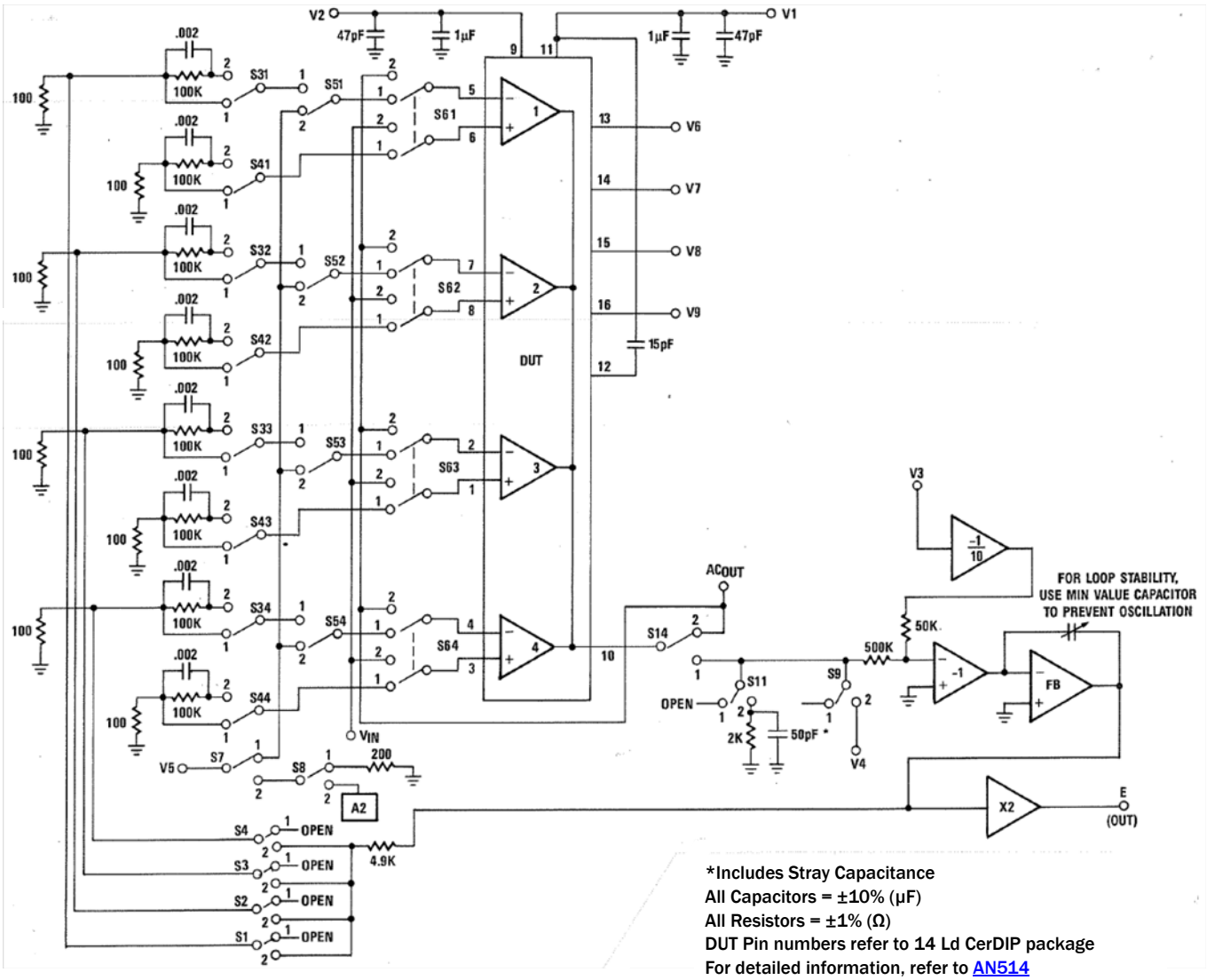
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 6), 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C and D Endpoints	1

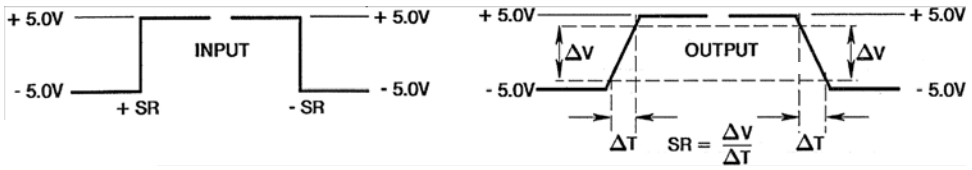
NOTES:

6. PDA applies to Subgroup 1 only.
7. The subgroup assignments of the parameters in these tables were patterned after DESC SMD #5962-87783.

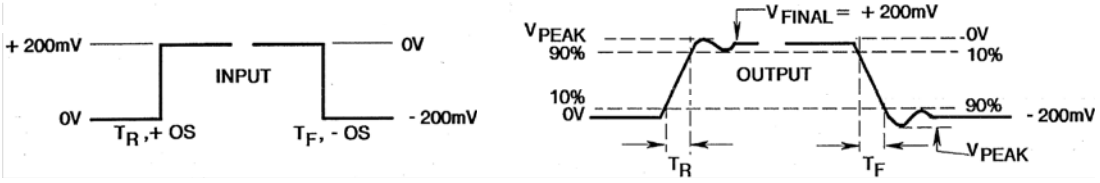
Test Circuit



Test Waveforms



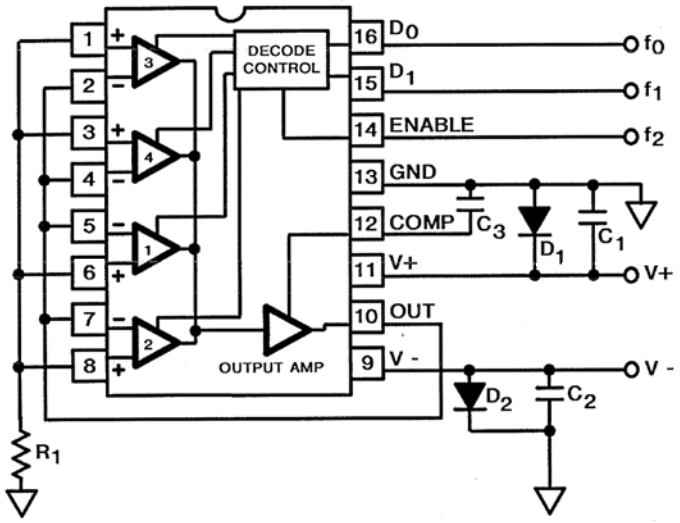
SLEW RATE WAVEFORMS



OVERSHOOT, RISE AND FALL TIME WAVEFORMS

Burn-In Circuit

HA-2400/883 CERAMIC DIP

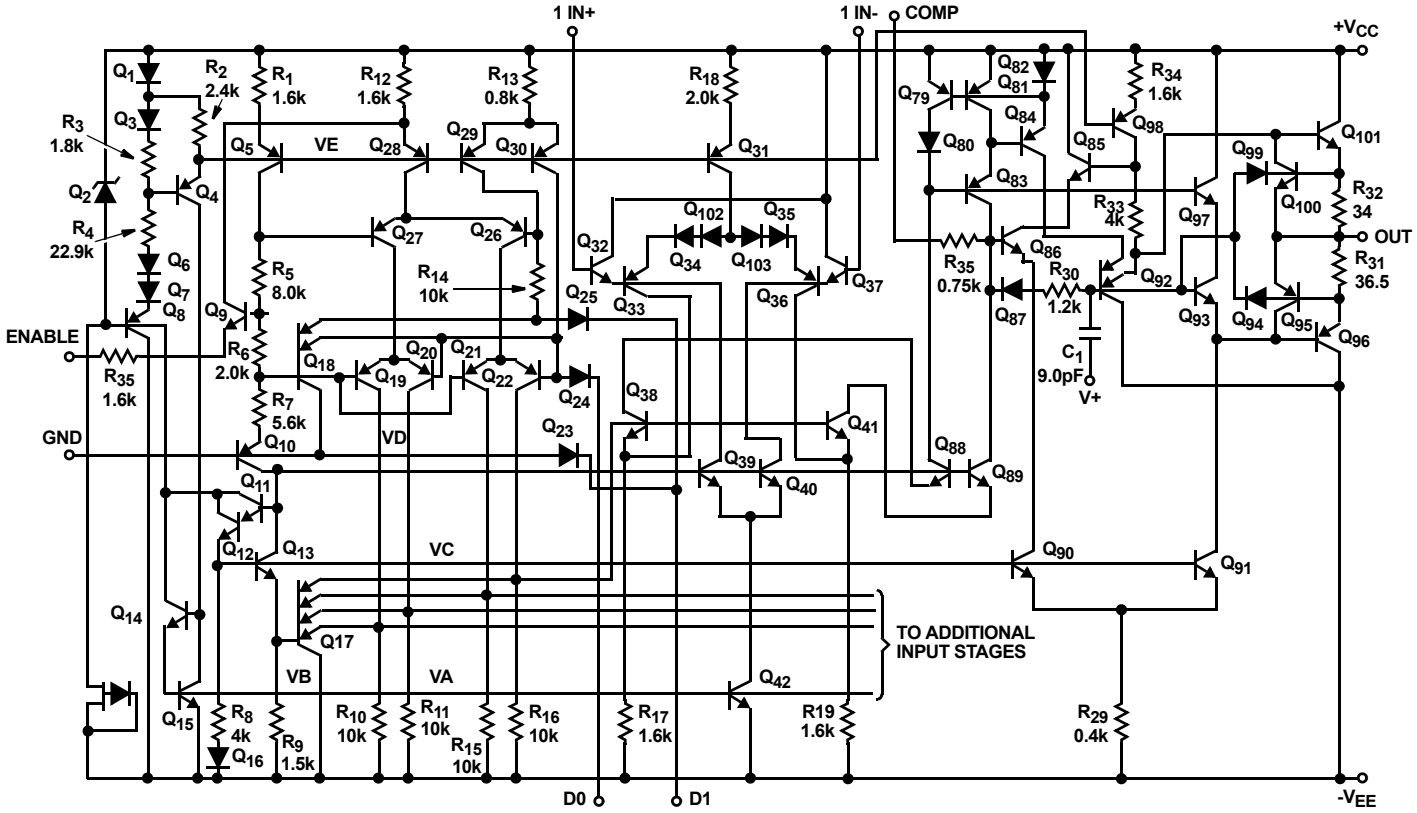


NOTES:

R_1 = 100kΩ/socket, 5% 1/4W (min)
$C_1 = C_2$ = 0.01µF per socket (min) or 0.1µF per row (min)
C_3 = 0.001µF per socket, 10%
D_1, D_2 = 1N4002 or equivalent per board
| (V+) - (V-) | = 30V

f_0 = 100kHz
f_1 = 50kHz
f_2 = 25kHz
} 50% Duty Cycle

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:

88mils x 67mils x 19mils ± 1mil
2240µm x 1710µm x 483µm ± 25.4µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:

$0.7 \times 10^5 A/cm^2$

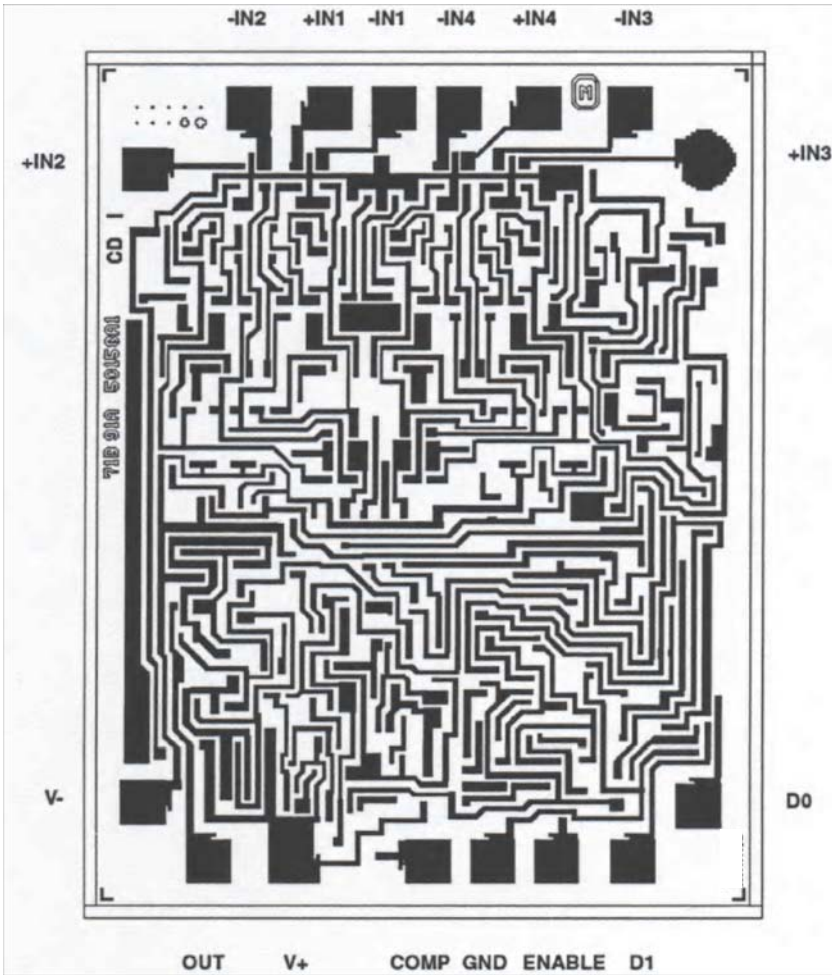
SUBSTRATE POTENTIAL (Powered Up): Unbiased

TRANSISTOR COUNT: 251

PROCESS: Bipolar Dielectric Isolation

Metallization Mask Layout

HA-2400/883



The information contained in this section has been developed through characterization and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Typical Performance Characteristics

Devices Characterized at: : $V_S = \pm 15V$, $V_{IL} = +0.5V$, $V_{IH} = +2.4V$. Values apply to each of the four channels, when addressed

PARAMETER	TEST CONDITIONS	TEMP. (°C)	TYP	UNITS
Offset Voltage	$V_{CM} = 0V$	+25	4	mV
Bias Current	$V_{CM} = 0V$	+25	50	nA
Offset Current	$V_{CM} = 0V$	+25	5	nA
Input Resistance		+25	30	MΩ
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = 20V_{P-P}$	+25	150	kV/V
Common Mode Rejection Ratio	$V_{CM} = \pm 5V_{DC}$	Full	100	dB
Gain Bandwidth Product	$R_L = 2k\Omega$, $C_L = 50pF$, $C_{COMP} = 0pF$, $A_V = +10V$	+25	40	MHz
Unity Gain Bandwidth	$R_L = 2k\Omega$, $C_L = 50pF$, $C_{COMP} = 15pF$, $A_V = +1V$	+25	8	MHz
Output Voltage Swing	$R_L = 2k\Omega$	Full	±12	V
Output Current	$V_{OUT} = \pm 10V$	+25	20	mA
$FPBW_1$	$V_P = 10V$ (Note 8)	+25	475	kHz
$FPBW_2$	$V_P = 10V$ (Note 8)	+25	125	kHz
Rise Time	$R_L = 2k\Omega$, $C_L = 50pF$, $C_{COMP} = 15pF$, $A_V = +1V$	+25	20	ns
Overshoot	$R_L = 2k\Omega$, $C_L = 50pF$, $C_{COMP} = 15pF$, $A_V = +1V$	+25	25	%
$Slew\ Rate_1$	$A_V = +1V/V$	+25	8	V/µs
$Slew\ Rate_2$	$A_V = +10V/V$	+25	30	V/µs
$Settling\ Time_1$	$V_O = 10V_{P-P}$ to 0.1%	+25	1.5	µs
Digital Logic Current	$V_{IN} = +5.0V$	Full	5	nA
	$V_{IN} = 0V$	Full	1	mA
Output Delay	To 10% of Final Value	+25	100	ns
Crosstalk	Unselected Input to Output, $V_{IN} = \pm 10V_{DC}$	+25	-110	dB
Supply Current	Not Loaded	+25	4.8	mA
PSRR	$\Delta V_S = \pm 10V$	Full	90	dB

NOTE:

8. FPBW = Slew Rate/$(2\pi V_{PEAK})$.

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Typical Performance Curves

$V\pm = \pm15V$, $T_A = +25°C$, unless otherwise specified.

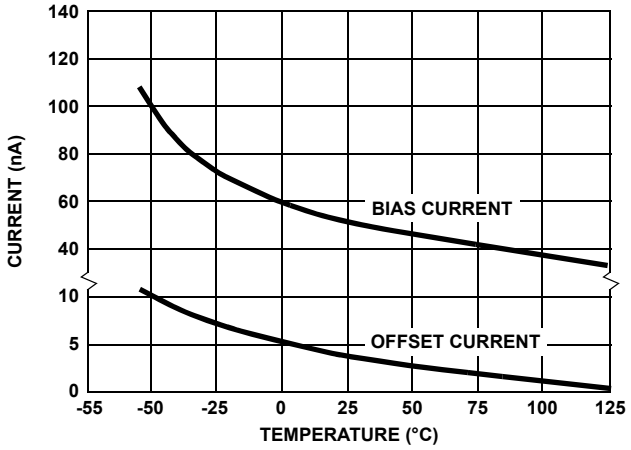

FIGURE 1. INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE

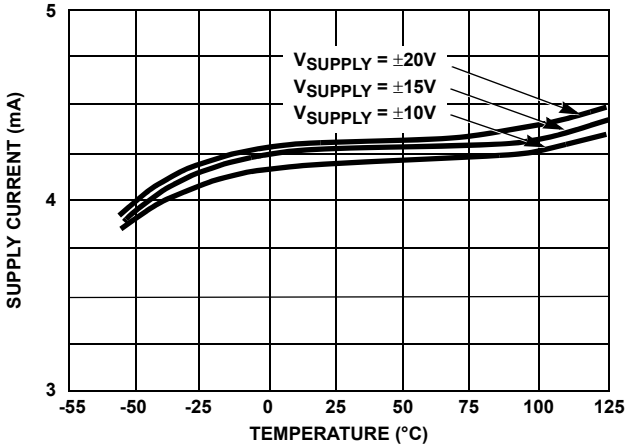

FIGURE 2. POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE

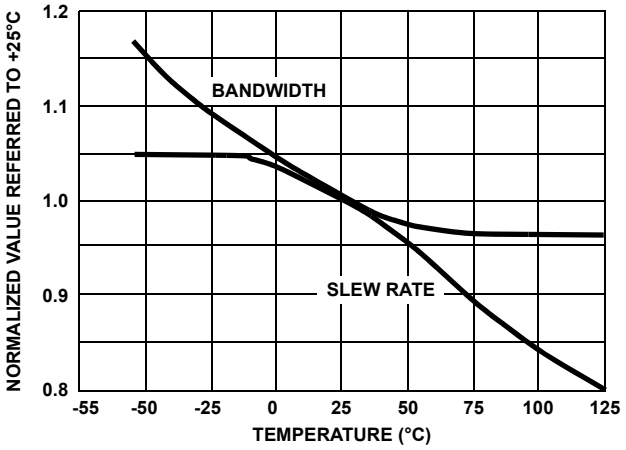

FIGURE 3. NORMALIZED AC PARAMETERS vs TEMPERATURE

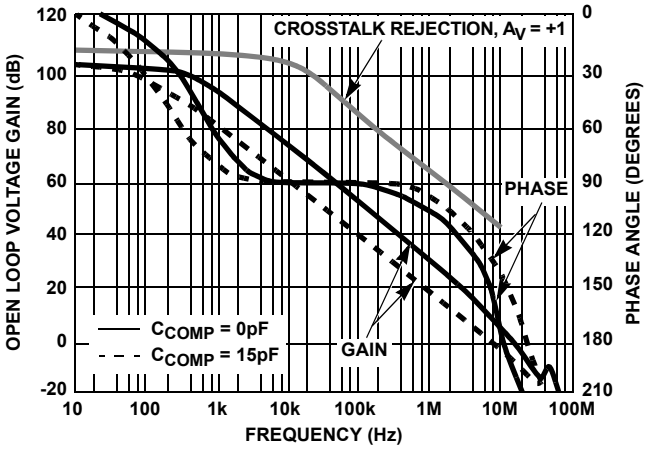

FIGURE 4. OPEN LOOP FREQUENCY AND PHASE RESPONSE

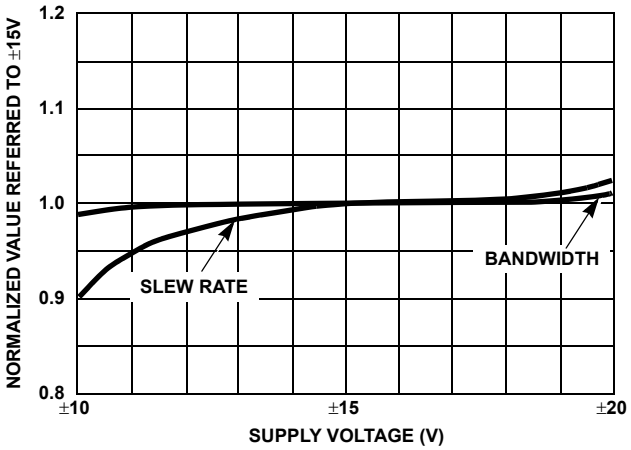

FIGURE 5. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

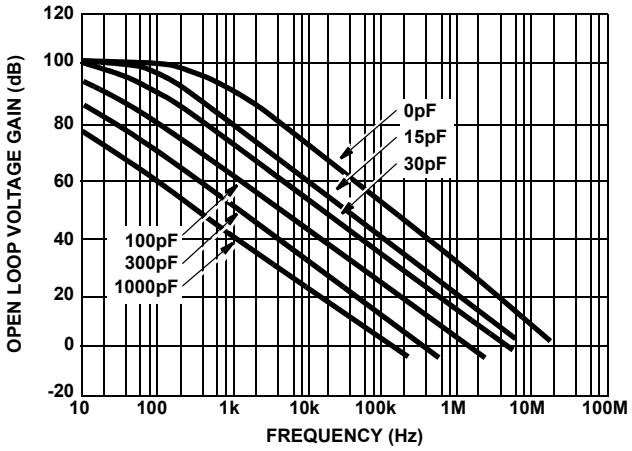

FIGURE 6. FREQUENCY RESPONSE vs C_{COMP}

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Typical Performance Curves

$V\pm = \pm15V$, $T_A = +25°C$, unless otherwise specified. **(Continued)**

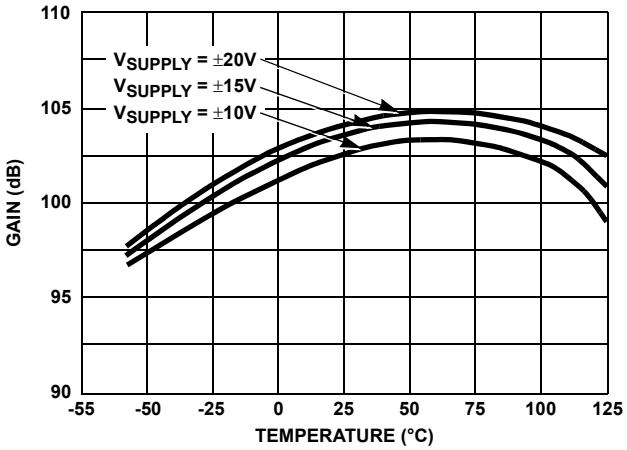


FIGURE 7. OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

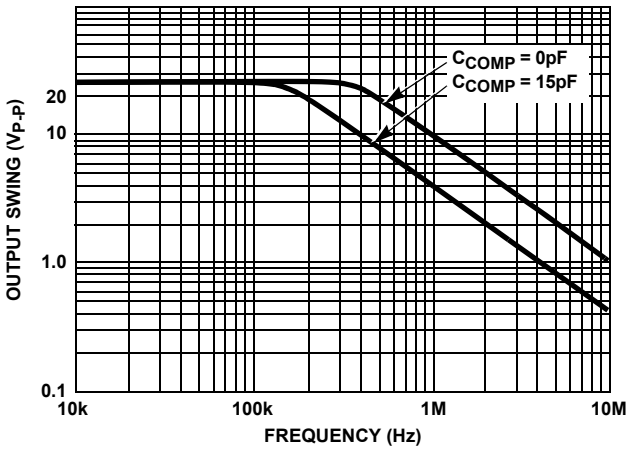


FIGURE 8. OUTPUT VOLTAGE SWING

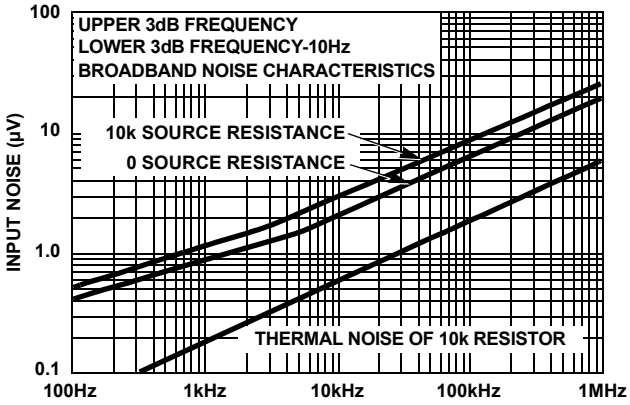


FIGURE 9. EQUIVALENT INPUT NOISE vs BANDWIDTH

Typical Applications (See Application Note AN514)

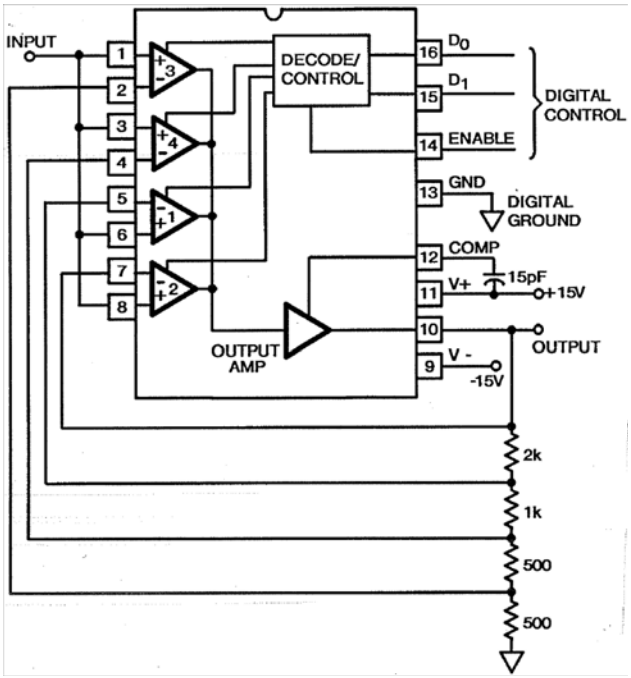
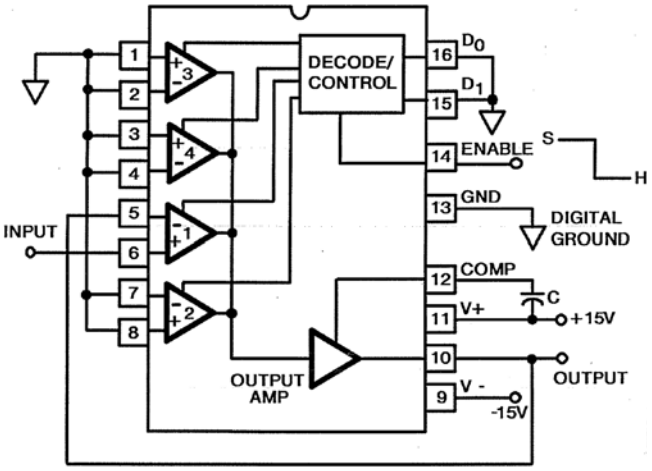


FIGURE 10. AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



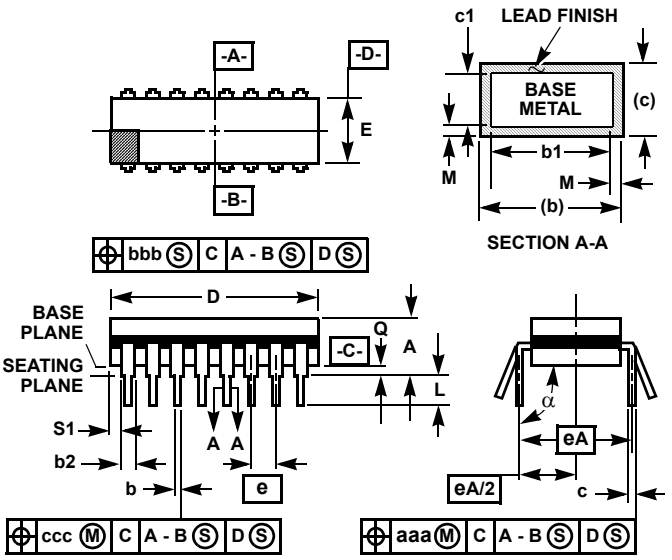
Sample Charging Rate $\frac{I_1}{C}$ V/s — $I_1 \approx 150 \times 10^{-6}$A

Hold Drift Rate $\frac{I_2}{C}$ V/s — $I_2 \approx 200 \times 10^{-9}$A @ +25°C; $\approx 600 \times 10^{-9}$A @ -55°C; $\approx 100 \times 10^{-9}$A @ +125°C

Switch Pedestal Error $\frac{Q}{C}$ V — $Q \approx 2 \times 10^{-12}$ Coulombs

FIGURE 11. SAMPLE AND HOLD

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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