# HA-2542

70MHz, High Slew Rate, High Output Current Operational Amplifier

FN2899
Rev.5.00
August 2002

The HA-2542 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Intersil D.I. technology this amplifier offers 350V/µs slew rate, 70MHz gain bandwidth, and ±100mA output current. Application of this device is further enhanced through stable operation down to closed loop gains of 2.

For additional flexibility, offset null and frequency compensation controls are included in the HA-2542 pinout.

The capabilities of the HA-2542 are ideally suited for high speed coaxial cable driver circuits where low gain and high output drive requirements are necessary. With 5.5MHz full power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse video amplifiers. Other applications utilizing the HA-2542 advantages include wideband amplifiers and fast sample-hold circuits.

For more information on the HA-2542, please refer to Application Note AN552 (Using the HA-2542), or Application Note AN556 (Thermal Safe-Operating-Areas for High Current Op Amps).

**For a lower power version of this product, please see the HA-2842 data sheet.**

## Part Number Information

| PART NUMBER | TEMP. RANGE ($^{o}$C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| HA3-2542-5 | 0 to 75 | 14 Ld PDIP | E14.3 |

## Features

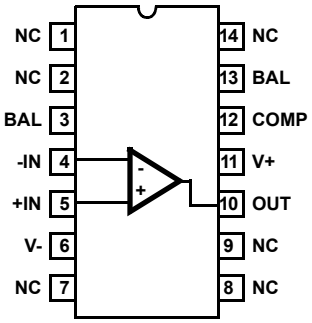
- Stable at Gains of 2 or Greater
- Gain Bandwidth . . . . . 70MHz
- High Slew Rate . . . . . .300V/µs (Min)
- High Output Current . . . . . .100mA (Min)
- Power Bandwidth . . . . . 5.5MHz (Typ)
- Output Voltage Swing . . . . . ±10V (Min)
- Monolithic Bipolar Dielectric Isolation Construction

## Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

## Pinout

**HA-2542 (PDIP)**
TOP VIEW



## Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) . . . . . .35V
Differential Input Voltage . . . . . .6V
Output Current . . . . . 50mA Continuous, 125mA$_{PEAK}$

## Operating Conditions

Temperature Range
HA-2542-5 . . . . . 0$^{o}$C to 75$^{o}$C

## Thermal Information

| Thermal Resistance (Typical, Note 2) | $\theta_{JA}$ ($^{o}$C/W) | $\theta_{JC}$ ($^{o}$C/W) |
|---|---|---|
| PDIP Package . . . . . | 95 | N/A |

Maximum Junction Temperature (Plastic Package, Note 1) . . 150$^{o}$C
Maximum Storage Temperature Range . . . . . -65$^{o}$C to 150$^{o}$C
Maximum Lead Temperature (Soldering 10s) . . . . . .300$^{o}$C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below 150$^{o}$C for plastic packages. By using Application Note AN556 on Safe Operating Area equations, along with the thermal resistances, proper load conditions can be determined. Heatsinking will be required in many applications. See the "Application Information" section to determine if heat sinking is required for your application.
2. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

$V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP. ($^{o}$C) | HA-2542-5 0$^{o}$C TO 75$^{o}$C | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **INPUT CHARACTERISTICS** | | | | | | |
| Offset Voltage | | 25 | - | 5 | 10 | mV |
| | | Full | - | 8 | 20 | mV |
| Average Offset Voltage Drift | | Full | - | 14 | - | $\mu V/^{o}C$ |
| Bias Current | | 25 | - | 15 | 35 | $\mu A$ |
| | | Full | - | 26 | 50 | $\mu A$ |
| Average Bias Current Drift | | Full | - | 45 | - | $nA/^{o}C$ |
| Offset Current | | 25 | - | 1 | 7 | $\mu A$ |
| | | Full | - | - | 9 | $\mu A$ |
| Input Resistance | | 25 | - | 100 | - | $k\Omega$ |
| Input Capacitance | | 25 | - | 1 | - | pF |
| Common Mode Range | | Full | $\pm10$ | - | - | V |
| Input Noise Voltage | 0.1Hz to 100Hz | 25 | - | 2.2 | - | $\mu V_{P-P}$ |
| Input Noise Density | f = 1kHz, $R_G = 0\Omega$ | 25 | - | 10 | - | $nV/\sqrt{Hz}$ |
| Input Noise Current Density | f = 1kHz, $R_G = 0\Omega$ | 25 | - | 3 | - | $pA/\sqrt{Hz}$ |
| **TRANSFER CHARACTERISTICS** | | | | | | |
| Large Signal Voltage Gain | $V_O = \pm10V$ | 25 | 10 | 30 | - | kV/V |
| | | Full | 5 | 20 | - | kV/V |
| Common Mode Rejection Ratio | $V_{CM} = \pm10V$ | Full | 70 | 100 | - | dB |
| Minimum Stable Gain | | 25 | 2 | - | - | V/V |
| Gain Bandwidth Product | $A_V = 100$ | 25 | - | 70 | - | MHz |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output Voltage Swing | | Full | $\pm10$ | $\pm11$ | - | V |
| Output Current (Note 3) | | 25 | 100 | - | - | mA |
| Output Resistance | | 25 | - | 5 | - | $\Omega$ |

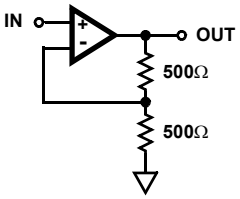
**Electrical Specifications** $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP. ($^oC$) | HA-2542-5 $0^oC$ TO $75^oC$ | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Full Power Bandwidth (Note 4) | $V_{PEAK}$ = 10V | 25 | 4.7 | 5.5 | - | MHz |
| Differential Gain (Note 5) | | 25 | - | 0.1 | - | % |
| Differential Phase (Note 5) | | 25 | - | 0.2 | - | Degree |
| Harmonic Distortion (Note 7) | | 25 | - | <0.04 | - | % |
| **TRANSIENT RESPONSE** (Note 6) | | | | | | |
| Rise Time | | 25 | - | 4 | - | ns |
| Overshoot | | 25 | - | 25 | - | % |
| Slew Rate | | 25 | 300 | 350 | - | V/µs |
| Settling Time | 10V Step to 0.1% | 25 | - | 100 | - | ns |
| | 10V Step to 0.01% | 25 | - | 200 | - | ns |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Supply Current | | 25 | - | 30 | - | mA |
| | | Full | - | 31 | 40 | mA |
| Power Supply Rejection Ratio | $V_S = \pm5V$ to $\pm15V$ | Full | 70 | 79 | - | dB |

NOTES:

3. $R_L = 50\Omega$, $V_O = \pm5V$, Output duty cycle must be reduced for $I_{OUT} > 50mA$ (e.g. ≤50% duty cycle for 100mA).
4. Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW $= \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
5. Differential gain and phase are measured at 5MHz with a 1V differential input voltage.
6. Refer to Test Circuits section of this data sheet.
7. $V_{IN} = 1V_{RMS}$; f = 10kHz; $A_V = 10$.

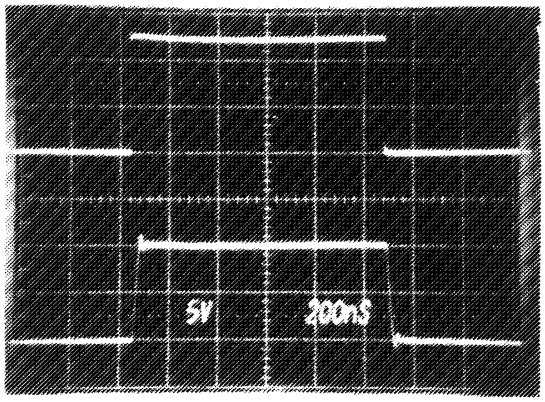
## *Test Circuits and Waveforms*




NOTES:

8. $V_S = \pm15V$.
9. $A_V = +2$.
10. $C_L \leq 10pF$.

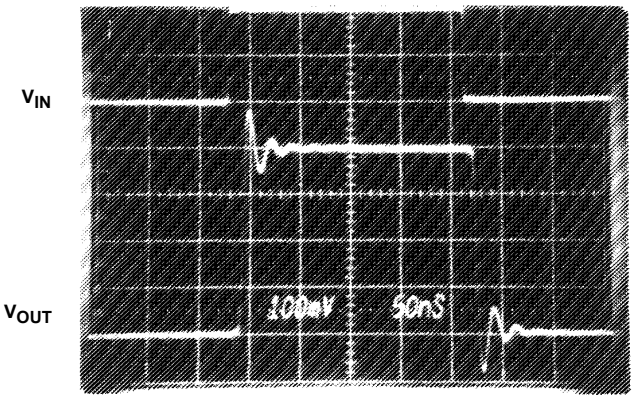
**TEST CIRCUIT**




Vertical Scale: $V_{IN}$ = 2.0V/Div., $V_{OUT}$ = 5.0V/Div.
Horizontal Scale: 200ns/Div.

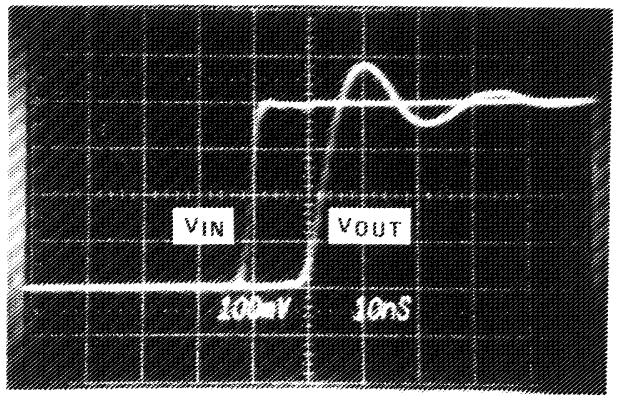
**LARGE SIGNAL RESPONSE**

## *Test Circuits and Waveforms* (Continued)



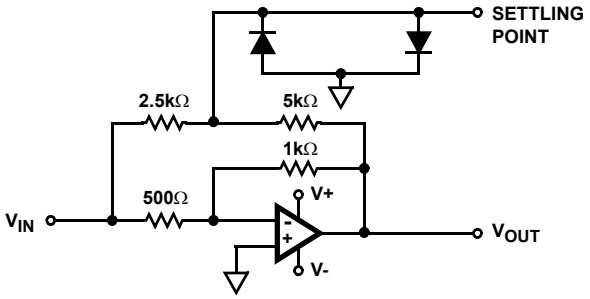

Vertical Scale: 100mV/Div.
Horizontal Scale: 50ns/Div.

**SMALL SIGNAL RESPONSE**




Vertical Scale: 100mV/Div.
Horizontal Scale: 10ns/Div.
$V_S = \pm 15V$, $R_L = 1k\Omega$. Propagation delay variance is negligible over full temperature range.

**PROPAGATION DELAY**

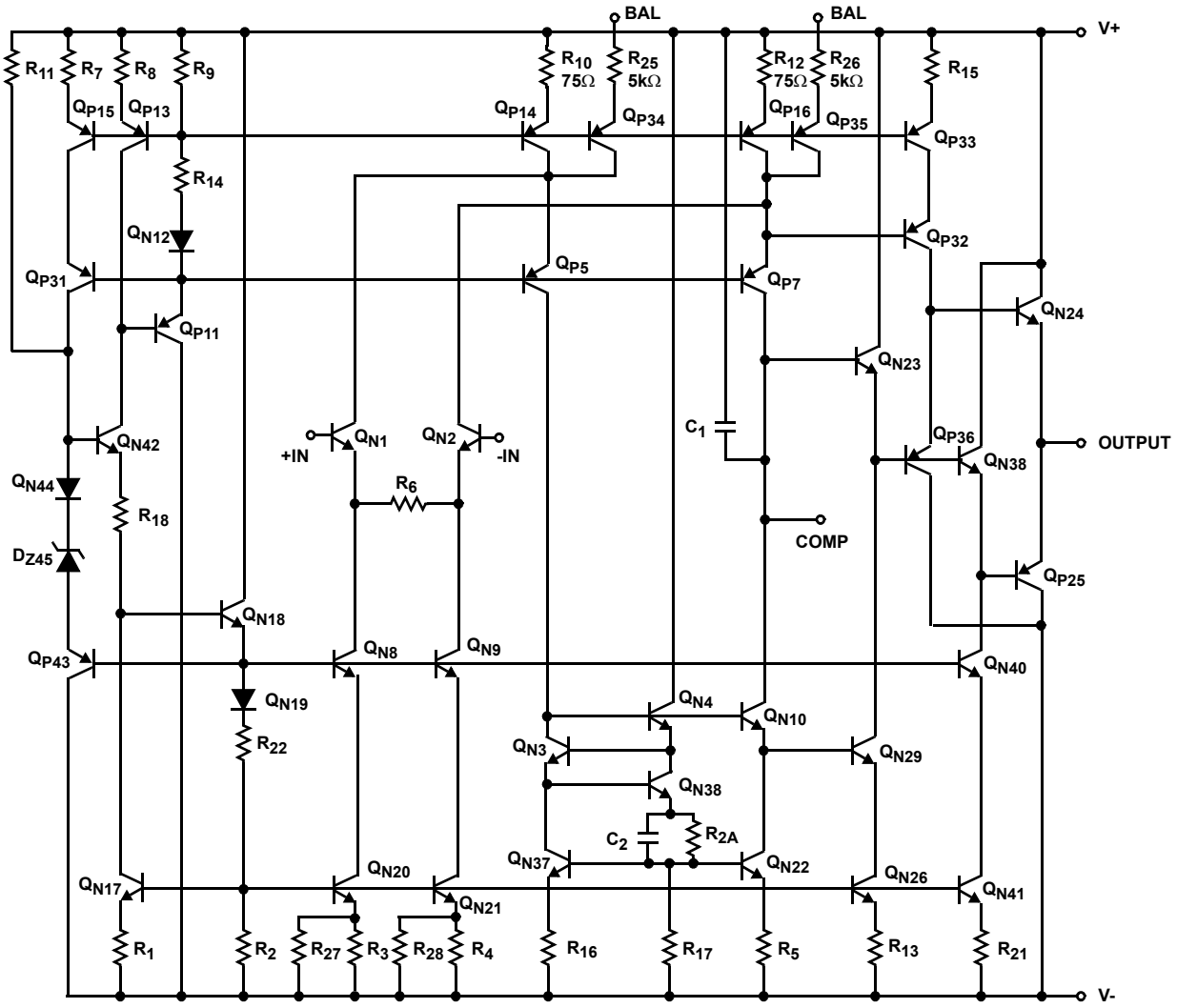



**SETTLING TIME TEST CIRCUIT** (SEE NOTES 11 - 15.)

NOTES:

11. $A_V = -2$.
12. Feedback and summing resistors must be matched (0.1%).
13. HP5082-2810 clipping diodes recommended.
14. Tektronix P6201 FET probe used at settling point.
15. For 0.01% settling time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.

## Schematic Diagram




## Application Information (Refer to Application Note AN552 for Further Information)

The Intersil HA-2542 is a state of the art monolithic device which also approaches the “ALL-IN-ONE” amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2542 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

The applications shown in Figures 2 through Figure 4 demonstrate the HA-2542 at gains of +100 and +2 and as a video cable driver for small signals.

### Power Dissipation Considerations

At high output currents, especially with the PDIP package, care must be taken to ensure that the Maximum Junction Temperature ($T_J$, see “Absolute Maximum Ratings” table) is not exceeded. As an example consider the HA-2542 in the PDIP package, with a required output current of 20mA at $V_{OUT}$ = 5V. The power dissipation is the quiescent power (1.2W = 30V x 40mA) plus the power dissipated in the output stage ($P_{OUT}$ = 200mW = 20mA x (15V - 5V)), or a total of 1.4W. The thermal resistance ($\theta_{JA}$) of the PDIP package is 100°C/W, which increases the junction temperature by 140°C over the ambient temperature ($T_A$). Remaining below $T_{JMAX}$ requires that $T_A$ be restricted to ≤ 10°C (150°C - 140°C). Heatsinking would be required for operation at ambient temperatures greater than 10°C.

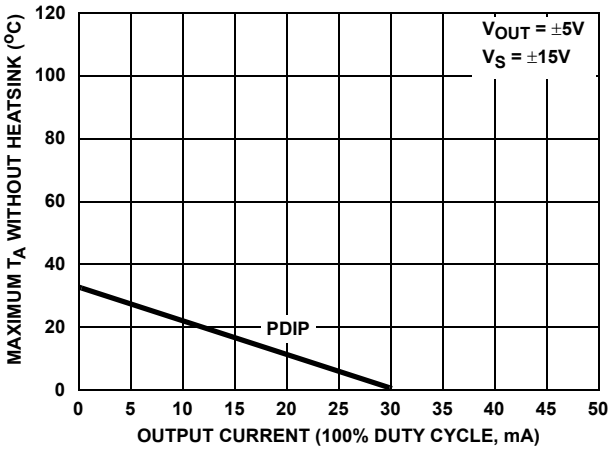



**FIGURE 1. MAXIMUM OPERATING TEMPERATURE vs OUTPUT CURRENT**

Allowable output power can be increased by decreasing the quiescent dissipation via lower supply voltages.

For more information please refer to Application Note AN556, “Thermal Safe Operating Areas for High Current Op Amps”.

### *Prototyping Guidelines*

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane: 2) connecting unused pins (NC) to the ground: 3) mounting feedback components on Teflon standoffs and or locating these components as close to the device as possible: 4) placing power supply decoupling capacitors from device supply pins to ground.

### *Frequency Compensation*

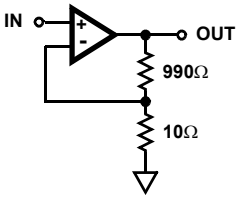
The HA-2542 may be externally compensated with a single capacitor to ground. This provides the user the additional flexibility in tailoring the frequency response of the amplifier. A guideline to the response is demonstrated on the typical performance curve showing the normalized AC parameters versus compensation capacitance. It is suggested that the user check and tailor the accurate compensation value for each application. As shown additional phase margin is achieved at the loss of slew rate and bandwidth.

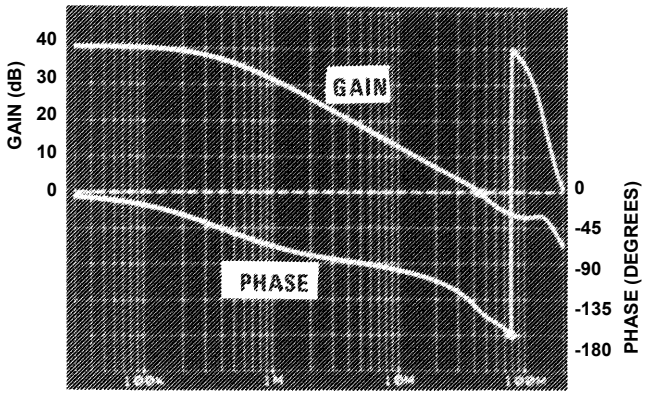
For example, for a voltage gain of +2 (or -1) and a load of 500pF/2kΩ, 20pF is needed for compensation to give a small signal bandwidth of 30MHz with 40° of phase margin. If a full power output voltage of ±10V is needed, this same configuration will provide a bandwidth of 5MHz and a slew rate of 200V/µs.

If maximum bandwidth is desired and no compensation is needed, care must be given to minimize parasitic capacitance at the compensation pin. In some cases where minimum gain applications are desired, bending up or totally removing this pin may be the solution. In this case, care must also be given to minimize load capacitance.

For wideband positive unity gain applications, the HA-2542 can also be over-compensated with capacitance greater than 30pF to achieve bandwidths of around 25MHz. This over-compensation will also improve capacitive load handling or lower the noise bandwidth. This versatility along with the ±100mA output current makes the HA-2542 an excellent high speed driver for many power applications.

## *Typical Applications*



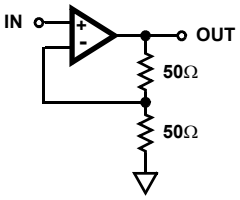



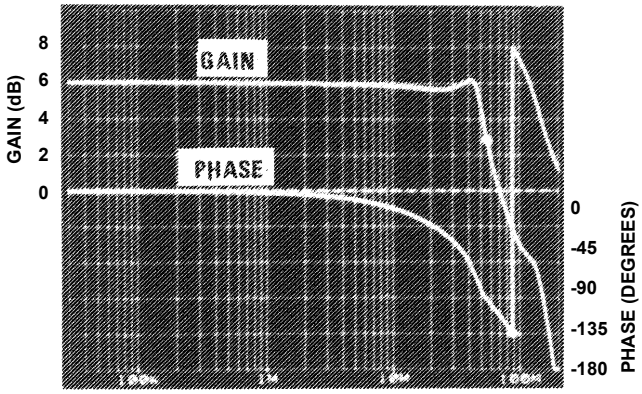

Frequency (0dB) = 44.9MHz,
Phase Margin (0dB) = 40°

**FREQUENCY RESPONSE**

**FIGURE 2. NONINVERTING CIRCUIT ($A_{VCL}$ = 100)**

## *Typical Applications* (Continued)

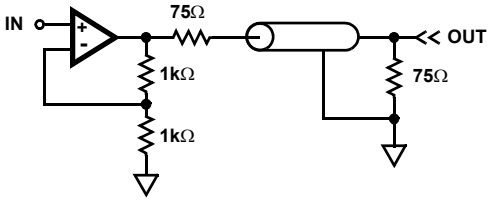


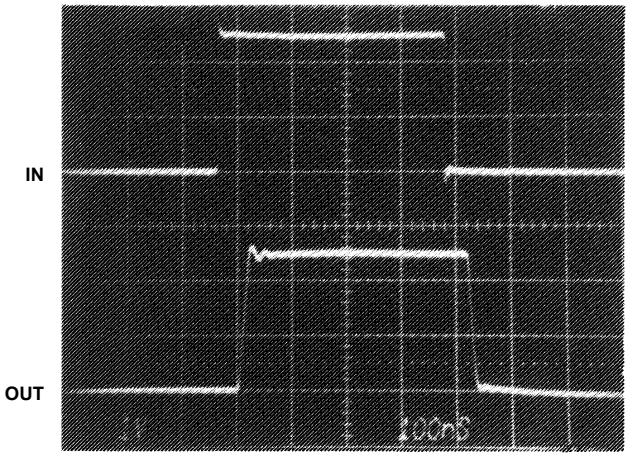




Frequency (dB) = 56MHz, Phase Margin (3dB) = 40°

FREQUENCY RESPONSE

**FIGURE 3. NONINVERTING CIRCUIT ($A_{VCL}$ = 2)**

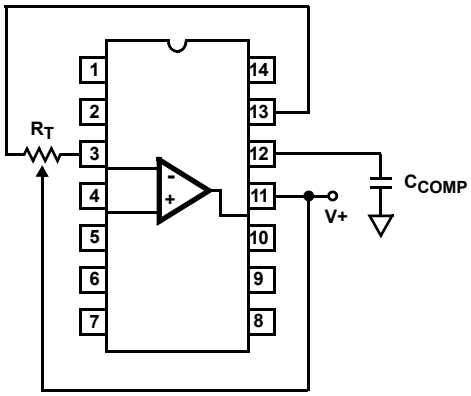



1V/Div.; 100ns/Div.

PULSE RESPONSE

**FIGURE 4. VIDEO CABLE DRIVER ($A_{VCL}$ = 2)**




NOTES:

16. Suggested compensation scheme 5pF - 20pF.
17. Tested Offset Adjustment Range is $|V_{OS}$ +1mV| minimum referred to output.
18. Typical range is ±20mV with $R_T$ = 5kΩ.

**FIGURE 5. SUGGESTED OFFSET VOLTAGE ADJUSTMENT AND FREQUENCY COMPENSATION**

## *Typical Performance Curves*

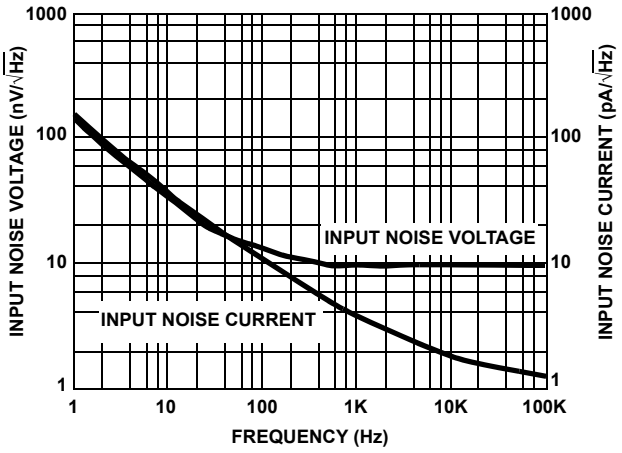



FIGURE 6. INPUT NOISE VOLTAGE AND INPUT NOISE CURRENT vs FREQUENCY

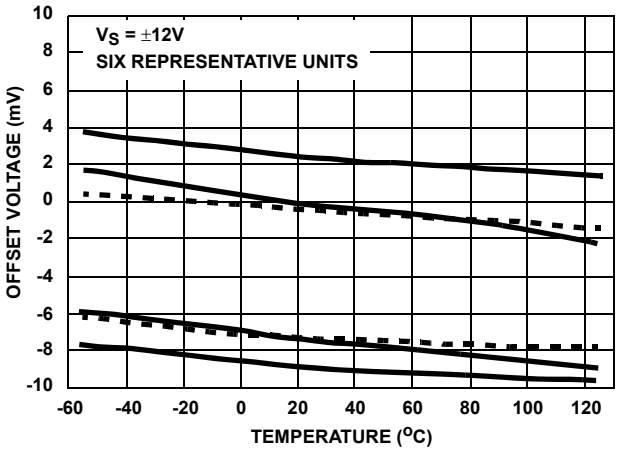



FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE

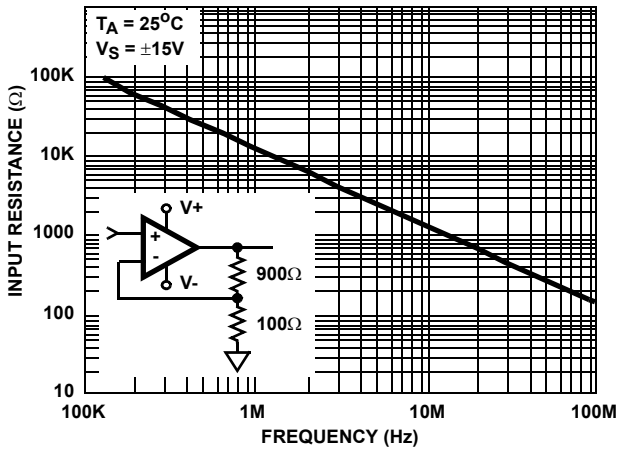



FIGURE 8. INPUT RESISTANCE vs FREQUENCY

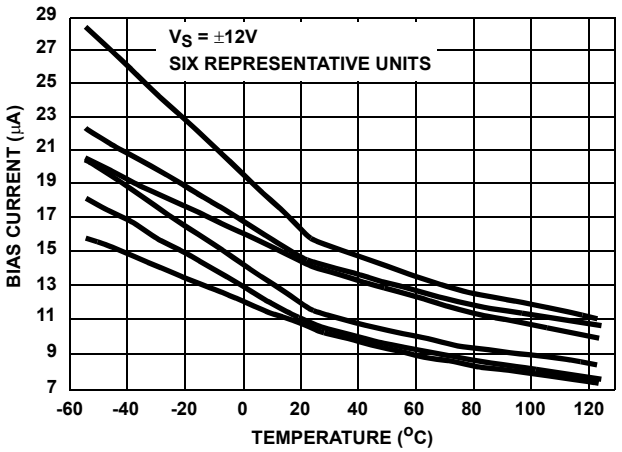



FIGURE 9. BIAS CURRENT vs TEMPERATURE

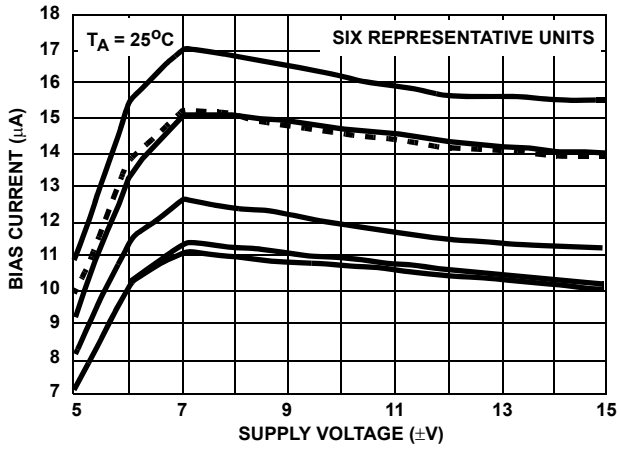



FIGURE 10. BIAS CURRENT vs SUPPLY VOLTAGE

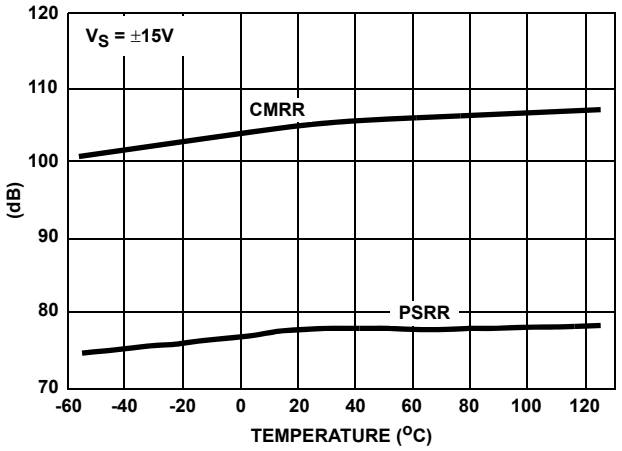



FIGURE 11. PSRR AND CMRR vs TEMPERATURE

## *Typical Performance Curves* (Continued)

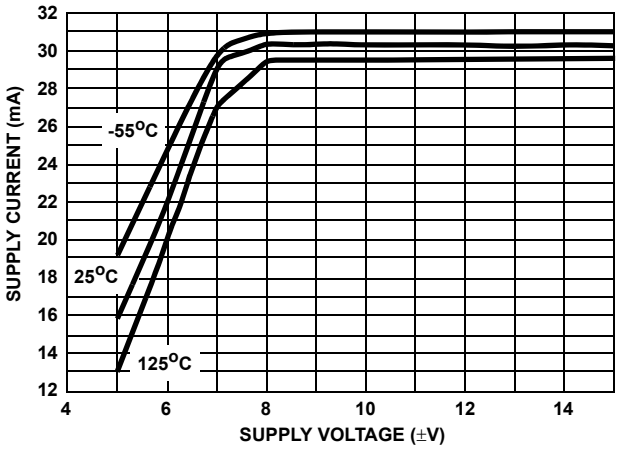



FIGURE 12. SUPPLY CURRENT vs SUPPLY VOLTAGE, AT VARIOUS TEMPERATURES

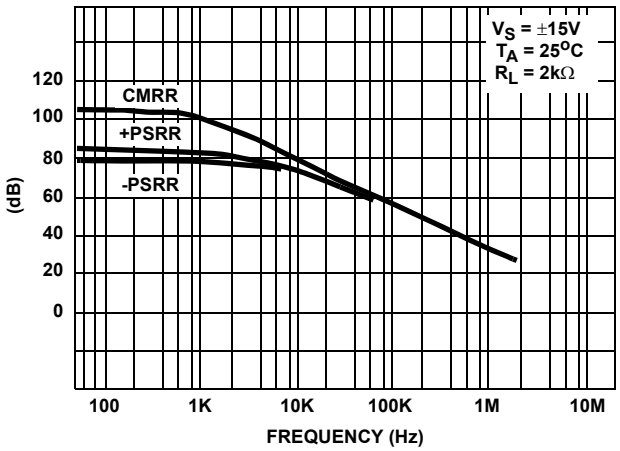



FIGURE 13. PSRR AND CMRR vs FREQUENCY

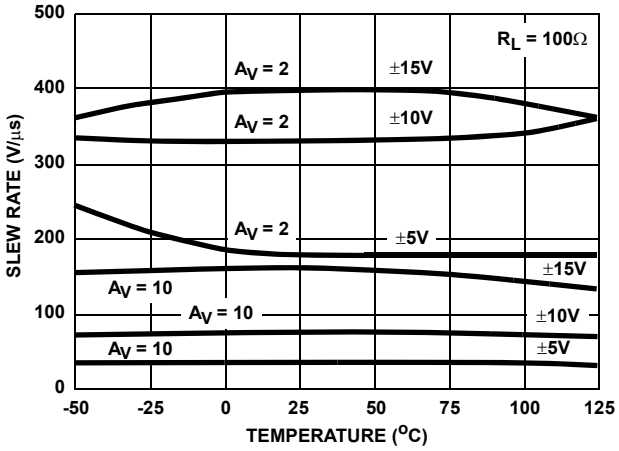



FIGURE 14. SLEW RATE vs TEMPERATURE AT VARIOUS SUPPLY VOLTAGES

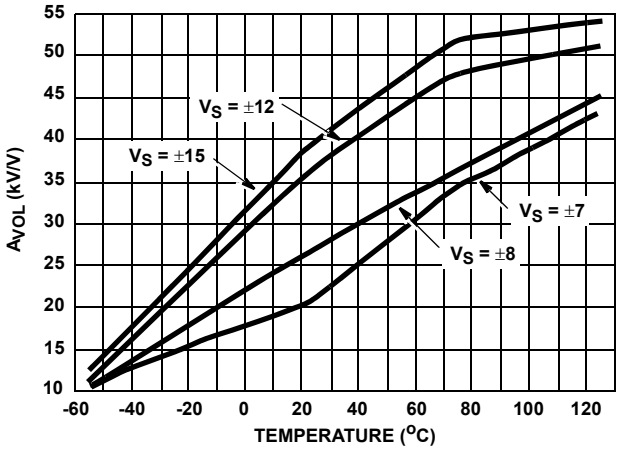



FIGURE 15. OPEN LOOP GAIN vs TEMPERATURE, AT VARIOUS SUPPLY VOLTAGES

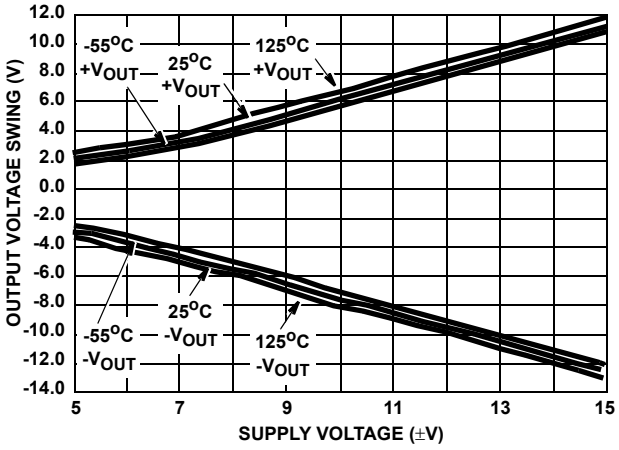



FIGURE 16. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE, AT VARIOUS TEMPERATURES

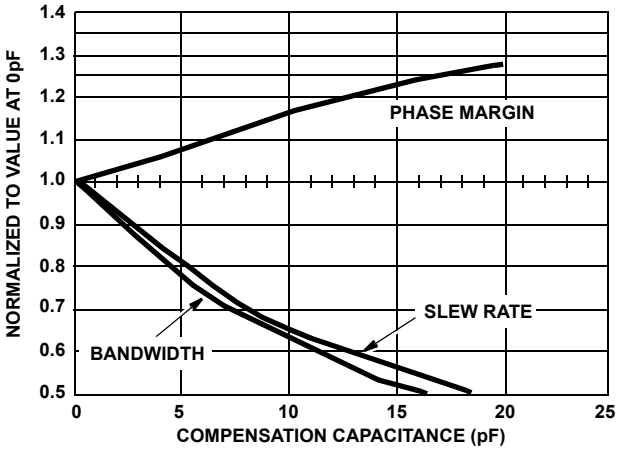



FIGURE 17. NORMALIZED AC PARAMETERS vs COMPENSATION CAPACITANCE

## *Typical Performance Curves* (Continued)

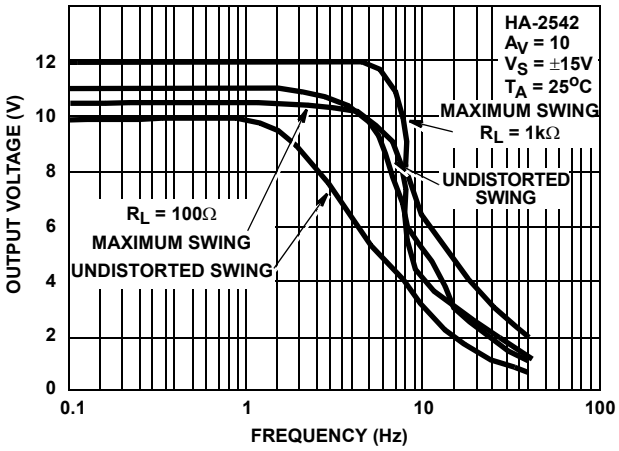



FIGURE 18. OUTPUT VOLTAGE SWING vs FREQUENCY

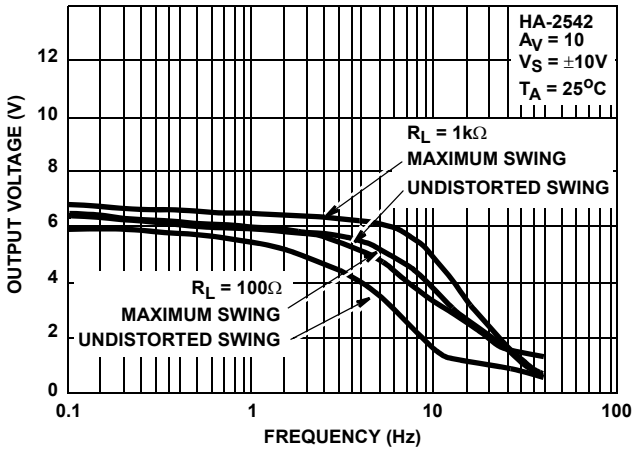



FIGURE 19. OUTPUT VOLTAGE SWING vs FREQUENCY

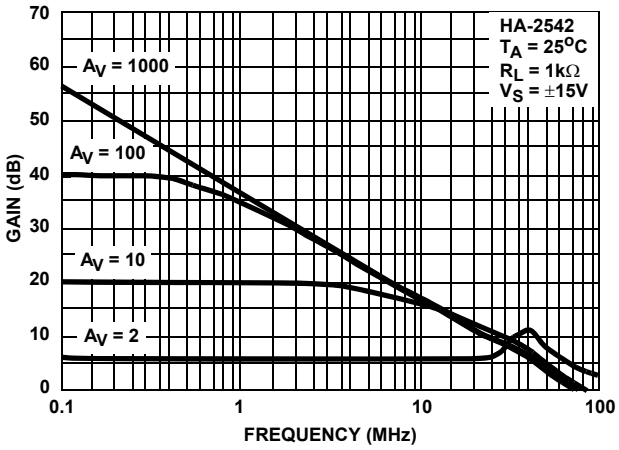



FIGURE 20. FREQUENCY RESPONSE CURVES

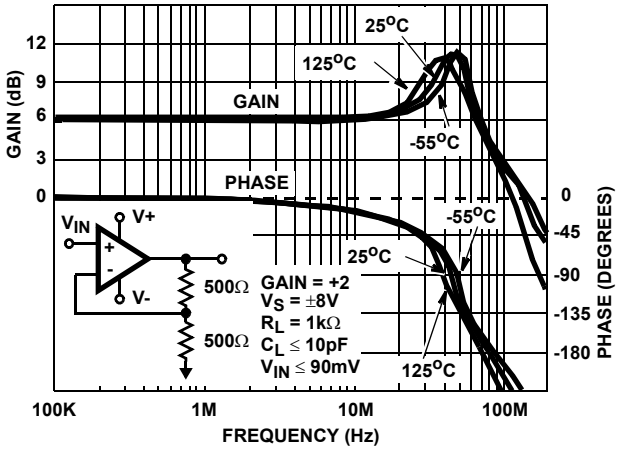



FIGURE 21. HA-2542 CLOSED LOOP GAIN vs TEMPERATURE

## Die Characteristics

**DIE DIMENSIONS:**

106 mils x 73 mils x 19 mils
2700µm x 1850µm x 483µm

**METALLIZATION:**

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

**PASSIVATION**

Type: Nitride ($Si_3N_4$) over Silox ($SiO_2$, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

**SUBSTRATE POTENTIAL (POWERED UP):**

V-

**TRANSISTOR COUNT:**

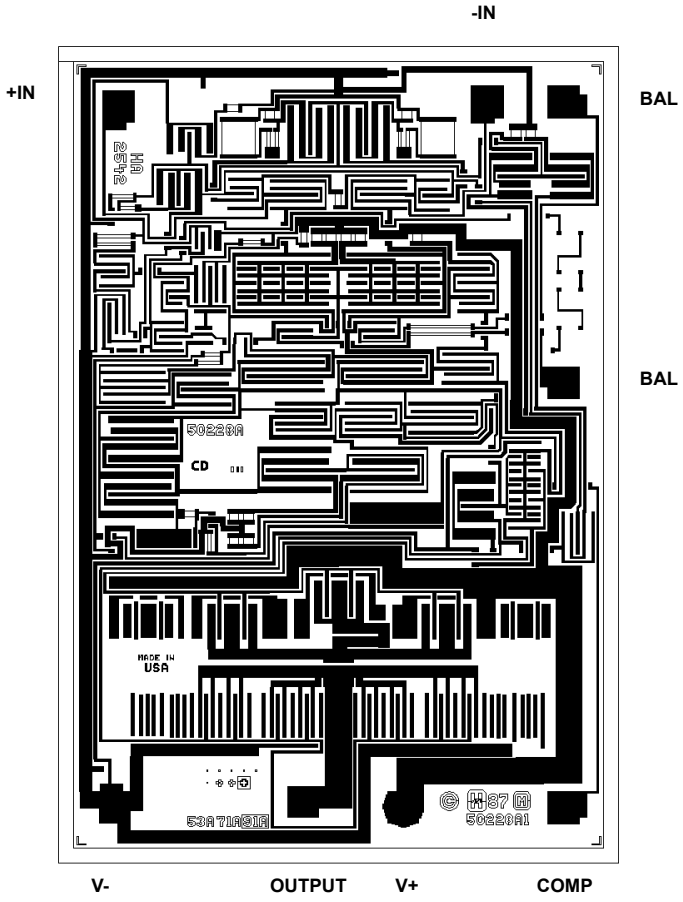
43

**PROCESS:**

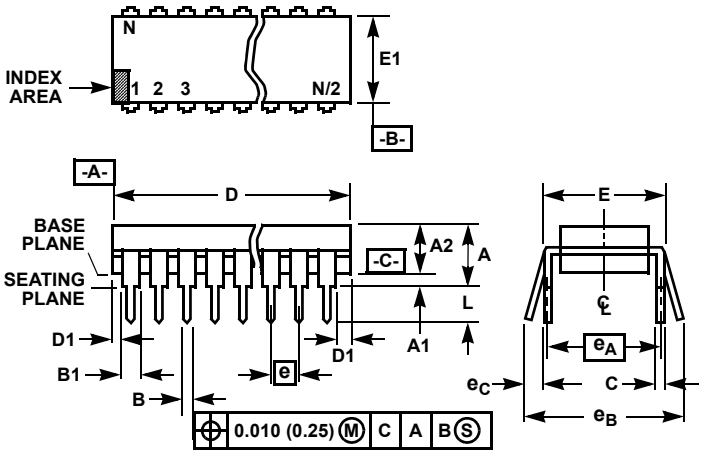
Bipolar Dielectric Isolation

## Metallization Mask Layout

**HA-2542**



## *Dual-In-Line Plastic Packages (PDIP)*




NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $e_A$ are measured with the leads constrained to be perpendicular to datum -C-.
7. $e_B$ and $e_C$ are measured at the lead tips with the leads unconstrained. $e_C$ must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E14.3** (JEDEC MS-001-AA ISSUE D)
**14 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.15 | 1.77 | 8 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.735 | 0.775 | 18.66 | 19.68 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| $e_A$ | 0.300 BSC | | 7.62 BSC | | 6 |
| $e_B$ | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 14 | | 14 | | 9 |

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