HA13631T

CD-ROM Combo Driver

HITACHI

ADE-207-320 (Z)
1st Edition
Feb. 2000

Description

The HA13631T is combination of Spindle, Forcus, Tracking, Slide, Tray designed for CD-ROM and have following functions and features.

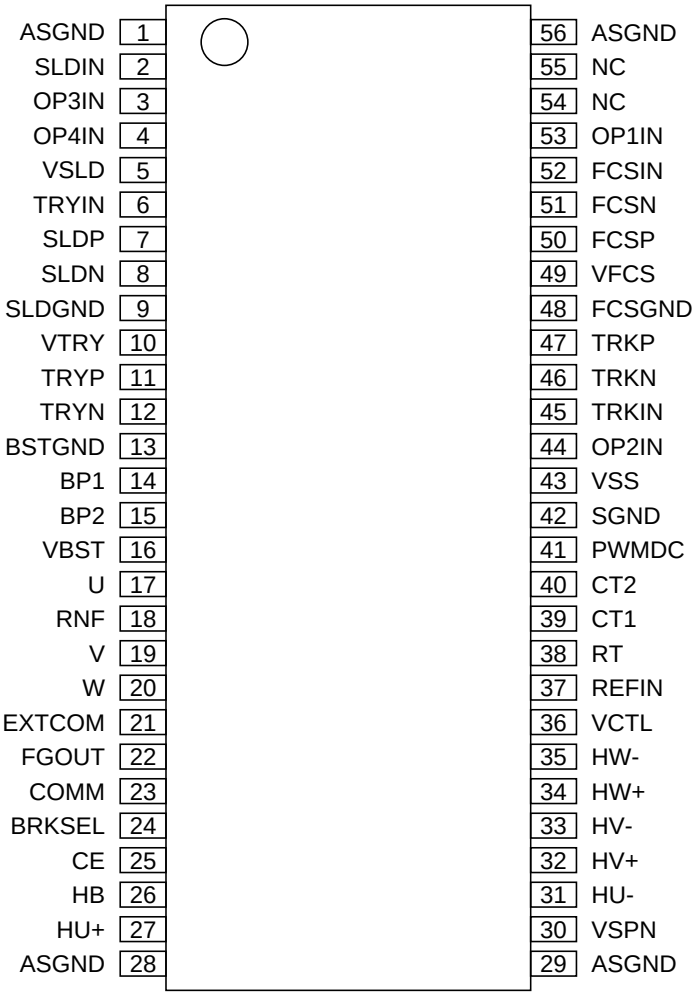
Functions

- 1.5 A spindle driver
- 0.75 A focus driver
- 0.75 A tracking driver
- 1.0 A slide driver
- 0.75 A tray driver
- Over temperature shut down (OTSD)

Features

- Corresponds to both of sensor motor and sensorless motor
- All direct PWM drive
- Low on resistance
- Low power dissipation
- Small thin surface mount package

Pin Arrangement



(Top view)

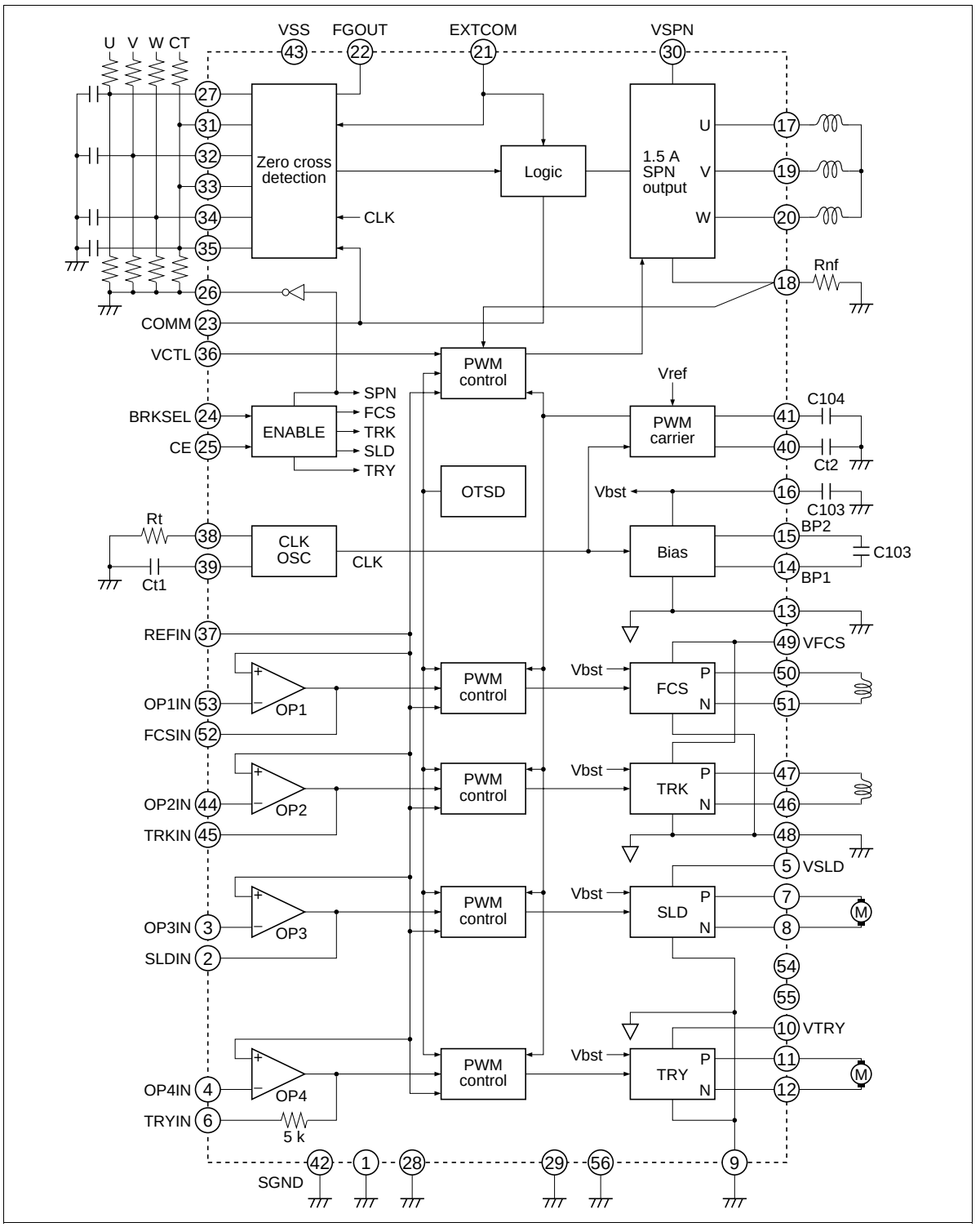
Pin Description

Pin No.	Pin Name	Function
1	ASGND	Actuator small signal GND
2	SLDIN	SLD driver control input
3	OP3IN	Inverted input of OP amp. 3 for SLD driver control
4	OP4IN	Inverted input of OP amp. 4 for TRY driver control
5	VSLD	SLD driver power supply
6	TRYIN	TRY driver control input
7	SLDP	SLD driver P output
8	SLDN	SLD driver N output
9	SLDGND	SLD and TRY driver GND
10	VTRY	TRY driver power supply
11	TRYP	TRY driver P output
12	TRYN	TRY driver N output
13	BSTGND	Booster GND
14	BP1	Booster pumping capacitor connection
15	BP2	Booster pumping capacitor connection
16	VBST	Booster output pin. This circuit generates a voltage about two times of the VSPN pin.
17	U	U phase output
18	RNF	SPN driver current detection
19	V	V phase output
20	W	W phase output
21	EXTCOM	COMM signal on/off control and FGOUT switching. (Refer to the Timing Chart)
22	FGOUT	FG output (Refer to the Timing Chart) open drain
23	COMM	Start-up clock input pin for sensorless (Refer to the Timing Chart)
24	BRKSEL	To select the brake mode (Refer to the Truth Table)
25	CE	Chip enable (Refer to the Truth Table)
26	HB	Hall bias switch
27	HU+	U-phase Hall +input, and U-phase B-EMF connection pin for sensorless
28	ASGND	Actuator small signal GND
29	ASGND	Actuator small signal GND
30	VSPN	SPN driver power supply
31	HU–	U-phase Hall –input, and center tap connection pin for sensorless
32	HV+	V-phase Hall +input, and V-phase B-EMF connection pin for sensorless
33	HV–	V-phase Hall –input, and center tap connection pin for sensorless

Pin Description (cont)

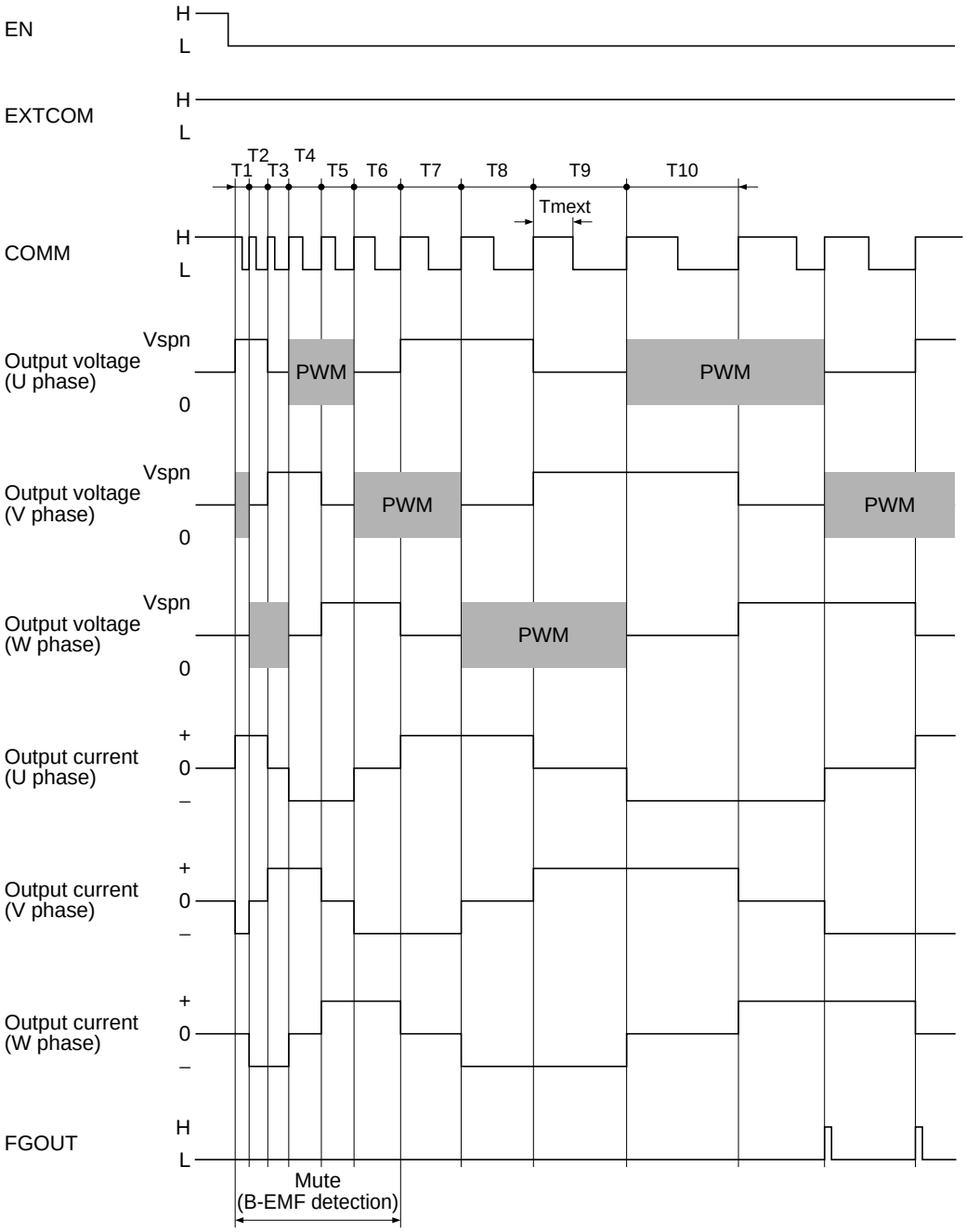
Pin No.	Pin Name	Function
34	HW+	W-phase Hall +input, and W-phase B-EMF connection pin for sensorless
35	HW–	W-phase Hall –input, and center tap connection pin for sensorless
36	VCTL	SPN driver control input
37	REFIN	Reference voltage for control inputs. Common to all drivers.
38	RT	Reference voltage. The IC's internal reference current is determined by this voltage and the external resistor Rt.
39	CT1	Time constant for clock oscillation. The oscillator frequency is determined by the external capacitor and resistor Ct1 and Rt.
40	CT2	Time constant for PWM carrier. The amplitude is determined by the value of the external capacitor Ct1.
41	PWMDC	Phase compensation connection pin for matching PWM carrier DC level with REFIN
42	SGND	SPN small signal GND
43	VSS	Control block power supply. 5 V
44	OP2IN	Inverted input of OP amp. 2 for TRK driver control
45	TRKIN	TRK driver control input
46	TRKN	TRK driver N output
47	TRKP	TRK driver P output
48	FCSGND	FCS and TRK driver GND
49	VFCS	FCS driver power supply
50	FCSP	FCS driver P output
51	FCSN	FCS driver N output
52	FCSN	FCS driver control input
53	OP1IN	Inverted input of OP amp. 1 for FCS driver control
54	NC	No connection
55	NC	No connection
56	ASGND	Actuator small signal GND

Block Diagram



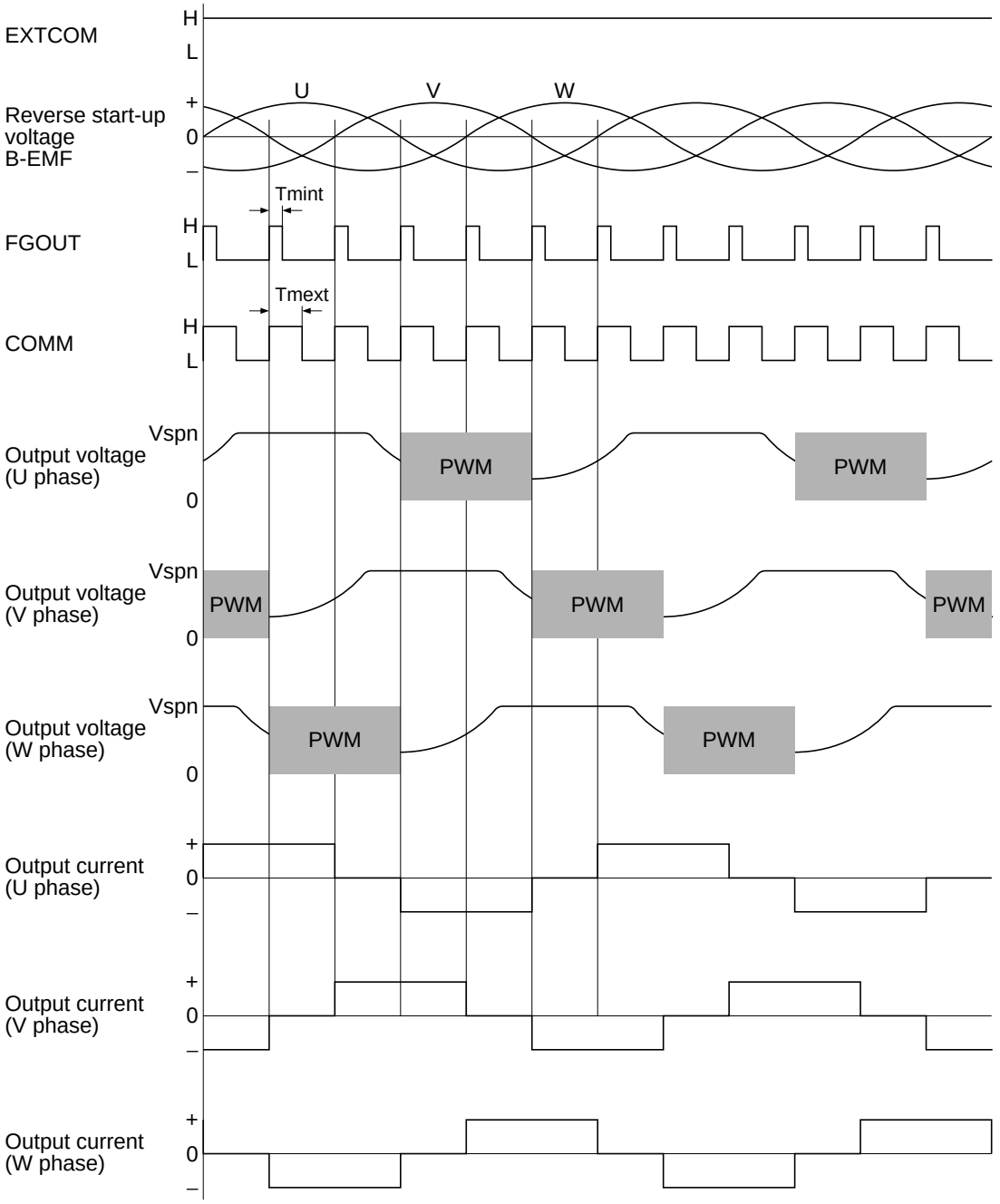
Timing Chart

1. Start-up



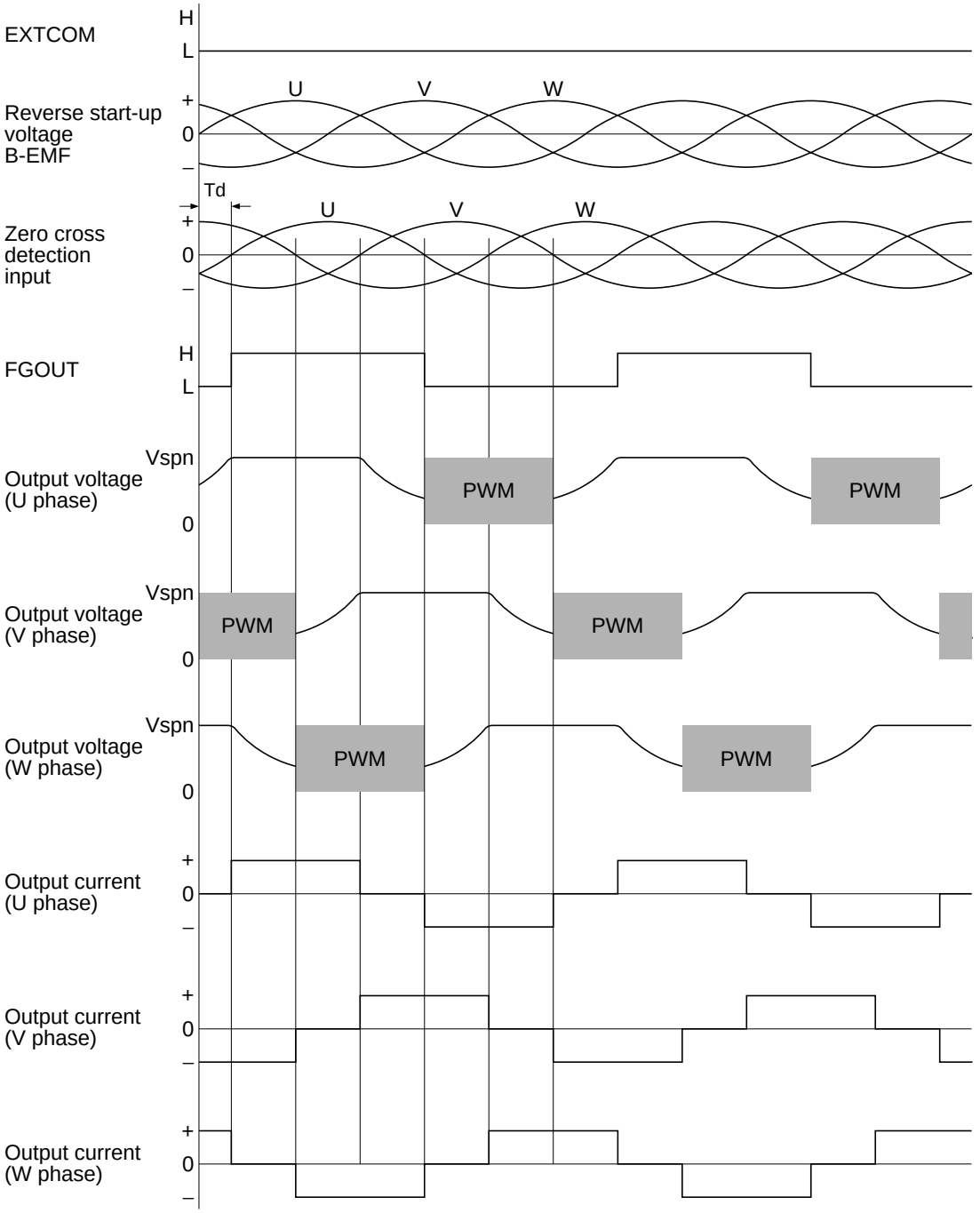
Notes: 1. T1 to T10, and Tmext are set by CPU.
2. B-EMF sensing is masked while COMM = H.
Also, when EXTCOM = H, B-EMF sensing is masked during the period from T1 to T6.

2. Acceleration



Note: 1. B-EMF sensing is masked while COMM = H (= Tmext) or FGOUT = H (= Tmint).
Tmext is set by the CPU.

3. Running



Notes: 1. Delay time Td is determined by C105 to C107, and R109 to R116.
Refer to the section of External Components.
2. B-EMF sensing is masked while FGOUT = H (= Tmint). The Tmint time is set internally.
Refer to the Electrical Characteristics.

Truth Table

Table 1 CE and BRKSEL

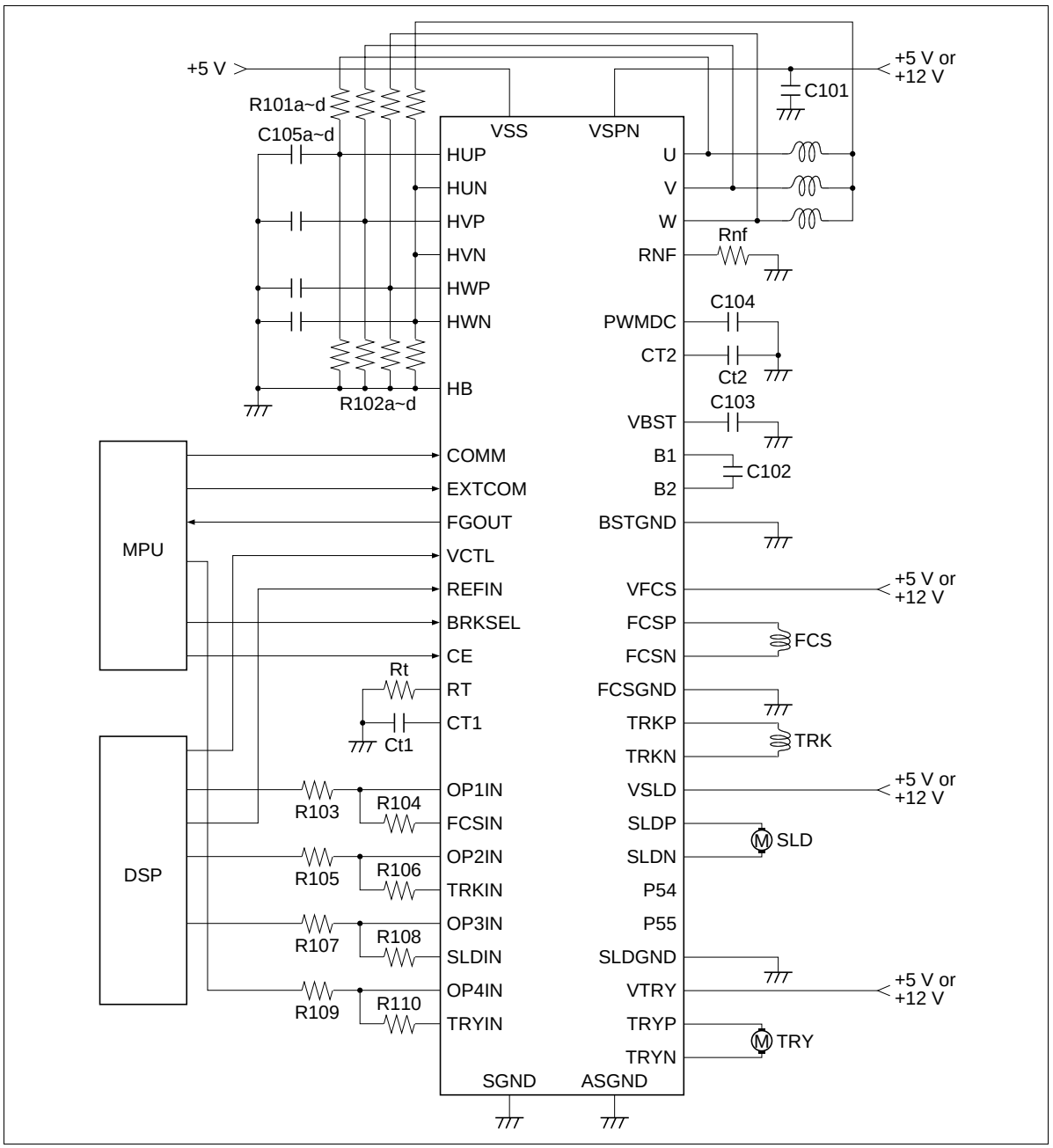
CE	BRKSEL	SPN Driver	FCS Driver	TRK Driver	SLD Driver	TRY Driver
L	L	Z	Z	Z	Z	Z
	H	Enable *2	Enable	Enable	Z	Enable
H	L	Enable *3	Enable	Enable	Enable	Z
	H	Enable *2	Enable	Enable	Enable	Z

Notes: 1. Z: Hi impedance
2. Short brake mode
3. Reverse brake mode

Table 2 EXTCOM and COMM

EXTCOM	COMM	T1~T6 Mask	T7~ Mask	FGOUT (@P = 12)	Logic
L	L	OFF	Internal	6 cycle/rotation	Corresponds to sensor
	H	OFF	Internal		Corresponds to sensorless
H	L	ON	Internal	36 pulse/rotation	
	H	ON	External		

Application



External Components

Parts No.	Reccomended Value	Reccomended Range	Purpose	Note
R101a~d	2.4 kΩ	≤ 22 kΩ	Filter resistor and atenuation for B-EMF	1
R102a~d	7.5 kΩ	≤ 22 kΩ	Filter resistor and atenuation for B-EMF	1
R103, R104	—	≤ 220 kΩ	for FCS driver gain setting	
R105, R106	—	≤ 220 kΩ	for TRK driver gain setting	
R107, R108	—	≤ 220 kΩ	for SLD driver gain setting	
R109, R110	—	≤ 220 kΩ	for TRY driver gain setting	5
Rnf	0.25 Ω	≥ 0.25 Ω	SPN driver current detection resistor	2
Rt	6.8 kΩ	≥ 5 kΩ	Reference current setting	
C101	—	≥ 0.1 μF	for Power supply by passing	
C102	0.1 μF	—	for Booster pumping	
C103	0.47 μF	—	for Booster output smoothing	
C104	2200 pF	—	for PWM carrier oscillation DC level adjustment	
C105a~d	0.1 μF	—	for B-EMF filter	1
Ct1	100 pF	—	Time constant for CLK oscillation	3, 4
Ct2	400 pF	—	PWM carrier generation time constant	3, 4

Notes: 1. The values of R101a~d, R102a~d, and C105a~d are determined by the following equation.

Where, Nomax : Maximum rotation speed (rpm)

P : Number of spindle motor poles (Total number of S poles and N poles)

$$\frac{R101}{R102} \geq \frac{1}{4} \quad \text{(at Vspn = 5 V)}$$

$$C105x = \frac{11}{Nomax\ P}\left(\frac{1}{R101x} + \frac{1}{R102x}\right)$$

2. The output current maximum value Iospnmax of SPN driver is controlled according to the following equation. However, Vspncl is the current limiter reference voltage. (See the electrical characteristics)

$$Iospnmax = \frac{Vspncl}{Rnf}$$

3. The CLK oscillation frequency fclk and Rt1 · Ct1 are related by the following equation.

$$fclk = \frac{Vrt}{2\ Ct1\ Rt\ (Vct1h - Vct1l)}$$

Where, Vrt : RT pin voltage (See the electrical characteristics)

Vct1h : CT1 pin high voltage (See the electrical characteristics)

Vct1l : CT1 pin low voltage (See the electrical characteristics)

4. The PWM carrier frequency fpwm and the amplitude Apwm are determined by the following equation.

$$fpwm = \frac{Vrt}{8\ Ct1\ Rt\ (Vct1h - Vct1l)}$$

$$Apwm = \frac{4\ Ct1}{Ct2}\ (Vct1h - Vct1l)$$

However, Ct2 = 4 Ct1

5. As 5 kΩ appears as an internal resistance at TRYIN (pin 6), caution is required when marking the gain setting.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Note
Control block supply voltage	Vss	7	V	1
SPN supply voltage	Vspn	7	V	1
FCS & TRK supply voltage	Vfcs	9.5	V	1
SLD supply voltage	Vsld	7	V	1
TRY supply voltage	Vtry	9.5	V	1
Input voltage	Vin	0 to Vss	V	2
SPN output current	Iospn	1.5 (2.5)	A	3
FCS output current	Iofcs	0.75 (1.5)	A	3
TRK output current	Iotrk	0.75 (1.5)	A	3
SLD output current	Iosld	1.0 (1.5)	A	3
TRY output current	Iotry	0.75 (1.5)	A	3
Power dissipation	Pt	2.5	W	4
Junction temperature	Tj	150	°C	1
Storage temperature range	Tstg	–55 to +125	°C	

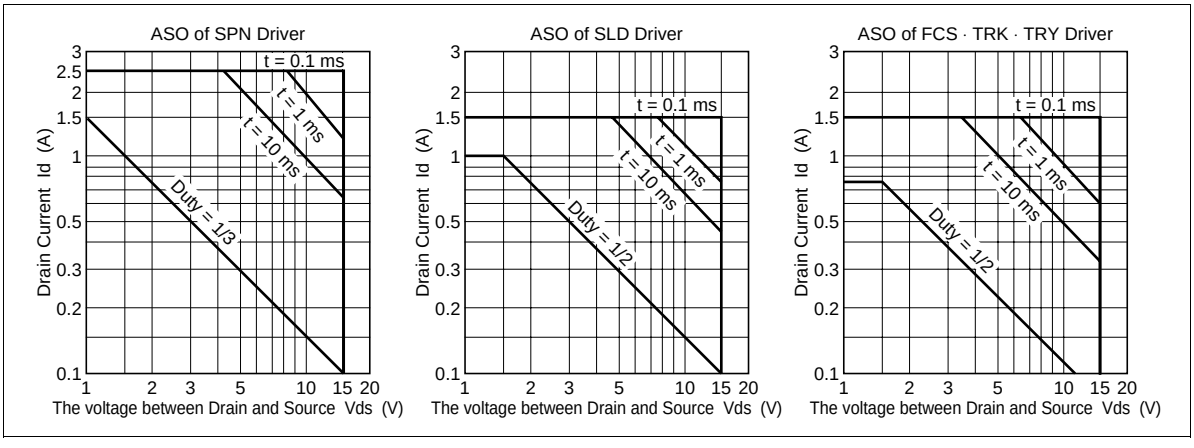
Note: 1. Operating range is shown below.

Vss = 4.5 to 5.5 V, Vspn = 4.25 to 5.75 V, Vfcs = 4.25 to 8.5 V, Vsld = 4.25 to 5.75 V, Vtry = 4.25 to 8.5 V, Tjopr = –20 to +135°C

When operating with Vfcs > Vss, it is necessary to set Vtry = Vfcs. Also, settings must be made that satisfy the following condition:

Vtry + Vss – Vsld ≤ 8.5 V

2. Applied to analog and logic input.
3. Values in parentheses are peak values. ASO (Area of Safety Operation) is shown below.



4. Thermal resistance is shown below.

θj-tab ≤ 6°C/W (back side tab soldering area is 70% or more)

θj-a1 ≤ 30°C/W (mounted on 4 layer glass-epoxy board, back side tab soldering area is 70% or more)

Electrical Characteristics

(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vsld = 12 V)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
Quiescent current		Iss0	—	0.2	0.5	mA	CE = L	VSS	
		Ispn0	—	0.1	0.2	mA		VSPN	
		Ifcs0	—	—	0.1	mA		VFCS	
		Isld0	—	—	0.1	mA		VSLD	
		Itry0	—	—	0.1	mA		VTRY	
		Iss1	—	25	35	mA	CE = H All load open	VSS	
		Ispn1	—	—	1.0	mA		VSPN	
		Ifcs1	—	—	1.0	mA		VFCS	
		Isld1	—	—	1.0	mA		VSLD	
		Itry1	—	4.0	6.0	mA		VTRY	
Logic input	Input current	Iin	—	—	±10	µA	Vin = 0 to Vss	EXTCOM,	
	Low level voltage	Vil	—	—	0.8	V		COMM,	
	High level voltage	Vih	2.0	—	—	V		BRKSEL, CE	
Logic output 1	Low level voltage	Vol	—	0.2	0.4	V	Io = 1 mA	FGOUT	
	Leakage current	$I_{CER}1$	—	—	±10	µA	V_{CE} = 5.5 V		
Logic output 2	Low level voltage	Vol	—	0.3	0.6	V	Io = 15 mA	HB	
	Leakage current	$I_{CER}1$	—	1.2	1.5	µA	V_{CE} = 5.5 V		
SPN driver	Output on resistance	Ronspn	—	1.2	1.5	Ω	Io = 1.0 A	U, V, W	1
	Leakage current	Ioffspn	—	—	±100	µA	Vspn = 15 V		
	Slew rate	SRspn	—	60	—	V/µs	Load open		5
	Current limiter voltage	Vspncl	—	0.25	±10%	V	Rnf = 0.25 Ω	RNF	
FCS/ TRK driver	Output on resistance	Ronfcs	—	3.0	3.75	Ω	Io = 0.5 A	FCSP/N, TRKP/N	1
	Leakage current	Iofffcs	—	—	±100	µA	Vfcs = 15 V		
	Slew rate	SRfcs	—	60	—	V/µs	Load open		5
SLD driver	Output on resistance	Ronsld	—	2.0	2.5	Ω	Io = 1.0 A	SLDP/N	1
	Leakage current	Ioffsld	—	—	±100	µA	Vsld = 15 V		
	Slew rate	SRsld	—	60	—	V/µs	Load open		5

Electrical Characteristics

(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vsld = 12 V) (cont)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
TRY driver	Output on resistance	Rontry	—	3.0	3.75	Ω	Io = 0.5 A	TRYP/N	1
	Leakage current	Iofftry	—	—	±100	µA	Vtry = 15 V		
	Slew rate	SRtry	—	125	—	V/µs	Load open		5
CLK OSC	RT voltage	Vrt	—	1.37	±5%	V		RT	
	CT1 charge current	Ict1p	—	180	±10%	µA	Rt = 6.8 kΩ	CT1	
	CT1 discharge current	Ict1n	—	–180	±10%	µA	Rt = 6.8 kΩ		
	CT1 high voltage	Vct1h	—	2.7	±0.1	V			
	CT1 low voltage	Vct1l	—	1.47	±0.1	V			
	CLK oscillation frequency	fclk	—	460	±10%	kHz	Ct1 = 100 pF		
Bias	Drive frequency	fbst	—	fclk/2	—	kHz		BP1	
	Output voltage	Vbst	16.0	16.5	—	V	Vspn = 12 V	VBST	
			9.0	9.5	—	V	Vspn = 5 V		
PWM carrier	PWM frequency	fpwm	—	fclk/4	—	kHz		CT2	
	CT2 charge current	Ict2p	—	180	±10%	µA	Rt = 6.8 kΩ		
	CT2 discharge current	Ict2n	—	–180	±10%	µA	Rt = 6.8 kΩ		
	DC feedback resistance	Rdc	—	20	±20%	kΩ		PWMDC	
	Offset voltage	Vospwm	—	—	±30	mV			
Zero cross detection	Common mode input voltage range	Vczd	0	—	4.0	V		HU+/–, HV+/–, HW+/–	
	Input voltage range	Vinzd	50	—	—	mVpp			
	Hysteresis	Vhyszd	11	16	21	mVpp			
	FGOUT pulse width	Tmint	—	64/ fclk	±4/ fclk	µs		FGOUT	
SPN control	Input current	Ictl	—	—	±3.0	µA	Vctl = 0.5 to 4.5 V	VCTL	
	Dead zone voltage	Vdzctl	±50	—	±200	mV			2
	REFIN voltage range	Vref	1.0	—	2.65	V		REFIN	4
	Control gain	Dspn	119	139	159	%/V	Ct2 = 680 pF, Ct1 = 100 pF	U, V, W	2

Electrical Characteristics

(Ta = 25°C, Vss = 5 V, Vspn = 12 V, Vfcs = 5 V, Vsld = 12 V) (cont)

Item			Symbol	Min	Typ	Max	Unit	Test Conditions	Applicable Pins	Note
OP1~ OP4	Input current		Iinop	—	—	±0.1	µA	Vin = 0 to Vss	OP1~4IN	
	Offset voltage		Vosop	—	—	±60	mV		FCSIN,	
	Open loop gain		Gvolop	—	64	—	dB	f = 1kHz	TRKIN,	5
	Gain bandwidth		Bop	—	1.6	—	MHz		SLDIN, TRYIN	5
	OP1~ OP3	Output low voltage	Voopl	—	—	0.5	V	Io = –0.2 mA	FCSIN, TRKIN, SLDIN	
		Output high voltage	Vooph	Vss –1.0	—	—	V	Io = 0.2 mA		
	OP4	Output low voltage	Voopl	—	—	0.5	V	Io = –0.03 mA	TRYIN	
		Output high voltage	Vooph	Vss –1.7	—	—	V	Io = 0.03 mA		
FCS/ TRK/ SLD/ TRY control	Quiescent offset duty		Dqfcs	—	—	±2	%	FCS/TRK/SLD/ TRYIN = REFIN	FCSP/N, TRKP/N, SLDP/N, TRYP/N	3
	Control gain		Dfcs	63	68	73	%/V	Ct2 = 680 pF, Ct1 = 100 pF		
OTSD	Operating temperature		Tsd	135	180	—	°C			5
	Hysteresis		Thys	—	80	—	°C			

Note: 1. Specified by sum of the upper and lower saturation voltages.

2. See figure 1. Where,

$$Dspn = \frac{\Delta D}{\Delta Vctl}$$

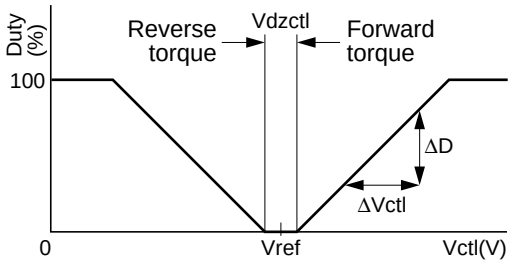


Figure 1

3. See figure 2. Where, x = fcs, trk, sld, try.

$$Dx = \frac{\Delta D}{\Delta Vxin}$$

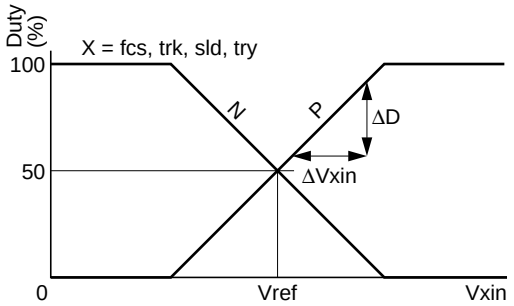
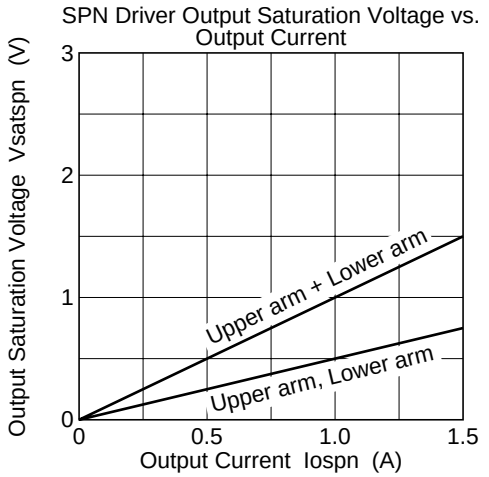
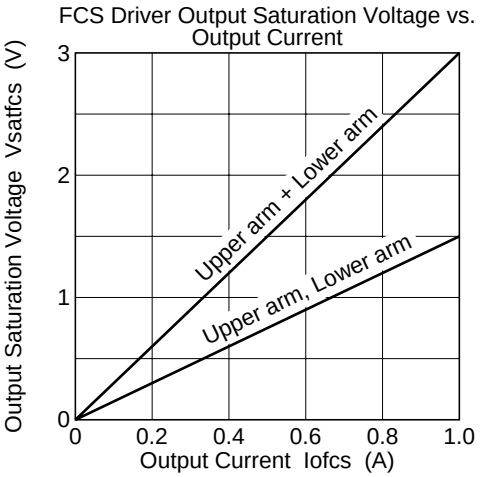


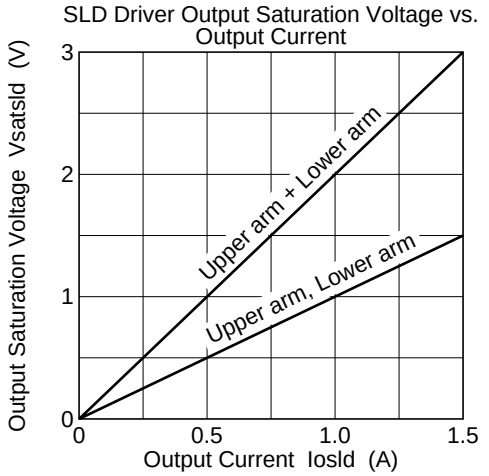
Figure 2

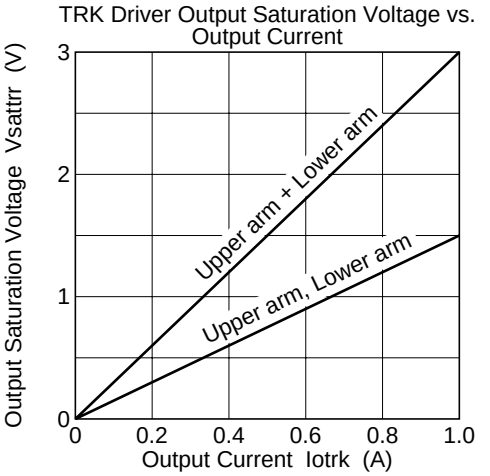
4. If Vref < 1.5 V, 100% PWM duty control may not be possible.
5. Design guide only.

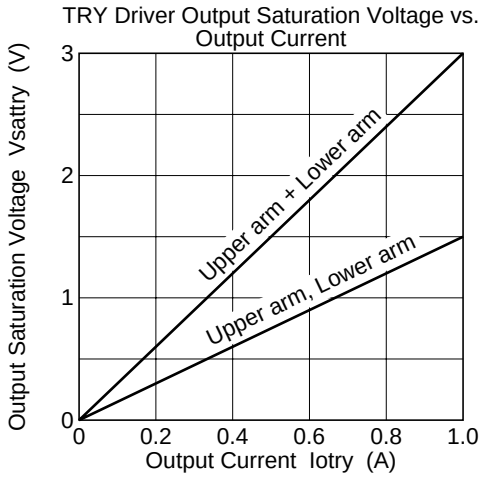
Reference Data

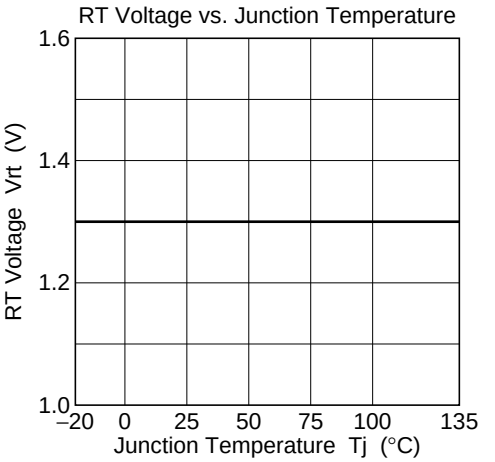






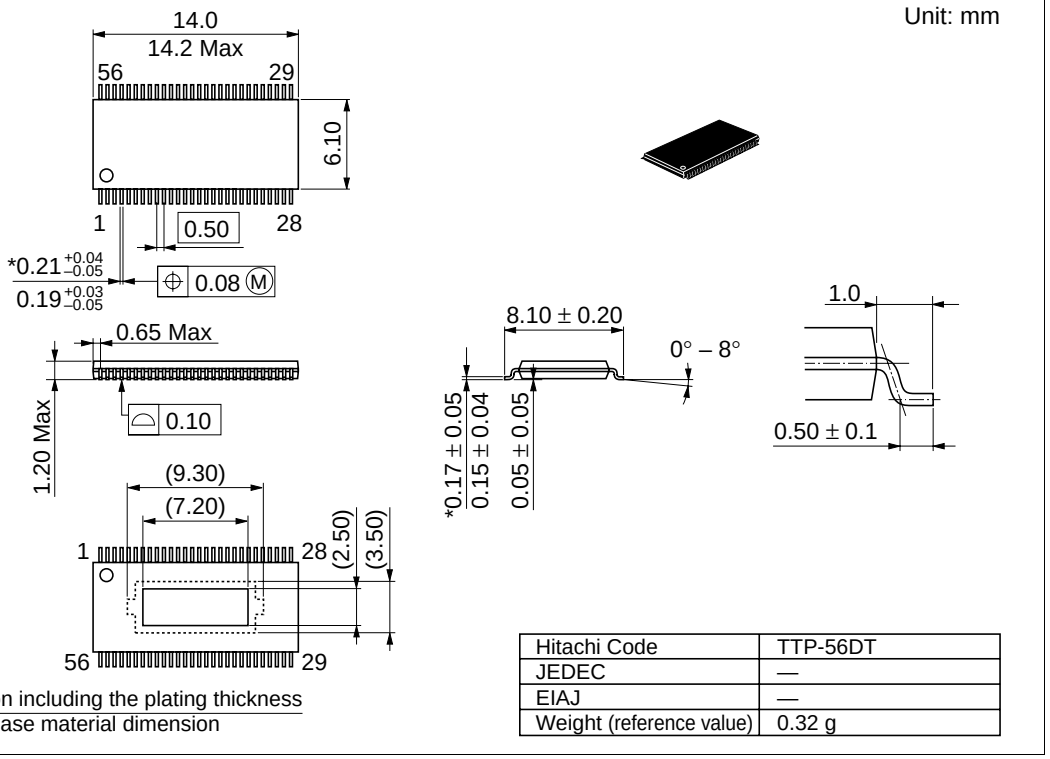






Package Dimensions

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-56DT
JEDEC	—
EIAJ	—
Weight (reference value)	0.32 g

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