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# HA16113FPJ

## Dual Watchdog Timers

# HITACHI

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The HA16113FPJ is a multifunction device that provides microprocessor systems with the necessary regulated power supply, monitors the supply voltage, and generates power-on reset and watchdog reset signals. It is ideally suited for battery-operated systems such as instrumentation systems.

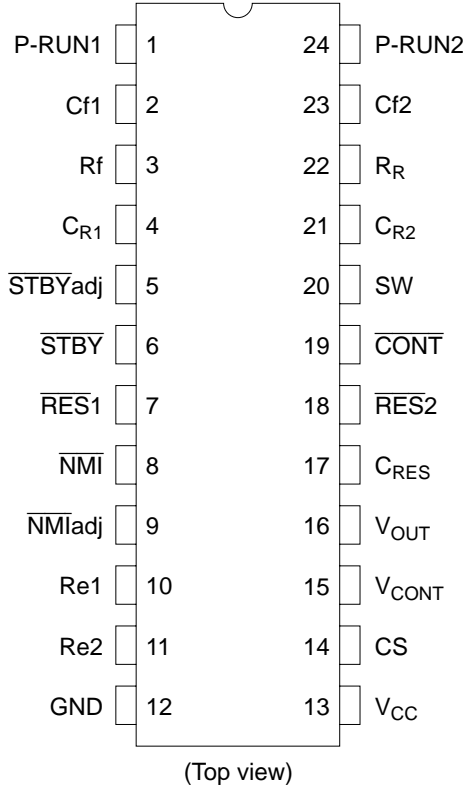
### Functions

- Regulated power supply
- Power-on reset
- Two built-in auto-reset circuits
- Two built-in watchdog timer circuits (WDT)
- Output voltage monitoring (LVI)

### Features

- Simultaneous or independent control of auto-reset outputs.
- Precisely regulated output voltage and accurate  $\overline{\text{NMI}}$  trigger voltage (both  $\pm 2\%$ ).
- Low-voltage control with  $\overline{\text{NMI}}$ , simultaneous  $\overline{\text{RES1}}$  and  $\overline{\text{RES2}}$ , and  $\overline{\text{STBY}}$  outputs.
- Independently selectable durations for power-on reset and auto-reset: power-on duration is common to both reset outputs; auto-reset durations can be selected independently.
- Reset command input pin ( $\overline{\text{CONT}}$ ) for second reset output ( $\overline{\text{RES2}}$ ).
- WDT filter function detects minimum pulse width and maximum period of P-RUN input pulses.

## Pin Arrangement



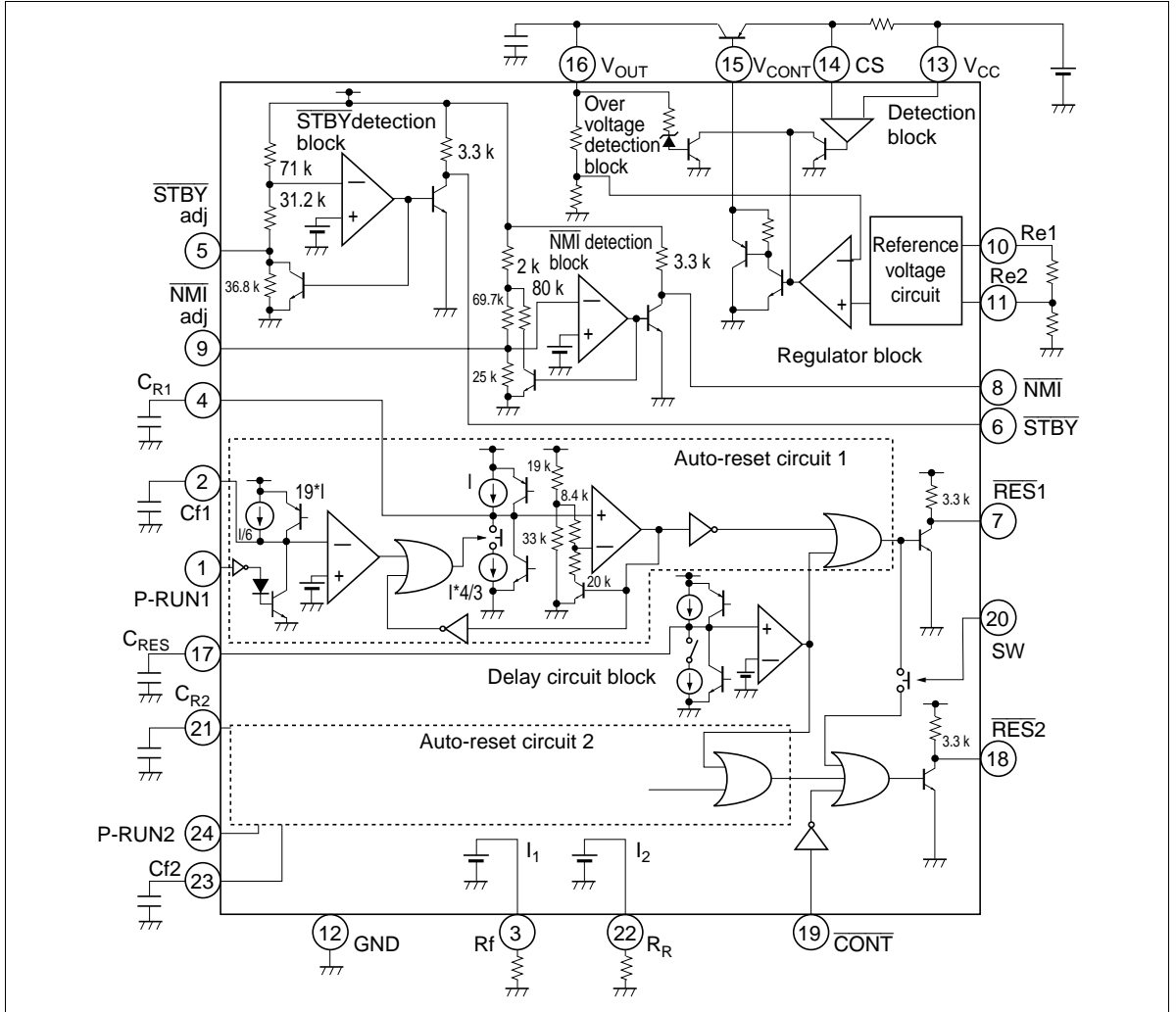
## Pin Description

Pin No.	Symbol	Function
1	P-RUN1	Input from main CPU to watchdog timer 1 (WDT1)
2	Cf1	For connecting capacitor Cf1 to determine WDT1 filter characteristic (frequency band)
3	Rf	For connecting common bias resistor Rf to determine WDT1 and WDT2 filter characteristics (frequency band), power-on reset time ( $t_{on}$ , common to RES1 and RES2), clock-off time of auto-reset circuits 1 and 2, reset high time ( $t_{RH1}$ and $t_{RH2}$ ), reset low time ( $t_{RL1}$ and $t_{RL2}$ ), and reset pulse delay at voltage drop and recovery. Use the resistor value from 100 k $\Omega$ to 500 k $\Omega$ .
4	C <sub>R1</sub>	For connecting capacitor C <sub>R1</sub> to determine $t_{on}$ for power-on reset and $t_{off1}$ , $t_{RH1}$ , and $t_{RL1}$ of auto-reset circuit 1.
5	STBY adj	For adjusting standby trigger voltage (insert a resistor between this pin and ground) Recommended range: $V_{H2} = 2.8$ to 4.0 V
6	STBY	Standby signal output
7	RES1	Reset signal output to main CPU
8	NMI	Low-voltage interrupt signal output for memory backup

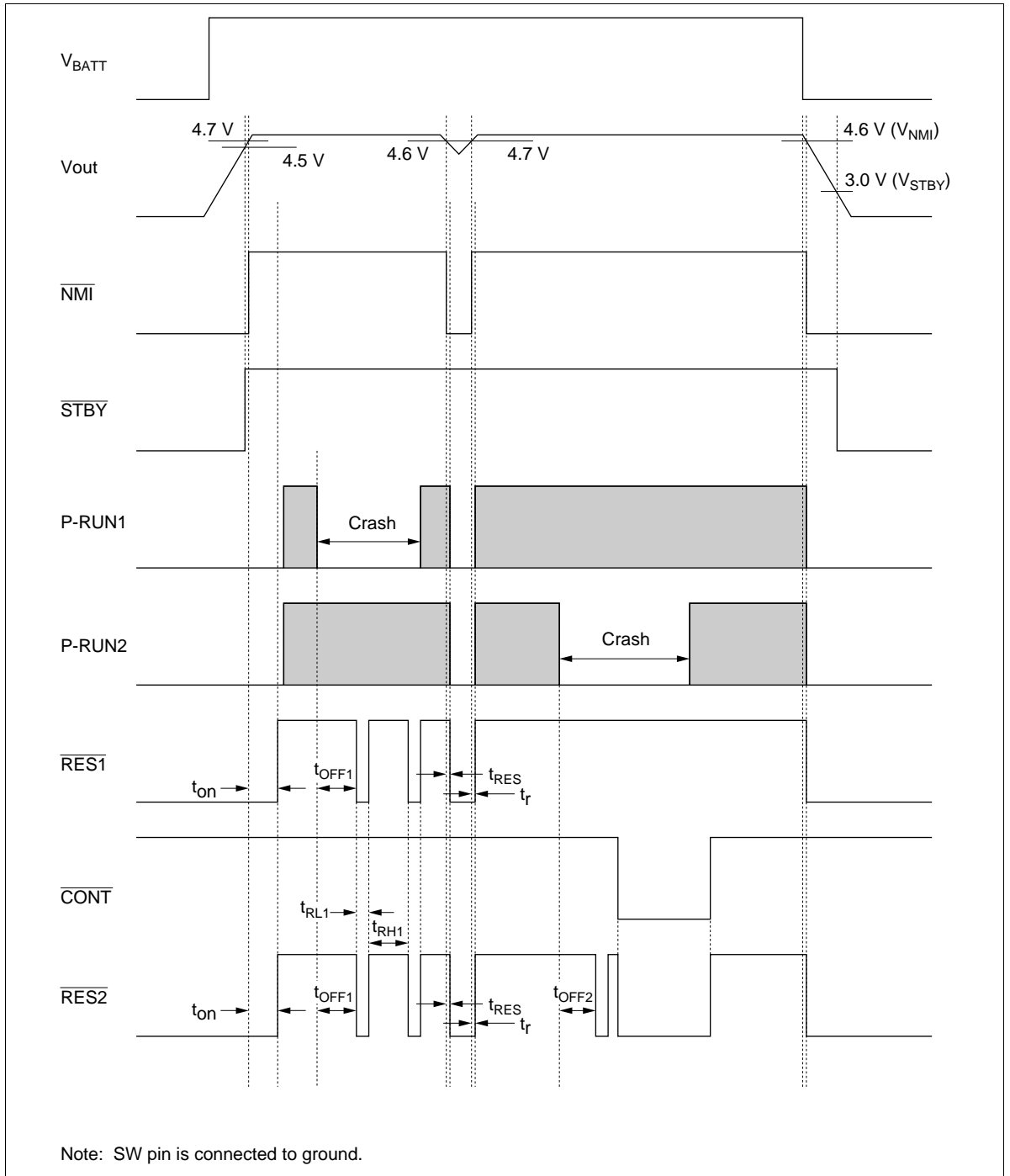
## Pin Description (cont)

Pin No.	Symbol	Function
9	$\overline{\text{NMI}}$ adj	For fine adjustment of Vout trigger level for $\overline{\text{NMI}}$ signal (insert a resistor between this pin and Vout or ground) Recommended range: $V_{H1} = 4.4$ to $5.2$ V
10	Re1	For connecting resistor Re1 to determine voltage Vout for microprocessor and IC internal circuits (insert between this pin and Re2)
11	Re2	For connecting resistor Re2 to determine voltage Vout for microprocessor and IC internal circuits (insert between this pin and ground)
12	GND	Ground
13	$V_{CC}$	Power supply input pin (operating range: 6 to 40 V)
14	CS	Input for detecting power supply current
15	$V_C$	For base control of external pnp transistor
16	Vout	Regulated voltage supplied to microprocessor and IC internal circuits Connect to collector of external pnp transistor
17	$C_{RES}$	Determines reset pulse delay at voltage drop and recovery. $\overline{\text{NMI}}$ output goes low as soon as Vout drops below $\overline{\text{NMI}}$ trigger level. If Vout remains below this level for time $t_{RES1}$ , both reset outputs also go low. When Vout recovers above $\overline{\text{NMI}}$ trigger level, first $\overline{\text{NMI}}$ output goes high, then after time $t_r$ , both reset outputs also go high. Times $t_{RES}$ and $t_r$ are adjusted by capacitor $C_{RES}$ inserted between this pin and ground.
18	$\overline{\text{RES2}}$	Reset signal output to sub CPU
19	$\overline{\text{CONT}}$	Input pin for resetting sub CPU on command, or when sub CPU crashes Low input at $\overline{\text{CONT}}$ causes low output at $\overline{\text{RES2}}$
20	SW	Selects simultaneous control, in which main and sub CPUs are both reset when main CPU crashes, or independent control, in which sub CPU is reset independently of main CPU Open— independent control; connected to ground— simultaneous control
21	$C_{R2}$	For connecting capacitor $C_{R2}$ to determine $t_{off2}$ , $t_{RH2}$ , and $t_{RL2}$ of auto-reset circuit 2
22	$R_R$	For connecting bias resistor $R_R$ to determine $t_{off1}$ , $t_{off2}$ , $t_{RH1}$ , $t_{RH2}$ , $t_{RL1}$ , and $t_{RL2}$ . Use the resistor value from 100 k $\Omega$ to 500 k $\Omega$ .
23	Cf2	For connecting capacitor Cf2 to determine WDT2 filter characteristic (frequency band)
24	P-RUN2	Input from sub CPU to watchdog timer 2 (WDT2)

## Block Diagram



Timing Waveforms



**Absolute Maximum Ratings (Ta = 25°C)**

<b>Item</b>	<b>Symbol</b>	<b>Value</b>	<b>Unit</b>
V <sub>CC</sub> power supply voltage	V <sub>CC</sub>	40	V
CS voltage	V <sub>CS</sub>	40	V
Control pin voltage	V <sub>C</sub>	40	V
Control pin current	I <sub>C</sub>	20	mA
Vout voltage	Vout	10	V
P-RUN voltage	V <sub>PRUN</sub>	Vout	V
SW voltage	V <sub>SW</sub>	Vout	V
$\overline{\text{CONT}}$ voltage	V <sub>CONT</sub>	Vout	V
$\overline{\text{RES}}$ current	I <sub>RES</sub>	5	mA
$\overline{\text{NMI}}$ current	I <sub>NMI</sub>	5	mA
$\overline{\text{STBY}}$ current	I <sub>STBY</sub>	5	mA
Power dissipation <sup>Note</sup>	P <sub>T</sub>	600	mW
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-50 to +125	°C

Note: At ambient temperatures up to Ta = 60°C. Derated by 9.8 mW/°C above this point.

**Electrical Characteristics** ( $T_a = 25^\circ\text{C}$ ,  $R_f = 180\text{ k}$ ,  $C_{f1} = C_{f2} = 0.01\ \mu\text{F}$ ,  $C_{R1} = C_{R2} = 0.1\ \mu\text{F}$ )

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	
Chip	Power supply current	$I_{CC}$	—	10	15	mA		
Regulator	Output voltage	$V_{O1}$	4.875	5.00	5.125	V	$V_{CC} = 6\text{ to }17.5\text{ V}$ $V_C\text{ current} = 5\text{ mA}$	
		$V_{O2}$	4.80	5.00	5.20	V	$V_{CC} = 6\text{ to }17.5\text{ V}$ $V_C\text{ current} = 10\text{ mA}$	
	Stability with respect to line voltage	$V_{oline}$	-50	—	50	mV	$V_{CC} = 6\text{ to }17.5\text{ V}$ $V_C\text{ current} = 10\text{ mA}$	
	Stability with respect to load current	$V_{oload}$	-100	—	100	mV	$V_C\text{ current} = 0.1\text{ to }15\text{ mA}$	
	Ripple rejection	$RREJ$	45	75	—	dB	$V_i = 0.5\text{ V}_{rms}$ $f_i = 1\text{ kHz}$	
	Short-circuit detection voltage	$V_{os}$	0.08	0.14	0.20	V		
	Temperature coefficient of output voltage	$\sigma V_o/\sigma T$	—	-40	—	ppm/ °C		
	Maximum adjustable output voltage	$V_{omax}$	—	—	7.0	V		
P-RUN1/2 input section	Low input voltage	$V_{IL1,2}$	—	—	0.8	V		
	High input voltage	$V_{IH1,2}$	2.0	—	—	V		
	High input current	$I_{IH1,2}$	—	0.3	0.5	mA	$V_{IH} = V_{OL}$	
Watchdog section (both $\overline{RES1}$ and $\overline{RES2}$ outputs)	Power-on time	$t_{on}$	25	40	60	ms		
	Clock-off time (1)	$t_{off1}$	80	130	190	ms	$R_R$ : open	
	Reset low time (1)	$t_{RL1}$	15	20	30	ms	$R_R$ : open	
	Reset high time (1)	$t_{RH1}$	40	60	90	ms	$R_R$ : open	
	Clock-off time (2)	$t_{off2}$	25	40	60	ms	$R_R$ : = 75 k $\Omega$	
	Reset low time (2)	$t_{RL2}$	4	6	9	ms	$R_R$ : = 75 k $\Omega$	
	Reset high time (2)	$t_{RH2}$	15	20	30	ms	$R_R$ : = 75 k $\Omega$	
LVI section	$\overline{NMI}$ trigger voltage	$V_{NMI}$	4.45	4.60	4.75	V		
	Hysteresis width of above	$V_{HYSN}$	25	50	100	mV		
	$\overline{STBY}$ trigger voltage	$V_{STBY}$	2.70	3.00	3.30	V		
	Hysteresis width of above	$V_{HYSS}$	1.35	1.50	1.65	V		
	$\overline{RES}$ pulse delay time	Drop	$t_{RES}$	—	200	—	$\mu\text{s}$	$C_{RES} = 1500\text{ pF}$
		Recovery	$t_r$	—	200	—	$\mu\text{s}$	$C_{RES} = 1500\text{ pF}$

**Electrical Characteristics** (Ta = 25°C, Rf = 180 k, Cf1 = Cf2 = 0.01 μF, C<sub>R1</sub> = C<sub>R2</sub> = 0.1 μF) (cont)

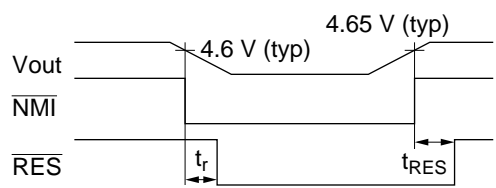
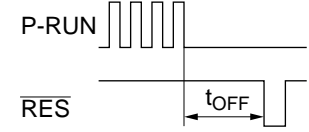
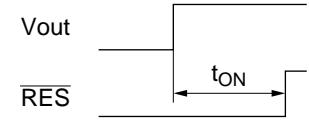
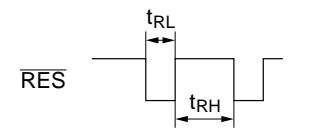
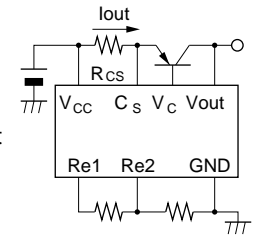
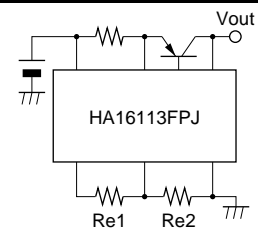
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
NMI output section	NMI low voltage	V <sub>OL1</sub>	—	—	0.4	V	I <sub>OL1</sub> = 2 mA
	NMI high voltage	V <sub>OH1</sub>	—	V <sub>O1</sub>	—	V	
	NMI function initial voltage	V <sub>STN</sub>	—	0.7	1.0	V	
STBY output section	STBY low voltage	V <sub>OL2</sub>	—	—	0.4	V	I <sub>OL2</sub> = 2 mA
	STBY high voltage	V <sub>OH2</sub>	—	V <sub>O1</sub>	—	V	
	STBY function initial voltage	V <sub>STS</sub>	—	0.7	1.0	V	
RES1/2 output section	RES1/2 low voltage	V <sub>OL3</sub>	—	—	0.4	V	I <sub>OL3,4</sub> = 2 mA
	RES1/2 high voltage	V <sub>OH3</sub>	—	V <sub>O1</sub>	—	V	
	RES1/2 function initial voltage	V <sub>STR</sub>	—	0.7	1.0	V	
CONT and SW input section	Low input voltage	V <sub>IL3</sub>	—	—	0.8	V	
	High input voltage	V <sub>IH3</sub>	2.0	—	—	V	
	Low input current	I <sub>IL3</sub>	-120	-60	—	μA	V <sub>IL3</sub> = 0 V
	High input current	I <sub>IH3</sub>	—	0.3	0.5	mA	V <sub>IH3</sub> = V <sub>OL</sub>
LVI section	Temperature coefficient of NMI trigger voltage	δV <sub>H1</sub> /δT	—	100	—	ppm/°C	
	Temperature coefficient of STBY trigger voltage	δV <sub>H2</sub> /δT	—	200	—	ppm/°C	



External Circuit Constant Calculations

Equations for the various functions are given below.  $C_{R1}$  and  $Cf1$  are for  $\overline{RES1}$ .  $C_{R2}$  and  $Cf2$  are for  $\overline{RES2}$ . (Values given in equations are for reference.)

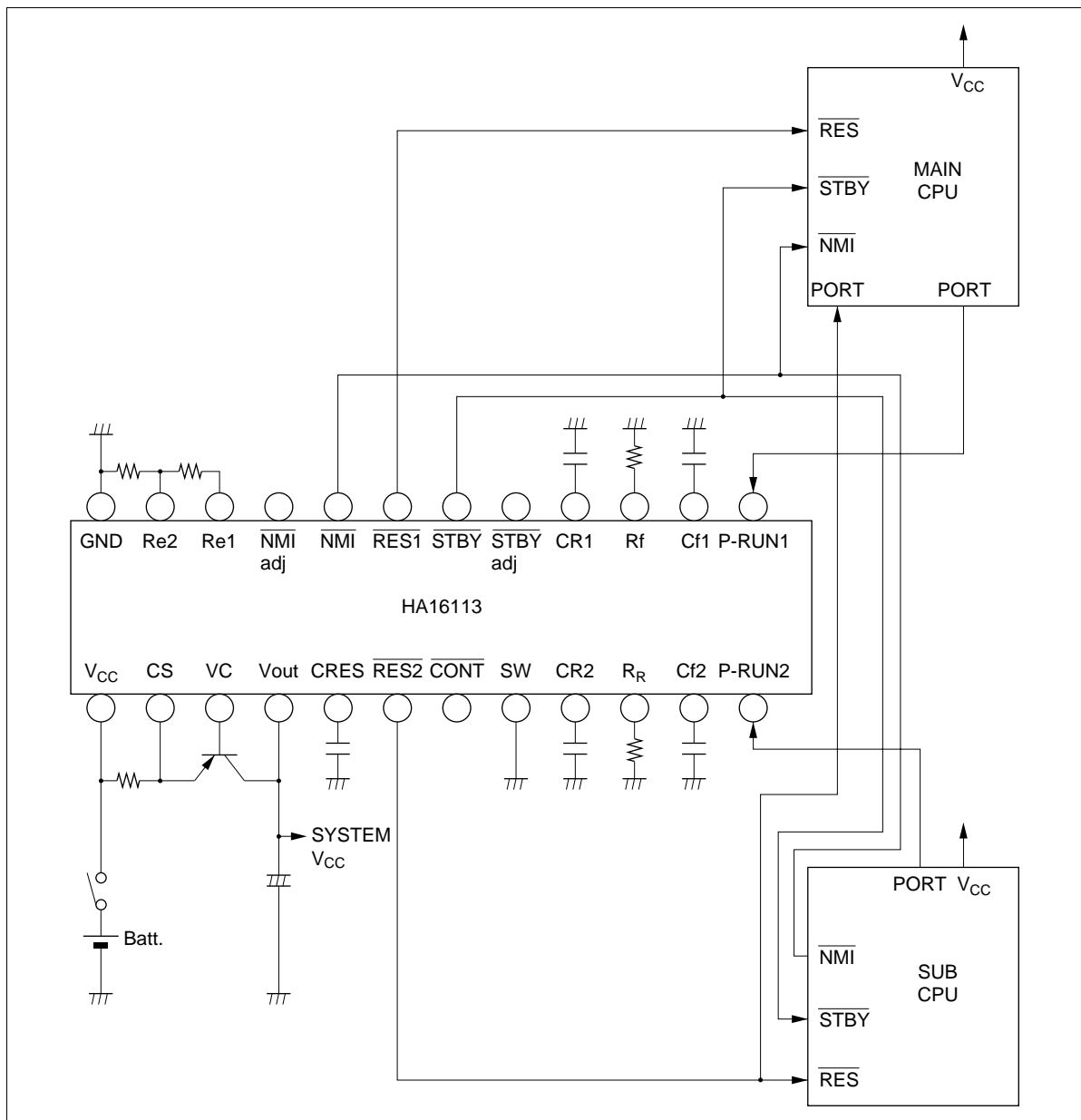
Item	Equation	Remarks
Regulated output voltage	$V_{out} = 0.388 \times \frac{Re2}{Re1} + 2.63$	If the desired $V_{out}$ is 5 V $\pm 2.5\%$ , recommended values are $Re1 = 1.5 \text{ k}\Omega$ and $Re2 = 9.1 \text{ k}\Omega$
Short-circuit detection voltage	$V_{CS} < I_{out} \times R_{CS}$	When this function operates, $V_{CONT}$ stops drawing current from the base of the external transistor, so $V_{out}$ output stops
Maximum output voltage	$V_{out} \text{ Max} < 7.0 \text{ V}$	Prevents microprocessor damage that would result if the output voltage were raised too high by mistake. The maximum output voltage is fixed.
$t_{RH}, t_{RL}$ (for both $\overline{RES1}$ and $\overline{RES2}$ )	$t_{RH} = 3.2 \times C_R \times R'$ $t_{RL} = 1.1 \times C_R \times R'$ $\left( R' = \frac{1}{\frac{1}{R_f} + \frac{1}{R_R}} \right)$	Determines the frequency and duty cycle of the reset pulse
$t_{ON}$ (for both $\overline{RES1}$ and $\overline{RES2}$ )	$t_{ON} = 2.2 \times C_R \times R_f$	Sets the time from the rise of $V_{out}$ to the clearing of $\overline{RES}$ output
$t_{OFF}$ (for both $\overline{RES1}$ and $\overline{RES2}$ )	$t_{OFF} = 6.1 \times C_R \times R'$ $\left( R' = \frac{1}{\frac{1}{R_f} + \frac{1}{R_R}} \right)$	Sets the time from when P-RUN pulses stop until the reset pulse is output
$t_r, t_{RES}$ (for both $\overline{RES1}$ and $\overline{RES2}$ )	$t_r = 0.75 \times C_{RES} \times R_f$ $t_{RES} = 0.625 \times C_{RES} \times R_f$	$t_r$ sets the time from the rise of $\overline{NMI}$ to the rise of $\overline{RES}$ , when $V_{out}$ drops by more than the $\overline{STBY}$ trigger voltage, then recovers. $t_{RES}$ is the time from the fall of $\overline{NMI}$ to the fall of $\overline{RES}$ .



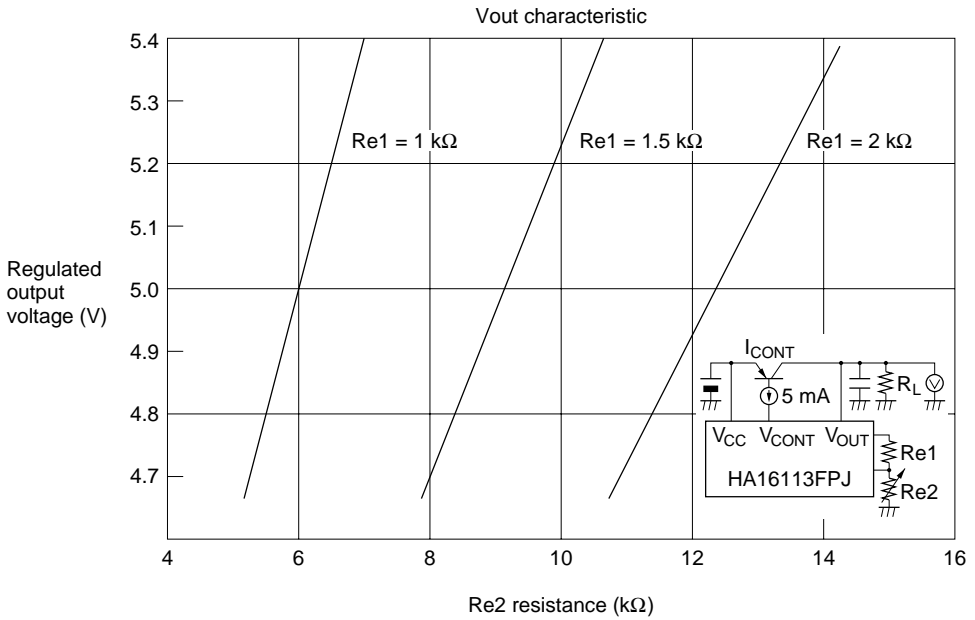
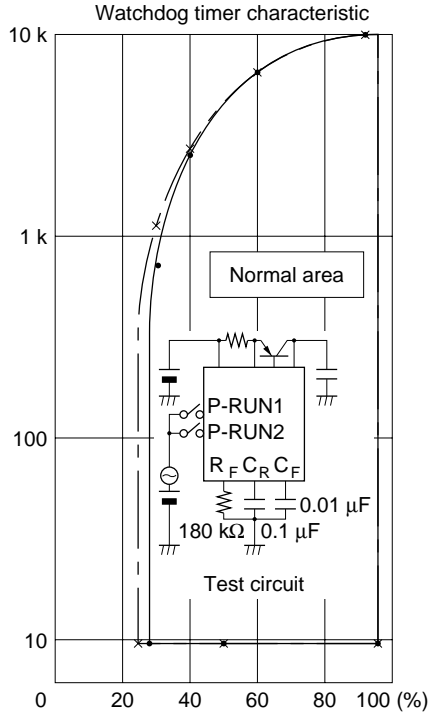
## External Circuit Constant Calculations (cont)

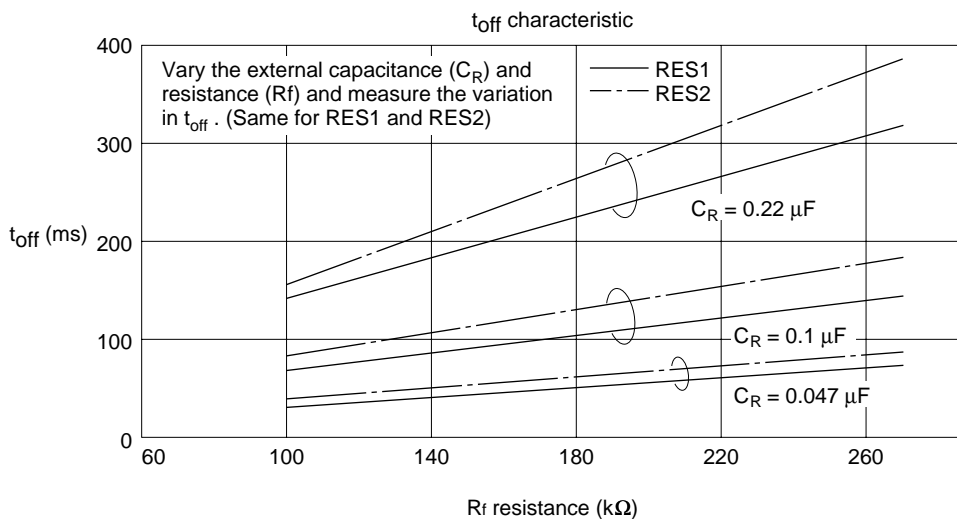
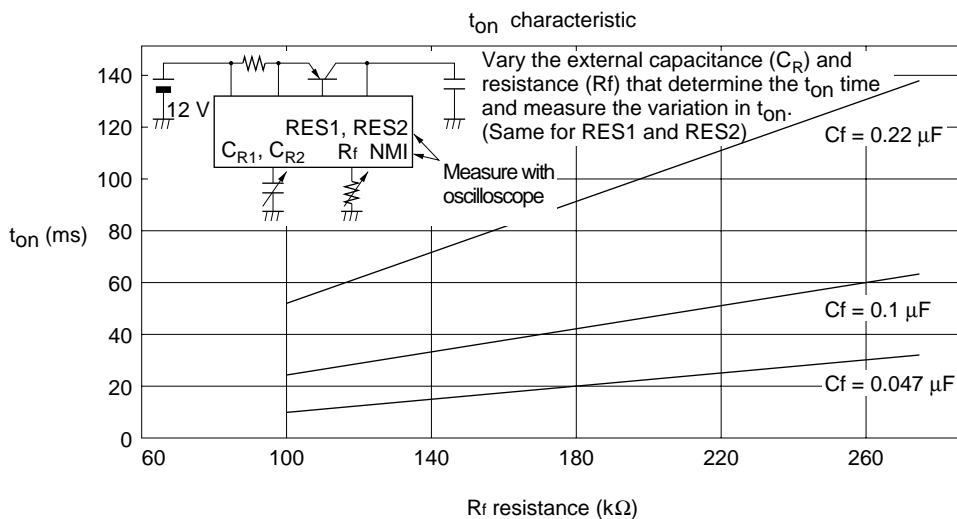
Item	Equation	Remarks
$V_{NMI}$	$V_{NMI} = 1.2 \times \left[ 1 + \frac{(R1 // 71.7)}{(R2 // 25)} \right]$ <p><math>\overline{NMI}</math> recovery voltage (<math>V_{NMI}</math> high) is:</p> $V_{NMI} \text{ high} = \left( \frac{86.65}{R1} + \frac{86.65}{R2 // 25} + 1.2 \right) \left( 1 + \frac{73.8}{R1} \right)$ <p>(R1 and R2 are in k<math>\Omega</math>)</p>	<p>Voltage at which the <math>\overline{NMI}</math> signal is output when <math>V_{out}</math> drops. The <math>\overline{NMI}</math> trigger voltage and <math>\overline{NMI}</math> recovery voltage can be trimmed by connecting resistors between the <math>\overline{NMI}adj</math> pin and <math>V_{out}</math> (R1), and between <math>\overline{NMI}adj</math> and GND (R2).</p>
$V_{STBY}$	$V_{STBY} = 1.47 \times \left[ 1 + \frac{71}{31.2 + (36.8 // R3)} \right]$ <p>(R3 is in k<math>\Omega</math>)</p>	<p>Voltage at which the <math>\overline{STBY}</math> signal is output when <math>V_{out}</math> drops. The <math>\overline{STBY}</math> trigger voltage can be adjusted by connecting a resistor (R3) between the <math>\overline{STBY}adj</math> pin and GND. The <math>\overline{STBY}</math> recovery voltage cannot be adjusted.</p>
WDT.	$\text{Line1} = \frac{0.31 \times (Du - 24)}{Cf \times Rf}$ $\text{Line2} = Du \text{ (= 25\%)*}$ $\text{Line3} = \frac{0.015}{Cf \times Rf}$ $\text{Line4} = \frac{1 - Du}{2.1 \times t_{RH}}$ $\text{Line5} = 99\%*$ <p>Du is the duty cycle of the P-RUN pulse.</p> $Du = \frac{t_{RH}}{t_{RL} + t_{RH}}$ <p>Note: Line2 and Line5 are fixed.</p>	<p>The watchdog timer function determines whether the P-RUN pulse is normal or not. A reset pulse is output if P-RUN is determined to be abnormal. The normal region is the part bounded by Line1 to Line3 (or Line4) in the diagram. Line4 applies in certain cases, depending on <math>C_R</math>, <math>C_f</math>, and the state of P-RUN.</p>

Operating Interconnections (example)

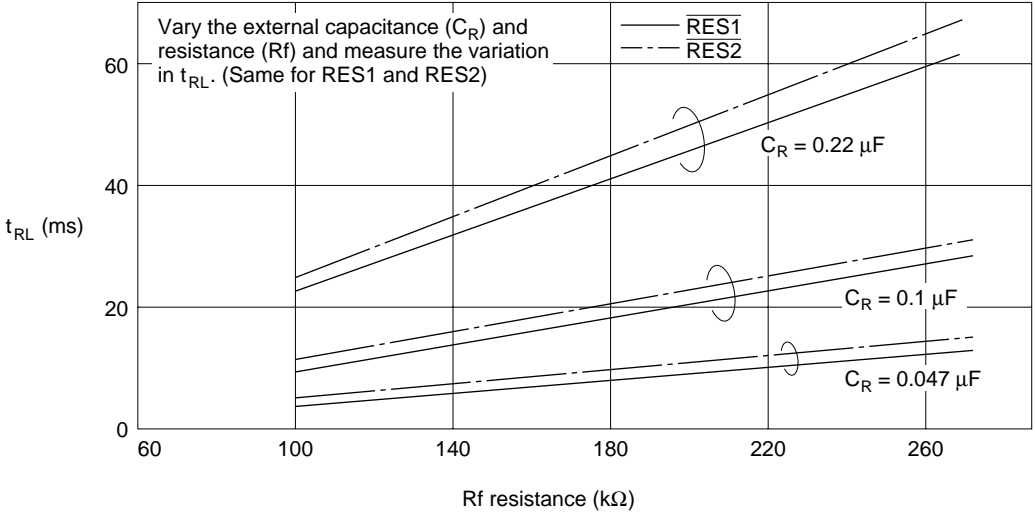


## Characteristic Curves

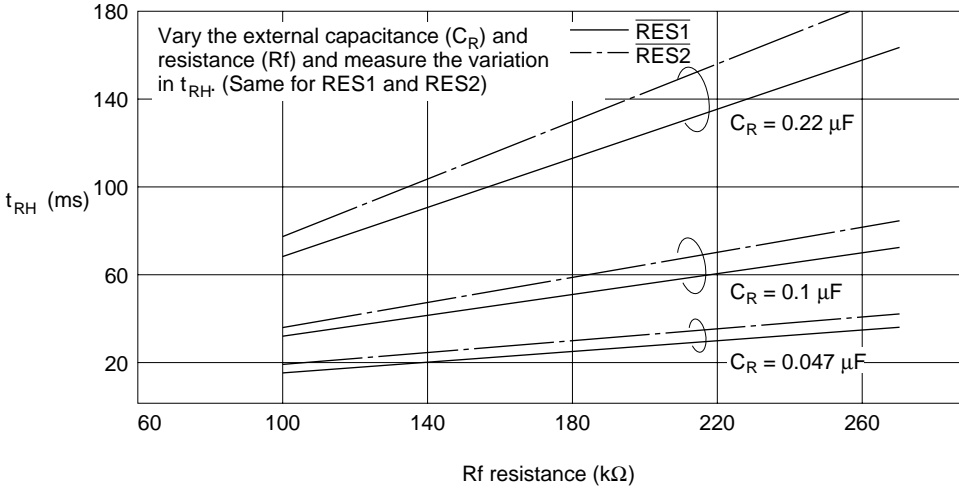


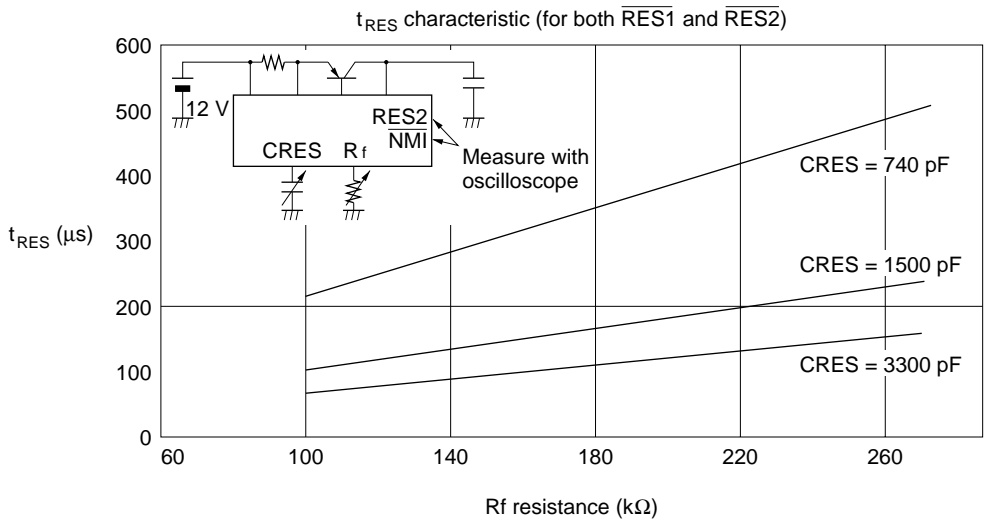
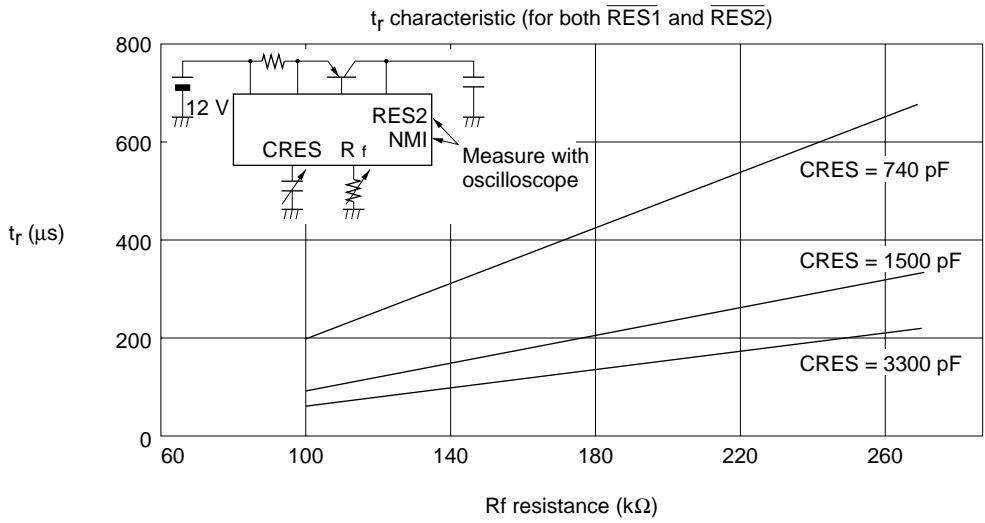


$t_{RL}$  characteristic



$t_{RH}$  characteristic





## Precautions

If the IC's ground potential varies suddenly by several volts due to wiring impedance (see figure 7), a false  $\overline{\text{RES}}$  pulse may be output. The reason for this is that potentials in the  $\overline{\text{RES}}$  pulse generating circuit change together with the  $V_{\text{out}}\text{-GND}$  potential. The reference potential of the comparator in figure 8 and the potential of the external capacitor have different impedances as seen from the comparator, causing a momentary inversion. The solution is to stabilize the ground potential. Two ways of stabilizing the IC's ground line are:

- Separate the IC's ground line from high-current ground lines.
- Increase the capacitance ( $C_0$ ) used to smooth the  $V_{\text{out}}$  output.

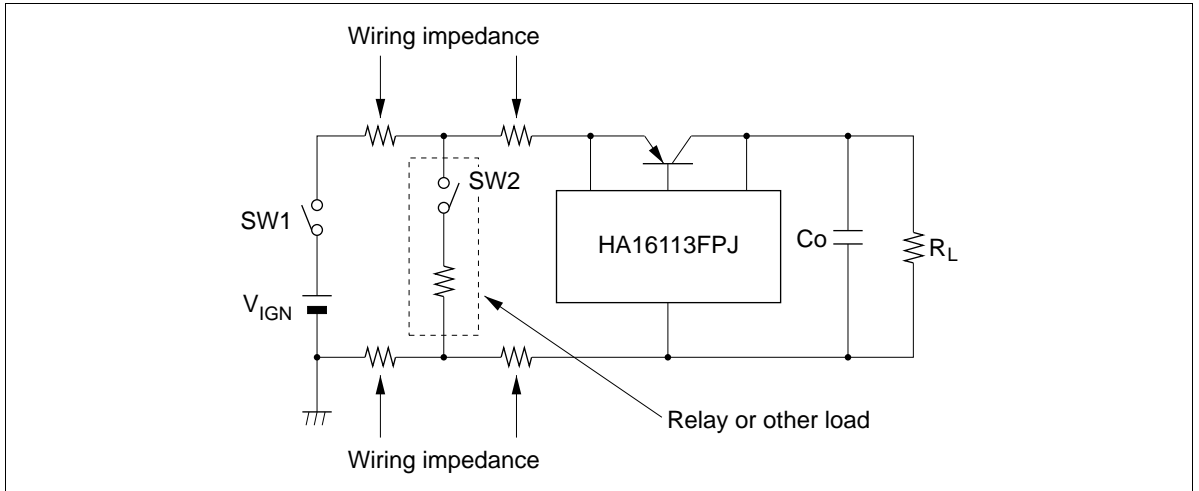


Figure 1 Typical Circuit

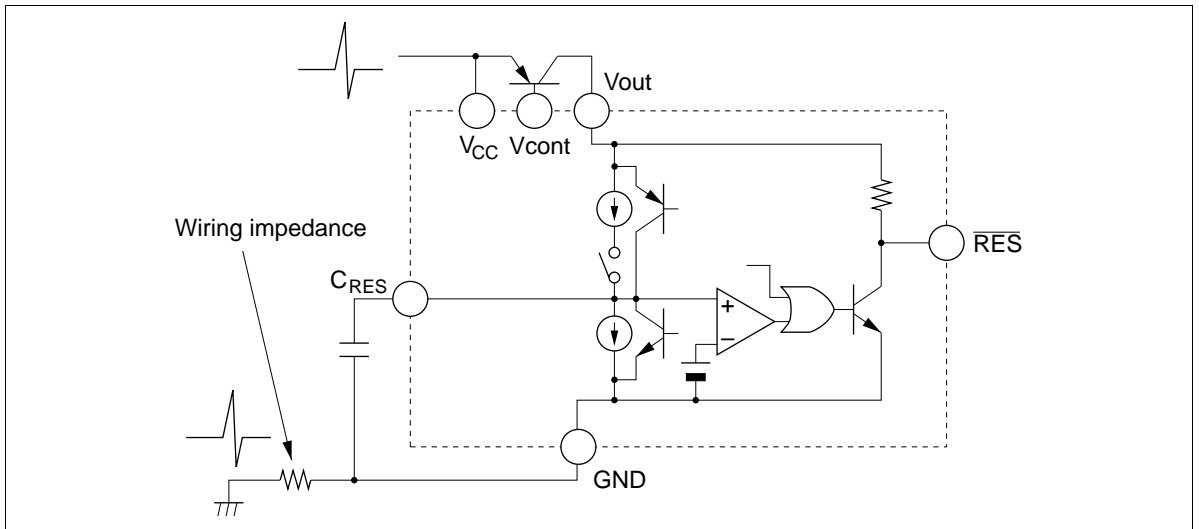
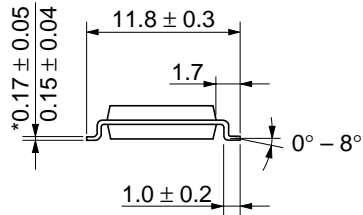
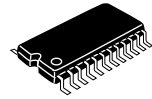
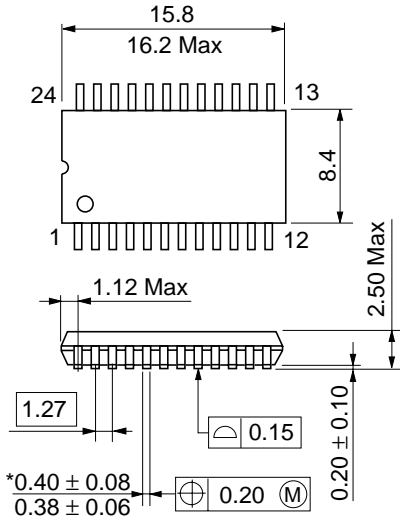


Figure 2  $\overline{\text{RES}}$  Comparator



Package Dimensions

Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-24D
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.6 g

## Cautions

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