

# HA16178P/FP

## Power Factor Correction Controller IC

REJ03D0903-0100

Rev.1.00

Jun 12, 2007

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### Description

The HA16178P/FP is a power-factor correction (PFC) controller IC.

This IC adopts continuous conduction mode as PFC operation.

Various functions such as over voltage detection, over current detection, soft start, feedback-loop disconnection detection, are incorporated in a single chip. This eliminates a significant amount of external circuitry.

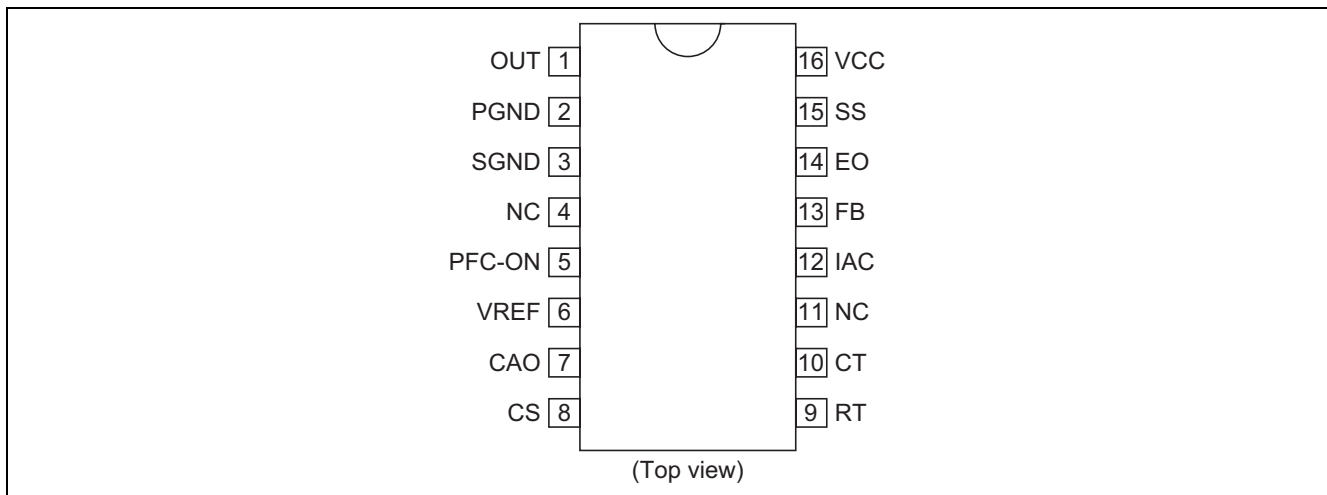
PFC operation can be turned on and off by an external control signal. By using this function, PFC operation can be disabled at low input voltage, allowing remote control from the secondary side.

A soft-start control pin provides for the easy adjustment of soft-start operation, and can be used to prevent overshooting of the output voltage.

### Features

- Maximum ratings
  - Power-supply voltage  $V_{CC}$ : 24 V
  - Operating junction temperature  $T_{jopr}$ :  $-40$  to  $125^{\circ}\text{C}$
- Electrical characteristics
  - VREF output voltage VREF:  $5.0\text{ V} \pm 3\%$
  - UVLO operation start voltage  $V_H$ :  $10.5 \pm 0.7\text{ V}$
  - UVLO operation stop voltage  $V_L$ :  $9.0 \pm 0.5\text{ V}$
  - PFC output maximum ON duty  $D_{max-out}$ : 95% (typ.)
- Functions
  - Continuous conduction mode
  - Over voltage detection
  - Over current detection
  - Soft start
  - Feedback loop disconnection detection
  - PFC function on/off control
  - Package lineup: SOP-16 and DILP-16

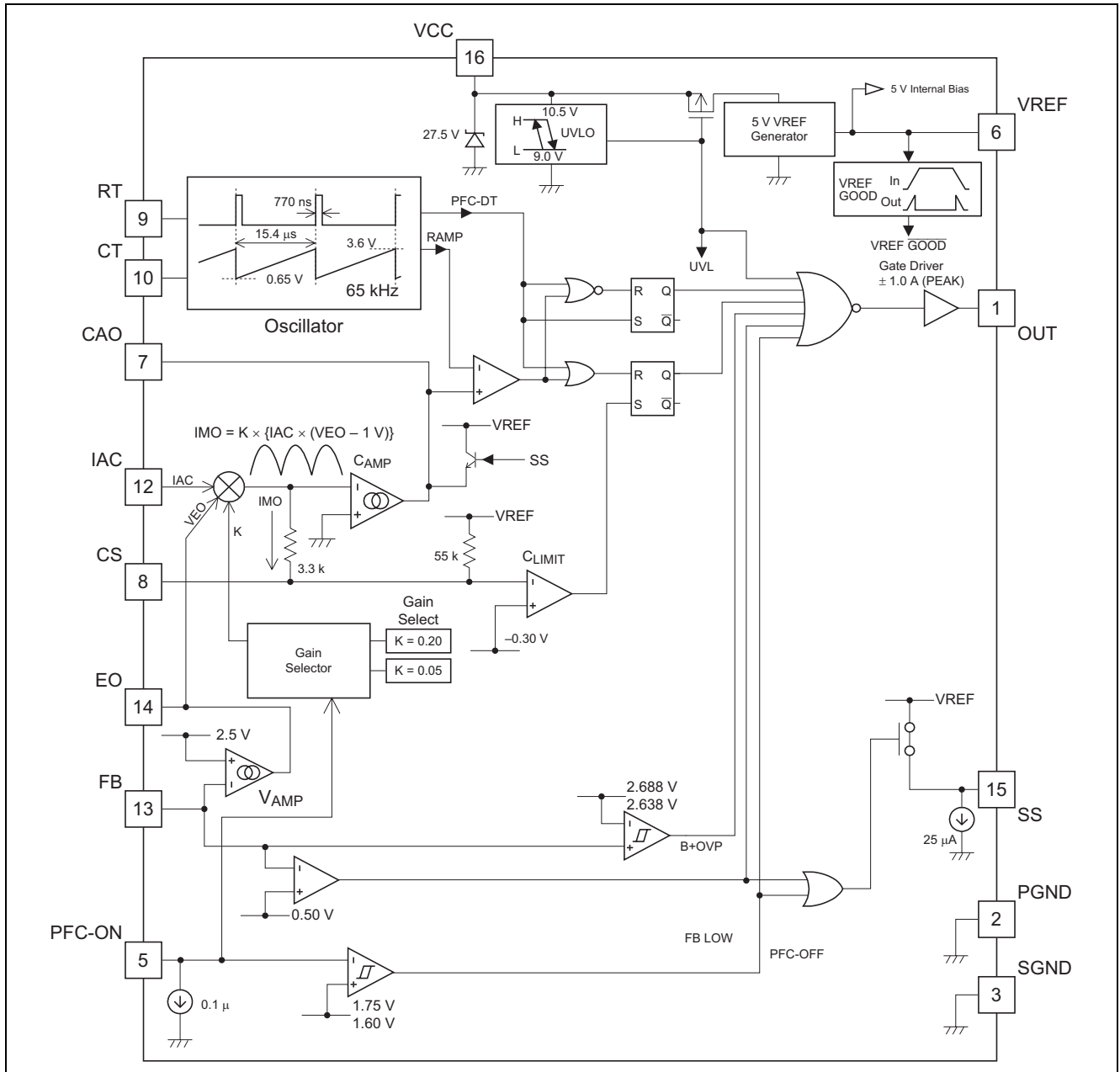
## Pin Arrangement



## Pin Description

| Pin No. | Pin Name | I/O          | Function  |
|---------|----------|--------------|---|
| 1       | OUT      | Output       | Power MOS FET gate driver output                  |
| 2       | PGND     | —            | Ground  |
| 3       | SGND     | —            | Ground  |
| 4       | NC       | —            | No connection                                     |
| 5       | PFC-ON   | Input        | PFC function on/off signal input                  |
| 6       | VREF     | Output       | Reference voltage output                          |
| 7       | CAO      | Output       | Current control error amplifier output            |
| 8       | CS       | Input/Output | Current sense signal input                        |
| 9       | RT       | Input/Output | Timing resistor for operational frequency adjust  |
| 10      | CT       | Output       | Timing capacitor for operational frequency adjust |
| 11      | NC       | —            | No connection                                     |
| 12      | IAC      | Input        | Multiplier reference current input                |
| 13      | FB       | Input        | Voltage control error amplifier input             |
| 14      | EO       | Output       | Voltage control error amplifier output            |
| 15      | SS       | Output       | Timing capacitor for soft start time adjust       |
| 16      | VCC      | Input        | Power supply voltage input                        |

## Block Diagram



## Absolute Maximum Ratings

(Ta = 25°C)

| Item                           | Symbol                    | Ratings                   | Unit | Note |
|--------------------------------|---------------------------|---------------------------|------|------|
| Supply voltage                 | VCC                       | 24                        | V    |      |
| OUT peak current               | I <sub>pk-out</sub>       | ±1.0                      | A    | 3    |
| OUT DC current                 | I <sub>dc-out</sub>       | ±0.1                      | A    |      |
| Terminal voltage               | Vi-group1                 | −0.3 to V <sub>cc</sub>   | V    | 4    |
|                                | Vi-group2                 | −0.3 to V <sub>ref</sub>  | V    | 5    |
| CAO voltage                    | V <sub>cao</sub>          | −0.3 to V <sub>caoh</sub> | V    |      |
| EO voltage                     | V <sub>eo</sub>           | −0.3 to V <sub>eoh</sub>  | V    |      |
| PFC-ON voltage                 | V <sub>pfc-on</sub>       | −0.3 to +6.5              | V    |      |
| PFC-ON clamp current           | I <sub>pfc-on-clamp</sub> | 300                       | μA   |      |
| RT current                     | I <sub>rt</sub>           | −200                      | μA   |      |
| CT current                     | I <sub>ct</sub>           | ±800                      | μA   |      |
| IAC current                    | I <sub>iac</sub>          | 1                         | mA   |      |
| CS voltage                     | V <sub>i-cs</sub>         | −1.5 to 0.3               | V    |      |
| VREF current                   | I <sub>o-ref</sub>        | −5                        | mA   |      |
| Power dissipation              | P <sub>t</sub>            | 1                         | W    | 6, 7 |
| Operating junction temperature | T <sub>j-opr</sub>        | −40 to 125                | °C   |      |
| Storage temperature            | T <sub>stg</sub>          | −55 to 150                | °C   |      |

Notes: 1. Rated voltages are with reference to the GND pin.

2. For rated currents, inflow to the IC is indicated by (+), and outflow by (−).

3. The transient current when driving a capacitive load.

4. This is the rated voltage for the following pins:

OUT

5. This is the rated voltage for the following pins:

VREF, FB, IAC, SS, RT, CT

6. HA16178P (DILP) type: θ<sub>ja</sub> = 120°C/W

7. HA16178FP (SOP) type: θ<sub>ja</sub> = 120°C/W

This is value mounted on glass epoxy board of 10% wiring density and 40 mm × 40 mm × 1.6 mm.

## Electrical Characteristics

(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

|               | Item                           | Symbol    | Min   | Typ   | Max   | Unit   | Test Conditions                       |
|---------------|--------------------------------|-----------|-------|-------|-------|--------|---------------------------------------|
| Supply        | Start threshold                | VH        | 9.8   | 10.5  | 11.2  | V      |                                       |
|               | Shutdown threshold             | VL        | 8.5   | 9.0   | 9.5   | V      |                                       |
|               | UVLO hysteresis                | dVUVL     | 1.0   | 1.5   | 2.0   | V      |                                       |
|               | Start-up current               | Is        | 140   | 200   | 260   | μA     | VCC = 9.5 V                           |
|               | Is temperature stability       | dIs/dTa   | —     | −0.3  | —     | %/°C   | * <sup>1</sup>                        |
|               | Operating current              | Icc       | 3.45  | 4.5   | 6.45  | mA     | IAC = 0 A, CL = 0 F                   |
| VREF          | Output voltage                 | Vref      | 4.85  | 5.00  | 5.15  | V      | Isourse = 1 mA                        |
|               | Line regulation                | Vref-line | —     | 5     | 20    | mV     | Isourse = 1 mA,<br>VCC = 12 V to 23 V |
|               | Load regulation                | Vref-load | —     | 5     | 20    | mV     | Isourse = 1 mA to 5 mA                |
|               | Temperature stability          | dVref     | —     | ±80   | —     | ppm/°C | Ta = −40 to 125°C * <sup>1</sup>      |
| Oscillator    | Initial accuracy               | fout      | 58.5  | 65    | 71.5  | kHz    | Measured pin: OUT                     |
|               | fout temperature stability     | dfout/dTa | —     | ±0.1  | —     | %/°C   | Ta = −40 to 125°C * <sup>1</sup>      |
|               | fout voltage stability         | fout-line | −1.5  | 0.5   | 1.5   | %      | VCC = 12 V to 18 V                    |
|               | CT peak voltage                | Vct-H     | —     | 3.6   | 4.0   | V      | * <sup>1</sup>                        |
|               | Ramp valley voltage            | Vct-L     | —     | 0.65  | —     | V      | * <sup>1</sup>                        |
|               | RT voltage                     | Vrt       | 1.07  | 1.25  | 1.43  | V      |                                       |
| Soft start    | Sink current                   | Iss       | 15.0  | 25.0  | 35.0  | μA     | SS = 2 V                              |
| Current limit | Threshold voltage <sup>1</sup> | VCL1      | −0.33 | −0.30 | −0.27 | V      | PFC-ON = 2 V                          |
|               | Delay to output                | td-CL     | —     | 280   | 500   | ns     | CS = 0 to −1 V                        |
| VAMP          | Feedback voltage               | Vfb       | 2.40  | 2.50  | 2.60  | V      | FB-EO Short                           |
|               | Input bias current             | Ifb       | −0.3  | 0     | 0.3   | μA     | Measured pin: FB                      |
|               | Open loop gain                 | Av-v      | —     | 60    | —     | dB     | * <sup>1</sup>                        |
|               | High voltage                   | Veoh      | 5.2   | 5.7   | 6.2   | V      | FB = 2.3 V, EO: Open                  |
|               | Low voltage                    | Veol      | —     | 0.1   | 0.3   | V      | FB = 2.7 V, EO: Open                  |
|               | Source current                 | Isrc-eo   | —     | −120  | —     | μA     | FB = 1.0 V, EO = 2.5 V                |
|               | Sink current                   | Isnk-eo   | —     | 120   | —     | μA     | FB = 4.0 V, EO = 2.5 V                |
|               | Transconductance               | Gm-v      | 150   | 200   | 290   | μA/V   | FB = 2.5 V, EO = 2.5 V                |
| CAMP          | Input offset voltage           | Vio-ca    | —     | (−10) | 0     | mV     | * <sup>1</sup>                        |
|               | Open loop gain                 | Av-ca     | —     | 60    | —     | dB     | * <sup>1</sup>                        |
|               | High voltage                   | Vcaoh     | 5.2   | 5.7   | 6.2   | V      |                                       |
|               | Low voltage                    | Vcaol     | —     | 0.1   | 0.3   | V      |                                       |
|               | Source current                 | Isrc-ca   | —     | −90   | —     | μA     | CAO = 2.5 V * <sup>1</sup>            |
|               | Sink current                   | Isnk-ca   | —     | 90    | —     | μA     | CAO = 2.5 V * <sup>1</sup>            |
|               | Transconductance               | Gm-c      | 150   | 200   | 290   | μA/V   | * <sup>1</sup>                        |

Note: 1. Design spec.

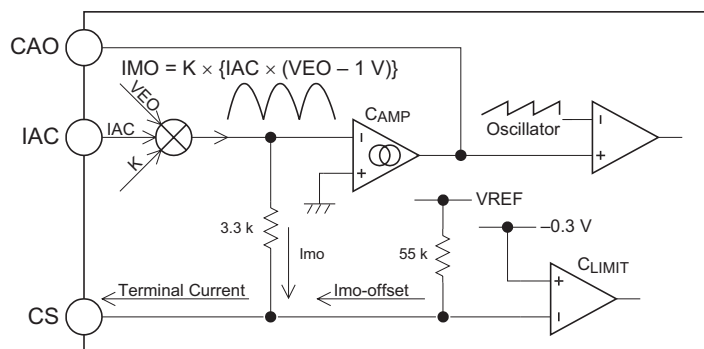
(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

|                    | Item                               | Symbol     | Min   | Typ   | Max   | Unit | Test Conditions                        |
|--------------------|------------------------------------|------------|-------|-------|-------|------|--|
| IAC/<br>Multiplier | IAC PIN voltage                    | Viac       | 1.6   | 2.3   | 3.0   | V    | IAC = 100 μA                           |
|                    | Terminal offset current            | Imo-offset | -136  | -90   | -73   | μA   | IAC = 0 A, CS = 0 V                    |
|                    | Output current<br>(PFC-ON = 2.5 V) | Imo1       | —     | -20   | —     | μA   | EO = 2 V, IAC = 100 μA <sup>*1,2</sup> |
|                    |                                    | Imo2       | —     | -60   | —     | μA   | EO = 4 V, IAC = 100 μA <sup>*1,2</sup> |
|                    | Output current<br>(PFC-ON = 5.5 V) | Imo3       | —     | -5    | —     | μA   | EO = 2 V, IAC = 100 μA <sup>*1,2</sup> |
|                    |                                    | Imo4       | —     | -15   | —     | μA   | EO = 4 V, IAC = 100 μA <sup>*1,2</sup> |
|                    | PFC-CS resistance                  | Rmo        | —     | 3.3   | —     | kΩ   | <sup>*1</sup>                          |
|                    | Gain voltage                       | Vpfc-gain  | (3.4) | (4.1) | (4.7) | V    | Gain = 0.125 <sup>*1</sup>             |
| OUT                | Minimum duty cycle                 | Dmin-out   | —     | —     | 0     | %    | CAO = 4.0 V                            |
|                    | Maximum duty cycle                 | Dmax-out   | 90    | 95    | 98    | %    | CAO = 0 V                              |
|                    | Rise time                          | tr-out     | —     | 30    | 100   | ns   | CL = 1000 pF                           |
|                    | Fall time                          | tf-out     | —     | 30    | 100   | ns   | CL = 1000 pF                           |
|                    | Low voltage                        | Vol1-out   | —     | 0.05  | 0.2   | V    | Iout = 20 mA                           |
|                    |                                    | Vol2-out   | —     | 0.5   | 2.0   | V    | Iout = 200 mA (Pulse Test)             |
|                    |                                    | Vol3-out   | —     | 0.03  | 0.7   | V    | Iout = 10 mA, VCC = 5 V                |
|                    | High voltage                       | Voh1-out   | 11.5  | 11.9  | —     | V    | Iout = -20 mA                          |
|                    |                                    | Voh2-out   | 10.0  | 11.0  | —     | V    | Iout = -200 mA (Pulse Test)            |

Notes: 1. Design spec.

2. Imo1 to Imo4 defined as,

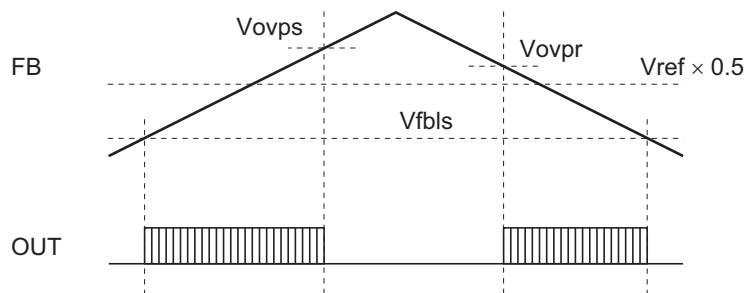
$$I_{mo} = (\text{CS Terminal Current}) - (I_{mo\text{-offset}})$$



(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

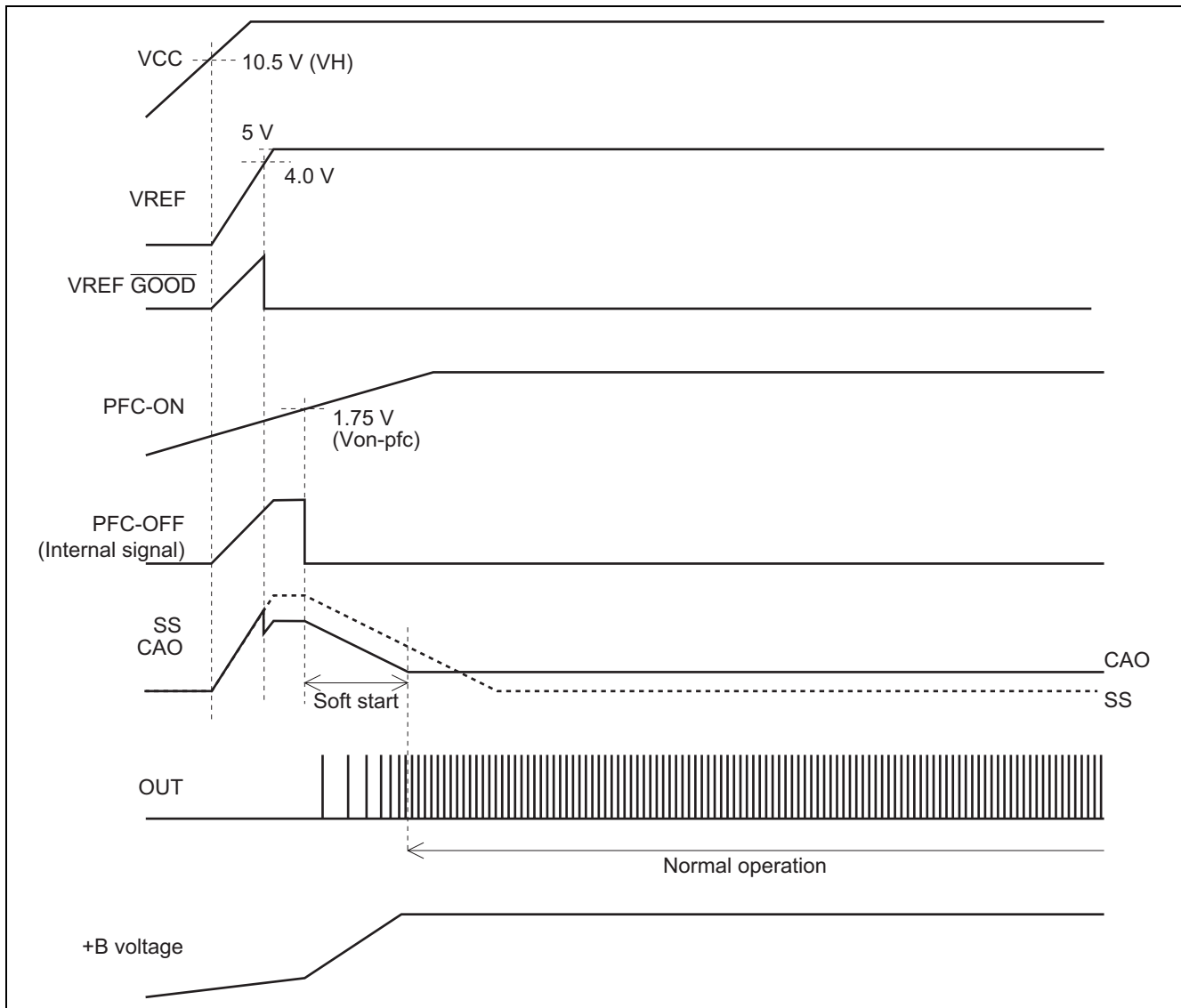
|                   | Item                 | Symbol   | Min   | Typ   | Max   | Unit | Test Conditions              |
|-------------------|----------------------|----------|-------|-------|-------|------|------------------------------|
| Supervisor/<br>PG | PFC enable voltage   | Von-pfc  | 1.62  | 1.75  | 1.87  | V    | Input pin: PFC-ON            |
|                   | PFC disable voltage  | Voff-pfc | 1.48  | 1.6   | 1.72  | V    | Input pin: PFC-ON            |
|                   | Input current        | Ipfc-on  | —     | 0.1   | 1.0   | μA   | PFC-ON = 2 V                 |
|                   | B+ OVP set voltage   | dVovps   | 0.125 | 0.188 | 0.250 | V    | Input pin: FB * <sup>1</sup> |
|                   | B+ OVP reset voltage | dVovpr   | 0.075 | 0.138 | 0.200 | V    | Input pin: FB * <sup>1</sup> |
|                   | FB low set voltage   | Vfbls    | 0.45  | 0.50  | 0.55  | V    | Input pin: FB                |

Note: 1.  $dVovps = Vovps - Vref \times 0.5$   
 $dVovpr = Vovpr - Vref \times 0.5$



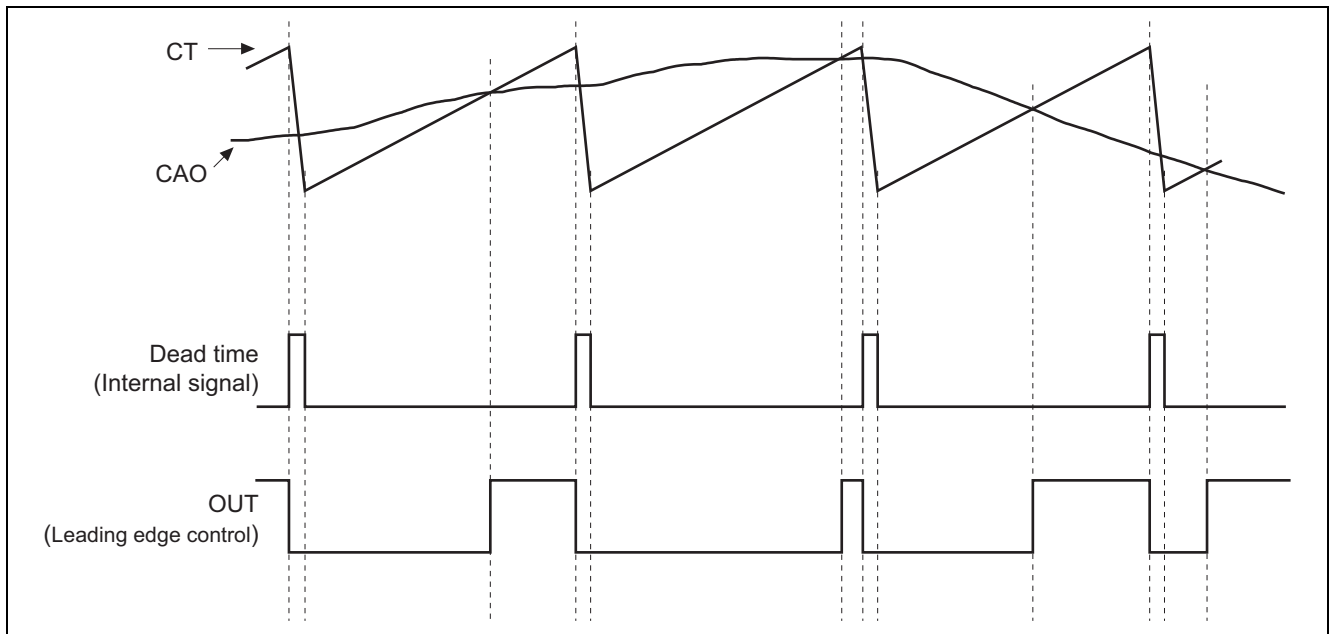
## Timing Chart

### 1. Start-up Timing

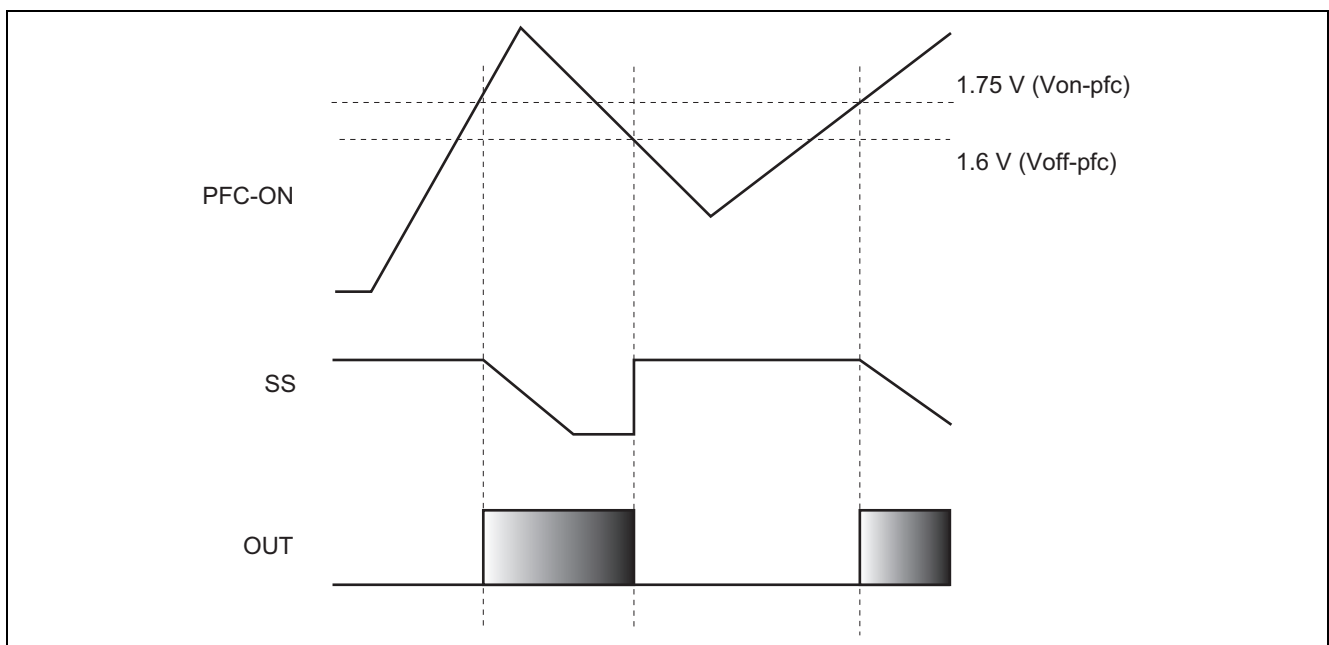




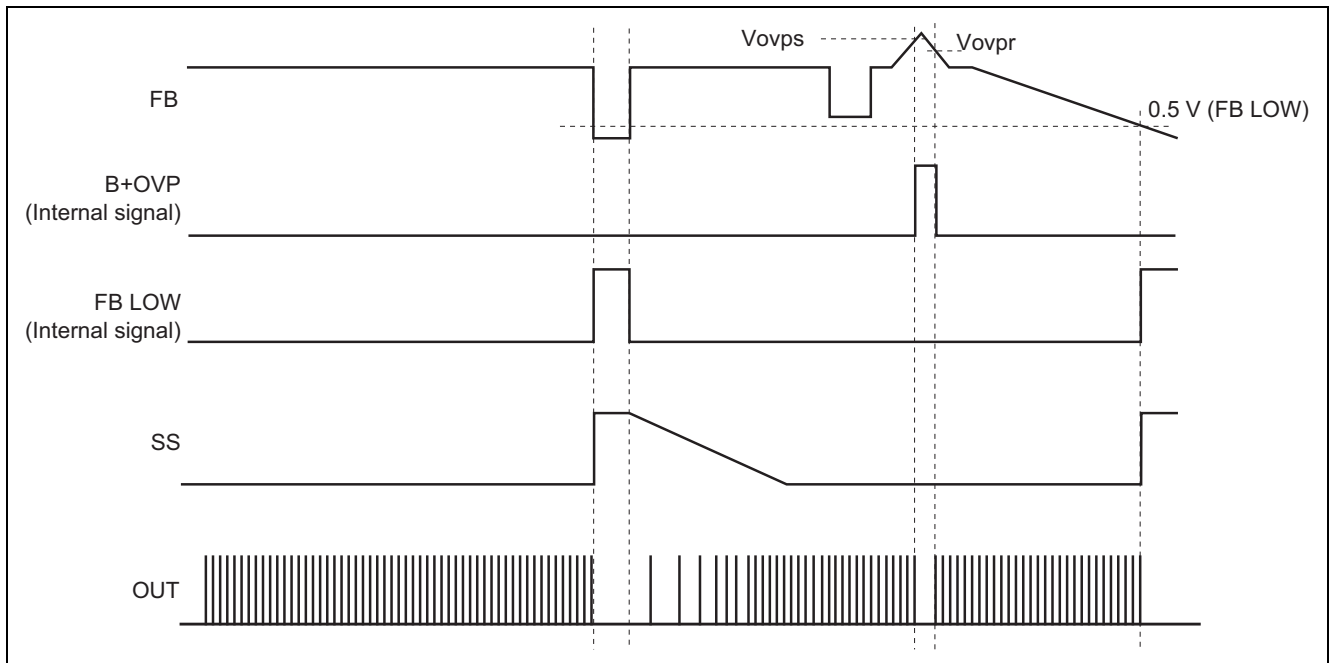
## 2. Oscillator, Gate Driver Output



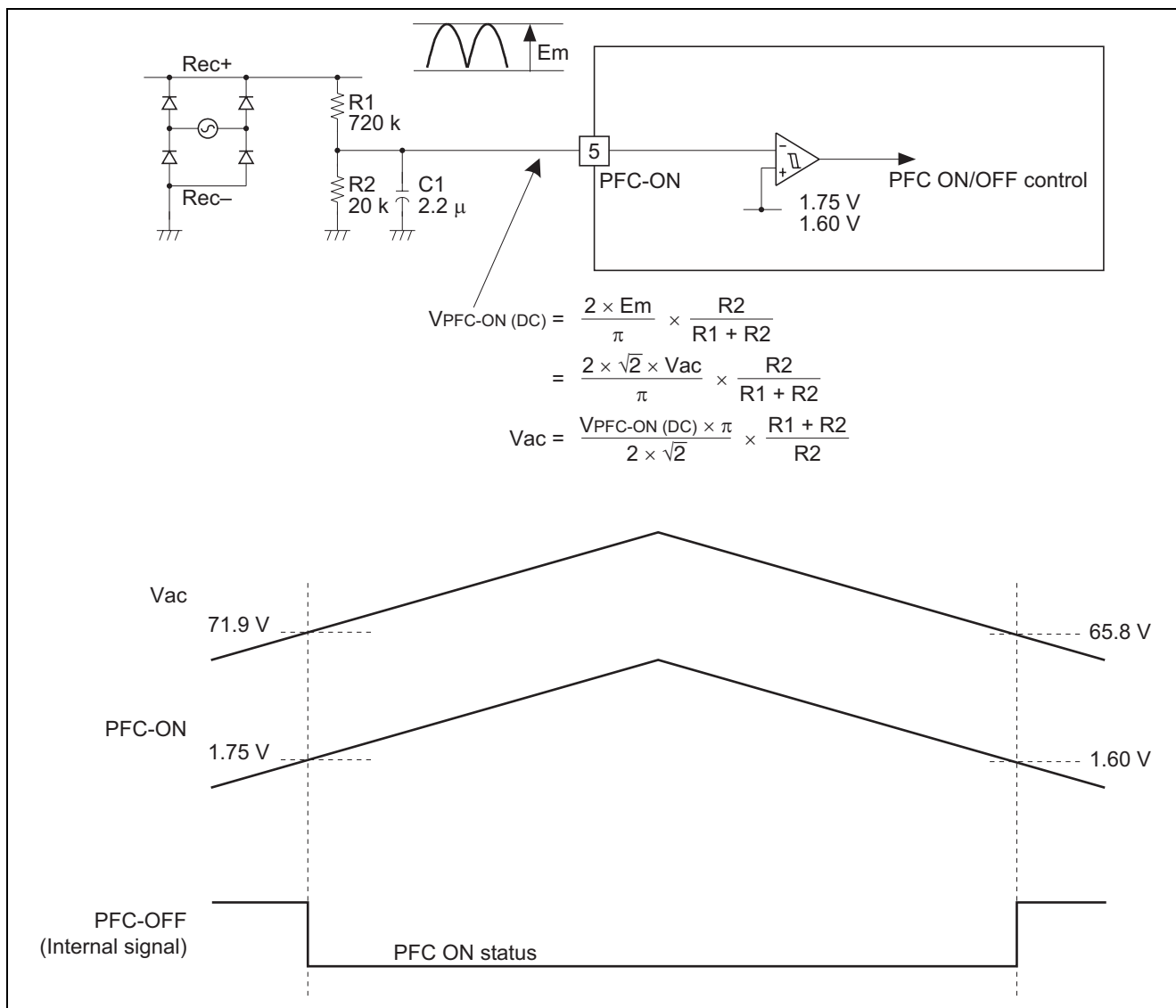
## 3. PFC Operation ON/OFF



## 4. FB Supervisor



## 5. PFC ON/OFF Function



## Description of Pin Functions

### OUT Pin:

The power MOS FET gate-drive signal is output from this pin, and takes the form of a rectangular waveform with an amplitude of VCC-GND.

### PGND Pin:

The ground terminal for OUT driver.

### SGND Pin:

The ground terminal for internal circuits.

### PFC-ON Pin:

This pin is applied smoothing voltage of rectified AC voltage. When 1.75 V (typ.) or more is applied to this pin, PFC operation starts. When the voltage is 1.6 V (typ.) or lower, the PFC operation stops.

### VREF Pin:

Temperature-compensated voltage with an accuracy of  $5\text{ V} \pm 3\%$  is output from this pin. The pin should supply no more than 5 mA (max.) source current. This pin has no sink capabilities.

### CAO Pin:

This pin is the current-error amplifier output, and is connected to the phase-compensation circuit of the current-error amp. The result of comparison of the voltage on this pin and the CT pin produces the pulse output from the OUT pin.

### CS Pin:

Current detection pin. The current is controlled to be proportional to the AC voltage and the power factor is corrected. When the voltage on this pin drops to  $-0.3\text{ V}$  (typ.) or below, over current detection circuit operates, and OUT pin is stopped.

### RT Pin:

A pin for frequency adjustment of the oscillator.

### CT Pin:

A pin for frequency adjustment of the oscillator.

### IAC Pin:

This pin is for detecting the input AC voltage waveform. For processing within the IC, the AC voltage waveform is converted to current information.

### FB Pin:

This pin is the input to the voltage error amp. This pin is applied to voltage divided PFC output with resistors. The feedback loop is intended to keep 2.5 V (typ.).

### EO Pin:

This pin is the output of the voltage error amp. This pin is connected to the phase-compensation circuit of the voltage error amp. The voltage on this pin is the input signal to the internal multiplier.

### SS Pin:

This pin is connected to GND or VREF via a capacitor. This pin is pulled up to the VREF pin voltage until PFC operation starts. When the voltage on the PFC-ON pin has reached 1.75 V (typ.) PFC operation is start and this pin flows 25  $\mu\text{A}$  source current. Operation of the CAO pin is affected by that of the SS pin, the pulse width of the OUT pin is limited, and this prevents overshooting when start up.

### VCC Pin:

IC power-supply pin. The IC starts up at 10.5 V (typ.), and stops at 9 V (typ.).

## Description of Functions

### 1. UVL Circuit

The UVL circuit monitors the VCC voltage. When the voltage is lower than 9.0 V, the IC is stopped. When the voltage is higher than 10.5 V, IC is started.

When operation of the IC is stopped by the UVL circuit, the driver circuit output is fixed low, output of VREF is stopped, and the oscillator is stopped.

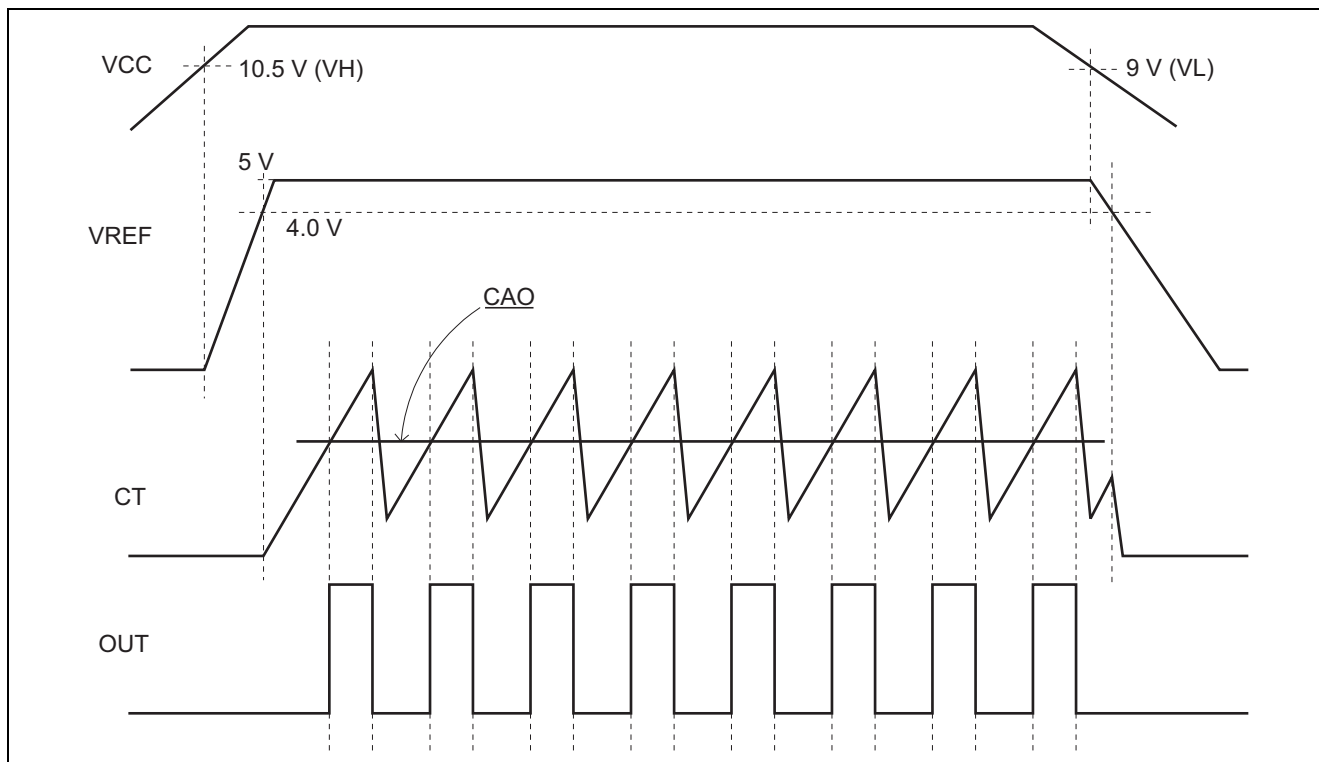


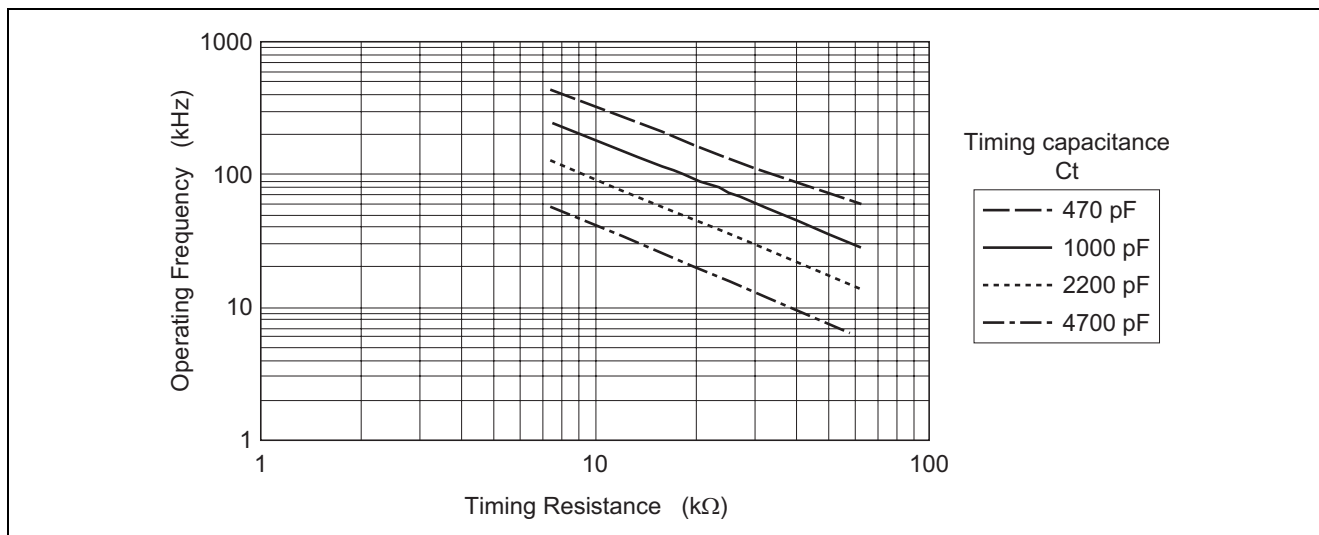
Figure 1 UVL Operation

## 2. Operating Frequency

The HA16178 operating frequency  $f_{osc}$  is determined by adjusting the timing resistor  $R_t$  (the RT pin, pin 9) and the timing capacitance  $C_t$  (the CT pin, pin 10). The operating frequency is approximated by the following expression:

$$f_{osc} = \frac{1.755 \times 10^6}{R_t (k\Omega) \times C_t (pF)} \quad (kHz)$$

When the IC is operated at high frequencies, the expression becomes less accurate due to IC internal delay time, etc. Please confirm operation the value with the actually mounted IC. The maximum operating frequency is 400 kHz. As a reference, the operating frequency data when the timing resistor and the timing capacitance are changed is shown in the below figure.



**Figure 2 Operating Frequency Characteristics**

### 3. Soft Start

This function prevents applying excessive stress on external components and overshooting of the PFC output voltage (B + voltage) when start up. The pulse width is gradually widening from 0% duty cycle. During soft-start operation, the SS and CAO signals lower with link. The duty cycle is controlled by the CAO signal.

The soft-start time can be set by an external capacity.

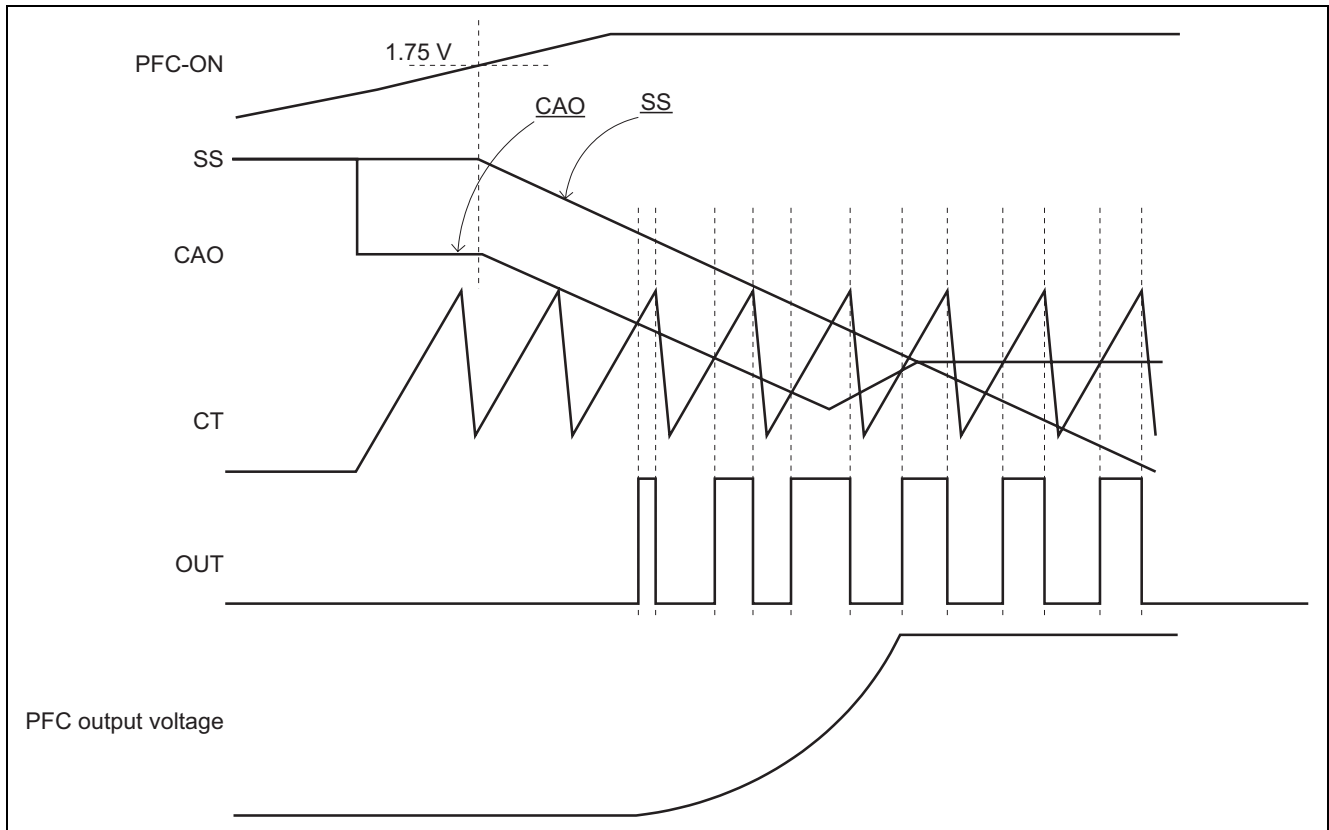
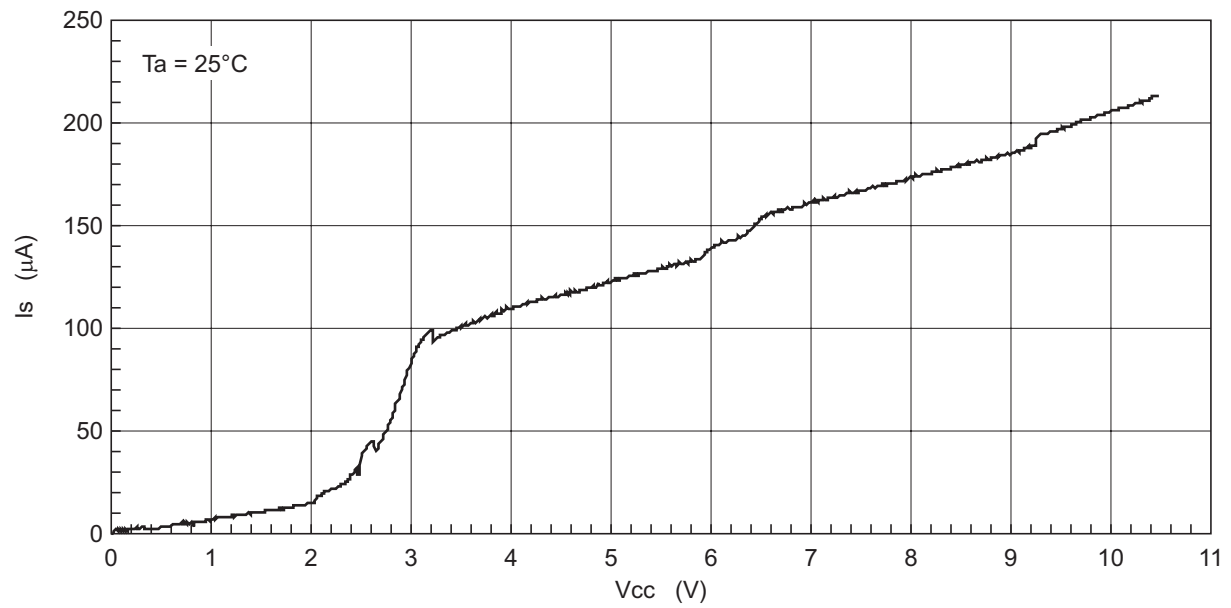


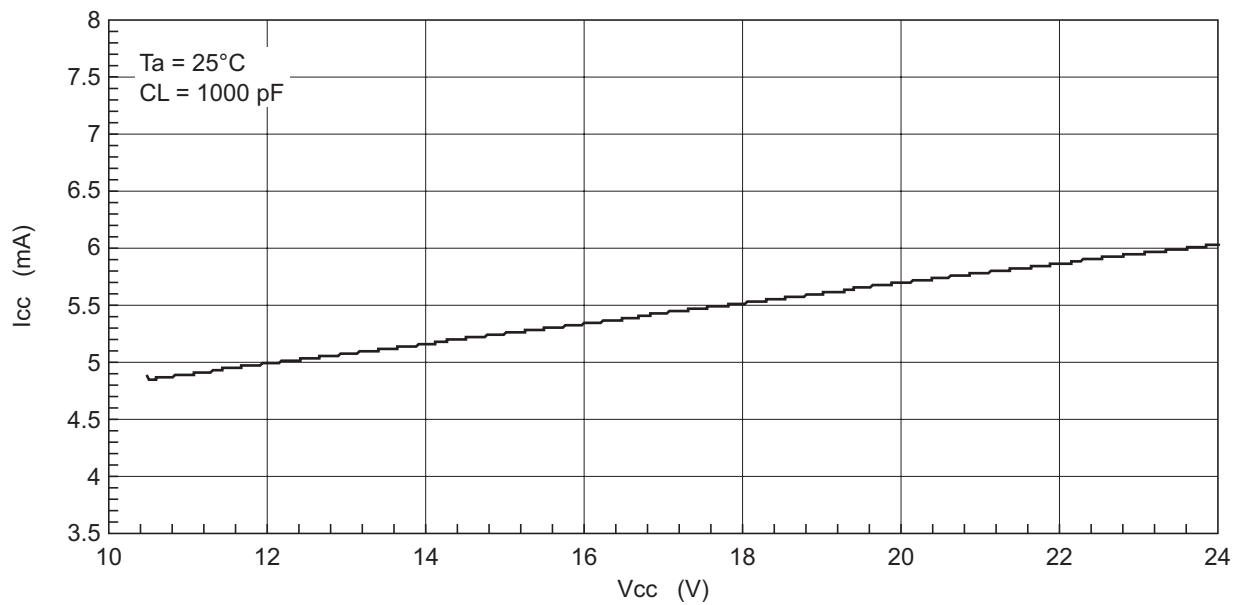
Figure 3 Soft-Start Operation Waveform

## Main Characteristics

Standby Current vs. Power Supply Voltage Characteristics

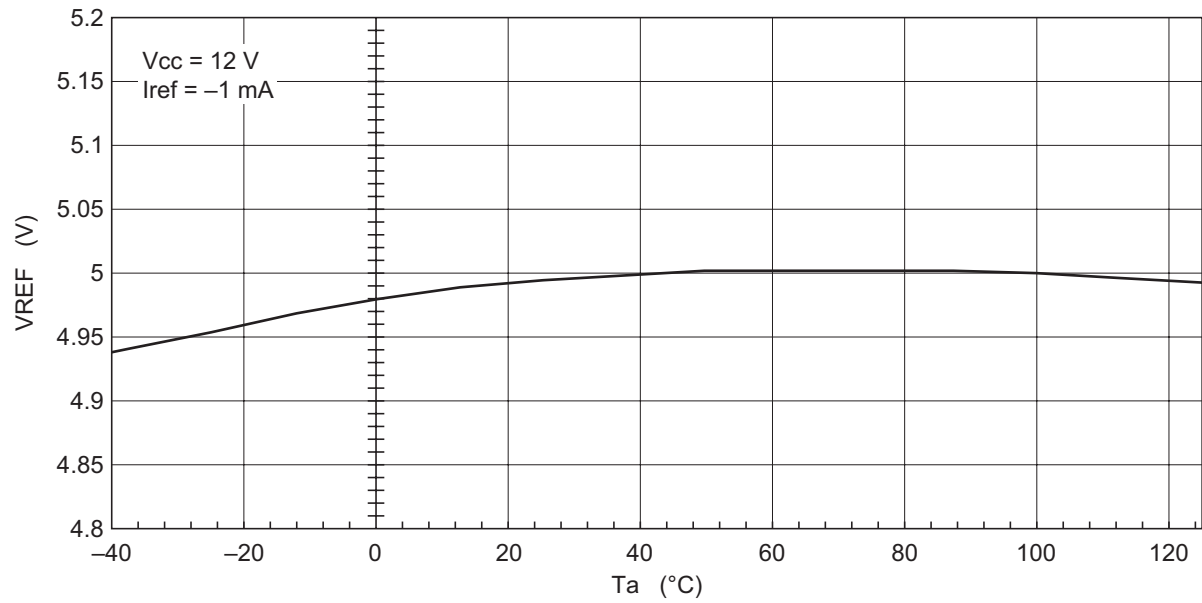


Power Dissipation vs. Power Supply Voltage Characteristics

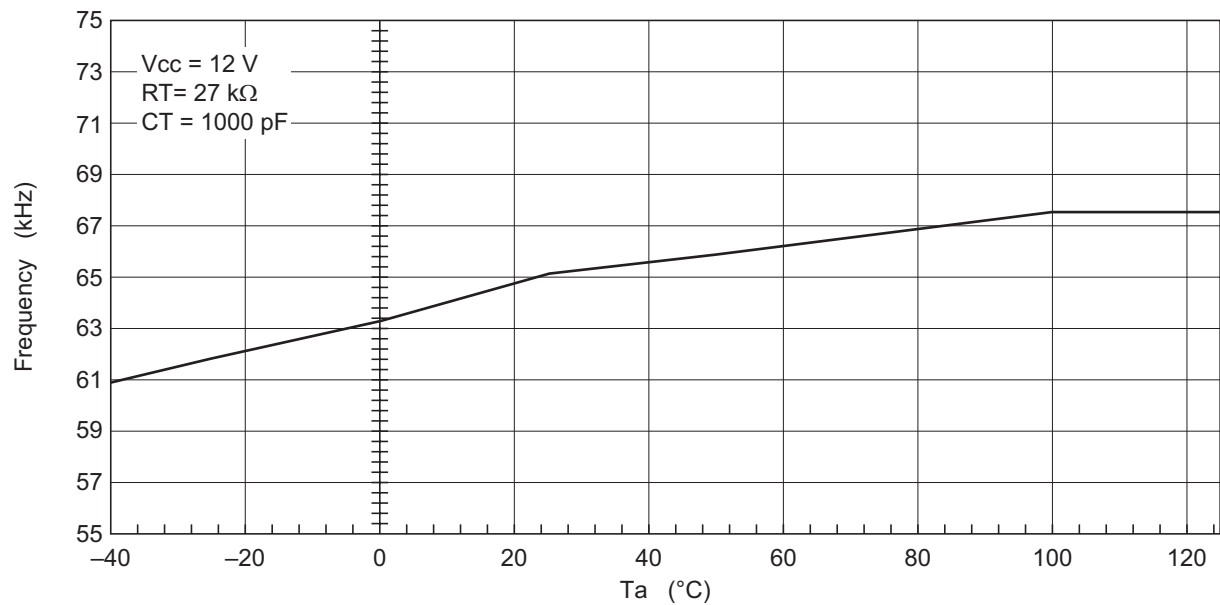


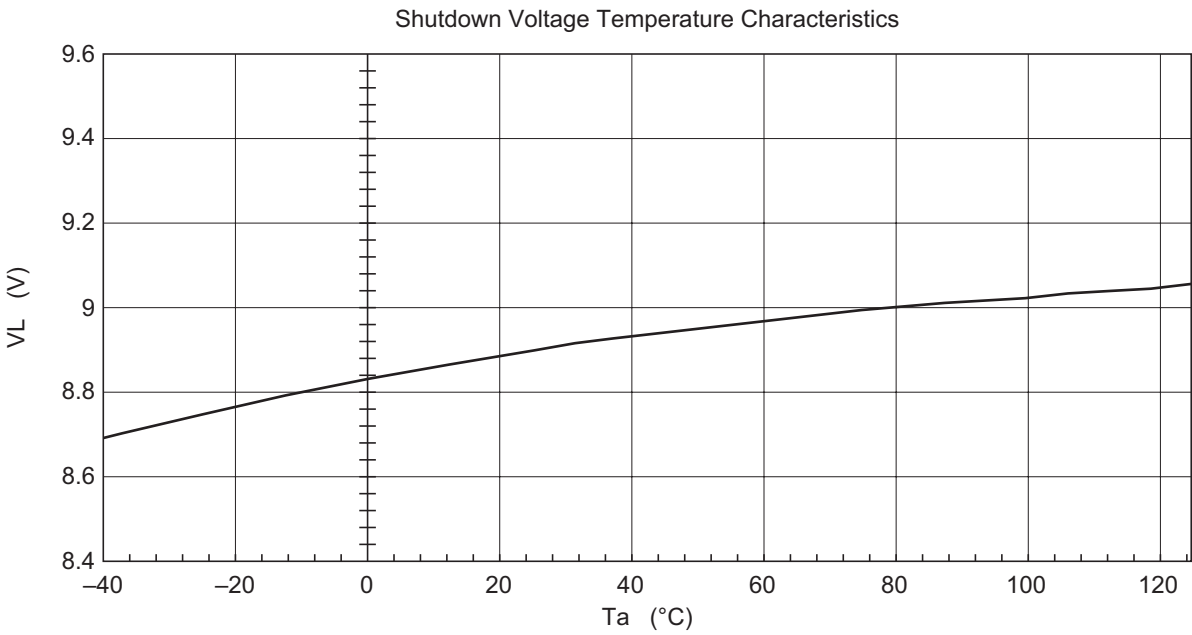
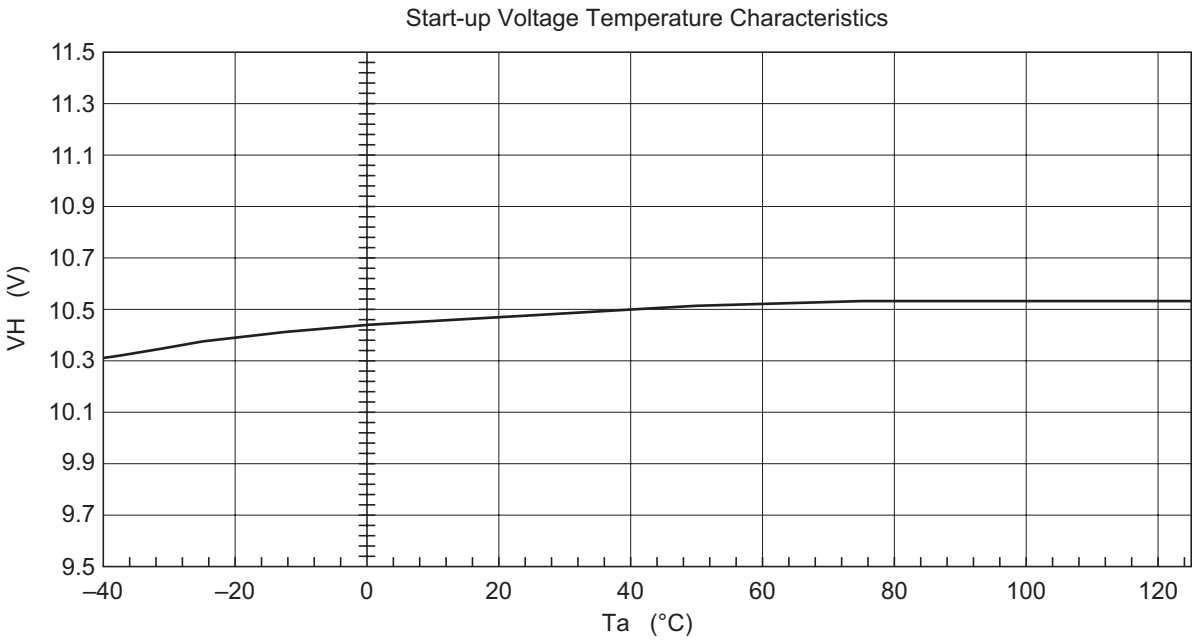


Reference Voltage Temperature Characteristics

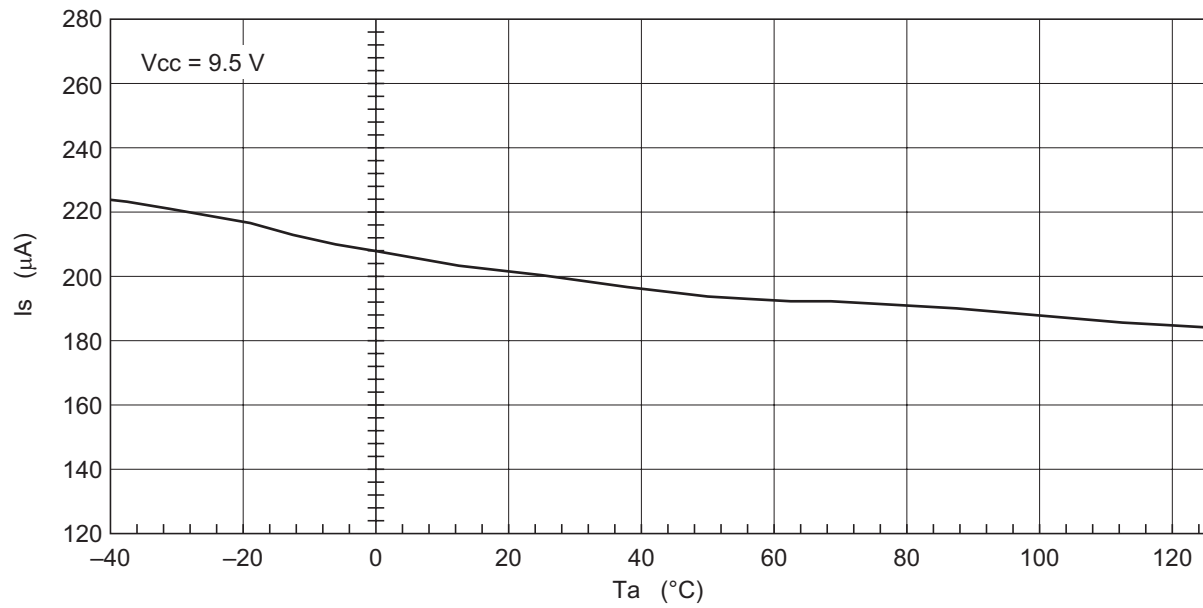


Operating Frequency Temperature Characteristics

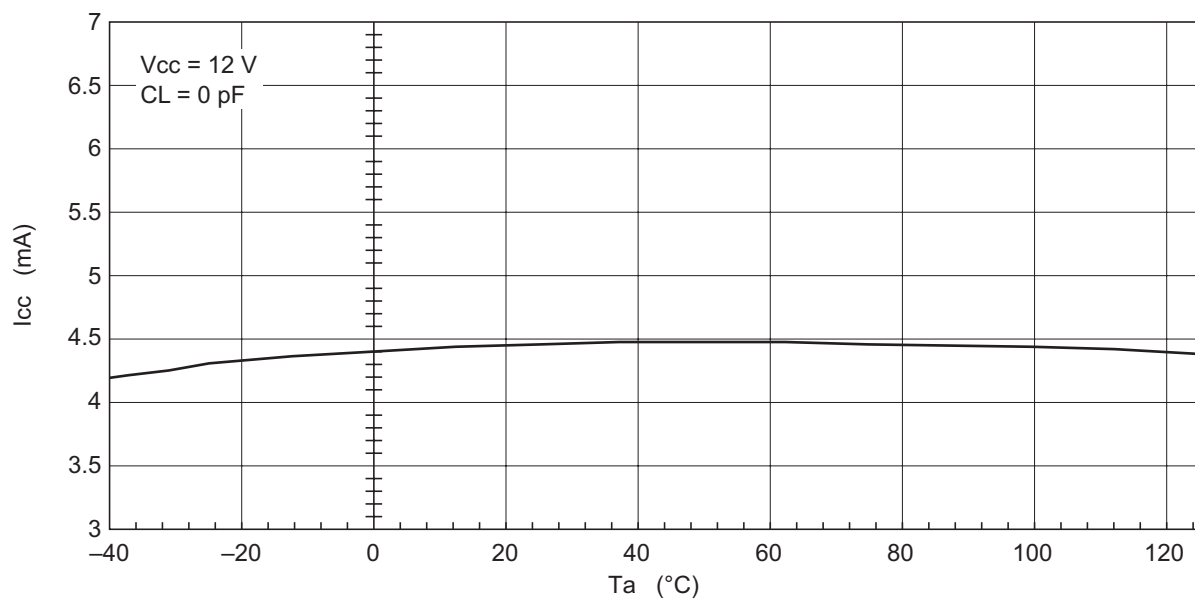




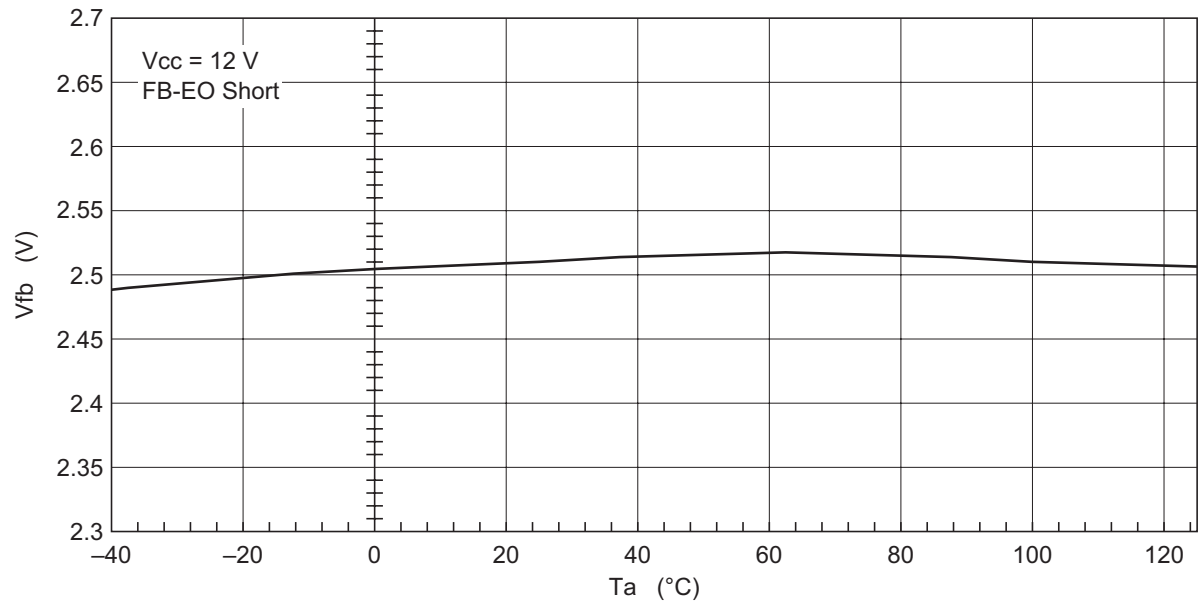
Standby Current Temperature Characteristics



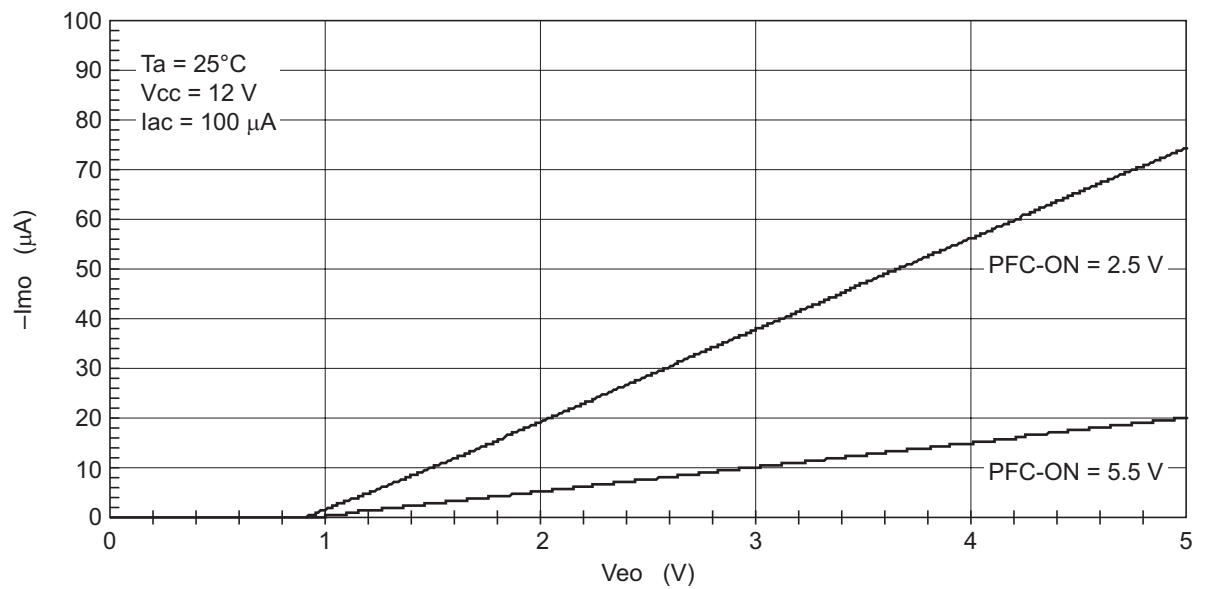
Operating Current Temperature Characteristics

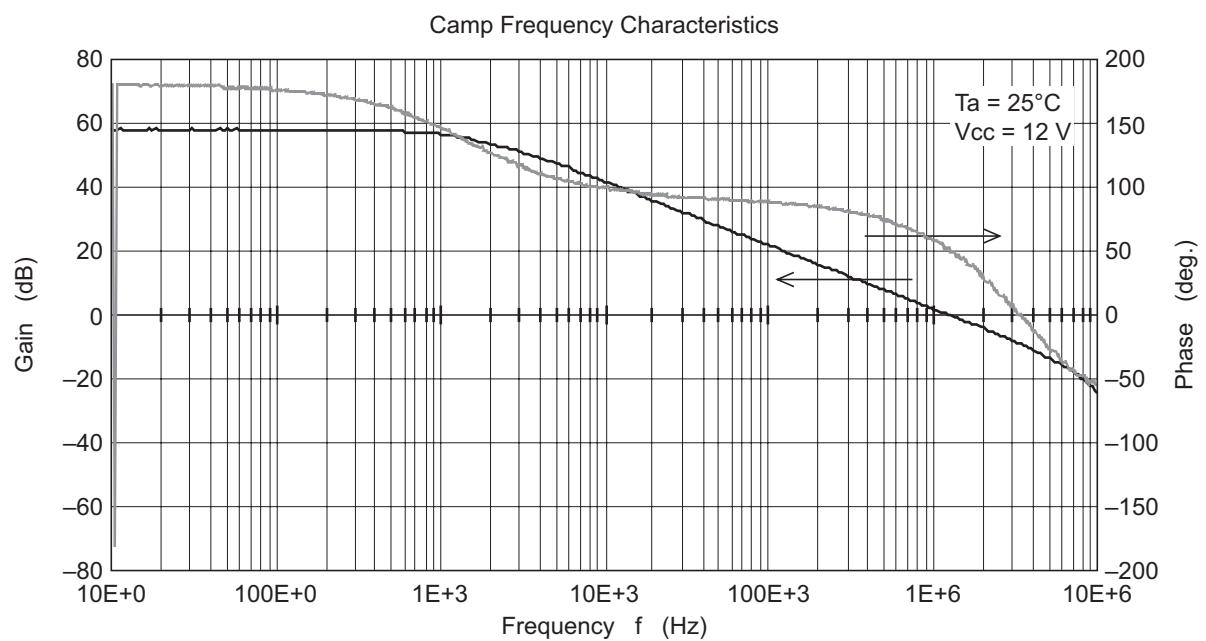
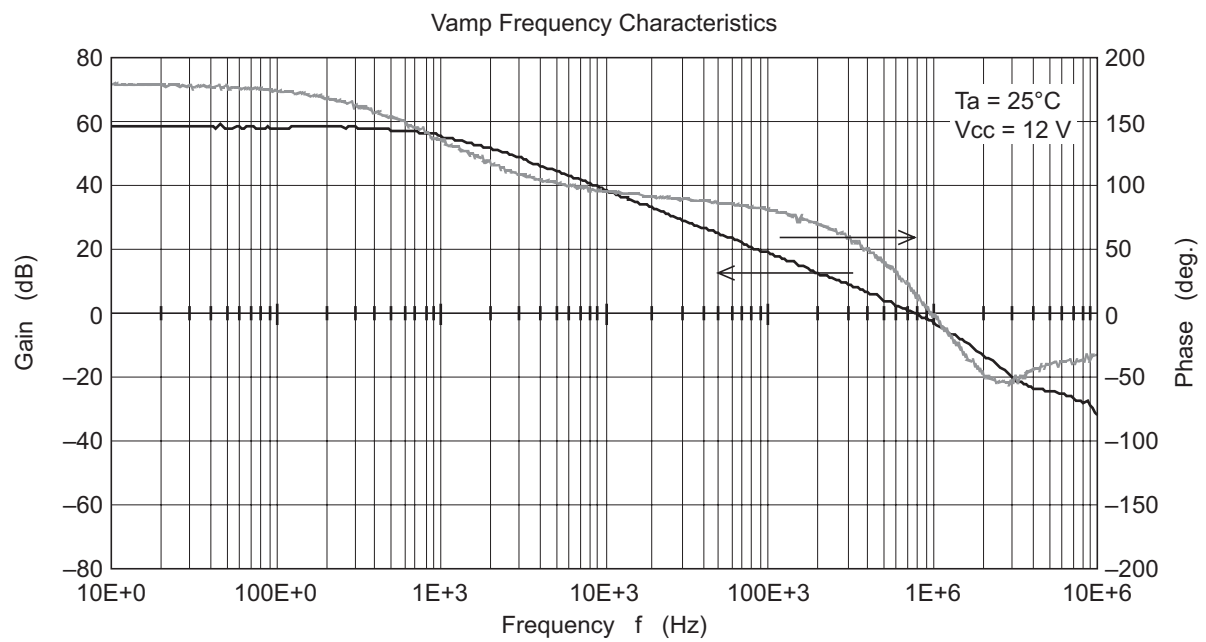


VAMP Feedback Voltage Temperature Characteristics



EO Pin Voltage vs. CS Pin Current Characteristics





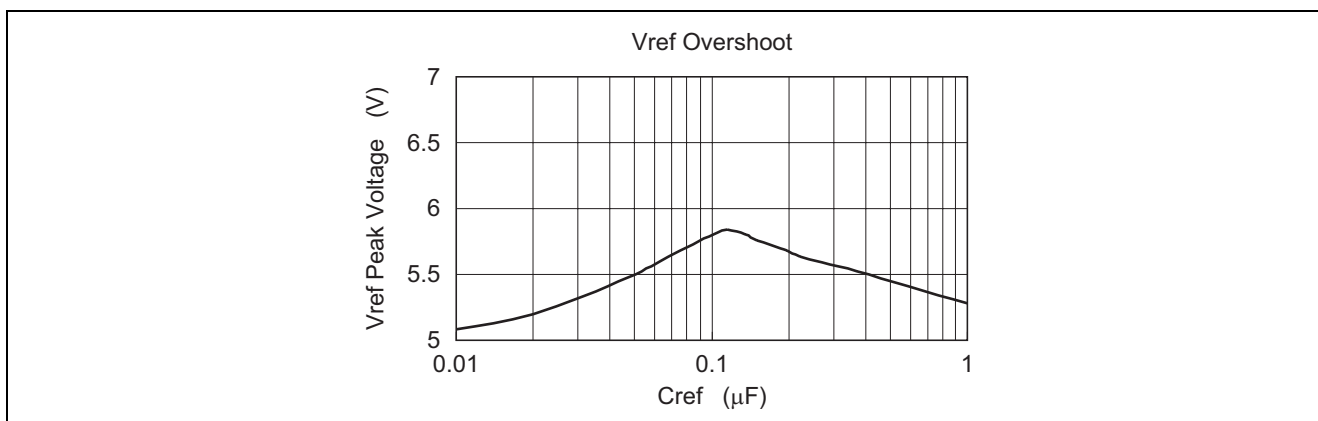
## Precautions on Usage

### 1. CS Pin

The CS pin is used to for detection in PFC control led current. When power supply is started up, the voltage drop of inrush current must not exceed the maximum rated value of the CS pin.

### 2. VREF Pin

For stabilization, be sure to connect a capacitor between the pin and ground. It possible to occur overshoot of VREF by connected capacitance. The degree of the overshoot will depend on the value of the connected capacitor. Pay particular attention to this point if you intend to use the VREF pin voltage as reference voltage for an external circuit.



**Figure 4 Overshoot on the VREF Pin vs. Capacitance**

### 3. PFC-ON Pin

In design of worldwide power supply, it is possible that calculated voltage exceed maximum rated voltage of PFC-ON pin. Actually, as a clamp circuit is included in the PFC-ON pin, the voltage is clamped however, clamp current must not exceed 300 μA.

### 4. OUT Pin

Undershooting or overshooting may occur due to the wiring of the OUT pin. These may bring to malfunctions of the IC. In such a case, prevent the undershooting or overshooting by using a Schottky barrier diode, etc.

### 5. Pattern Layout

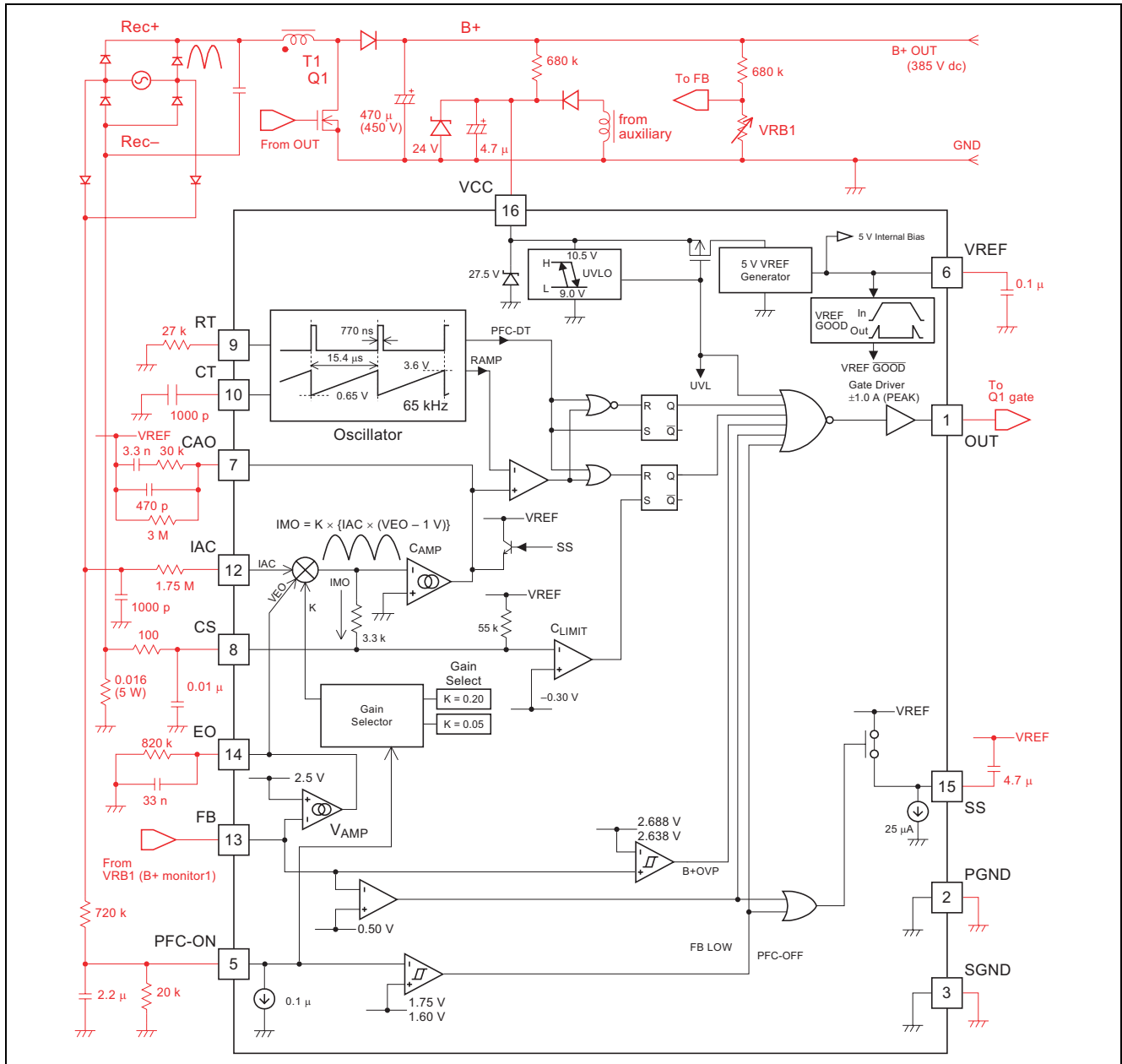
In designing the pattern layout, pay as much attention as is possible to the following points.

- (1) Place the stabilizing capacitor for the VREF pin as close to the IC as possible, and keep the wiring short.
- (2) Place the timing resistor of the RT pin as close to the IC as possible, and keep the wiring short.
- (3) Place the phase compensation circuit for the CAO pin as close to the IC as possible, and keep the wiring short.
- (4) Place the timing capacitor for the CT pin as close to the IC as possible, and keep the wiring short.
- (5) Place the stabilizing capacitor for the VCC pin as close to the IC as possible, and keep the wiring short.
- (6) Place the IC pins and their wiring as far from high-voltage switching lines (particularly the drain voltage for the power MOS FET) as possible and in general design the wiring to minimize switching noise.
- (7) It is probable that stability of operation is achieved by inputting signals via filters to pins with input functions. Note, however, that such filter circuits can affect the bias conditions for pins that have both input and output functions.

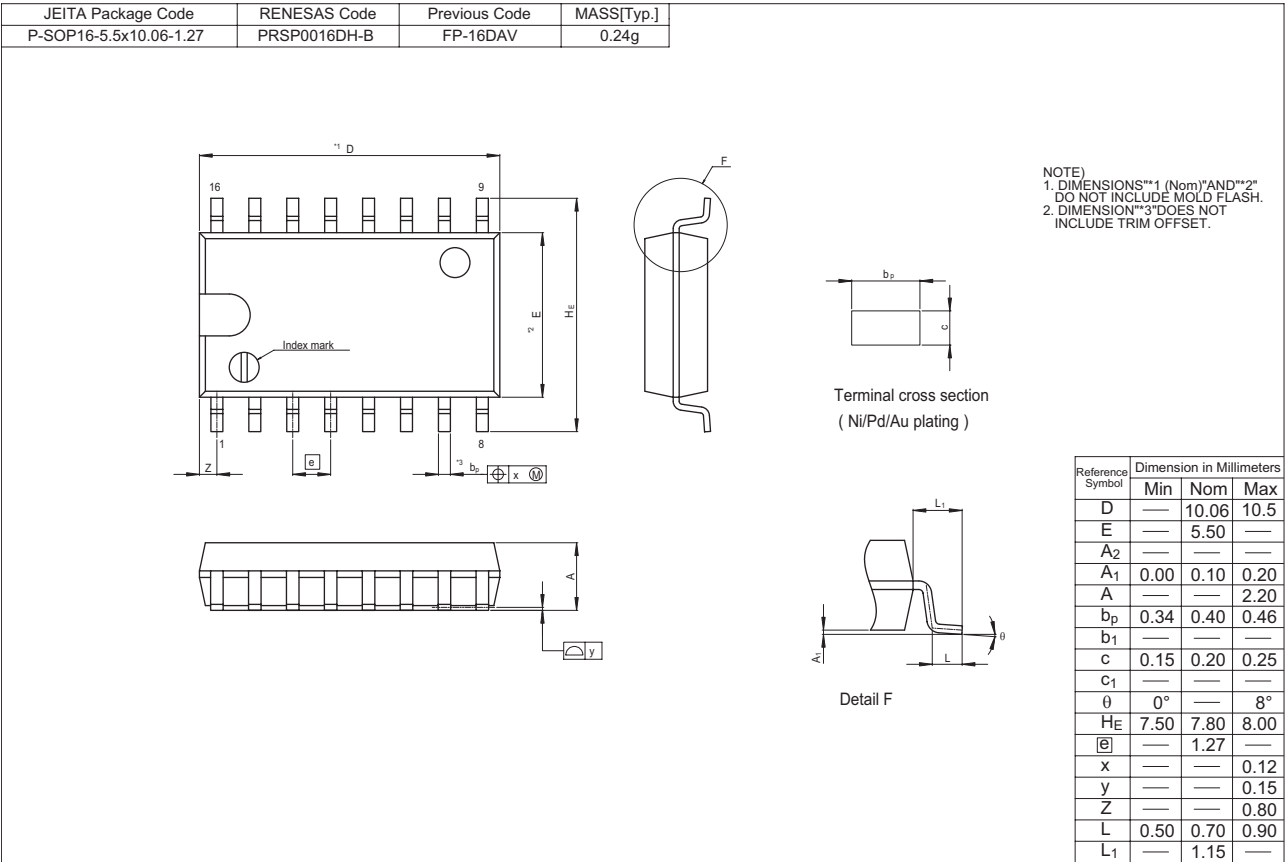
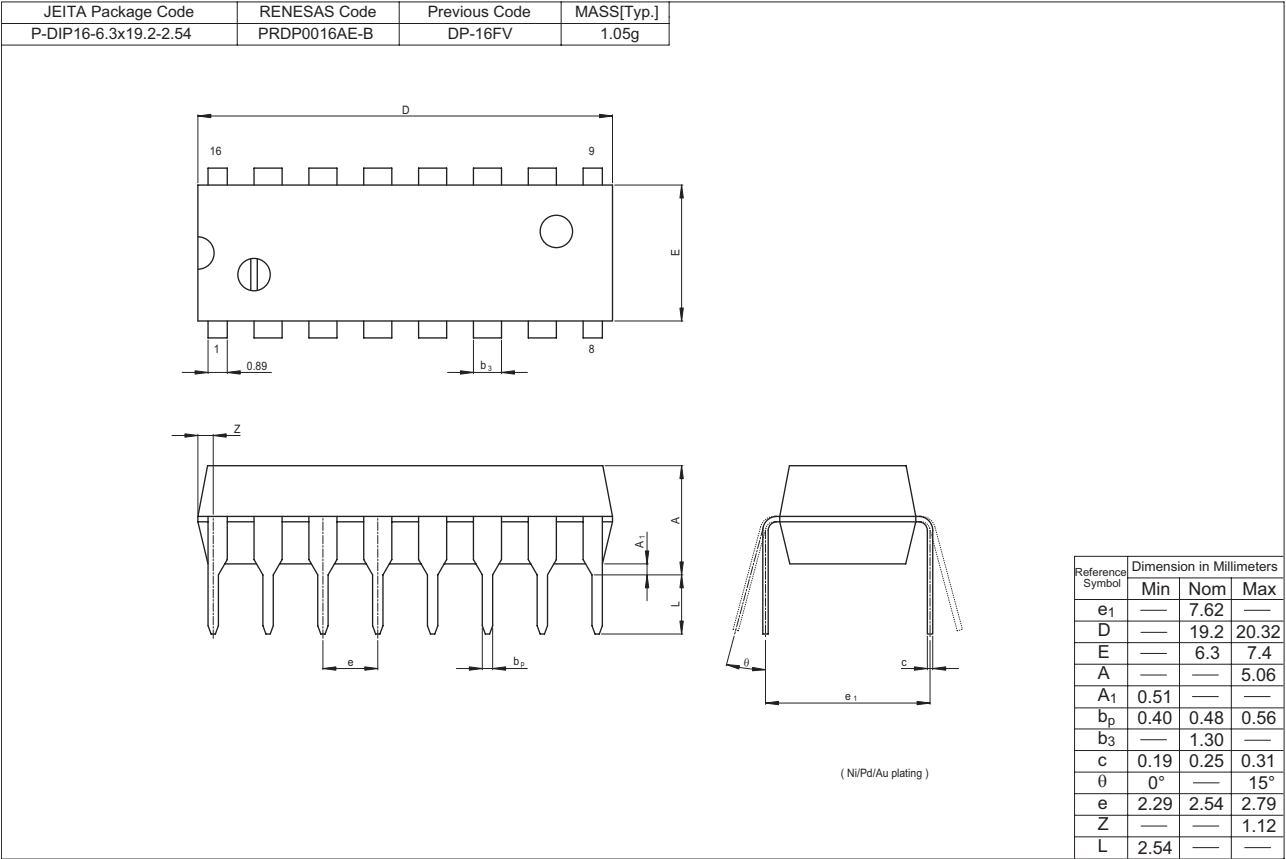
### 6. About NC Terminal

NC terminal uses open.

## System Diagram



Package Dimensions





Notes:

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